Instruction Throughput and Latency README

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REVISION HISTORY

Date	Revision	Description
April 2024	001	Initial release of document

README

Review all information in this README file prior to using the "Throughput and Latency" csv files.

File Formats:

csv file format

- Iform - "Iform" is the XED term for variants of instructions. Please consider them experimental and subject to change.
- Xed url: https://intelxed.github.io/
- Example: ANDNPD_XMMxuq_MEMxuq
- Instruction name: ANDNPD
- Instruction sources: src0 XMM, src1 MEM
- Regsize - source register size
- Mask - this instruction does not use a mask (k register)

Definitions

Throughput:

The number of clock cycles required to wait before the issue ports are free to accept the same instruction again. This number can be lower than 1, e.g., 0.5 or 0.33, indicating that multiple instructions could be executed in parallel in a given cycle. For instructions that execute at allocation, 1/alloc_width (1/6 for Golden Cove microarchitecture) was used as throughput in the tables.

Latency

The number of clock cycles that are required for the CPU to complete the execution of all of the µops that form an instruction.

The file contains partial throughput / latency data:

- Not all instructions appear in the database.
- Not all instructions that do appear have both their throughput and their latency specified.

If you require data that is missing, we suggest using the values available in the previous generation throughput and latency document (available here: https://software.intel.com/en-us/articles/intel-sdm#optimization) as a reasonable approximation.

Note that actual throughput measured on Intel processors may vary by up to 0.1 cycles. Also, latency may sometimes vary due to dynamic microarchitectural conditions, and in this case we report the average rounded to the nearest integer value. In all cases we assume data read from DCU or written to store-buffers.