intel

Quality & Reliability Vol. 6: Intel Advanced Packaging Technology Ensures High Quality & Reliability

Technical Paper

Table of Contents

Introduction..1
Advanced Packaging Technology..2
Package Q&R Verification....................4
Conclusion..6

Introduction

Advanced packaging technology plays a critical role in delivering high quality, reliable semiconductors. The term advanced packaging refers to the techniques and technologies used to assemble and interconnect multiple semiconductor chips within a single package. Intel innovations in advanced packaging allow for the creation of complex integrated circuits with enhanced performance, functionality, and efficiency.

Advanced packaging is helping meet customer demand for larger and denser processors due to emerging applications in exascale computing and Artificial Intelligence (AI). These applications require high-performance, low-power chips that can rapidly process massive quantities of data.

Recent innovations allow Intel to enable systems with high computing density (with high bandwidth and low latency) through heterogenous package architectures, those that can integrate multiple chiplets (modular chips) with different functionalities. Enabled by advanced packaging technology, Intel develops new architectures and higher density processors which result in high-performing systems at a reasonable cost.

Intel's advanced packaging technologies extend and drive Moore's Law as the company aspires to a trillion transistors in a package by 2030. Intel leads the industry in advanced packaging and has done so for decades. Our innovation allow multiple chips on a package to be connected side by side or stacked on top of one another in a 3D fashion (Foveros) and Embedded Multi-die Interconnect Bridge (EMIB), which facilitates high-speed communication between different chips.

This paper reviews the latest Intel innovation, including how we use advanced packaging technologies to ensure high quality and reliability. It explains Intel's unique packaging quality and reliability verification process, developed to make sure that complex Intel products meet or exceed customer expectations.

Advanced Packaging Technology

Foveros Direct 3D is an Intel technology that enables direct attach of one or more chiplets to an active base tile to create complex system modules. Chiplets are small pieces of silicon that perform a specific function. The term "direct attach" refers to the thermocompression bonding of copper vias, either attaching individual chiplets to those on a wafer, or attaching stacks of multiple wafers. Foveros allows Intel and its foundry customers to integrate different computing chips to optimize cost and energy efficiency.

Customer Benefits of Intel Foveros Direct 3D Technology

Intel Foveros Direct 3D technology benefits customers in several ways compared to traditional packaging technology. These include the following:

- Improved Performance: Foveros Direct 3D allows for stacking different types of chips, such as CPU, GPU, and memory, vertically on top of each other. This arrangement minimizes the distance signals need to travel between components, reducing latency and improving overall system performance.

- Space Efficiency: By stacking chips vertically, Foveros Direct 3D enables a more compact design, saving precious space on circuit boards. This is especially valuable for devices where size constraints are critical, such as mobile devices.

- Power Efficiency: Shorter signal paths and improved thermal management contribute to increased power efficiency. This is crucial for extending battery life in portable devices and reducing energy consumption in data centers and other power-hungry applications.

- Customization and Modularity: Foveros Direct 3D allows for mixing and matching different types of chips in a single package, enabling greater customization and modularity in hardware design. This flexibility can lead to more tailored solutions for specific applications and better optimization of resources.

- Scalability: The modular nature of Foveros Direct 3D facilitates scalability, allowing manufacturers to create products with varying levels of performance and capabilities by combining different chip configurations.

The resulting connection bandwidth is determined by the copper via pitch (and resulting density). The first generation of Foveros Direct 3D uses copper bonding at a pitch of 9um (microns). Future generations of the technology are currently under development.

Individual CPU chiplets sitting on a large "local" cache create a complete module. This module can then be replicated to scale up the computing capabilities of a system. The variations in the number of cores and cache sizes among these modules allow for the creation of a range of products, known as a SKU stack, to meet different performance and cache requirements.

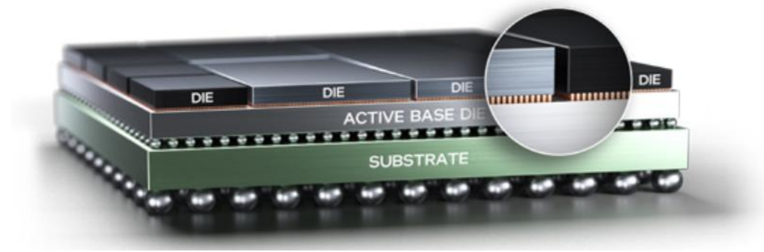

Figure 1: Foveros Direct 3D enables high-bandwidth and low latency interconnects between stacked chips.

Embedded Multi-die Integrated Bridge (EMIB) is a proven technology that offers a compelling solution for customers seeking high-performance, power-efficient, and cost-effective semiconductor packaging solutions across a wide range of applications.

How EMIB Technology Benefits Customers

EMIB technology can benefit customers in several important ways including the following:

- Design Flexibility: EMIB facilitates the integration of diverse components, such as CPUs, GPUs, FPGAs, and memory, into a single package. This provides designers with greater flexibility to create customized solutions tailored to specific use cases, leading to more efficient and optimized systems.

- Reduced Footprint: By enabling the stacking of multiple chips within a compact package, EMIB helps reduce the overall footprint of the system. This is particularly advantageous for space-constrained applications such as mobile devices, where minimizing size and weight is critical.

- Lower Power Consumption: EMIB's efficient interconnect design reduces power consumption compared to traditional packaging methods. By minimizing signal transmission distances and reducing energy loss, EMIB contributes to improved power efficiency and longer battery life in mobile devices and other power-sensitive applications.

- Cost-Effectiveness: EMIB can help lower system costs by enabling the integration of multiple components into a single package. This reduces the need for additional components and complex interconnects, simplifying system design and assembly processes.

EMIB enables high bandwidth connectivity between multiple large chiplets without the use of a silicon interposer. EMIB technology can also be used to connect multiple compute modules made with the Foveros Direct 3D technology described above. This combination of EMIB and Foveros in a single package is called **EMIB 3.5D**. It enables the creation of flexible, heterogeneous computing systems.

Individual tiles or modules can either be identical (such as to create a scalable compute architecture) or they can be disparate (such as to connect compute modules with I/O tiles or with DRAM modules). The scalability and flexibility enabled by the innovation of EMIB 3.5D allows for the creation of systems packaging with a total silicon surface area far greater than was achievable with silicon interposers alone.

Intel Foundry customers can now benefit from 2nd-generation EMIB technology. This has reduced the bump pitch from 55 to 45 microns, allowing customers to achieve higher bandwidth connectivity. This can be achieved either with Foveros Direct 3D chiplets or with multiple Input/Output (I/O) chiplets, providing versatile high-performance solutions for complex chip designs.

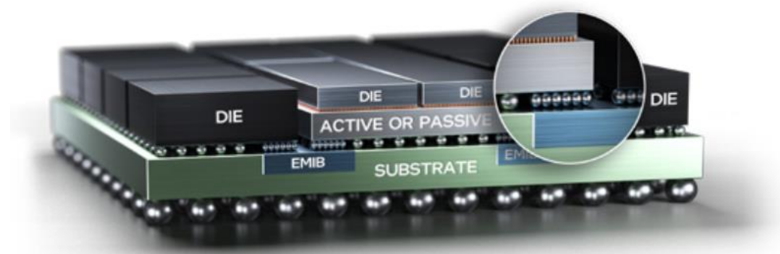

Figure 2: EMIB 3.5D. Combination of EMIB and Foveros enables the creation of flexible and heterogeneous systems with significantly larger total silicon surface area within a single package.

Package Quality & Reliability Verification

To ensure Intel products meet or exceed quality and reliability expectations, we devote significant effort to developing and qualifying package technologies. Advanced technologies such as Foveros Direct 3D and EMIB require a more complex verification process. Intel's comprehensive process enables us to deliver the highest possible quality and reliability.

Intel adheres to industry standards for semiconductor reliability, often exceeding them. The Intel package quality and reliability verification process includes both detailed modeling and rigorous experimental testing. This includes comprehensive stress testing and accelerated lifetime testing. Intel packaging often carry certifications that attest to their reliability and quality.

Intel also researches and implements advanced materials that offer better thermal management, electrical performance, and mechanical stability. High-precision manufacturing techniques reduce the likelihood of defects and improve overall package integrity. Robust quality control and continuous improvement based on field data analysis and customer feedback are also critical to the package verification process.

Intel Package Verification Process

This section reviews the Intel physics-based Quality & Reliability Verification (QRV) process, highlighting key methods of package reliability testing. Intel completes the QRV process on our products by the time of product launch, ensuring that products will meet customer quality and reliability needs. Since verification happens concurrent with product development, we can thoroughly diagnose and fix issues prior to launch. Intel successfully completed this verification process on the packaging technologies used in products including Intel® Core™ Ultra Processors, Intel® Xeon® Processors, and Intel® Data Center GPU Max. One of the latest Intel products using this verification process is Intel® Xeon® 6 with E-cores, launched in June 2024.

The Intel QRV process starts by defining the correct requirements early in product design. It involves comprehensive product design and technology development integration, the implementation of robust and controlled manufacturing processes and systems, and ultimately leads to QRV testing on the finished product.

During QRV testing, Intel uses both standards- and knowledge-based qualification strategies. Intel makes use of industry accepted standards, such as Joint Electron Device Engineering Council (JEDEC), alongside its own internally developed stress methodologies. These ensure that Intel products are shipped with the highest possible quality while considering the cost and practicality of requirements.

Advanced packaging technology is certified with knowledge-based reliability evaluations consistent with industry standards for components. This approach is based on an understanding of failure mechanisms and end user conditions expected to be encountered by the package. Accelerated environmental stress tests are utilized to characterize relevant failure modes. Intel proprietary reliability simulation tools are used to analyze the statistical reliability failure models and empirically derived acceleration factors to estimate overall field life.

QRV Stress Tests

QRV stress tests are conducted on units that have completed the regular manufacturing flow. In all cases, a failure is defined as a failure to meet datasheet parameters as measured by the appropriate production and/or engineering tester. Examples of Intel QRV tests and descriptions include the following:

1. Temperature Cycling (T/C)

Temperature Cycling is a test performed to evaluate the mechanical integrity portion of the intrinsic operating reliability failure rate. Temperature cycle testing is conducted in conformance with the procedures defined in JEDEC standards. Thermo-mechanically induced damage results from differences in the material properties of the constituent materials over the range of cycling temperatures. Mechanical failure mechanisms such as solder joint fatigue, package cracking, and Interlayer Dielectric (ILD) cracking in the die and package are accelerated by this stress.

This test is conducted in conformance with the procedures as defined in JEDEC Standard JESD22-A104. As an example, in TCB testing, the devices are alternately exposed to high (125 °C) and low (-55 °C) temperatures with a ramp rate of 15°C to 30°C per minute and a dwell time of 15 minutes. Heating and cooling are done by convection using temperature cycling chambers. Parts are functionally and parametrically tested during readouts using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

2. High Temperature Storage (Bake)

Intel performs a high temperature bake, with no applied electrical bias, to evaluate the thermal integrity portion of the intrinsic operating reliability failure rate. Bake tests are used to evaluate the thermo-mechanical reliability of the component over a range of high temperatures to simulate long-term sustained use and high temperature storage. Temperature induced failures commonly result from materials degradation and metal reactions that may result in variations in mechanical properties. The test is conducted in conformance with the procedures defined in the JEDEC standard. The bake evaluation accelerates failure mechanisms such as single bit charge loss, bond degradation, ionic contamination, contact integrity, and metal void propagation.

This test is conducted in conformance with the procedures defined in JEDEC Standard JESD22-A103 at an elevated temperature of 150°C, as an example for Condition B of the standard. Parts are functionally and parametrically tested after stressing using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

3. Accelerated Moisture Resistance (HAST)

Highly Accelerated Stress Test is a high temperature/high humidity stress performed on non-hermetic devices to evaluate the moisture reliability portion of the intrinsic operating failure rate. HAST testing is used to evaluate the reliability of the component at elevated temperature ranges and high humidity environments without electrical BIAS. Typical failure mechanisms from this stress include corrosion of metal and contamination induced threshold shifts due to moisture.

This test is conducted in conformance with the procedures defined in JEDEC Standard JESD22-A118 (unbiased). The devices are placed in a 110°C and 85% relative humidity stress chamber as an example for Condition B of the standard. Parts are functionally and parametrically tested after stressing using an automated tester. A failure is defined as any device failing to meet datasheet specifications.

Conclusion

This paper provides a comprehensive overview of two unique advanced packaging technology innovations developed by Intel – Foveros Direct 3D and EMIB – and how we utilize them to facilitate a high quality and reliability experience. It also reviews the Intel package quality and reliability verification process, which is designed to make sure Intel products meet or exceed industry standards.

Intel will continue to innovative in advanced packaging technology and quality and reliability verification as we strive to meet the challenges of today’s complex computing environment. By committing significant resources to identifying potential issues, finding root causes, and fixing them prior to product launch, Intel is ready to meet demanding customer needs today and in the future.