Intel® Time Coordinated Computing Technology (TCC) User Guide

(Public-Version[1])

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[1] An enhanced version of this guide with additional information regarding Intel's Time Coordinated Computing Technolgy offering is available for customers under NDA at RDC #786715

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Revision History

Date	Revision	Description
August'24	1.0	Initial release of public version
September '24	1.1	Added Intel® Ethernet Controller i226 AVNU Component Certification

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1.0 Introduction

A major shift is happening at the edge in markets such as Manufacturing and Energy, both for Oil & Gas and Utilities, as well as many other market segments spanning Health, Aviation, Retail, and many more. This transformation towards software-defined solutions is driven by multiple factors such as reducing cost, new technologies such as AI & 5G, improving quality and efficiency, and changes in the workforce. A key element of this transformation is to support operational workloads on general purpose compute platforms which drives a need to support real-time workloads along with best-effort workloads on the same system. Intel® Time Coordinated Computing Technology (TCC) enabled platforms deliver optimized compute- and time-performance for real-time applications and include support for IEEE*[1] 802.1 Time Sensitive Networking (TSN) over converged networks (wireless and wired).

Intel's Time Coordinated Computing Technology offering comprises of a comprehensive set of optimizations throughout the complete platform stack all the way from Intel silicon to the application layer. These optimizations are designed to make Intel platforms with real-time support achieve high determinism in the presence of best effort workloads running on the same system.

Time Coordinated Computing Technology provides the following key values:

- Timely & reliable data processing: Better out-of-box real-time performance for deterministic workloads
- Doing more with the same system: Maximum efficiencies by aggregating real-time and best-effort applications on a single system

[1] Other names and brands may be claimed as the property of others.

- Timely & reliable data delivery: Support for IEEE Time Sensitive Networking (TSN) over converged networks
- Future-proofing designs: Scale between Intel Atom® processors, Intel® Core™ processors, and Intel® Xeon® processors as well as across processor generations

The current version of this document describes real-time features and optimizations across several processor families and generations. Some features are not available on all product stock keeping units (SKUs) and product families. Contact your Intel representative for details.

Real-time applications (also called "workloads") must execute within a certain amount of time, consistently, across numerous iterations. While specific requirements vary by use case, real-time applications typically perform the following sequence of tasks:

1. Process new input such as a sensor measurement or camera video streams.
2. Perform a computation such as a new motion vector or object detection bounding box of a computer vision workload.
3. Control an actuator or render a result.
4. Ensure actions are tightly synchronized or happen at the exact same time.

Furthermore, these applications often have a deadline. They must complete the tasks within a certain time, which may range in typical applications from microseconds to milliseconds.

On processors with TCC support, Intel provides the following support for real-time applications:

- Selected processors with features to minimize worst-case execution time (WCET) within the system.
- Selected processors with time synchronization optimizations.
- Ethernet controllers and wireless connectivity solutions that support IEEE 802.1 Time-Sensitive Networking (TSN) standards.
- Validated configuration guidance as the base for Intel's key performance indicators (KPIs) of time performance.

- Reference software to help development of real-time systems using Intel processors and connectivity solutions.

1.1 About This Document

This document provides guidance on how to utilize Intel's platforms for real-time usages, including some technology background as well as recommendations and examples on how to prepare Intel's real-time capable edge platforms for use with real-time applications. This document is for anyone working on these components, such as:

- System engineers preparing a system to support real-time applications.
- Engineers at ODMs and OEMs setting up systems and preparing the base platform software as well as validating its readiness for real-time.
- Software developers developing and validating SW applications and middleware with real-time requirements to work on Intel systems.

Consider this document the starting point for understanding how to best use Intel platforms for real-time usages. This document:

- Introduces the basics of running real-time workloads on Intel systems.
- Introduces real-time hardware features and related software.

Additional information on using Intel's platforms for real-time usages is provided in the more comprehensive NDA version of this guide (RDC# 786715)

Note: This document is not intended to provide a comprehensive specification for real-time features or software implementations. Where feasible, reference documentation has been cited that gives further technical detail for the topics discussed.

2.0 Real-time Capabilities Overview

2.1 Hardware Features

Intel® Core™ Processors, Intel Atom® Processors and Intel® Xeon® Processors with Intel® Time Coordinated Computing (TCC) provide hardware features to optimize real-time compute performance and support ethernet controllers with IEEE TSN support to optimize network traffic.

In this chapter, the hardware features are described at a high level. These features include HW-, FW- and SW-level optimizations throughout Intel's platform stack.

2.1.1 Hardware Optimizations Overview

Intel's Time Coordinated Computing Technology offering comprises of many optimizations throughout Intel's processors and connectivity solutions targeted at improving real-time performance in a mixed criticality environments comprised of real-time workloads as well as best-effort workloads running concurrently on Intel platforms and utilizing the same network connections and networks.

2.1.1.1 Time Synchronization Optimizations

- Precision Time Coordination: Clocks from SOC subsystem can be more precisely correlated in software via hardware time-stamping.
- Timed-GPIO: GPIO output that can be precisely coordinated in software (via Platform Sync) leveraging pulse-per-second (PPS)
- PCI Express* Precision Time Measurement (PTM): enables precise coordination of events across multiple components with independent local time clocks.
- IEEE 1588 (PTP) support in all Intel end-point connectivity solutions. IEEE 802.1AS TSN profile of IEEE 1588 supported in many Intel end-point connectivity solutions.

2.1.1.2 Timeliness Optimizations

- Power State Transition Optimizations: Enable CPU to keep executing instructions while its frequency is increasing or decreasing. While on early platforms with TCC support, e.g., Intel Atom® x6000 Series Processors and 11th Generation Intel® Core™ Processors), Intel recommended disabling many power management capabilities, subsequent additional improvements have changed such recommendations to allow some power management features to remain enabled with minimal impact to real-time behavior. In addition, Intel® Speed Shift technology together with other P-State options may be used to boost real-time performance by increasing the core frequency on select cores.
- Memory/Cache Allocation Optimizations: Partitioning of shared caches at the way level between classes of service (L2 & L3 Cache) - Intel® Cache Allocation Technology (CAT); Limit amount of cache available to GPU (GT-CLOS).
- Interrupt Request (IRQ) Optimizations: Optimize processor microcode & other overhead in the critical path for interrupts in the CPU core; Allow devices to deliver interrupts directly to the guest OS without requiring preprocessing by the hypervisor.
- Fabric and PCIe Virtual Channels: Virtual channels on Fabric and PCIe available to high priority workloads.
- Intel® Speed Shift for Edge Compute Applications enables specific assignment of processor performance to where it is most needed
- Support of IEEE 801.1AS, 802.1Qbv, 802.1Qav, 802.1Qbu/3br in all end-point connectivity solutions to take advantage of TSN features becoming common in edge networks.

2.2 Supported Hardware

Intel offers real-time support on a wide variety of platforms and SKUs. Time Coordinated Computing Technology support includes a set of optimizations in the SOC hardware and processor microcode including support for L2 and LLC (L3) Cache Allocation Technology (CAT) as well as IEEE Time Sensitive Networking (TSN) support in our connectivity offering.

2.2.1 Intel processors with Time Coordinated Computing Technology support

A wide variety of Intel processors support Time Coordinated Compute technology including many versions and SKUs of Intel® Xeon® processors, Intel ® Core™ processors, and Intel Atom® processors. Appendix A provides a detailed list of processors and SKUs offering TCC support.

Note: For the latest details on specific SKUs and platform capabilities, please refer to the information provided at: https://www.intel.com/content/www/us/en/products/details/embedded-processors.html.

2.2.2 TSN-capable Ethernet Controllers

Intel platforms with real-time support feature TSN over Ethernet via Intel's discrete i226-LM/IT Ethernet Controllers and on select processor SKUs and product families via integrated Ethernet MACs (for Intel® Core™ S-Series processors the R680E SKU of PCH is required for integrated 2.5Gb Ethernet with TSN support)

In September 2024 the Intel® Ethernet Controller i226 became the first endpoint device granted Avnu Alliance Component Certification for compliance with the IEEE 802.1AS (Timing and Synchronization for Time-sensitive Applications) and IEEE 802.1Qbv (Enhancements for Scheduled Traffic) standards under the IEEE TSN toolbox.

Table 1: TSN-capable Ethernet Controllers

Ethernet solution	Number of Ports	Media-Access Control (MAC)	Base-T PHY	Supported on
Discrete Intel® Ethernet Controller i226 LM/IT (2.5GbE with TSN and vPro support)	1 port per i226	Discrete PCIe device (MAC/PHY combo)		All TCC supported processors Avnu Alliance Component Certified for compliance with the IEEE 802.1AS and IEEE 802.1Qbv Avnu Certified Component Registry
Integrated 2.5GbE MAC	1 port	Yes	3rd Party	• 11th Generation Intel® Core™ UP3-Series Processors

Ethernet solution	Number of Ports	Media-Access Control (MAC)	Base-T PHY	Supported on
				• 13th Generation Intel® Core™ U-, P-, H- Series Processors • Intel Atom® x7000E series processors
Integrated 2.5GbE MACs	2 ports	Yes (1 per port)	3rd Party	• 13th Generation Intel® Core™ S-Series Processors (R680E SKU of PCH only) • 12th Generation Intel® Core™ S-Series Processors (R680E SKU of PCH only) • Intel® Xeon® W-11000E Series Processors
Integrated 2.5GbE MACs	3 ports	Yes (1 per port)	3rd Party	• Intel Atom® x6000E series processors

The ethernet controllers with TSN support can operate at multiple speeds: 10Mbps, 100Mbps, 1Gbps, and 2.5Gbps and in either full duplex or half duplex mode.

The integrated ethernet MAC with TSN support is accessed by Intel's processor cores through system software as a PCI express Root Complex Integrated Endpoint (RCiEP) via PCH I/O Fabric (PSF2) and only supports the SGMII interface.

To support Ethernet with TSN, the integrated ethernet MACs require 3rd party Ethernet PHYs external to the SOC. Supported PHYs are generally listed in the product briefs of the processor families.
Note: Many other Intel® Ethernet Controllers support IEEE 1588 and PTM but have limitations on other TSN aspects, e.g., IEEE 802.1Qbv or 802.1Qav (See product specifications for details).

2.2.3 TSN capable Altera® FPGA solutions

Intel provides various FPGA products that include Time Sensitive Networking support, some of them specifically targeted at switched endpoints. The following products are currently offered:

FPGA product	Number of Ports	TSN support
Cyclone® V	3x/5x 1Gb/s port Switch	Yes (TTTech IP) IEEE802.1AS, Qbv, Qbu, Qcc, CB, Qci
Cyclone® 10	5x-7x 1 Gbps	Yes (TTTech IP) IEEE802.1AS, Qbv, Qbu, Qcc, CB, Qci
Arria® 10	5x-7x 1 Gbps	Yes (TTTech IP) IEEE802.1AS, Qbv, Qbu, Qcc, CB, Qci

2.2.4 TSN-capable Wireless Solutions

Intel is working on providing TSN support over 5G and Wi-Fi on select Intel platforms. This section will be updated as such TSN capabilities will be available.

2.3 TCC enabled Software

Intel provides software that enables developers to access TCC hardware features, including BIOS support, Linux* kernel driver and user-space patches, and sample applications. In addition, Intel is working with ecosystem partners to deliver TCC and IEEE TSN support as part of 3rd party SW solutions.

2.3.1 Operating System Support

Intel provides Linux* OS support by upstreaming Linux kernel driver and user space patches to open-source libraries and utilities (iproute2, ethtool, linuxptp, etc.). In addition, Intel is working with commercial Linux distribution vendors to integrate upstreamed patches in their commercial distributions.

In addition, Intel is working with select real-time operating system vendors to enable support for intel TCC capabilities, including support for TSN capable ethernet controllers.

2.3.2 Hypervisor Support

Intel enables 3rd party Hypervisors for real-time support and validates select capabilities with opensource ACRN and KVM Hypervisors.

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* Other names and brands may be claimed as the property of others.

2.3.3 UEFI-BIOS Support

Many of the control registers involved in configuring a platform for real-time usage are accessible through the BIOS.

Intel's reference BIOS includes various TCC enhancements including an option called Time Coordinated Computing Mode (TCC Mode), a single BIOS switch that optimizes the firmware settings for low latency. If your BIOS vendor has included support for TCC Mode, enabling this setting is a quick way to optimize your firmware configuration for real-time support.

2.3.4 Slim Bootloader Support

Like the UEFI-BIOS, Intel's Slim Bootloader (SBL) reference provides a configuration option to enable or disable TCC Mode.

2.3.5 Time-Sensitive Networking Reference Software

Intel provides a small set of TSN sample/reference applications available at https://github.com/intel/iotg_tsn_ref_sw.

3.0 Time Coordinated Computing Quick Start Guide

3.1 Getting started with Intel® TCC

As mentioned in Chapter 2, Intel platforms are designed to support various applications and workloads and serve a broad range of markets. Intel's Time Coordinated Computing Technology offering is designed to expand these markets to add support for workloads requiring real-time capabilities (low latencies, deterministic processing, and accurate time synchronization).

Many elements influence the real-time performance of a platform including HW and SW choices, BIOS and SW settings as well as ways to configure shared resources on the platform. As described in the previous chapters, TCC is comprised of many optimizations in hardware and software. The level of determinism required strongly depends on the real-time workload. Hence, not every implementation will require all the TCC optimizations available on Intel platforms to be enabled. This chapter describes some of the basic considerations of running real-time workloads on Intel platforms.

The following table provides guidance on how to approach usage of the capabilities offered.

1	Choose an Intel platform with TCC support	This ensures your platform has all the needed capabilities to support real-time workloads. This generally also includes choosing a connectivity solution with IEEE TSN support.
2	SW stack selection	Select the best RTOS and Hypervisor to fit your needs (e.g., Linux Preempt-RT)
3	Apply Real-time kernel boot parameters	Follow the directions for low latency configuration of your OS by your OS vendor (kernel boot parameters)
4	Pin your real-time workload to cores	Pinning a real-time workload to a core takes away some real-time performance variance. In a Hybrid system pinning allows allocating the real-time workload to the type of core best fitting the needs of the workload.

5	Configure platform for Time Coordinated Computing via BIOS, providing the most flexibility for mixed criticality applications	Evaluate the overall performance of your system as well as your ability to support your real-time workloads after enabling **TCC Mode** in your BIOS. If your system does not support TCC Mode, there are ways to configure your BIOS manually, details on such options are available in the NDA version of this Intel® TCC User Guide (RDC#786715). For many applications enabling TCC Mode or equivalent BIOS settings will likely be sufficient!
6	**If needed:** Allocate L2/3 cache to high priority workloads	Use Intel® Cache Allocation Technology to allocate an amount of cache for the real-time workload to utilize.
7	**If needed:** Configure Intel® Speed Shift to increase real-time performance for edge compute applications	Use Intel® Speed Shift technology to boost core frequency on cores with high priority real-time workloads.

3.2 Hardware Configuration

Intel processors are designed to be configurable to address many unique customer requirements. Such requirements can come in the form of form factor (layout), thermal, performance, and cost. The combination of these requirement categories will ultimately determine board characteristics like memory type & speed, memory layout, and I/O layout. Regardless, for best real-time performance, Intel recommends:

- Populating ≥ 1 DIMM/channel for each available memory channel on the board (populating more DIMMs and more memory generally allows for quicker access to more data)
- Utilizing PCI Express slots attached to CPU die for lowest latency / highest throughput network connections. Note that the other available PCIe slots will also be sufficient for many real-time workloads and do also support many real-time optimizations (e.g., Precision Time Measurement - PTM).

Note: Refer to the documentation provided by the board or system vendor to identify which PCI Express connectors route to the CPU die.

3.3 Firmware Configuration

Intel's reference BIOS includes multiple knobs relevant to configure the BIOS for real-time performance. Such knobs include enabling and disabling specific functionalities that tend to impact real-time performance, such as some power-, frequency-, and thermal-management features, Hyperthreading and capabilities like PCIe Precision Time Measurement.

3.3.1 TCC Mode

TCC enabled platforms generally offer *TCC Mode*, a single BIOS/SBL knob that optimizes the firmware settings for low latency. TCC mode includes a wide range of real-time optimizations including the following:

- Power states and frequency transition optimizations
- Configuration of TCC features, e.g.,:
  - Limit amount of cache available to GPU.
  - Optimize IO device utilization of Cache (for select platforms).
  - Set up virtual channels for VC-capable endpoints.

For UEFI BIOS, the TCC Mode option is generally found in the following BIOS menu, but specific naming may vary in your BIOS:
Intel Advanced Menu > Intel® Time Coordinated Computing

For Slim Boot Loader (SBL), this configuration option is found in the following configuration file in the SBL source directory:
Platform\CommonBoardPkg\CfgData\CfgData_Tcc.yaml
You can override the enable or disable TCC Mode using the ConfigEditor tool. For more information on updating the settings using this tool, refer to the SBL wiki:
https://slimbootloader.github.io/how-tos/enable-intel-tcc.html#open-sbl-defaultconfiguration-data
For generic ConfigEditor info, refer to:
https://slimbootloader.github.io/tools/ConfigTools.html?highlight=configeditor#configeditor

If your BIOS/SBL vendor has included support for TCC Mode, Intel recommends enabling this setting as a starting point for optimizing the firmware settings for real-time.

TCC Mode configures various existing BIOS/SBL settings to predetermined values. The settings altered by TCC mode can be set independently for granular control of specific capabilities whether TCC mode is enabled[1] or not. We generally recommend not deviating from the default Intel TCC Mode values to ensure consistent configuration that is optimized for general real-time performance.

Due to TCC mode optimizing the platform for Time Coordinated Computing including changing some SOC power settings, enabling TCC mode adds approximately 1 Watt to the TDP of the processor.

In cases where your BIOS does not include support for TCC Mode, please see Appendix B for platform specific settings that can be used to manually implement the equivalent TCC Mode functionality.

In cases where your BIOS does not include support for TCC Mode, please highlight this gap to your board or system vendor. Intel provides additional information on how to configure many relevant BIOS settings manually in the NDA version of this Intel® TCC User Guide (RDC#786715).

Note: BIOS configuration for some options can be overridden by the operating system. Specifically, when using Linux, the relevant kernel parameters should be supplied during boot to prevent the OS from altering the BIOS settings.

Note: Altering hardware and software power management features can negatively affect real-time performance and general compute performance for various I/O paths.

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[1] For older platforms, like Intel Atom® X6000 series processors and 11th Generation Intel® Core® processers, some settings set by TCC mode cannot be altered once TCC mode is enabled

3.3.2 Power Management settings

As mentioned in Chapter 2, Intel has optimized power management capabilities on recent platforms resulting in improvements of Time Coordinated Computing performance even with some power management enabled. Starting with the 12th Generation Intel® Core™ processors and the Intel Atom® x7000 Series processors, TCC Mode no longer changes the default settings of Intel® Speed Shift Technology and Intel® Speed Step Technology. In addition, we keep Intel® Turbo Boost technology enabled during our real-time performance measurements on those platforms.

3.4 Operating System Configuration

The operating system is a critical element for real-time optimization and options depend heavily on the particular operating system used. For Linux, there are some key parameter settings Intel uses for real-time performance measurements but Linux distribution vendors offer their own guidance on how to optimize their Preempt-RT capable OS versions for real-time operation.

Canonical Real-time Ubuntu*[1]: Tuning a real-time kernel
RedHat RHEL*: Understanding RHEL for Real-time
SuSE*: SUSE Linux Enterprise Real Time

The above links provide guidance for those Linux distributions. In general Intel recommends a properly configured BIOS, which will eliminate the need for the OS to redundantly disable known sources of jitter. As such the following Linux boot command could be used to ensure the timestamp counter in the CPU is used and interrupts to the cores reserved for real-time are avoided:

```
clocksource=tsc
tsc=reliable
nmi_watchdog=0
nosoftlockup
idle=poll
isolcpus=X-Y[2]
```

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[1] Other names and brands may be claimed as the property of others.
[2] While isolcpus use is not generally advised as it cannot be changed at run-time, for real-time applications it can be used for CPU isolation.

rcu_nocbs=X-Y
nohz_full=X-Y
irqaffinity=0

where X and Y are the range of cores dedicated to real time tasks

3.5 Optimal Clock Synchronization Accuracy

IO devices that support PCIe Precision Time Measurement (PTM) provide the highest degree of clock synchronization accuracy. Intel platforms support Precision Time Coordination out of the box, enabling accurate clock synchronization within the SOC.

3.5.1 Enabling PTM

Most Intel processors support PCIe PTM. PTM functionally can generally be enabled/disabled in BIOS. In most cases PTM functionality is enabled by default. If not already enabled, there are generally two ways to enable PTM:

1) If your BIOS supports Intel TCC Mode, the easiest way is to enable TCC mode. Enabling Intel TCC Mode was described in Chapter 3.3. TCC mode will automatically enable PTM on all PCIe connections on the processor.
2) If your UEFI BIOS does not support TCC Mode you can enable PTM for each PCIe connection separately (This may not be supported on all SOCs). The BIOS Menu items can generally be found at **Intel Advanced > System Agent (SA) Configuration > PCI Express Configuration** and **Intel Advanced > PCH-IO Configuration > PCI Express Configuration.** The action generally needs to be repeated for any PCIe the user wishes to enable.

To take advantage of PTM, all devices connected to a PCIe port will need to also support PTM. For example, if a PCIe-switch is used to connect several ethernet controllers to a single PCIe port on the SOC, the PCIe switch as well as the etherent devices will need to support PTM.

3.6 Cache Allocation for Real-time Workloads

In real-time system designs, it is often necessary to have control over shared resources to ensure that an adequate amount of that resource is available when needed by the application. Failure to allocate sufficient resources can lead to a performance degradation of the real-time application, causing it to miss execution deadlines.

System caches are one of the shared resources that, depending on the amount of contention, can drastically affect the performance of a real-time application. Intel provides the ability to partition cache resources using Cache Allocation Technology (CAT), which, depending on processor family and generation, may be available on both the L2 Cache and Last level Cache (LLC). Both L2- and LLC-CAT are available on TCC enabled Intel processors, however on TCC enabled Intel® Core™ processors and Intel Atom® processors, LLC (L3-cache) is non-architectural, meaning the feature availability is not exposed via CPUID and therefore not accessible by most OS commands like in this case 'resctrl' in Linux. Methodologies to configure CAT on those processors that are available for non-architectural CAT are described in the version of this document available to customers under NDA.

Intel configures a simple Cache partitioning scheme using CAT when running real-time performance measurements. This simple scheme divides the cache in half, creating one half dedicated to the real-time application(s) and the other for best effort application(s).

3.7 Setting up Intel's connectivity solutions as part of a TSN based network.

Setting up a TSN based network and how to best link Intel's connectivity solutions with TSN support is outside the scope of this document. Intel is offering some guidance for TSN in a Linux environment using Intel's ethernet solutions for customers under NDA in the Ethernet Time-Sensitive Networking on Linux* for Intel® Processors & Ethernet Controller i225/i226 – Get Started Guide which can be found in RDC, document number: 6164446.

3.8 Example: Configuring a 13th Generation Intel® Core™ i7-13800HRE platform for real-time

This example outlines the high-level steps of preparing a 13th Generation Intel® Core™ platform for real-time usage.

Hardware selection:

- Intel® Core™ i7-13800HRE Processor
  - 14 Cores, 6 performance cores & 8 efficiency cores
  - 24MB of LLC (L2 Cache)
  - Integrated graphics
- Memory: Populate all DIMM slots
- Intel® Ethernet Controller I226 on PCIe port PEG (Port 1)

Configuring the Firmware

Enable TCC Mode in BIOS which will configure various BIOS menus for best real-time performance. In addition, it will configure all PCIe slots for Precision Time Measurement (PTM) and enable GT-CLOS, which limits the amount of cache the integrated graphics has access to.

Choosing and Configuring the Operating System

In the example we assume Real-time Ubuntu* optimized for Intel platforms is used.[1]

Apply kernel parameters to isolate cores for real-time workloads and correct clock usage. In this example we are planning to use P cores 4 & 5 for real-time usage and P-cores 0 - 3 as well as E-cores 6 - 13 for housekeeping and best effort workloads:

clocksource=tsc tsc=reliable nmi_watchdog=0 nosoftlockup idle=poll isolcpus=4-5 rcu_nocbs=4-5 nohz_full=4-5 irqaffinity=0[2]

Cache partitioning.

[1] Please contact Canonical for access to Real-time Ubuntu

[2] Follow Canonical's guidance on configuring other kernel boot parameter settings on real-time Ubuntu

In this example we are following the simple cache partitioning scheme described previously, dividing the cache in half: one half dedicated to the real-time application(s) and the other for best effort application(s). The Intel® Core™ Processor i7-13800HRE Processor contains 24MB of LLC (L3) cache that can be partitioned using the model specific, non-architectural implementation of L3 Cache Allocation Technology found on Intel® Core™ processors that support Time Coordinated Computing. (See Figure 1)

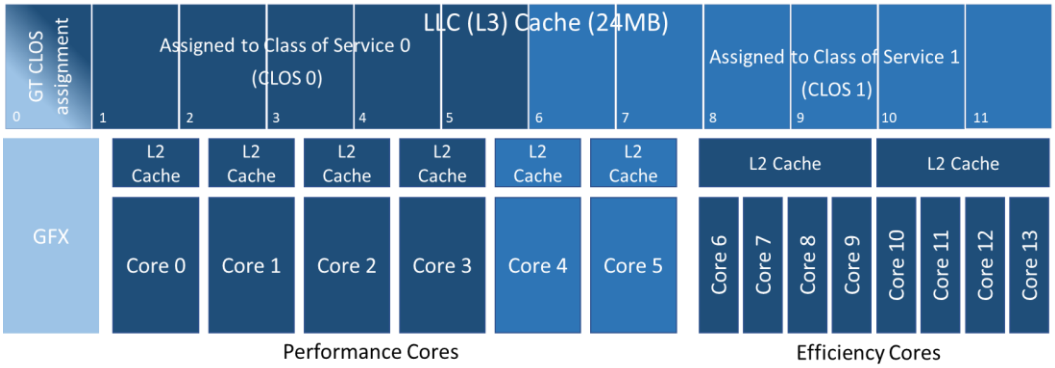

Figure 1: Cache allocation example for 13th Gen Intel® Core™ Processor i7-13800HRE example with GT CLOS enabled via TCC Mode in BIOS

Table 3 shows how the 24MB last level cache can be partitioned in half, with P cores 0-3, all E cores and Gfx operating with Class of Service 0 (CLOS 0) being assigned half the cache and P cores 4, and 5, which will be used for real-time workloads, operating on Class of Service 1 (CLOS 1) the other half of cache. [1]

For completeness, the equivalent commands for programming the MSRs directly are also shown. The MSR's used for configuring the cache masks are L3_MASK_0 (address 0xC90) and L3_MASK_1 (address 0xC91). The MSR used for associating a class of service to a core is PQR_ASSOC (address 0xC8F).

The 13th Gen Intel® Core™ Processor i7-13800HRE last level cache has a capacity bitmask (CBM) length of 12 (0xFFF), so each class of

[1] Cache assignment to specific cores is done via Class of service (CLOS designation). Cache is assigned to a specific CLOS and cores run with a specific CLOS assigned to them.

service will be assigned a CBM length of 6 (0x3F and 0xFC0, respectively) when partitioning the cache in half.

The intel-cmt-cat “pqos” utility is an alternate way to program the cache allocation.

Table 2: Partitioning the cache in half on the 13th Gen Intel® Core™ Processor i7-13800HRE.

Using intel-cmt-cat “pqos” utility	Model Specific Register (MSR) programming	Comments
pqos --iface=msr -e "llc:0=0x3F;llc:1=0xFC0"	wrmsr 0xC90 0x3F wrmsr 0xC91 0xFC0	Assign ½ the cache to CLOS 0 Assign ½ the cache (non-overlapping) to CLOS 1
pqos --iface=msr -a "llc:0=0-3, 6-13;llc:1=4,5"	wrmsr -p 0 0xC8F 0x000000000 wrmsr -p 1 0xC8F 0x000000000 wrmsr -p 2 0xC8F 0x000000000 wrmsr -p 3 0xC8F 0x000000000 … wrmsr -p 4 0xC8F 0x100000000 wrmsr -p 3 0xC8F 0x100000000	Assign CLOS 0 to Cores 0-3 (performance cores) Also assign CLOS 0 to all efficiency cores (6-13) using the same command (not shown) Assign CLOS 1 to Cores 4 and 5

Note: The “–iface=msr” extension is necessary to make the pqos command work on non-architectural CAT.

Note: While disabling all caches, may have been an approach in the past for microcontrollers, it is not a recommend path for Intel SOCs.

Pinning real-time workloads to specific cores.
During run-time any real-time workloads should be pinned to the cores designated for high priority workloads (in this example Cores 4 and 5). This applies to the actual real-time workloads as well as any needed

IRQ interrupt handling for such workloads. For best performance you pin the real-time workload to one Core (e.g., Core 4) and the real-time IRQ handling to the other (Core 5).

Note: Please refer to guidance from your OS vendor on how to pin workloads to cores.

3.9 Intel® Speed Shift technology for edge computing to boost real-time performance.

Setting the frequency of cores that have real-time workloads pinned to them to a higher fixed frequency (HFM) using Intel® Speed Shift technology can boost the real-time performance of those workloads. However, this benefit comes at a cost. Running cores above the HFM frequency impacts reliability and, to stay within the TDP guard bands, may cause more extensive throttling of other cores.

On current Intel platforms the P-state of performance cores, p-cores, can be selected independently per core. Efficiency cores, e-cores, are typically grouped in sets of four cores per module and the P-state can be selected per module.

When set correctly, the real-time cores will constantly run at the set frequency, while other cores will still vary their frequencies as directed by the processor or the OS, including the possibility of throttling as needed. The below figure shows the behavior of various cores. In this example, two cores, labeled RT cores, are set to 3.6Ghz, the rest of the cores are ‘floating’ up to their set max-frequency values, in this example, p-cores up to 2.5GHz, e-cores up to 1.2Ghz, and the integrated GPU up to 1.3GHz.

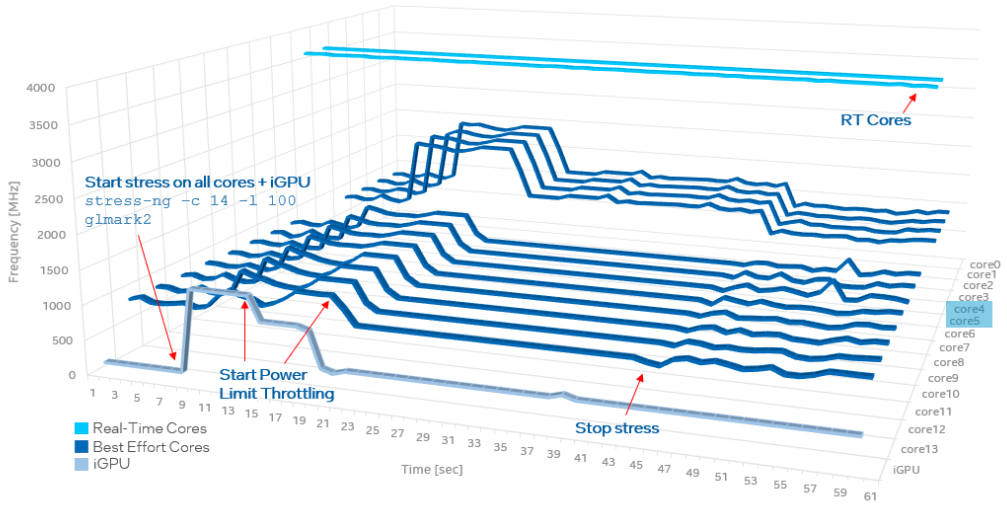

Figure 2: Core behavior when using Intel® Speed Shift technology for edge computing when system is loaded to induce throttling.

Setting some cores to such a higher frequency allows for lower average latencies and reduced jitter for the real-time workloads running on those cores.

3.9.1 Impact of using Intel® Speed Shift technology for edge computing on component reliability and overall system performance.

Setting even just a few cores to a higher, fixed frequency does not come without a cost. Due to higher internal frequency, voltages, and subsequent higher temperature and power, such settings will negatively impact the reliability expectations of the CPU and should be used with careful consideration.

Higher temperatures and power consumption also affects the overall system TDP and depending on the usage may adversely affect the performance of the rest of the cores and the graphics as the processor and OS will automatically throttle those cores and the graphics engine to avoid damage.

To address such concerns, we are describing a specific enveloping configuration on the highest performing SKU of a swim lane that can be leveraged into lower performing SKUs of the same processor family without significant impact on reliability. Such an enveloping configuration example is described in the next section.

3.9.2 Example Configuration using Intel® Speed Shift technology on Intel® Core™ 13th Generation H-series processors.

In this example we are using Intel® Speed Shift Technology to set 2 p-cores to a higher frequency and limit the max frequencies of the rest of the P-Cores, all e-cores, the integrated graphics, and the LLC/Ring to their respective HVM frequencies.

To use Intel® Speed Shift Technology for edge computing, it is essential to enable it in the BIOS. The following BIOS settings are recommended:

Ref BIOS menu	BIOS setting	State	Comment
Intel Advanced Menu > Power & Performance > CPU – Power Management Control	Turbo Boost	Enabled	When disabled, turns off Intel® Turbo Boost Technology.
	Intel Speed Shift Technology	Enabled	When disabled, turns off Intel® Speed Shift Technology.
	Intel Speed Step	Enabled	When disabled, turns off Intel Speed Step® technology.
	Energy Efficient Turbo	Disabled	When enabled, turbo frequency is opportunistically lowered to increase efficiency
	HWP Autonomous EPP Grouping	Disabled	When enabled, HWP autonomous requests same p-state for all cores with same EPP value
Intel Advanced Menu > Power &Performance > GT Power Management Control	GT Max Turbo Frequency	300MHz	When set, the GT Max Turbo Frequency is set to the selected value.

Software can detect Intel® Speed Shift technology support using the CPUID instruction. Below are the model-specific registers (MSRs) to be used to configure P-Cores, e-cores, and the LLC/Ring with Intel® Speed Shift technology for this specific example:

MSR details	Setting	Comment
HWP Enable MSR Register: IA32_PM_Enable Address: 0x770	0x1	Switches on Hardware P-States
HWP Request MSR Register: IA32_HWP_REQUEST Address: 0x774	#P-Cores core 0: 0xf000000080002006 core 1: 0xf000000081002006 core 2: 0xf000000082002006 core 3: 0xf000000083002006 core 4: 0xf0000000002e2e2e core 5: 0xf0000000002e2e2e #E-Cores core 6: 0xf000000085001204 core 7: 0xf000000086001204 core 8: 0xf000000087001204 core 9: 0xf000000088001204 core 10: 0xf000000089001204 core 11: 0xf00000008a001204 core 12: 0xf00000008b001204 core 13: 0xf00000008c001204	Set's the frequencies and preferences per core. Used by the OS to provide hints (min, max, desired, energy performance preferences to HWP)
HWP Capabilities MSR Register: IA32_HWP_CAPABILITIES Address: 0x771		Lists HWP performance range
Ring Ratio Limit MSR Register: MSR_RING_RATIO_LIMIT Address: 0x620	0x1E1E	Sets the minimum and maximum frequency ratio of the LLC/Ring

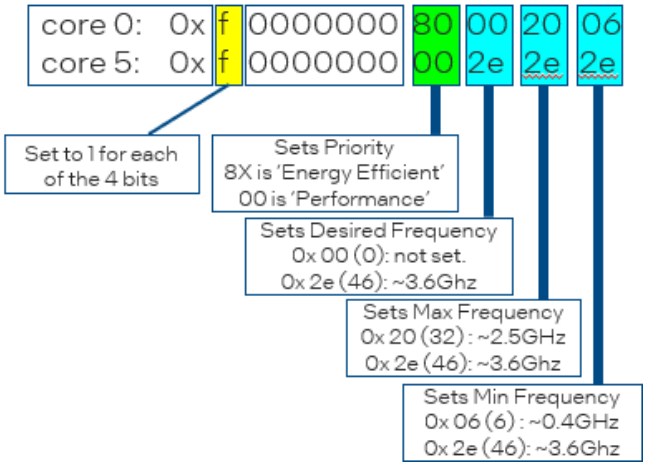

Figure 3: Intel® Speed Shift Technology settings per core frequencies.

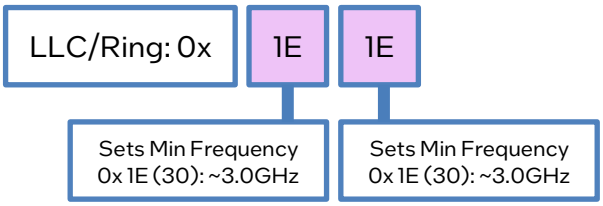

Figure 4: Intel® Speed Shift Technology settings for LLC/Ring frequencies.

Generally, the following formulas should be used to arrive at the right frequency settings:

Performance Cores:

	'Desired Frequency in GHz' * 10 *1.27		**= Decimal-**	**→ Hex- Setting**
2.5 GHz example:	2.5	* 10 *1.27	= 32	→ 0x20
3.6 GHz example:	3.6	* 10 *1.27	= 46	→ 0x2e
0.4 GHz example:	0.4	* 10 *1.27	= 6	→ 0x06

Efficiency Cores:

	'Desired Frequency in GHz' * 10 *1.0		**= Decimal-**	**→ Hex-Setting**
1.8 GHz example:	1.8	* 10 *1.0	= 18	→ 0x12
0.4 GHz example:	0.4	* 10 *1.0	= 4	→ 0x04

LLC/Ring (Un-core)

	'Desired Frequency in GHz' * 10 *1.0		**= Decimal-**	**→ Hex-Setting**
3.0 GHz example:	3.0	* 10 *1.0	= 30	→ 0x1E

The amount of throttling occurring on other cores heavily depends on the total load applied by the customer as well as the thermal solution used. If needed customers should evaluate using lower frequency settings than the ones described in this enveloping configuration. Especially for the graphics it may be best to set the frequency to the

lowest value that fulfills the workload requirements to reduce throttling of the LLC/Ring.

SKU	# of cores	Base Frequency	TDP	Temperature & use condition	Cores w/ higher frequency	Rest of p-cores	E-cores:	GfX
Intel® Core™ i7-13800HRE (RPL H682)	6 P-cores 8 E-cores	2.5GHz	45W	Extended Temp Industrial use condition	2 of n P-Cores fixed at 3.6GHz	n-2 P-Cores, max frequency at HFM (2.5GHz)	All e-cores, max frequency at HFM (1.8 GHz)	Max frequency at HFM
					Performance Setting (No throttling)	Energy efficiency setting (Will be throttling as needed)		

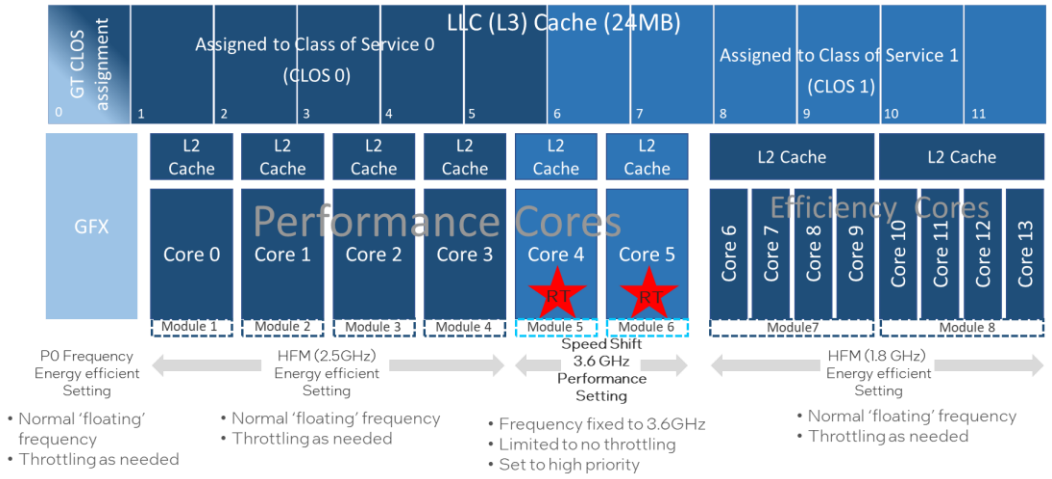

Figure 5: Example of Intel(r) Speed Shift configuration for edge ompute applications

As mentioned in the previous section, using Intel® Speed Shift technology in that manner may impact reliability and overall system performance.

For customers under NDA Intel provides a reliability assessment for the described configuration. This information is available in the Intel® TCC User Guide (RDC #786715). This allows customers to confidently configure their systems to increase the performance of real-time workloads running on specific cores when setting the Max-frequencies at or below the prescribed values, 3.6GHz for up to two cores and HVM on all remaining cores and GFX. While Intel® Turbo Technology is enabled, cores can only reach the prescribed max frequencies, never reaching the much higher turbo frequency of that processor. Depending on the thermal solution used and the workloads running, lower Max-frequencies may be more suitable to avoid throttling of the non-RT cores.

3.10 Using Timed-GPIO

Sometimes it's not enough for software to be told what the current OS/CPU time is "now". For example, when precision time synchronization is an application requirement it can be extremely useful to verify (at least in the lab) the accuracy of the CPU's notion of "now" using a hardware signal to represent ground truth. This is facilitated with a pair of one or more Timed-GPIO (TGPIO) pins that generate a hardware high voltage at precisely the moment the time "ticks" to the next second, followed by a return to low voltage / ground. This aptly named Pulse Per Second (PPS) is commonly used to test synchronization between hardware components as for example:

- Connect both the TGPIO and the PPS of a PTP-capable hardware component (e.g., an Ethernet NIC such as Intel® Ethernet Controller i226) to an oscilloscope, allowing the test engineer to measure the worst-case time difference between the two signals (which, if synchronized, will both go from low to high simultaneously). This is particularly useful to measure the difference in time accuracy between a NIC and the CPU when PCIe PTM is enabled vs. disabled.

Intel's TGPIO driver triggers a pulse per second (PPS) continuously when installed, allowing engineers to check synchronization or align synchronization to the signal on the TGPIO pin. The TGPIO PPS driver is available in mainline Linux.

4.0 Terminology

Terminology

Term	Description
API	Application Programming Interface
ASPM	Active State Power Management
BKC	Best Known Configuration
BSP	Board Support Package
C-State	A core power state requested by the Operating System Directed Power Management (OSPM) infrastructure that defines the degree to which the process is “sleeping”.
CAT	Cache Allocation Technology
CBM	Capacity Bit Mask
CMF	Coherent Memory Fabric
COS	Class of Service
CPS	Cyber-physical systems
CRBs	Customer Reference Boards
Deadline	The time when some computation or data must complete or arrive. For some applications, computations or data that arrive late are no longer useful.
E2E	End-to-end
ECC	Error-correcting-code
EDS	External Design Specification
FuSA	Functional Safety
IFWI	Integrated Firmware Image
IHS	Integrated Heat Spreader
Intel® RDT	Intel® Resource Director Technology
TCC	Time Coordinated Computing A modern approach to architecting distributed, synchronized, scalable computing systems that address real-time application requirements for cyber-physical systems (CPS). TCC moves beyond traditional real-time systems based on simple microcontrollers.

Term	Description
IOSF	Input/Output Scalable Fabric
IoT	Internet of Things
Jitter	The difference between the maximum and minimum of some quantity, such as latency measured in units of time. Jitter matters a lot at sensors and actuators, but other mechanisms (such as TSN mechanisms) typically hide software-execution jitter (so long as WCET bounds are satisfied).
KPI	Key Performance Indicator
LCC	Low Core Count
L2	Level 2 cache
L3/LLC	Last level cache
Latency	The duration of time between two events; for example, the time a signal is detected, and a response is received, or the time between an application sending a UDP message until it arrives on the Ethernet wire, or the time required to execute a code segment.
MSR	Model-specific registers are a group of registers available primarily for the operating-system or executive procedures (that is, code running at privilege level 0). These registers control items such as the following: • debug extensions • performance-monitoring counters • machine- check architecture • memory type ranges (MTRRs)
MMIO	Memory Map IO
MVC	Multi Virtual Channel
Noisy neighbor	An application or device, the functioning of which, affects the device or application with temporal requirements (e.g., because of shared resources). Temporal Isolation seeks to reduce the deleterious effect of a noisy neighbor.
OPC UA	A platform-agnostic standard for communication between devices using an “Unified Architecture”, created by the OPC Foundation focusing on the needs of industrial automation.
OSPM	Operating System Directed Power Management
P-State	A power-performance, implantation-dependent state of devices or processors that indicate power and frequency levels.

Term	Description
PCH	Platform Controller Hub
PCS	Physical Coding Sublayer
PCIe*	Peripheral Component Interconnect express*
PM	Power Management
PPS	Pulse Per Second
PTM	Precision Time Measurement, specified by the PCI SIG
PREEMPT_RT	The PREEMPT_RT patch (also the -rt patch or RT patch) makes Linux* into a Real-Time Operating System (RTOS) to a large degree.
RCU	Read-Copy-Update
RDC	Resource & Design Center
Real-time application	An application that requires a complete execution within some WCET with a specified level of reliability. For example, “Has to finish running every millisecond without missing a deadline in 7 days.” Typically, a real-time application contains a sequence of three tasks: sense > compute > actuate and increasingly uses a network to interconnect these. The extent to which a missed deadline impacts the overall system is sometimes described using “soft”, “firm”, and “hard” real-time, but we avoid these terms, preferring to quantify the reliability with number of 9s.
RTCP	Real-Time Compute Performance (Intel developed real-time performance benchmark)
RTOS	Real-Time Operating System
SA	System Agent
SGMII	Serial Gigabit Media-Independent Interface
SKU	Stock Keeping Unit
STA	Station Management
TBI	Ten-Bit Interface
TC	Traffic Classes
TDP	Thermal Design Power

Term	Description
Temporal Isolation	The degree to which a system can meet the time-related requirements of a real-time workload when the workload is running alongside other workloads on the system. In a typical system, concurrent workloads create contention for shared resources that can cause spikes in latency and increased jitter for the real-time workload. TCC capabilities help mitigate concurrent workload interference.
Time-Sensitive Networking (TSN)	A task-group of IEEE 802.1 that creates / amends the Ethernet and other standards, enabling dramatically better worst-case time performance (time-synchronization & latency). Also used to describe the standards / amendments from the TSN task group. https://1.ieee802.org/tsn/
Time synchronization	The degree to which two or more systems or devices agree on what time it is, to within some maximum error. Enables sensors, compute systems, actuators, and network elements to operate on a global schedule. Enables time-coordinated computing devices to time-division multiplex real-time and non-real-time tasks, measure latencies, and detect violation of deadlines. Enables an RTOS to schedule a task at a specific time.
TGPIO	Timed-General Purpose I/O
UDP	User Datagram Protocol
UEFI	Unified Extensible Firmware Interface
VCs	Virtual Channels
Workload	An application that performs some useful computational work, including (perhaps) receiving input, performing computation, and generating an output.
WCET	Worst-case execution time. The maximum measured latency of the compute portion of an application, across multiple iterations. WCET relates to reliability, described by “the number of 9s”. For instance, reliability of two 9s refers to missing the deadline 1 out of 100 times.

§

Appendix A - Intel processors with Time Coordinated Computing Technology support

A.1 Intel® Xeon™ Processors with Intel® TCC support

Note: For the latest details on specific SKUs and platform capabilities, please refer to the information provided at: Intel® Xeon™ Processors

A.1.1 Intel® Xeon™ D-2700 and D-1700 Processors

The following SKUs provide support for Time Coordinated Computing Technology (check intel.com for the most up-to-date product information).

Intel® Xeon™ D-2700 and D-1700 processors with Intel® TCC support.

	D-2752TER	D-1746TER	D-1735TR	D-1715TER	D-1712TR
Use Condition	Embedded	Embedded	Embedded	Embedded	Embedded
Cores	12	10	8	4	4
TDP	77W	67W	59W	50W	40W
TCC	Yes	Yes	Yes	Yes	Yes

A.1.2 Intel® Xeon™ W-11000E Series Processors

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

Intel® Xeon™ W-11000E Series processors with Intel® TCC support

	W-11865MRE	W11865MLE
Use Condition	Industrial	Industrial
Cores	8	8
TDP	45W	25W
TCC	Yes	Yes

	W-11555MRE	W-11555MLE	W-11155MRE	W-11155MLE
Use Condition	Industrial	Industrial	Industrial	Industrial
Cores	6	4	4	6
TDP	45W	25W	35W	25W
TCC	Yes	Yes	Yes	Yes

A.2 Intel® Core™ Processors with Intel® TCC support

Note: For the latest details on specific SKUs and platform capabilities, please refer to the information provided at: Intel® Core™ Processors

A.2.1 14th Generation Intel® Core™ Processors (S Series)

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

14th Generation Intel® Core™ S-series Processors with Intel® TCC support (Corporate/Mainstream)

	i9-14900	i7-14700	i5-14500	i5-14400	i3-14100
Use Condition	PC Client	PC Client	PC Client	PC Client	PC Client
Cores[1]	24 (8 + 16)	20 (8 + 12)	14 (6 + 8)	10 (6 + 4)	8 (4 + 0)
TCC	Yes	Yes	Yes	Yes	Yes

	i9-14901E	I7- 14701E	I5- 14501E	I5- 14401E
Use Condition	PC Client	PC Client	PC Client	PC Client
Cores[2]	8 P-cores	8 P-cores	6 P-cores	6 P-cores
TCC	Yes	Yes	Yes	Yes

14th Generation Intel® Core™ S-series Processors with Intel TCC support (Low Power)

	I9-13900T	i7-14700T	i5-14500T	i5-14400T	i3-14100T
Use Condition	PC Client	PC Client	PC Client	PC Client	PC Client
Cores[1]	24 (8 + 16)	20 (8 + 12)	14 (6 + 8)	10 (6 + 4)	8 (4 + 0)
TCC	Yes	Yes	Yes	Yes	Yes

[1] Processor cores listed first are the total number of cores in the processor followed by the number of Performance-cores and number of Efficient-cores in parentheses.
[2] Processor cores listed first are the total number of cores in the processor followed by the number of Performance-cores and number of Efficient-cores in parentheses.

	i9-14901TE	I7-14701TE	I5-14501TE	I514401TE
Use Condition	PC Client	PC Client	PC Client	PC Client
Cores[1]	8 P-cores	8 P-cores	6 P-cores	6 P-cores
TCC	Yes	Yes	Yes	Yes

A.2.2 13th Generation Intel® Core™ Processors (U/P/H Series)

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

13th Generation Intel® Core™ U-Series Processors (15W) with Intel® TCC support

	i7-1365UE	i5-1345UE	I5-1335UE	i3-1315UE
Use Condition	Gen Embedded	Gen Embedded	Gen Embedded	Gen Embedded
Cores[1]	10 (2 + 8)	10 (2 + 8)	10 (2 + 8)	6 (2 + 4)
TCC	Yes	Yes	Yes	Yes

	i7-1365URE	i5-1345URE	i3-1315URE	I7-1366URE (Fusa)
Use Condition	Industrial	Industrial	Industrial	Industrial
Cores[1]	10 (2 + 8)	10 (2 + 8)	6 (2 + 4)	10 (2 + 8)
TCC	Yes	Yes	Yes	Yes

13th Generation Intel® Core™ P-Series Processors (28W) with Intel® TCC support

	i7-1370PE	i5-1350PE	i5-1340PE	i3-1320PE
Use Condition	Gen Embedded	Gen Embedded	Gen Embedded	Gen Embedded
Cores[1]	14 (6 + 8)	12 (4 + 8)	12 (4 + 8)	8 (4 + 4)
TCC	Yes	Yes	Yes	Yes

[1] Processor cores listed first are the total number of cores in the processor followed by the number of Performance-cores and number of Efficient-cores in parentheses.

	i7-1370PRE	i5-1350PRE	i3-1320PRE	I7-1375PRE (Fusa)
Use Condition	Industrial	Industrial	Industrial	Industrial
Cores[1]	14 (6 + 8)	12 (4 + 8)	8 (4 + 4)	14 (6 + 8)
TCC	Yes	Yes	Yes	Yes

13th Generation Intel® Core™ H-Series Processors (45W) with Intel® TCC support

	i7-13800HE	i5-13600HE	i3-13300HE
Use Condition	Gen Embedded	Gen Embedded	Gen Embedded
Cores[1]	14 (6 + 8)	12 (4 + 8)	8 (4 + 4)
TCC	Yes	Yes	Yes

	i7-13800HRE	i5-13600HRE	i3-13300HRE
Use Condition	Industrial	Industrial	Industrial
Cores[1]	14 (6 + 8)	12 (4 + 8)	8 (4 + 4)
TCC	Yes	Yes	Yes

A.2.3 13th Generation Intel® Core™ Processors (S Series)

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

13th Generation Intel® Core™ S-series Processors with Intel® TCC support (Corporate/Mainstream)

	i9-13900	i7-13700	i5-13500	i5-13400	i3-13100
Use Condition	PC Client	PC Client	PC Client	PC Client	PC Client
Cores[1]	24 (8 + 16)	16 (8 + 8)	14 (6 + 8)	10 (6 + 4)	4 (4 + 0)
TCC	yes	Yes	Yes	Yes	Yes

[1] Processor cores listed first are the total number of cores in the processor followed by the number of Performance-cores and number of Efficient-cores in parentheses.

	i9-13900E	i7-13700E	i5-13500E	i5-13400E	i3-13100E
Use Condition	Embedded	Embedded	Embedded	Embedded	Embedded
Cores[1]	24 (8 + 16)	16 (8 + 8)	14 (6 + 8)	10 (6 + 4)	4 (4 + 0)
TCC	Yes	Yes	Yes	Yes	Yes

13th Generation Intel® Core™ S-series Processors with Intel® TCC support (Low Power)

	i7-13700T	i5-13500T	i3-13100T
Use Condition	PC Client	PC Client	PC Client
Cores[1]	16 (8 + 8)	14 (6 + 8)	4 (4 + 0)
TCC	Yes	Yes	Yes

	i9-13900TE	i7-13700TE	i5-13500TE	i3-13100TE
Use Condition	Embedded	Embedded	Embedded	Embedded
Cores[1]	24 (8 + 16)	16 (8 + 8)	14 (6 + 8)	4 (4 + 0)
TCC		Yes	Yes	Yes

A.2.4 12th Generation Intel® Core™ Processors (S-Series)

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

12th Generation Intel® Core™ S-series Processors with Intel® TCC support

	i9-12900E	i7-12700E	i5-12500E	i3-12100E
Use Condition	Embedded	Embedded	Embedded	Embedded
Cores[2]	16 (8 + 8)	12 (8 + 4)	6 (6 + 0)	4 (4 + 0)
TDP	65W	65W	65W	65W
TCC	Yes	Yes	Yes	Yes

[1] Processor cores listed first are the total number of cores in the processor followed by the number of Performance-cores and number of Efficient-cores in parentheses.
[2] Processor cores listed first are the total number of cores in the processor followed by the number of Performance-cores and number of Efficient-cores in parentheses.

A.2.5 11th Generation Intel® Core™ Processors (UP3 Series)

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

11th Generation Intel® Core™ UP3-Series Processors with Intel® TCC support

	i7-1185GRE	I5-1145GRE	I3-1115GRE
Use Condition	Industrial	Industrial	Industrial
Cores	4	4	2
TDP	28W	28W	28W
TCC	Yes	Yes	Yes

A.3 Intel Atom® Processors with Intel® TCC support

Note: For the latest details on specific SKUs and platform capabilities, please refer to the information provided at: Intel Atom® Series Processors

A.3.1 Intel Atom® x7000E, x7000RE, and x7000C Series Processors

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

Intel Atom® x7000RE Series Processors with Intel® TCC support (Industrial)

	X7211RE	X7213RE	X7433RE	X7835RE
Use Condition	Embedded, Industrial, and Communication			
Cores	2	2	4	8
TDP	6W	9W	9W	12W
TCC	Yes	Yes	Yes	Yes
FuSa	No	No	No	No

Intel Atom® x7000C Series Processors with Intel® TCC support (Communication)

	X7203C	X7405C	X7809C
Use Condition	Embedded and Communication		
Cores	2	4	8
TDP	9W	12W	25W
TCC	Yes	Yes	Yes
FuSa	No	No	No

Intel Atom® x7000E Series Processors with Intel® TCC support

	X7211E	X7425E	X7213E
Use Condition	Embedded		
Cores	2	4	2
TDP	6W	12W	10W
TCC	Yes	Yes	Yes

	X7211E	X7425E	X7213E
FuSa	No	No	No

A.3.2 Intel Atom® x6000E Series Processors

The following SKUs provide support for Intel® TCC (check intel.com for the most up-to-date product information).

Intel Atom® x6000E Series Processors with Intel® TCC support

	x6212RE	X6414RE	X6425RE	X6200FE	X6427FE
Use Condition	Industrial	Industrial	Industrial	Industrial	Industrial
Cores	2	4	4	2	4
TDP	6W	9W	12W	4.5W	12W
TCC	Yes	Yes	Yes	Yes	Yes
FuSa	No	No	No	Yes	Yes

Intel Atom® x6000E Series Performance Upgrade Processors with Intel® TCC support

	X6214RE	X6416RE
Use Condition	Industrial	Industrial
Cores	2	4
TDP	6W	9W
TCC	Yes	Yes
FuSa	No	No