Intel® 800 Series Chipset Family Platform Controller Hub (PCH)

Specification Update

Revision 001

October 2024

832375-001

Contents

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Revision History

Revision	Description	Release Date
001	• Initial release	October 2024

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1 Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents table. This document is a compilation of device and document errata and specification clarifications and changes. It is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into the specification update and are no longer published in other documents. This document may also contain information that has not been previously published.

1.1 Affected Documents

Document Title	Document Number
Intel® 800 Series Chipset Family Platform Controller Hub (PCH) Datasheet, Volume 1 of 2	833778
Intel® 800 Series Chipset Family Platform Controller Hub (PCH) Datasheet, Volume 2 of 2	834576
Intel® Core™ Ultra 200S Series Processors Datasheet, Volume 1 of 2	832586
Intel® Core™ Ultra 200S Series Processors Datasheet, Volume 2 of 2	834966

1.2 Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

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2 Identification Information

2.1 Marking

Table 2-1. PCH Lines Component Identification

PCH Stepping	Top Marking	Notes
B0	SRPEZ	Desktop Intel® Z890 Chipset

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3 Summary Tables of Changes

The following tables indicate the Specification Changes, Errata, Specification Clarifications, or Documentation Changes, which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

3.1 Codes Used in Summary Table

Status	Description
Doc	Document change or update that is implemented.
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel® hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.
N/A	This erratum is not applicable to the listed product/stepping or the Specification Change does not apply to the listed product/stepping.
X	Specification Changes apply to the listed product/stepping.

3.2 Errata Summary Table

Erratum ID	Intel® 800 Series Chipset Stepping	Errata
	B0	
001	No Fix	Processor C-States With USB Full-Speed or Low-Speed Device Hotplug
002	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
003	No Fix	I^2S Audio Channels Swapped With High Frame Polarity in Device Mode
004	No Fix	xHCI Out of Order ACK Due to LCRD1
005	No Fix	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
006	No Fix	SPI0 Dual IO Mode With SPI0_IO2 And SPI0_IO3 Connected to SPI Device
007	No Fix	Non-Responsive USB Port After Disconnecting Full-speed Device

3.3 Specification Changes

No.	Specification Changes
	No specification changes for this revision of the specification update.

3.4 Specification Clarifications

No.	Specification Clarifications
	No specification clarifications for this revision of the specification update.

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4 Errata Details

001	Processor C-States With USB Full-Speed or Low-Speed Device Hotplug
Problem	When doing a hotplug on a USB hub with two or more USB Full-speed or Low-speed devices each with a 1 ms service interval interrupt endpoint, a race condition may occur between the PMC and the xHCI controller.
Implication	The processor may fail to enter C3 or deeper package C-States. Note: This erratum has only been observed in a synthetic environment.
Workaround	None identified. This condition is recovered after the xHCI controller has successfully entered D3.
Status	For the steppings affected, refer to the Summary Table of Changes.

002	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
Problem	On USB 3.2 Gen 1x1 only capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.
Implication	There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

003	I^2S Audio Channels Swapped With High Frame Polarity in Device Mode
Problem	When the I^2S interface is in device mode, the audio controller may not be correctly configured if the audio codec requires high frame polarity.
Implication	Due to this erratum, the left and right audio channels may swap when frame polarity is set to high.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

004	xHCI Out of Order ACK Due to LCRD1
Problem	A delay in the availability of LCRD1 (Link Credit 1) from a USB 3.2 hub, with two or more downstream USB 3.2 bulk endpoint devices engaged in SuperSpeedPlus concurrent transfers, may lead to the connected xHCI controller sending the ACK and Status of a transfer packet out of order.
Implication	Due to this erratum, a USB 3.2 bulk endpoint device may not respond to subsequent transfers. It may be possible for a device driver to recover the USB 3.2 device.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

005	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
Problem	The PTM Propagation Delay Adaptation Interpretation B (PTMPDAIB) Bit is implemented at Configuration Space (CFG) Offset 158h instead of at 50h as documented in the PCI-SIG PTM Byte Ordering Adaptation Engineering Change Notice (ECN).
Implication	End Point Device (EPD) software that implements the PTM Byte Ordering Adaptation ECN will not be able to program their PTMPDAIB Bit correctly since it is located at a different register offset.
Workaround	None identified. To mitigate this issue, EPD software that implements the PTM Byte Ordering Adaptation ECN must access PTMPDAIB at CFG Offset 158h.
Status	For the steppings affected, refer to the Summary Table of Changes.

006	SPI0 Dual IO Mode With SPI0_IO2 And SPI0_IO3 Connected to SPI Device
Problem	On systems with dual IO mode enabled, SPI0_IO2 and SPI0_IO3 may momentarily drive low before these signals are pulled high by internal resistors during boot from the G3 state.
Implication	Due to this erratum, unexpected system behavior may occur on systems when SPI0_IO2 and SPI0_IO3 signals are connected to an SPI device.
Workaround	None identified. To mitigate this erratum, do not connect SPI0_IO2 and SPI0_IO3 to an SPI device in SPI0 dual IO mode enabled systems.
Status	For the steppings affected, refer to the Summary Table of Changes.

007	Non-Responsive USB Port After Disconnecting Full-speed Device
Problem	Disconnecting a USB full-speed device from the USB port while the xHCI controller is in the process of sending the Start of Frame may cause the USB 2.0 functionality to become unresponsive for that specific port.
Implication	Due to this erratum, USB 2.0 devices may not be recognized on the USB port until a host controller reset occurs. Intel has only observed this behavior in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

5 Specification Changes

There are no specification changes in this revision of the Specification Update.

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6 Specification Clarification

There are no specification clarifications in this revision of the Specification Update.

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