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Intel® Infrastructure Processing Unit Adapter E2100-CCQDA2HL

Enables rapid innovation and seamlessly fits into a broad range of PCIe-compliant servers

Key Features

- Intel® IPU SoC E2100 with 200Gb Ethernet bandwidth
- Full-height, half-length, PCIe 4.0 x16 form factor
- Single-width, passive heatsink

- 2x QSFP56 ports
- Supports 2 x 100GbE, 4 x 25GbE, or 1x 200GbE interfaces
- RDMA with Falcon reliable transport and RoCEv2 protocols

Designed as a full-height half-length card with a 75W power envelope, the Intel® Infrastructure Processing Unit (Intel® IPU) Adapter E2100-CCQDA2HL with 200Gb Ethernet bandwidth that fits seamlessly into a broad range of PCIe-compliant servers. It features a rich packet-processing pipeline and includes NVMe, RDMA with Falcon reliable transport or RoCEv2 protocols, and compression and crypto accelerators. The E2100-CCQDA2HL delivers the high-performance infrastructure acceleration that data centers demand.

The Arm Neoverse N1 compute complex allows customer-provided software to execute features ranging from complex packet-processing pipelines to storage transport, device management, and telemetry. By combining acceleration hardware and software running in the compute complex, this IPU adapter enables the rapid innovation necessary for the modern data center.

Agile Platform for Flexible Deployments

The E2100-CCQDA2HL offers three main advantages to data center infrastructure managers and workloads running in Cloud, Enterprise, and Telco Cloud data centers.

Separation and isolation of infrastructure workloads. Whether tenants in a cloud environment or application workloads in an edge or enterprise environment, IPUs optimize host CPU applications by removing the infrastructure overhead from traditional host-based network and storage infrastructure applications.

Offload virtualized networks to the IPU, where the accelerators can process tasks more efficiently. For an IaaS, host CPUs can be used for more workload-intensive tasks and greater revenue.

Replace previously necessary local disk storage with detached virtualized storage. This architecture enables flexible allocation of disk storage, lowering overall costs.

Accelerators

A pivotal movement for large Cloud Service Providers is the shift from legacy network standards like TCP to modern protocols that deliver data with better latency, predictability, and enhanced performance. The Intel IPU SoC E2100 supports multiple hardened accelerators that enable the high performance, low latency, and better efficiency required in the new generation of data centers.

Falcon protocol over RDMA

Falcon is a hardware-assisted transport layer designed for high-performance, low-latency connections at scale in Ethernet data center networks. It enables easy deployment into existing networking infrastructure and supports backward compatibility with applications running on top of RDMA and NVMe interfaces.

RoCEv2 protocol over RDMA

RoCEv2 is a host-offload, kernel-bypass technology that enables direct memory-to-memory data communication between applications over a network. It provides high-throughput and low-latency performance for high-speed Ethernet by eliminating three major sources of networking overhead: TCP/IP networking stack processing, memory copies, and application context switches. RoCEv2 operates on top of UDP/IP and is routable over IP networks.

High-performance NVMe

NVMe delivers storage offload with built-in support for encryption and compression using the crypto and compression accelerator. Additionally, high-performance PCIe devices are exposed to the host processor, enabling infrastructure providers to implement their storage protocol of choice using the ARM cores on the IPU.

Inline Crypto Engine (ICE)

The ICE and the packet processor are part of the network subsystem pipeline and support IPSec and PSP full offload.

Lookaside Crypto and Compression Engine (LCE)

The LCE improves throughput on big data, file systems, and databases. Data in transit is intact using authenticity, integrity and privacy protocols. Data at rest provides device-level encryption, storage-level encryption, and data protection on disk.

Improved Packet Processing Efficiency

The flexible packet processor enables data-plane use cases such as network virtualization, microservices, physical networking, telemetry and several legacy and advanced use cases for Cloud, Enterprise, and Telco.

The packet processing engine supports up to 200Mpps and provides flexibility for defining and customizing the behavior of network data planes.

Dedicated Compute for Infrastructure Processing

The adapter compute complex is equipped with 16 Arm Neoverse N1 cores and is tightly coupled with the network subsystem.

The accelerators can access the system-level cache as the last-level cache, providing high-bandwidth and low-latency connections. A combination of hardware and software packet processing enables custom configuration.

Programmable Port Configuration

This adapter's port speed and number of ports can be configured on demand, reducing network adapter validation and simplifying deployment.

Use Cases

Intel® Infrastructure Processing Unit Software Development Kit (Intel® IPU SDK) is a software stack that runs on the compute complex. Developers can use it to create targeted customer solutions.

- **Artificial Intelligence:** Used as a front-end adapter in AI clusters to improve security, virtualized cloud and storage offload, and high-performance networking. Falcon or RoCEv2 RDMA can address long-tail latency in the scale-out network of a training cluster.
- **Tenant Hosting:** Virtualized network and storage functionality; abstraction interface for tenants to access cloud services; hosts customer control plane; provides custom device support.
- **Accelerators as a Service:** Enables network-to-device memory data path; provides service abstraction for access to devices while implementing functions like QoS.
- **Appliance:** Performs packet processing on a per-packet or per-flow basis; can soft terminate packets.
- **Smart Switch:** Multiple IPUs perform packet processing for select top-of-rack (ToR) packets.
- **Kubernetes Acceleration:** Offloads container networking and, optionally, container storage to the IPU.

Complete Software Framework

Intel demonstrates a robust commitment to Open Source software by promoting collaboration and innovation within the development community. Intel IPUs offer a wealth of developer-friendly features within its comprehensive software stack.

Intel IPU Adapter E2100-CCQDA2HL is designed with Intel IPU SoC E2100 and includes these features:
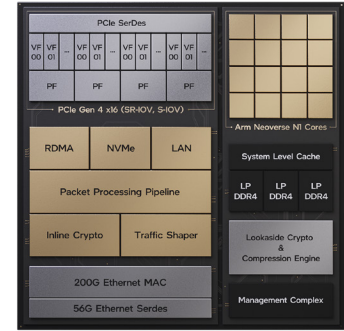
Ethernet

- 2x QSFP56 ports
- Supports 2x 100GbE, or 4x 25GbE with breakout cable, or 1x 200GbE interfaces

PCIe

- Up to 4 hosts
- PCIe 4.0 x16, SMBus
- PCIe CEM 4.0 (electrical) and PCIe CEM 5.1 (mechanical) specifications
- Up to 75W total adapter power delivered via standard PCIe CEM edge

Management Interface

- 1000BASE-T front panel RJ45 port to E2100 manageability
- 1x RJ45 Connector to Data Center Management Network Specification
- USB 2.0 high-speed interface per CEM 6 proposal

Packet Processing Engine

- P4 Programmable Pipeline with Inline IPsec, Hardware Connection Tracking and Stateful ACLs
- Up to 1M LPM Routes, up to 16M Exact Match Entries, 1M Meters/Policers/Shapers, TCAM and range tables
- Programmable Parsing, Multi-stage Match-Action, Mirroring, Multicast, Modification and Recirculation

Compute Complex

- 16 Arm Neoverse N1 cores with 64 KB L1 cache and 512 KB L2 cache per core
- Coherent Mesh Network Interconnect with 32MB System Level Cache (SLC)
- 3 channels of 16GB LPDDR4x memory totaling 48GB

Storage and NVMe Features

- NVMe Initiator Offload
- Customized Storage Protocols with AES-XTS and CRC offloads on the Compute Complex
- Hardware paths support up to 6M 4KB R/W IOPS simultaneously Security and Crypto
- NVMe storage device, total of 120GB

RDMA

- 200Gbps throughput
- RDMA with RoCEv2 standard libraries
- Falcon – reliable low-latency hardware transport
- Supports 6 physical functions (4x Intel Xeon Processors, 1x ARM compute complex, and 1x integrated management complex

Security

- Internal/External RoT, Secure Boot, Secure Debug, TRNG via management complex
- 200Gb Bulk Crypto per direction including TLS offload
- Lookaside Cryptography and Compression Engine (LCE)
- Support for chained operations
- Inline IPSec engine supports PSP AES-GCM 128/256
- Meets Security Standard SP800-193
- Trusted Platform Module 2.0

Software Stack

The programmable P4 stack including toolchain, debuggers, analyzers, and application-facing libraries enabling all the Intel IPU packet-processing capabilities.

- Storage offload support through industry-standard SPDK plugins
- Packet I/O support through both standard kernel interfaces and DPDK
- Supports Infrastructure Programmer Development Kit (IPDK)
- Supports DMTF Redfish

IPU OS Support

- Host: Rocky Linux, Red Hat
- ACC: Rocky Linux

Adapter Features

Data Rate Supported	200/100/25GbE
Bus Type/Bus Width	PCIe 4.0 x16
Controller	Intel IPU SoC E2100
Dimensions	169mm x111mm; full-height, half-length, single-width card, compliant with CEM 5.1 mechanical specification.

Certifications and Compliance

Hardware Certifications	cURus, CE, FCC, ICES, CB, UKCA, VCCI, ACMA, KCC, BSMI and Morocco
RoHS Compliance	EU RoHS, BMSI RoHS, EU WEEE, EU REACH, China RoHS

Supported Physical Layer Interfaces

	1x200GbE	2x100GbE	4x25GbE
DACs	200GBASE-CR4 (Port 0 only)	100GBASE-CR4 100GBASE-CR2	25GBASE-CR (Port 0 only)
Optics and AOCs	Class 6 (3.5 W) SR4 Commercial temp Optics transceivers and AOCs	Class 4 (3.5 W) SR4 commercial temp AOCs Class 4 (3.5 W) SR4 commercial temp optics transceivers Class 6 (4.5 W) DR1 commercial temp optics transceivers	Class 4 (3.5 W) SR4 commercial temp AOC breakouts

Technical Specifications

Storage Humidity	Maximum: 85% relative humidity at 25 °C
Storage Temperature	-40 °C to 70 °C (-40 °F to 158 °F)
Operating Temperature	0 °C to 45 °C (32 °F to 113 °F)

Product Order Code

Configuration	Product Code
Dual Port	E2100CCQDA2G1HL

Customer Support

For customer support options in North America visit:
intel.com/content/www/us/en/support/contact-support.html

Product Information

For information about Intel® Infrastructure Processing Units, visit: intel.com/ipu

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