

AGILEX™ 5 FPGA E-SERIES 065B PREMIUM DEVELOPMENT KIT

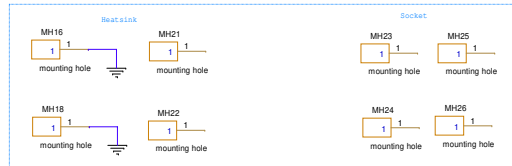
REV	DATE	PAGES	DESCRIPTION
A1	05/30/2024	A8	Initial Release
A2	09/23/2024	A8	Update to Altera logo, and Altera copy right declaration
B1			

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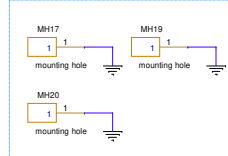
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 TA N20886-002

PBA N11816-101
 PB N18468-002
 PCB MPN 100-0330713-A2

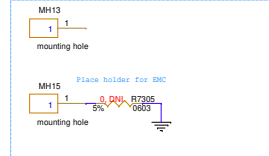
Mounting hole for FPGA



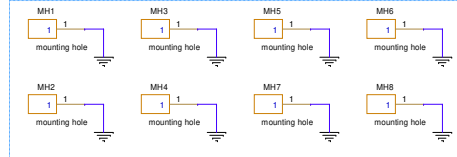
Mounting hole for HPS DC



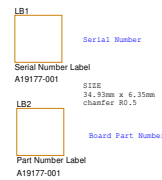
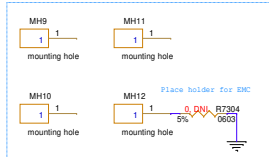
Mounting hole for top VR heatsink



Mounting hole for board



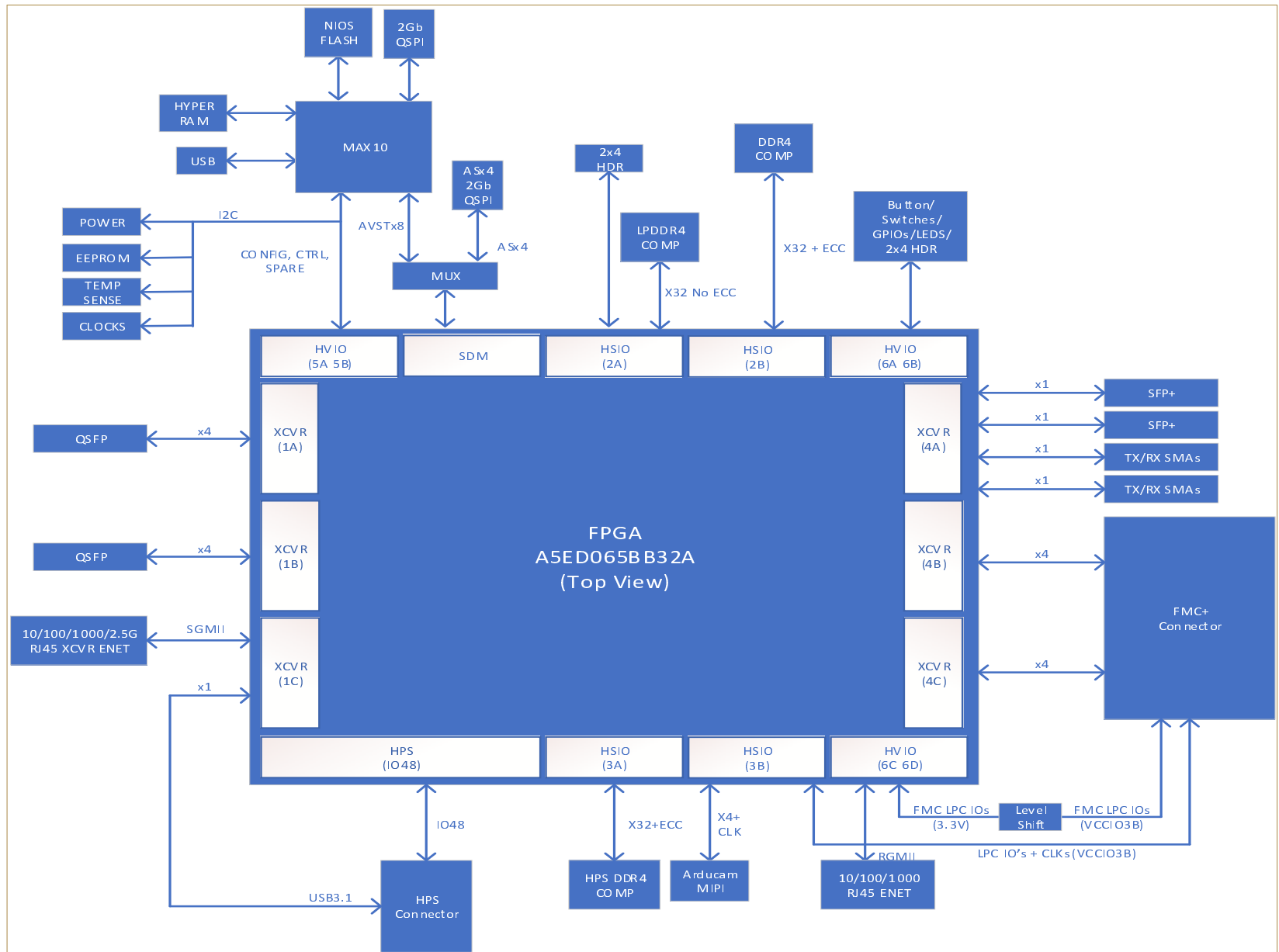
Mounting hole for bottom VR heatsink



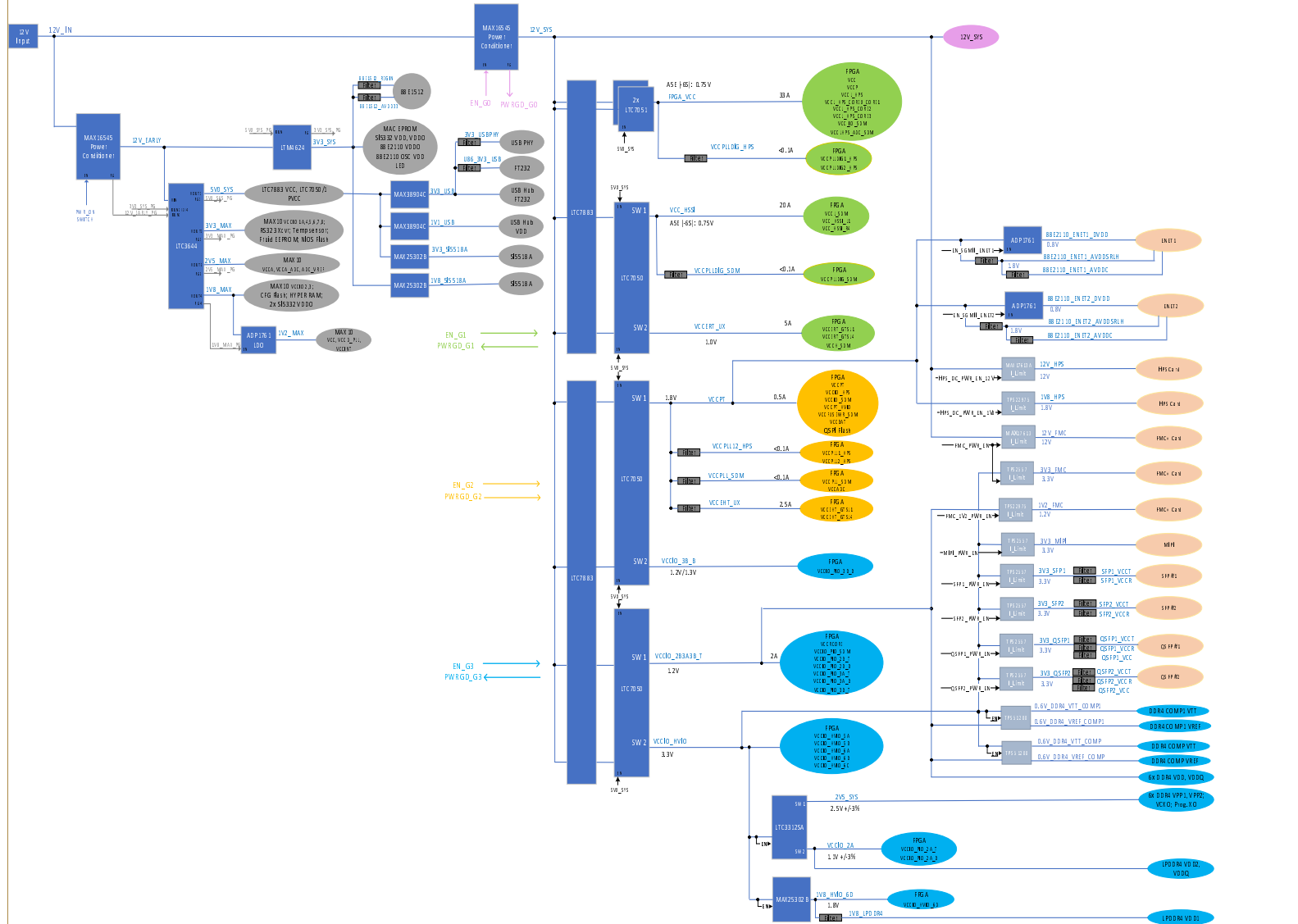
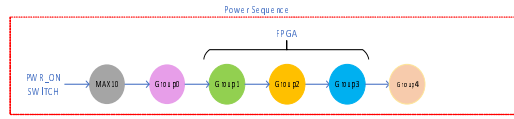
Pin information reference:
 A5ED065 ES Device
 B32A Version: 2023-07-03

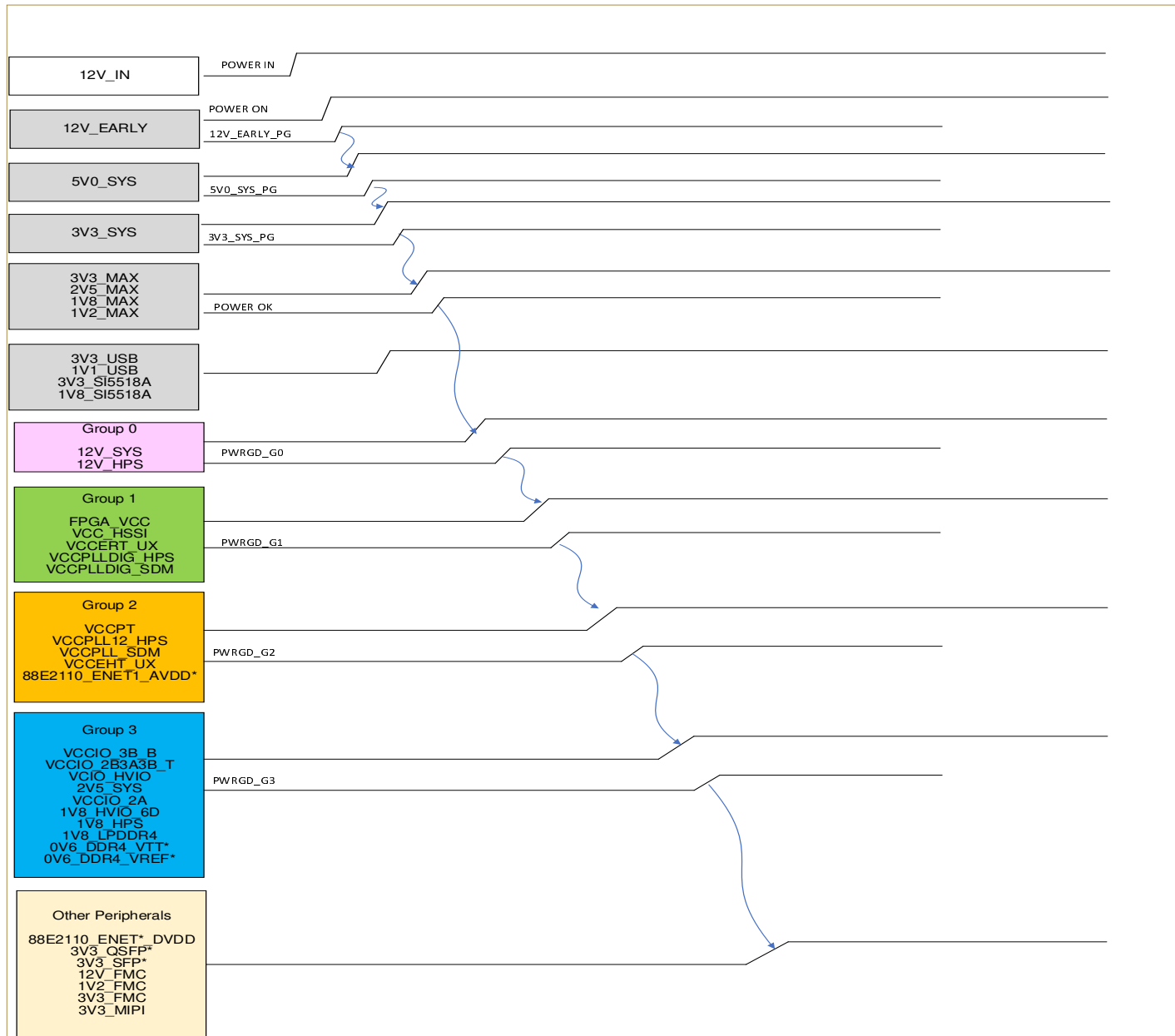


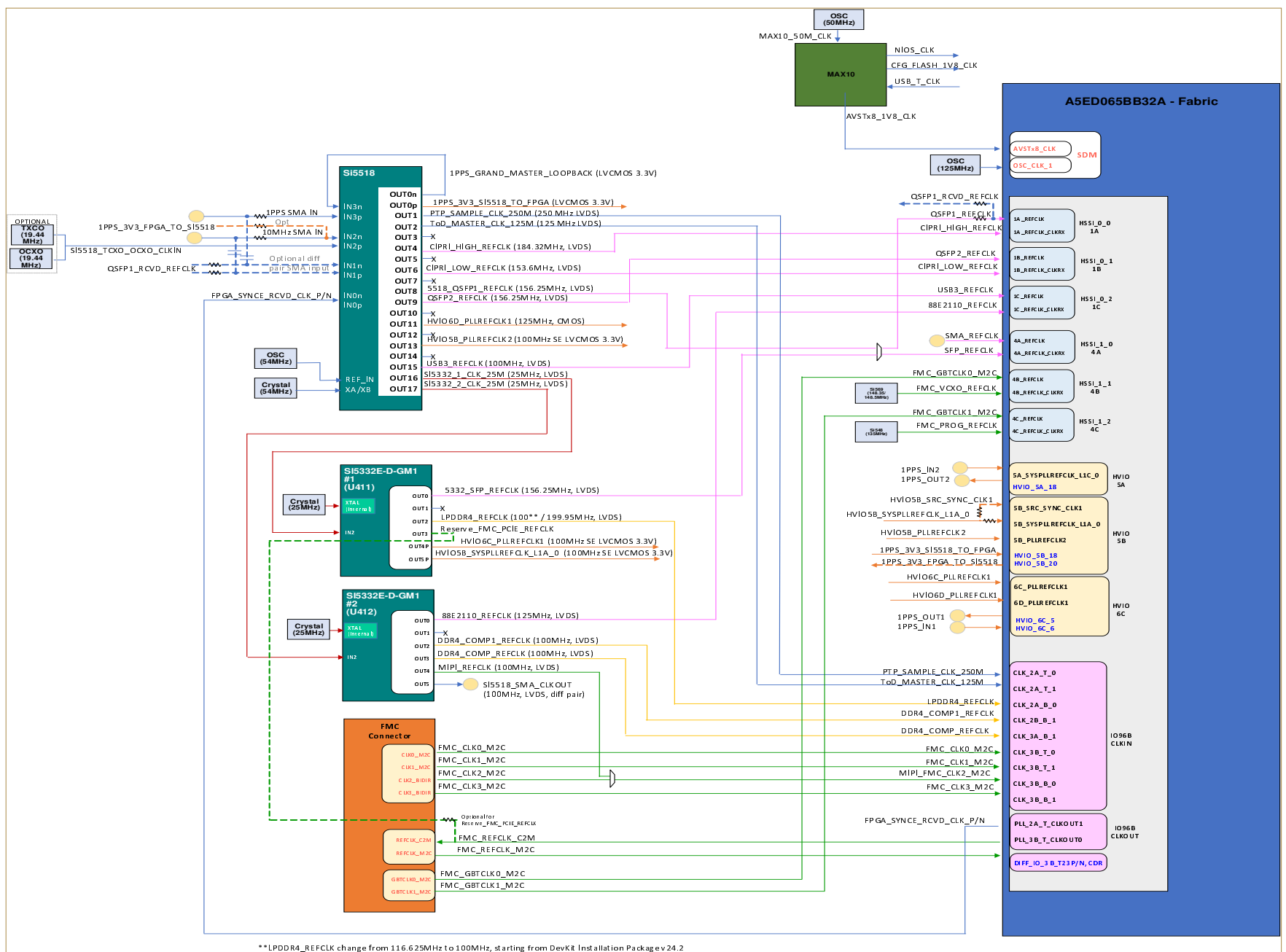
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Recommendation:
 Dev Kit power tree design are for reference.
 Recommend customer to scale power solution based on design requirements

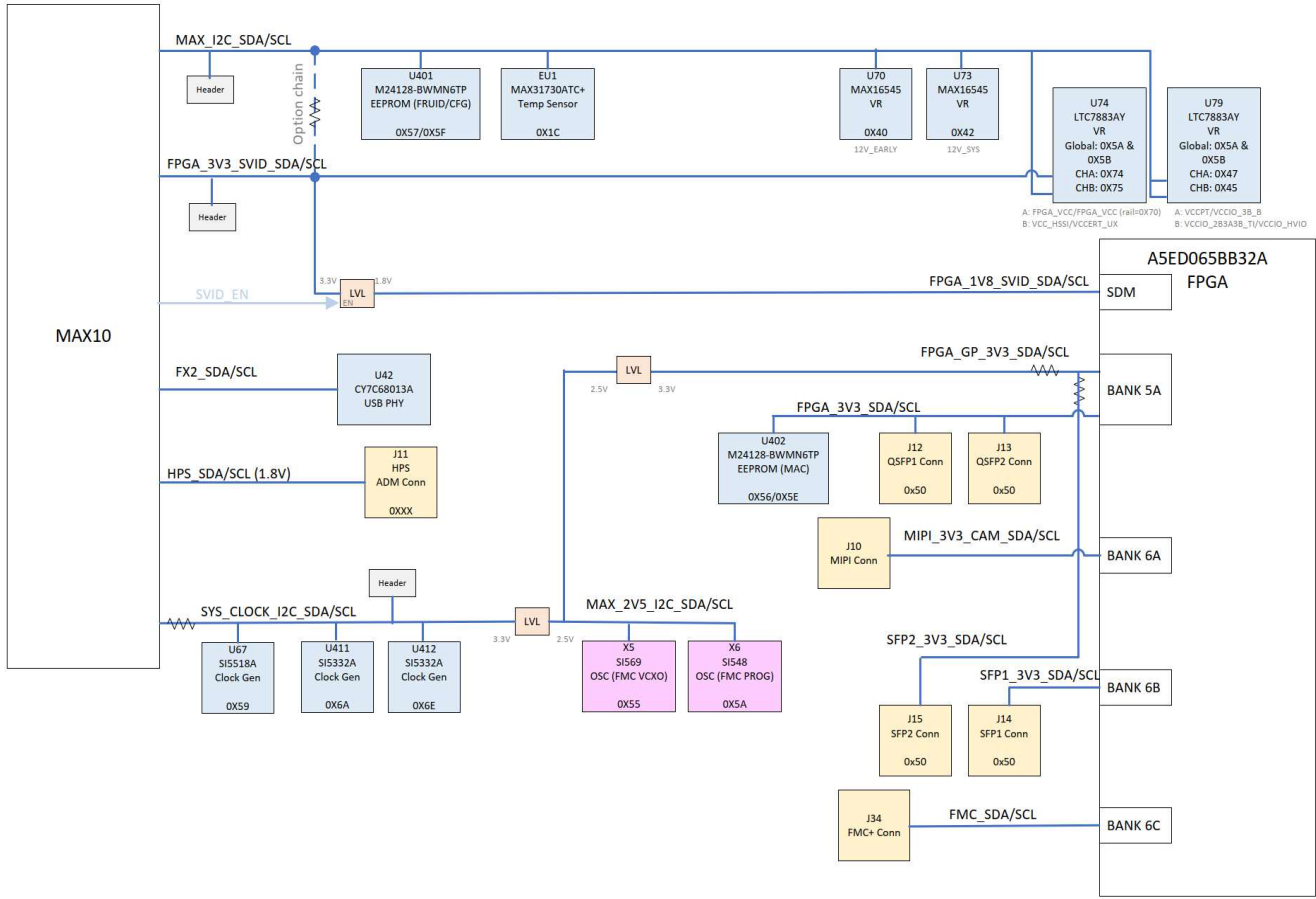




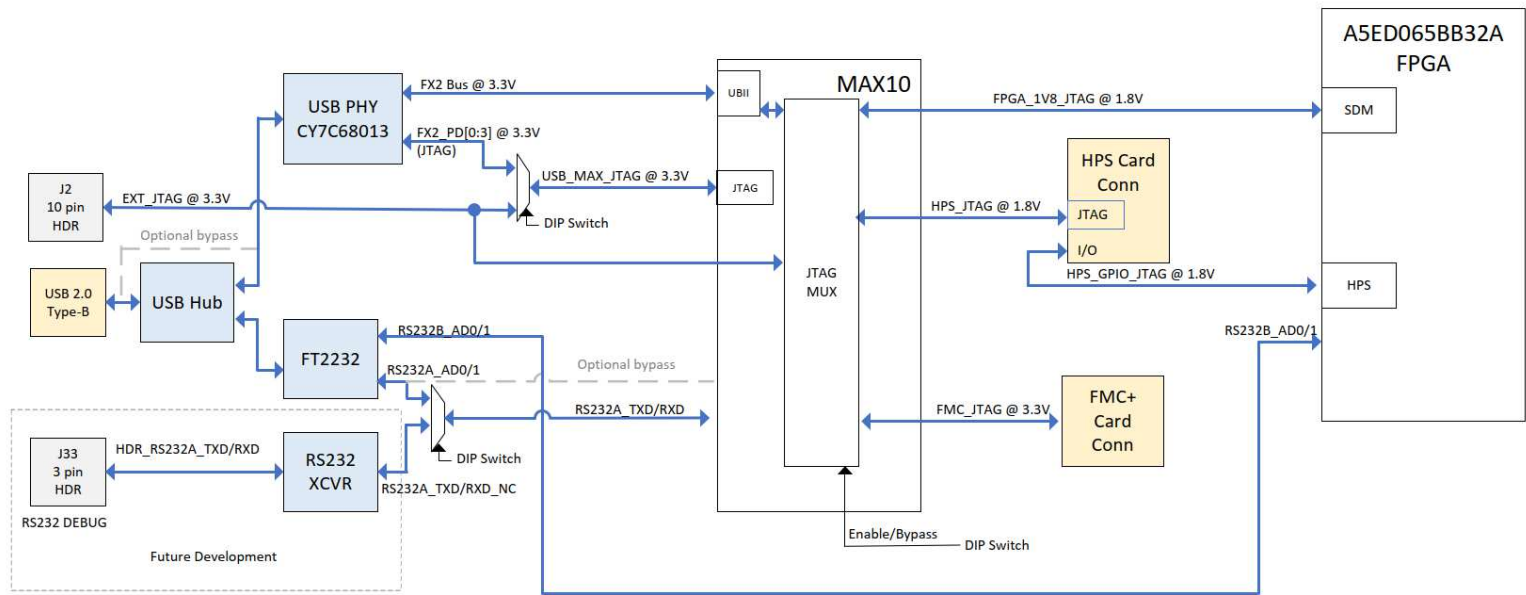


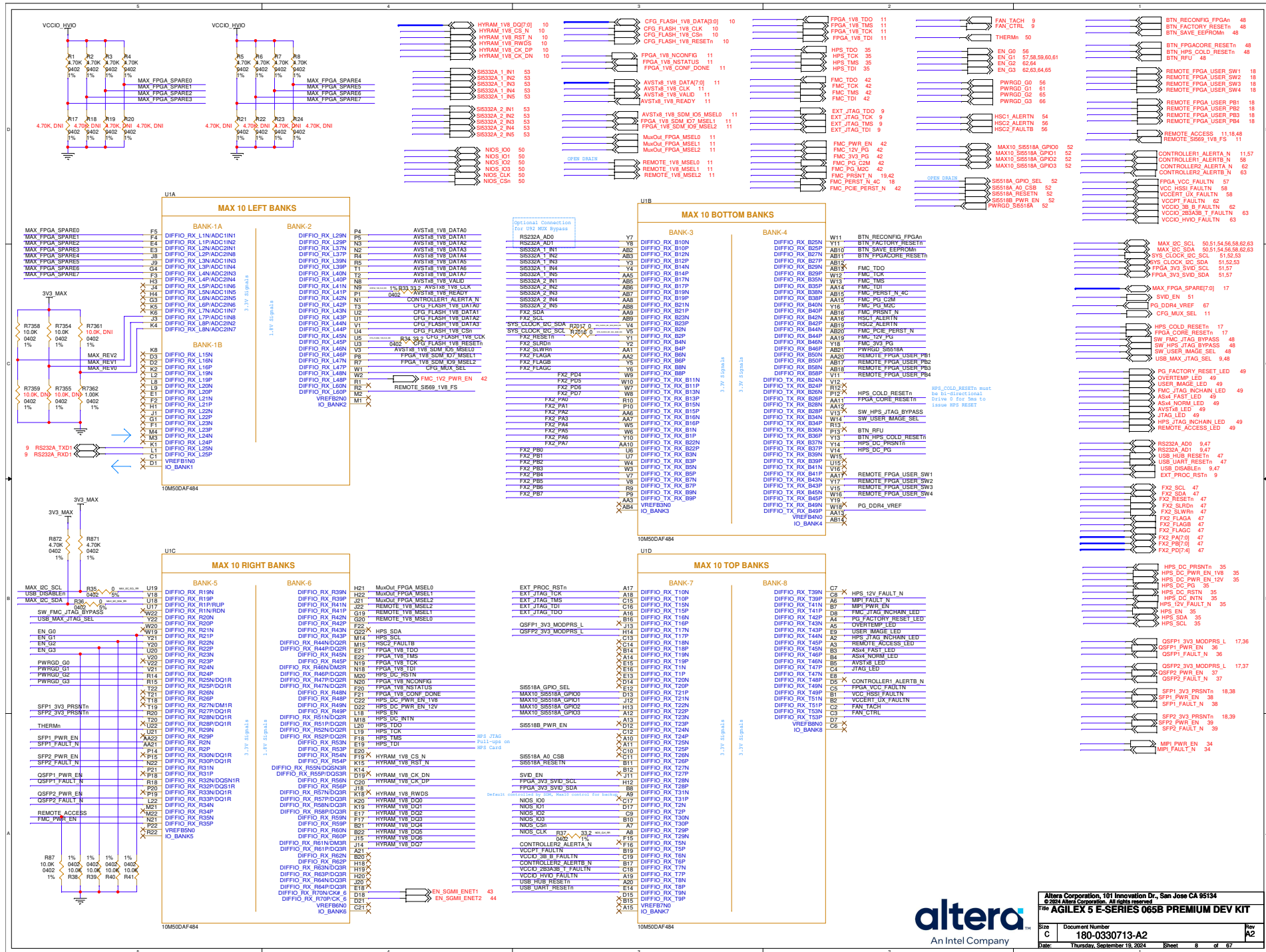
**LPDDR4_REFCLK change from 116.625MHz to 100MHz, starting from DevR8 Installation Package v 24.2

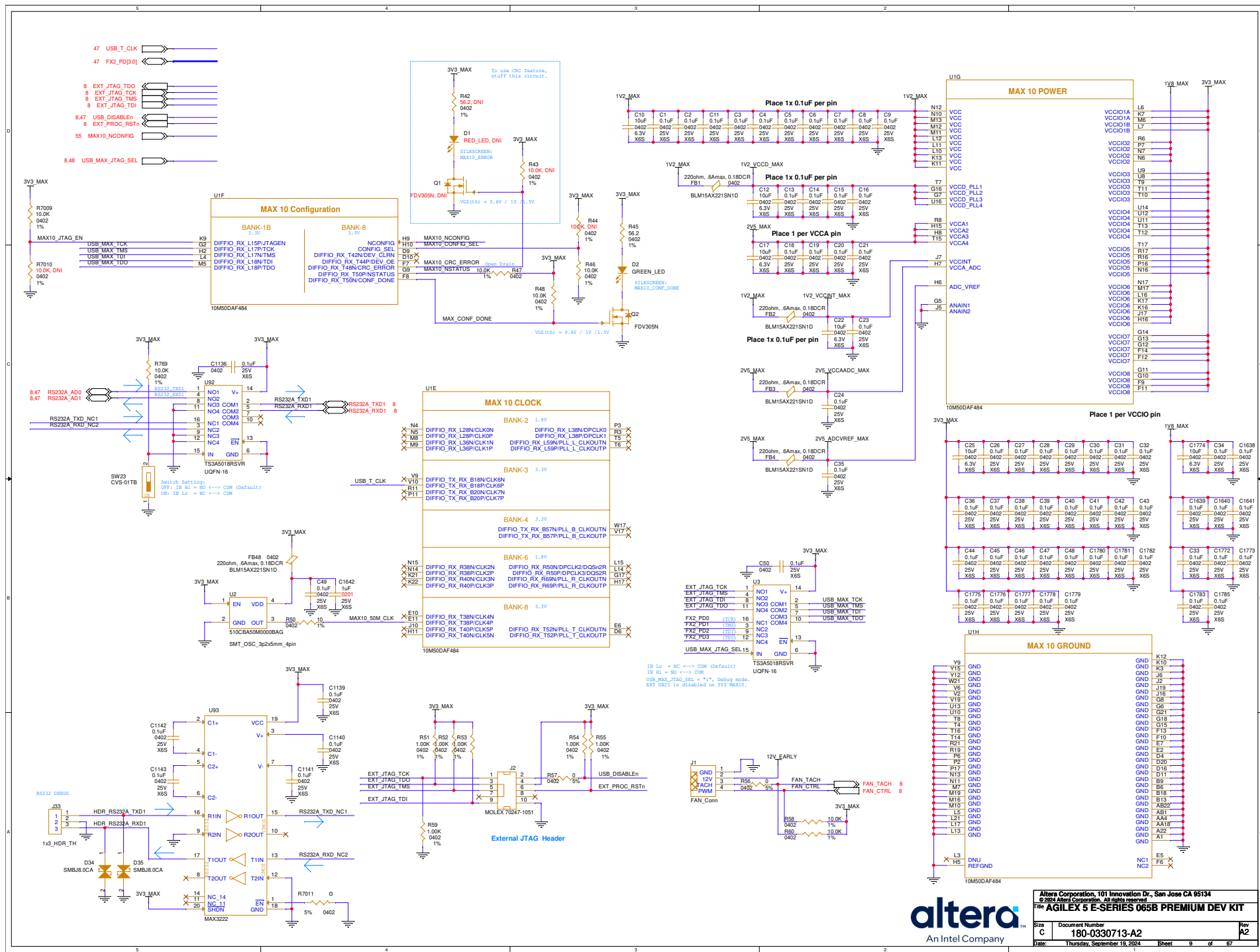




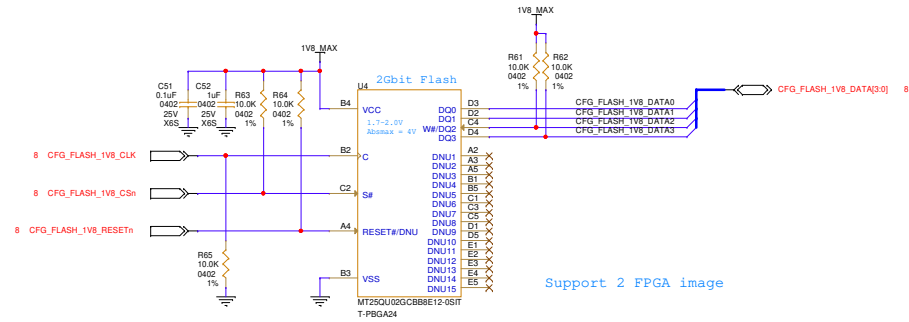
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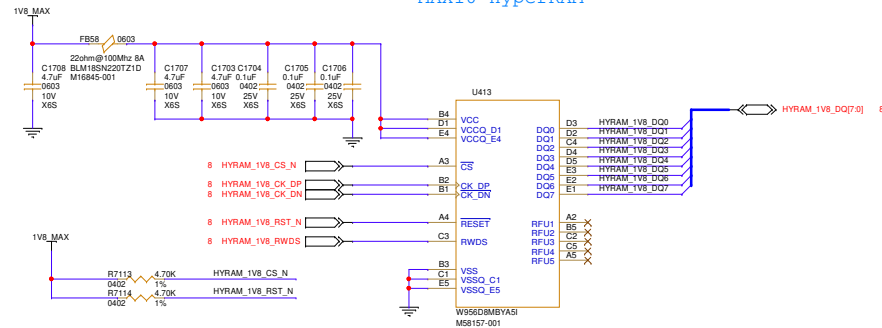




AVST CFG Flash



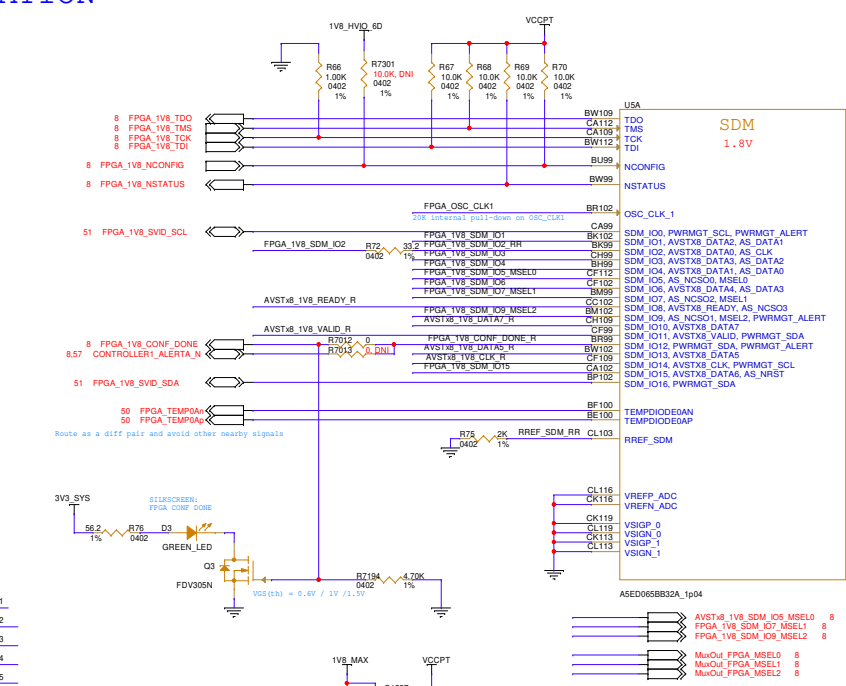
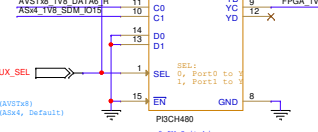
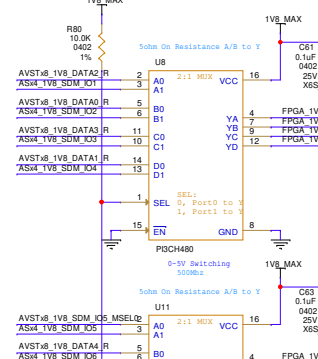
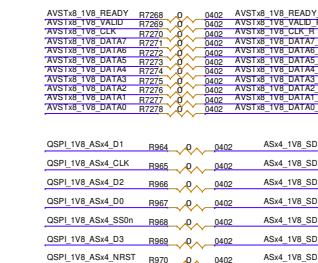
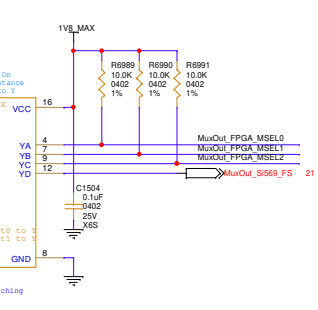
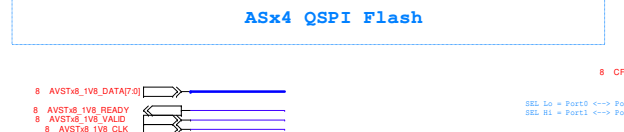
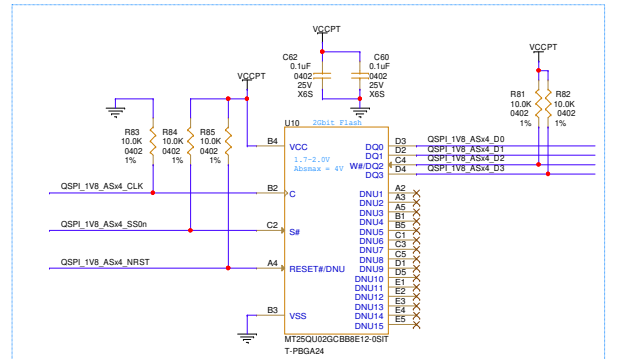
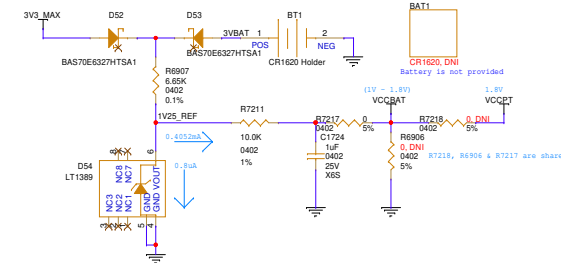
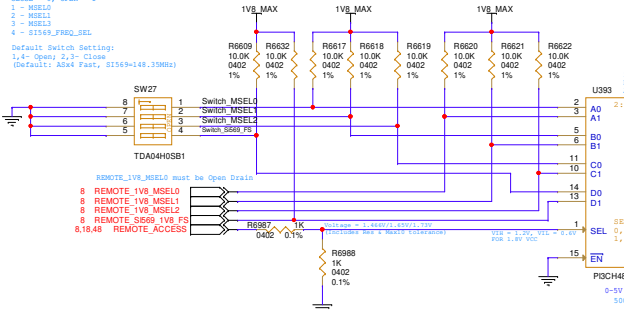
MAX10 HyperRAM



SDM CONFIGURATION

SLICESCREEN:
CLOSE = 0, OPEN = 1
1 = MSEL0
2 = MSEL1
3 = MSEL2
4 = S1649_FPGA_SEL

Default Switch Settings:
1-4: Open, 2-3: Close
(Default: A04 Fmt, S1649=148.33MHz)



Pins	MSEL	CFG_MUX_SEL = 0		CFG_MUX_SEL = 1	
		Avalon-ST x8	PWR_SCL	AS (normal mode)	PWR_SCL
SDM_IO0		AVSTx8_DATA2	AS_DATA1		
SDM_IO1		AVSTx8_DATA0	AS_CLK		
SDM_IO2		AVSTx8_DATA3	AS_DATA2		
SDM_IO3		AVSTx8_DATA1	AS_DATA0		
SDM_IO4	MSEL0	AVSTx8_DATA4	AS_nCS00		
SDM_IO6		AVSTx8_DATA4	AS_DATA3		
SDM_IO7	MSEL1	HPS_COLD_nRESET	AS_nCS02		
SDM_IO8		AVST_READY	AS_nCS03		
SDM_IO9	MSEL2		AS_nCS01		
SDM_IO10		AVSTx8_DATA7			
SDM_IO11		AVSTx8_VALID	HPS_COLD_nRESET		
SDM_IO12		CONF_DONE	CONF_DONE		
SDM_IO13		AVSTx8_DATA5			
SDM_IO14		AVSTx8_CLK			
SDM_IO15		AVSTx8_DATA6	AS_nRST		
SDM_IO16		PWR_SDA	PWR_SDA		

CONFIG MODE	MSEL2	MSEL1	MSEL0
A04 FMT	0	0	1
Default			
ASx4 NORM	0	1	1
AVSTx8	1	1	0
JTAG	1	1	1

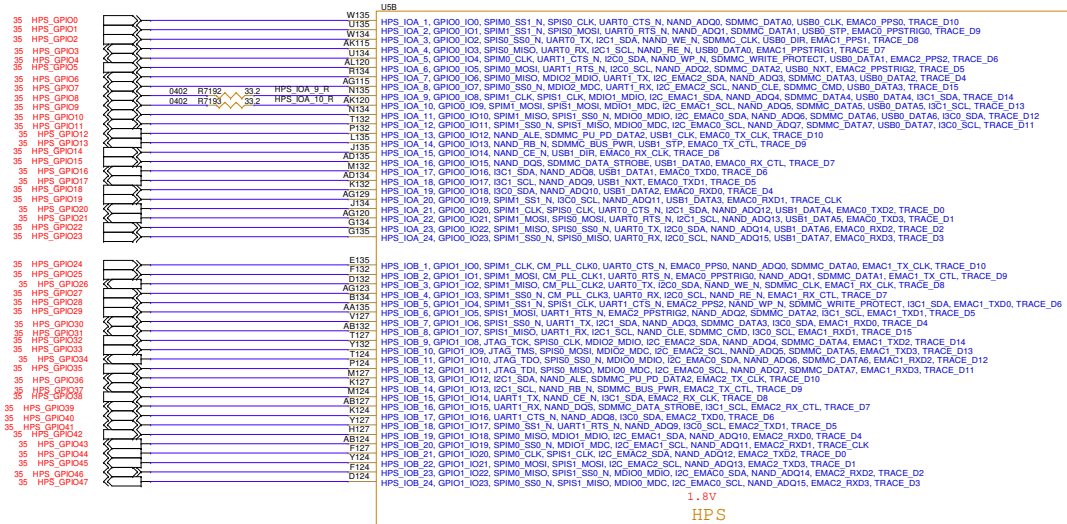
Note: MSEL0 is shared with QSPI1_S0 which has a pull-up. MSEL0 should make MSEL0 Open Drain.

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HPS BANK IO48

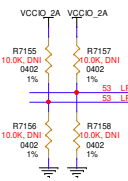
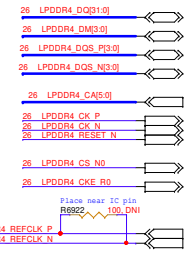


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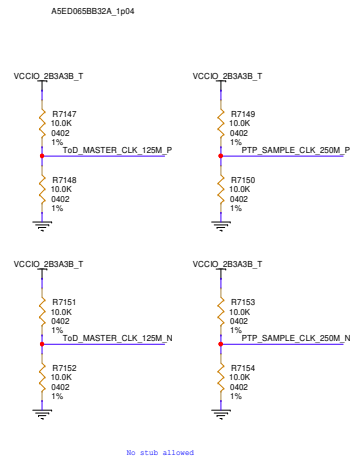
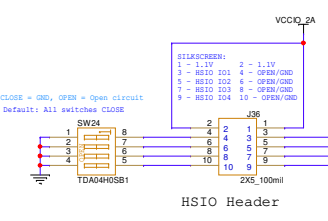
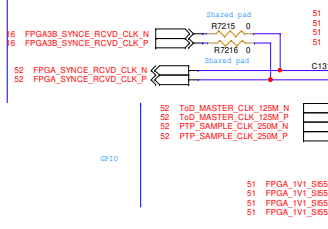
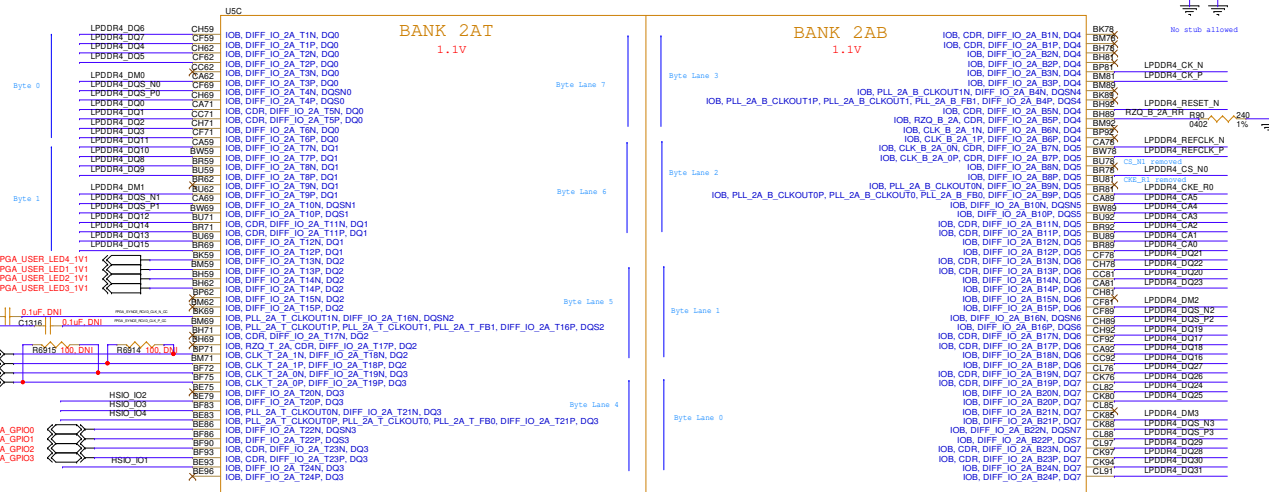
HSIO BANKS 2A1 AND 2A2



Please refer to Agilent EMIF User Guide for pin assignment rules.

SWAP RULES:
 1) Entire Byte Lanes can be swapped.
 2) DQ bits within a byte lane can be swapped.
 3) DQ_P/DQ_N DM signals are fixed locations

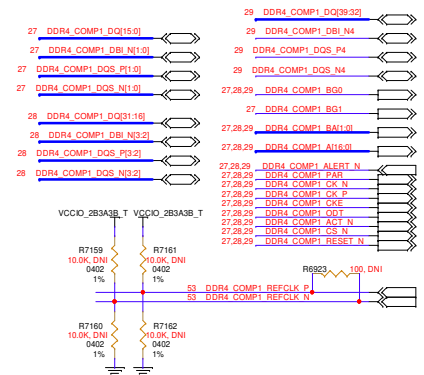
SIGNAL RULES:
 1) Entire Byte Lanes can be swapped.
 2) DQ bits within a byte lane can be swapped.
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HSIO BANKS 2BL AND 2BR



Please refer to Agilix EMIF User Guide for pin assignment rules.

Bank	Pin	Signal	IOB	IOB Config
BANK 2BT 1.2V	CC19	DDR4_COMP1_DQ36	IOB_DIFF	IO_2B_T1N, DQ8
	CH22	DDR4_COMP1_DQ34	IOB_DIFF	IO_2B_T1P, DQ8
	CF22	DDR4_COMP1_DQ38	IOB_DIFF	IO_2B_T2N, DQ8
	CF22	DDR4_COMP1_DQ38	IOB_DIFF	IO_2B_T2P, DQ8
	CG22	DDR4_COMP1_DQ32	IOB_DIFF	IO_2B_T3N, DQ8
	CG22	DDR4_COMP1_DQ32	IOB_DIFF	IO_2B_T3P, DQ8
	CF28	DDR4_COMP1_DQS_P4	IOB_CDR	DIFF_IO_2B_T4N, DQSN8
	CA31	DDR4_COMP1_DQS_N4	IOB_CDR	DIFF_IO_2B_T4P, DQSN8
	CF31	DDR4_COMP1_DQS_P4	IOB_CDR	DIFF_IO_2B_T5N, DQ8
	CF31	DDR4_COMP1_DQS_P4	IOB_CDR	DIFF_IO_2B_T5P, DQ8
BANK 2BB 1.2V	BW38	DDR4_COMP1_BG0	IOB_CDR	DIFF_IO_2B_B1N, DQ12
	BU38	DDR4_COMP1_BA0	IOB_CDR	DIFF_IO_2B_B1P, DQ12
	BU38	DDR4_COMP1_ALERT_N	IOB_CDR	DIFF_IO_2B_B2N, DQ12
	BU41	DDR4_COMP1_A16	IOB_CDR	DIFF_IO_2B_B2P, DQ12
	BR41	DDR4_COMP1_A15	IOB_CDR	DIFF_IO_2B_B3N, DQ12
	CA48	DDR4_COMP1_A14	IOB_CDR	DIFF_IO_2B_B3P, DQ12
	BW49	DDR4_COMP1_A13	IOB_CDR	DIFF_IO_2B_B4N, DQSN12
	BU52	DDR4_COMP1_A12	IOB_CDR	DIFF_IO_2B_B4P, DQSN12
	BW52	RZO_B_2B_PPR	IOB_CDR	DIFF_IO_2B_B5N, DQ12
	BU49	DDR4_COMP1_REFCLK_N	IOB_RZO	B_2B_CDR, DIFF_IO_2B_B5P, DQ12

SWAP RULES:
 1) Unlike byte lanes can be swapped.
 2) IO bits within a byte lane can be swapped.
 3) DQS_P/N, DBI signals are fixed locations.
 4) ECC bytes must be connected to Byte Lane 7.
 5) For A16 devices, DQ0 & DQ1 must be connected to one A16 device and placed on adjacent byte lane unless they are separated by ADD/ODD lane.

SWIZZLE RULES:
 PIN_SWIZZLE_CMO_0=0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55,56,57,58,59,60,61,62,63,64,65,66,67,68,69,70,71,72,73,74,75,76,77,78,79,80,81,82,83,84,85,86,87,88,89,90,91,92,93,94,95,96,97,98,99,100,101,102,103,104,105,106,107,108,109,110,111,112,113,114,115,116,117,118,119,120,121,122,123,124,125,126,127,128,129,130,131,132,133,134,135,136,137,138,139,140,141,142,143,144,145,146,147,148,149,150,151,152,153,154,155,156,157,158,159,160,161,162,163,164,165,166,167,168,169,170,171,172,173,174,175,176,177,178,179,180,181,182,183,184,185,186,187,188,189,190,191,192,193,194,195,196,197,198,199,200,201,202,203,204,205,206,207,208,209,210,211,212,213,214,215,216,217,218,219,220,221,222,223,224,225,226,227,228,229,230,231,232,233,234,235,236,237,238,239,240,241,242,243,244,245,246,247,248,249,250,251,252,253,254,255,256,257,258,259,260,261,262,263,264,265,266,267,268,269,270,271,272,273,274,275,276,277,278,279,280,281,282,283,284,285,286,287,288,289,290,291,292,293,294,295,296,297,298,299,300,301,302,303,304,305,306,307,308,309,310,311,312,313,314,315,316,317,318,319,320,321,322,323,324,325,326,327,328,329,330,331,332,333,334,335,336,337,338,339,340,341,342,343,344,345,346,347,348,349,350,351,352,353,354,355,356,357,358,359,360,361,362,363,364,365,366,367,368,369,370,371,372,373,374,375,376,377,378,379,380,381,382,383,384,385,386,387,388,389,390,391,392,393,394,395,396,397,398,399,400,401,402,403,404,405,406,407,408,409,410,411,412,413,414,415,416,417,418,419,420,421,422,423,424,425,426,427,428,429,430,431,432,433,434,435,436,437,438,439,440,441,442,443,444,445,446,447,448,449,450,451,452,453,454,455,456,457,458,459,460,461,462,463,464,465,466,467,468,469,470,471,472,473,474,475,476,477,478,479,480,481,482,483,484,485,486,487,488,489,490,491,492,493,494,495,496,497,498,499,500,501,502,503,504,505,506,507,508,509,510,511,512,513,514,515,516,517,518,519,520,521,522,523,524,525,526,527,528,529,530,531,532,533,534,535,536,537,538,539,540,541,542,543,544,545,546,547,548,549,550,551,552,553,554,555,556,557,558,559,560,561,562,563,564,565,566,567,568,569,570,571,572,573,574,575,576,577,578,579,580,581,582,583,584,585,586,587,588,589,590,591,592,593,594,595,596,597,598,599,600,601,602,603,604,605,606,607,608,609,610,611,612,613,614,615,616,617,618,619,620,621,622,623,624,625,626,627,628,629,630,631,632,633,634,635,636,637,638,639,640,641,642,643,644,645,646,647,648,649,650,651,652,653,654,655,656,657,658,659,660,661,662,663,664,665,666,667,668,669,670,671,672,673,674,675,676,677,678,679,680,681,682,683,684,685,686,687,688,689,690,691,692,693,694,695,696,697,698,699,700,701,702,703,704,705,706,707,708,709,710,711,712,713,714,715,716,717,718,719,720,721,722,723,724,725,726,727,728,729,730,731,732,733,734,735,736,737,738,739,740,741,742,743,744,745,746,747,748,749,750,751,752,753,754,755,756,757,758,759,760,761,762,763,764,765,766,767,768,769,770,771,772,773,774,775,776,777,778,779,780,781,782,783,784,785,786,787,788,789,790,791,792,793,794,795,796,797,798,799,800,801,802,803,804,805,806,807,808,809,810,811,812,813,814,815,816,817,818,819,820,821,822,823,824,825,826,827,828,829,830,831,832,833,834,835,836,837,838,839,840,841,842,843,844,845,846,847,848,849,850,851,852,853,854,855,856,857,858,859,860,861,862,863,864,865,866,867,868,869,870,871,872,873,874,875,876,877,878,879,880,881,882,883,884,885,886,887,888,889,890,891,892,893,894,895,896,897,898,899,900,901,902,903,904,905,906,907,908,909,910,911,912,913,914,915,916,917,918,919,920,921,922,923,924,925,926,927,928,929,930,931,932,933,934,935,936,937,938,939,940,941,942,943,944,945,946,947,948,949,950,951,952,953,954,955,956,957,958,959,960,961,962,963,964,965,966,967,968,969,970,971,972,973,974,975,976,977,978,979,980,981,982,983,984,985,986,987,988,989,990,991,992,993,994,995,996,997,998,999,1000.

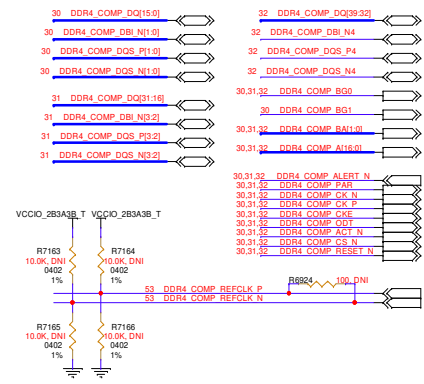
SWAP RULES:
 ADDS/ODD/CTS8 signal locations are fixed and cannot be swapped.

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the AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

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HSIO BANKS 3A1 AND 3A2



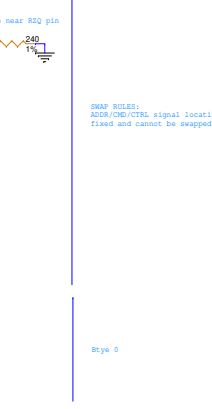
Please refer to Agilent EMIF User Guide for pin assignment rules.

USE	BANK 3A1 1.2V	BANK 3A2 1.2V
DDR4_COMP_DQ03	A91	IOB_DIFF_IO_3A_T1N_DQ16
DDR4_COMP_DQ05	B88	IOB_DIFF_IO_3A_T1P_DQ16
DDR4_COMP_DQ06	A94	IOB_DIFF_IO_3A_T2N_DQ16
DDR4_COMP_DQ07	B91	IOB_DIFF_IO_3A_T2P_DQ16
DDR4_COMP_DQ11	X897	IOB_DIFF_IO_3A_T3N_DQ16
DDR4_COMP_DQ14	B101	IOB_DIFF_IO_3A_T3P_DQ16
DDR4_COMP_DQ15	A101	IOB_CDR_DIFF_IO_3A_T3N_DQ16
DDR4_COMP_DQ16	A110	IOB_CDR_DIFF_IO_3A_T3P_DQ16
DDR4_COMP_DQ17	B105	IOB_CDR_DIFF_IO_3A_T3N_DQ16
DDR4_COMP_DQ18	B103	IOB_CDR_DIFF_IO_3A_T3P_DQ16
DDR4_COMP_DQ19	B106	IOB_DIFF_IO_3A_T4N_DQ16
DDR4_COMP_DQ20	B94	IOB_DIFF_IO_3A_T4P_DQ16
DDR4_COMP_DQ21	F84	IOB_DIFF_IO_3A_T5N_DQ17_AVST_DATA10
DDR4_COMP_DQ22	M57	IOB_DIFF_IO_3A_T5P_DQ17_AVST_DATA8
DDR4_COMP_DQ23	X867	IOB_DIFF_IO_3A_T6N_DQ17_AVST_DATA7
DDR4_COMP_DQ24	B95	IOB_DIFF_IO_3A_T6P_DQ17_AVST_DATA9
DDR4_COMP_DQ25	K67	IOB_DIFF_IO_3A_T7N_DQ17_AVST_DATA6
DDR4_COMP_DQ26	X867	IOB_DIFF_IO_3A_T7P_DQ17_AVST_DATA8
DDR4_COMP_DQ27	M57	IOB_DIFF_IO_3A_T8N_DQ17_AVST_DATA5
DDR4_COMP_DQ28	K68	IOB_DIFF_IO_3A_T8P_DQ17_AVST_DATA4
DDR4_COMP_DQ29	M98	IOB_CDR_DIFF_IO_3A_T11N_DQ17_AVST_DATA3
DDR4_COMP_DQ30	F98	IOB_CDR_DIFF_IO_3A_T11P_DQ17_AVST_DATA2
DDR4_COMP_DQ31	H98	IOB_CDR_DIFF_IO_3A_T12N_DQ17_AVST_DATA1
DDR4_COMP_DQ32	M94	IOB_CDR_DIFF_IO_3A_T12P_DQ17_AVST_DATA0
DDR4_COMP_DQ33	T84	IOB_DIFF_IO_3A_T13N_DQ18
DDR4_COMP_DQ34	V84	IOB_DIFF_IO_3A_T13P_DQ18
DDR4_COMP_DQ35	M84	IOB_DIFF_IO_3A_T14N_DQ18
DDR4_COMP_DQ36	K84	IOB_DIFF_IO_3A_T14P_DQ18
DDR4_COMP_DQ37	T87	IOB_DIFF_IO_3A_T15N_DQ18
DDR4_COMP_DQ38	X867	IOB_DIFF_IO_3A_T15P_DQ18
DDR4_COMP_DQ39	M55	IOB_PLL_3A_T_CLKOUT1N_DIFF_IO_3A_T16N_DQS18
DDR4_COMP_DQ40	K95	IOB_PLL_3A_T_CLKOUT1P_DIFF_IO_3A_T16P_DQS18
DDR4_COMP_DQ41	P95	IOB_CDR_DIFF_IO_3A_T17N_DQ18
DDR4_COMP_DQ42	F95	IOB_CDR_DIFF_IO_3A_T17P_DQ18
DDR4_COMP_DQ43	V95	IOB_CLK_T_3A_1N_DIFF_IO_3A_T18N_DQ18
DDR4_COMP_DQ44	V94	IOB_CLK_T_3A_1P_DIFF_IO_3A_T18P_DQ18
DDR4_COMP_DQ45	V87	IOB_CLK_T_3A_0N_DIFF_IO_3A_T19N_DQ19
DDR4_COMP_DQ46	V96	IOB_CLK_T_3A_0P_DIFF_IO_3A_T19P_DQ19
DDR4_COMP_DQ47	V98	IOB_DIFF_IO_3A_T20N_DQ19
DDR4_COMP_DQ48	X867	IOB_DIFF_IO_3A_T20P_DQ19
DDR4_COMP_DQ49	X867	IOB_PLL_3A_T_CLKOUT0N_DIFF_IO_3A_T21N_DQ19
DDR4_COMP_DQ50	X867	IOB_PLL_3A_T_CLKOUT0P_DIFF_IO_3A_T21P_DQ19
DDR4_COMP_DQ51	X867	IOB_DIFF_IO_3A_T22N_DQS19_AVST_CLK
DDR4_COMP_DQ52	X867	IOB_DIFF_IO_3A_T22P_DQS19_AVST_DATA15
DDR4_COMP_DQ53	AC100	IOB_CDR_DIFF_IO_3A_T23N_DQ19_AVST_DATA14
DDR4_COMP_DQ54	AG100	IOB_CDR_DIFF_IO_3A_T23P_DQ19_AVST_DATA13
DDR4_COMP_DQ55	AG100	IOB_DIFF_IO_3A_T24N_DQ19_AVST_DATA12
DDR4_COMP_DQ56	AG100	IOB_DIFF_IO_3A_T24P_DQ19_AVST_DATA11

USE	BANK 3A3 1.2V	BANK 3A4 1.2V
IOB_CDR_DIFF_IO_3A_B1N_DQ20	AB105	DDR4_COMP_B00
IOB_CDR_DIFF_IO_3A_B1P_DQ20	V105	DDR4_COMP_BAT
IOB_DIFF_IO_3A_B2N_DQ20	AB108	DDR4_COMP_BAT
IOB_DIFF_IO_3A_B2P_DQ20	V108	DDR4_COMP_ALERT_N
IOB_DIFF_IO_3A_B3N_DQ20	AK104	DDR4_COMP_A15
IOB_DIFF_IO_3A_B3P_DQ20	AK107	DDR4_COMP_A15
IOB_DIFF_IO_3A_B4N_DQ20	AB114	DDR4_COMP_A14
IOB_DIFF_IO_3A_B4P_DQ20	AG111	DDR4_COMP_A12
IOB_CDR_DIFF_IO_3A_B5N_DQ20	AK111	RZO_B_3A_0N
IOB_CDR_DIFF_IO_3A_B5P_DQ20	AB117	DDR4_COMP_REFCLK_P
IOB_CLK_B_3A_1N_DIFF_IO_3A_B7P_DQ21	K105	DDR4_COMP_A11
IOB_CLK_B_3A_1P_DIFF_IO_3A_B8P_DQ21	M105	DDR4_COMP_A10
IOB_CDR_DIFF_IO_3A_B7N_DQ21	P105	DDR4_COMP_A9
IOB_CDR_DIFF_IO_3A_B7P_DQ21	V105	DDR4_COMP_A8
IOB_CDR_DIFF_IO_3A_B8N_DQ21	T108	DDR4_COMP_A7
IOB_CDR_DIFF_IO_3A_B8P_DQ21	V108	DDR4_COMP_A6
IOB_PLL_3A_B_CLKOUT0N_DIFF_IO_3A_B9N_DQ21	K114	DDR4_COMP_A5
IOB_PLL_3A_B_CLKOUT0P_DIFF_IO_3A_B9P_DQ21	M114	DDR4_COMP_A4
IOB_PLL_3A_B_CLKOUT1N_DIFF_IO_3A_B10N_DQ21	T117	DDR4_COMP_A3
IOB_PLL_3A_B_CLKOUT1P_DIFF_IO_3A_B10P_DQ21	V117	DDR4_COMP_A2
IOB_CDR_DIFF_IO_3A_B11N_DQ21	P114	DDR4_COMP_A1
IOB_CDR_DIFF_IO_3A_B11P_DQ21	T114	DDR4_COMP_A0
IOB_CDR_DIFF_IO_3A_B12N_DQ21	V108	DDR4_COMP_PA8
IOB_CDR_DIFF_IO_3A_B12P_DQ21	M108	DDR4_COMP_PA8
IOB_CDR_DIFF_IO_3A_B13N_DQ22	F108	DDR4_COMP_PA7
IOB_CDR_DIFF_IO_3A_B13P_DQ22	D108	DDR4_COMP_PA6
IOB_CDR_DIFF_IO_3A_B14N_DQ22	V108	DDR4_COMP_PA5
IOB_CDR_DIFF_IO_3A_B14P_DQ22	F108	DDR4_COMP_PA4
IOB_CDR_DIFF_IO_3A_B15N_DQ22	D108	DDR4_COMP_PA3
IOB_CDR_DIFF_IO_3A_B15P_DQ22	F114	DDR4_COMP_PA2
IOB_CDR_DIFF_IO_3A_B16N_DQ22	D114	DDR4_COMP_PA1
IOB_CDR_DIFF_IO_3A_B16P_DQ22	F114	DDR4_COMP_PA0
IOB_CDR_DIFF_IO_3A_B17N_DQ22	K117	DDR4_COMP_CS_N
IOB_CDR_DIFF_IO_3A_B17P_DQ22	H117	DDR4_COMP_RESET_N
IOB_CDR_DIFF_IO_3A_B18N_DQ22	F117	DDR4_COMP_BGT
IOB_CDR_DIFF_IO_3A_B18P_DQ22	A118	DDR4_COMP_DO0
IOB_CDR_DIFF_IO_3A_B19N_DQ23	B113	DDR4_COMP_DQ5
IOB_CDR_DIFF_IO_3A_B19P_DQ23	A113	DDR4_COMP_DQ5
IOB_CDR_DIFF_IO_3A_B20N_DQ23	B116	DDR4_COMP_DQ1
IOB_CDR_DIFF_IO_3A_B20P_DQ23	B116	DDR4_COMP_DQ1
IOB_CDR_DIFF_IO_3A_B21N_DQ23	A126	DDR4_COMP_DO2
IOB_CDR_DIFF_IO_3A_B21P_DQ23	B126	DDR4_COMP_DO2
IOB_CDR_DIFF_IO_3A_B22N_DQ23	B126	DDR4_COMP_DO3
IOB_CDR_DIFF_IO_3A_B22P_DQ23	B126	DDR4_COMP_DO3
IOB_CDR_DIFF_IO_3A_B23N_DQ23	A128	DDR4_COMP_DO4
IOB_CDR_DIFF_IO_3A_B23P_DQ23	B128	DDR4_COMP_DO4
IOB_CDR_DIFF_IO_3A_B24N_DQ23		
IOB_CDR_DIFF_IO_3A_B24P_DQ23		

SWAP RULES:
1) Device Byte Lanes can be swapped.
2) DQ bits within a Byte Lane can be swapped.
3) DQS/PQS/DTM signals are fixed locations.
4) ECC Byte must be connected to Byte Lane 7.
5) For all devices, IO₂ & IO₁ must be connected to one x16 device and placed on adjacent Byte Lane unless they are separated by ADD/OEN Lane.

SWIZZLE RULES:
SWIZZLE_CHANNELS=0, X, X, X, 1, 2, 9, 20C
PIN_SWIZZLE_CHANNELS=0, 2, 4, 6, 1, 3, 5, 7
PIN_SWIZZLE_CHANNELS=1, 3, 5, 7, 11, 14, 16, 18, 9
PIN_SWIZZLE_CHANNELS=2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 52, 54, 56, 58, 60, 62, 64, 66, 68, 70, 72, 74, 76, 78, 80, 82, 84, 86, 88, 90, 92, 94, 96, 98, 100, 102, 104, 106, 108, 110, 112, 114, 116, 118, 120, 122, 124, 126, 128, 130, 132, 134, 136, 138, 140, 142, 144, 146, 148, 150, 152, 154, 156, 158, 160, 162, 164, 166, 168, 170, 172, 174, 176, 178, 180, 182, 184, 186, 188, 190, 192, 194, 196, 198, 200, 202, 204, 206, 208, 210, 212, 214, 216, 218, 220, 222, 224, 226, 228, 230, 232, 234, 236, 238, 240, 242, 244, 246, 248, 250, 252, 254, 256, 258, 260, 262, 264, 266, 268, 270, 272, 274, 276, 278, 280, 282, 284, 286, 288, 290, 292, 294, 296, 298, 300, 302, 304, 306, 308, 310, 312, 314, 316, 318, 320, 322, 324, 326, 328, 330, 332, 334, 336, 338, 340, 342, 344, 346, 348, 350, 352, 354, 356, 358, 360, 362, 364, 366, 368, 370, 372, 374, 376, 378, 380, 382, 384, 386, 388, 390, 392, 394, 396, 398, 400, 402, 404, 406, 408, 410, 412, 414, 416, 418, 420, 422, 424, 426, 428, 430, 432, 434, 436, 438, 440, 442, 444, 446, 448, 450, 452, 454, 456, 458, 460, 462, 464, 466, 468, 470, 472, 474, 476, 478, 480, 482, 484, 486, 488, 490, 492, 494, 496, 498, 500, 502, 504, 506, 508, 510, 512, 514, 516, 518, 520, 522, 524, 526, 528, 530, 532, 534, 536, 538, 540, 542, 544, 546, 548, 550, 552, 554, 556, 558, 560, 562, 564, 566, 568, 570, 572, 574, 576, 578, 580, 582, 584, 586, 588, 590, 592, 594, 596, 598, 600, 602, 604, 606, 608, 610, 612, 614, 616, 618, 620, 622, 624, 626, 628, 630, 632, 634, 636, 638, 640, 642, 644, 646, 648, 650, 652, 654, 656, 658, 660, 662, 664, 666, 668, 670, 672, 674, 676, 678, 680, 682, 684, 686, 688, 690, 692, 694, 696, 698, 700, 702, 704, 706, 708, 710, 712, 714, 716, 718, 720, 722, 724, 726, 728, 730, 732, 734, 736, 738, 740, 742, 744, 746, 748, 750, 752, 754, 756, 758, 760, 762, 764, 766, 768, 770, 772, 774, 776, 778, 780, 782, 784, 786, 788, 790, 792, 794, 796, 798, 800, 802, 804, 806, 808, 810, 812, 814, 816, 818, 820, 822, 824, 826, 828, 830, 832, 834, 836, 838, 840, 842, 844, 846, 848, 850, 852, 854, 856, 858, 860, 862, 864, 866, 868, 870, 872, 874, 876, 878, 880, 882, 884, 886, 888, 890, 892, 894, 896, 898, 900, 902, 904, 906, 908, 910, 912, 914, 916, 918, 920, 922, 924, 926, 928, 930, 932, 934, 936, 938, 940, 942, 944, 946, 948, 950, 952, 954, 956, 958, 960, 962, 964, 966, 968, 970, 972, 974, 976, 978, 980, 982, 984, 986, 988, 990, 992, 994, 996, 998, 1000.



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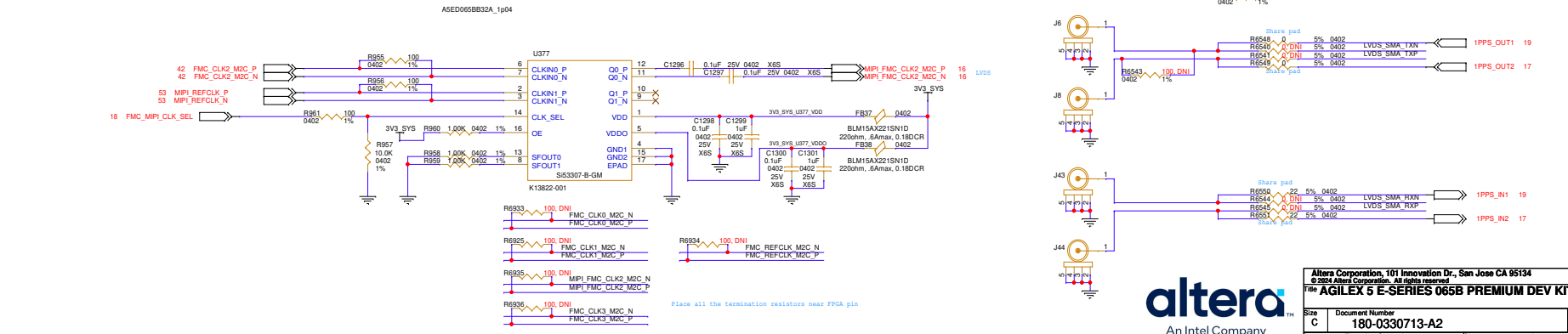
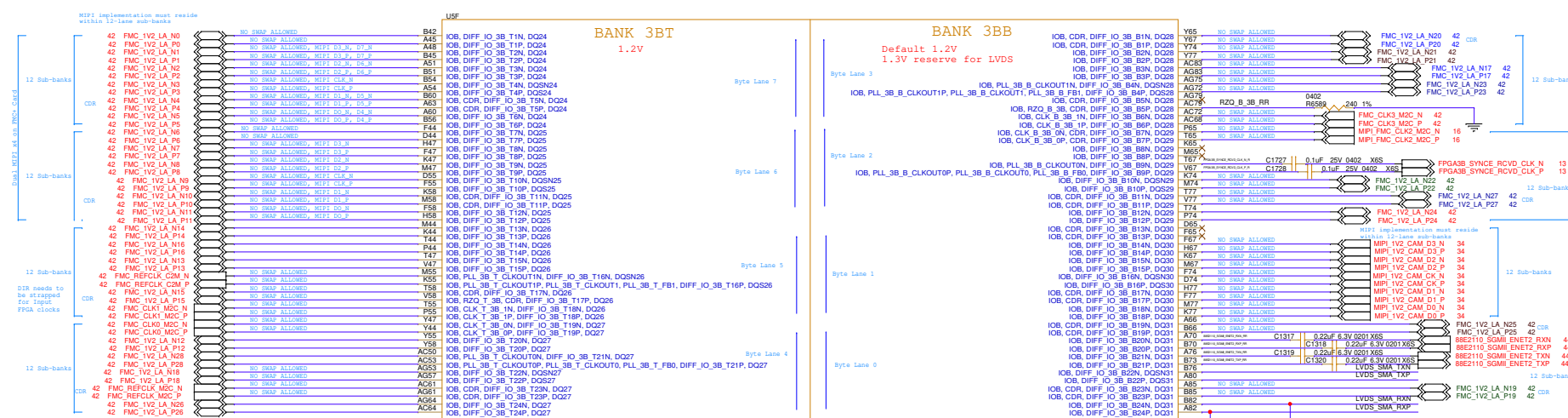
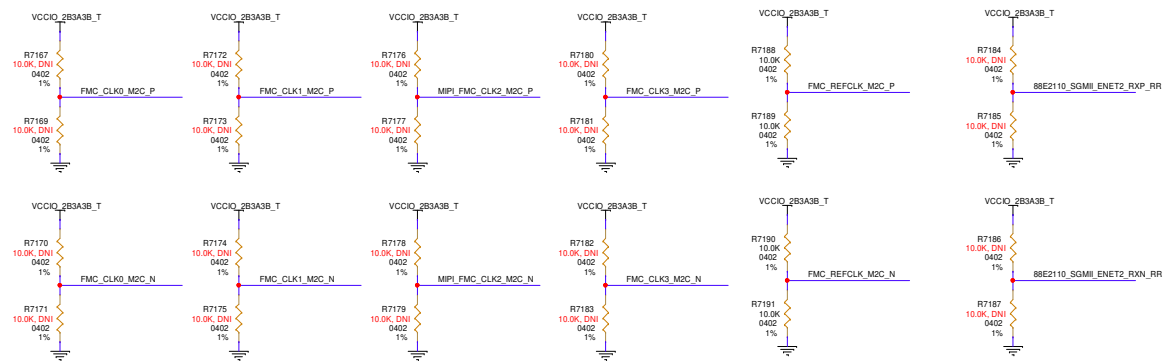
Pin placement restriction for MIPI & LVDS mixing with LVCMS0:

HSIO BANKS 3BL AND 3BR

IO Lane Used for MIPI	Width	Restricted Pin Used As LVCMS0	
		Pin Index	Pin Number
IO Lane 1	1 data + 1 clock	P26	V77
	2 data + 1 clock	P26	V77
IO Lane 6	4 data + 1 clock	P26, P10	V77, B66
	1 data + 1 clock	P75, P87	K58, B60
	4 data + 1 clock	P87, P70, P82	B60, K44, D44
IO Lane 7	1 data + 1 clock	P86; P2 from Bank 3A	A63, B130
	2 data + 1 clock	P77; P2 from Bank 3A	D55, B130
	4 data + 1 clock	P77, P83, P94; P2 from Bank 3A	D55, F44, A45, B130
IO Lane 6 and 7	8 data + 1 clock	P70, P82, P83, P89, P94	K44, D44, F44, B54, A45

IO Lane Used for LVDS	Function	Restricted Pin Used As LVCMS0	
		Pin Index	Pin Number
IO Lane 0	LVDS_SMA_RX	P3	A85
IO Lane 2	LVDS_SMA_TX	-	-
IO Lane 2	FPGA3B_SYNC_RCV_D_CLK	-	-
IO Lane 3	MIPI_FMC_CLK2_M2C	P43	AC83
IO Lane 3	FMC_CLK3_M2C	P38, P41	AC79 (R2Q), AG75
IO Lane 4	FMC_REFCLK_M2C	P40, P48	AG72, AC64
IO Lane 4	FMC_CLK0_M2C	P57, P67	Y55, T47
IO Lane 5	FMC_CLK1_M2C	P62	V58
IO Lane 5	FMC_REFCLK_C2M	P74	M58

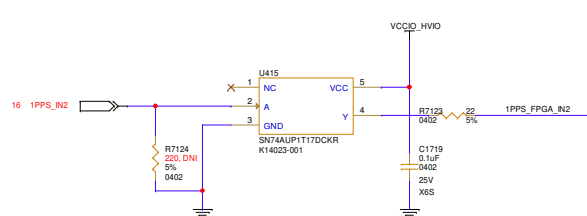
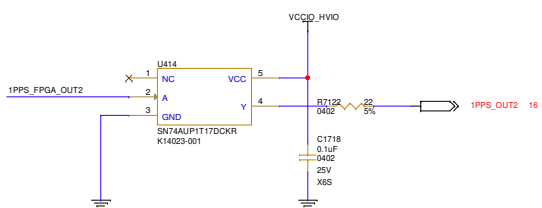
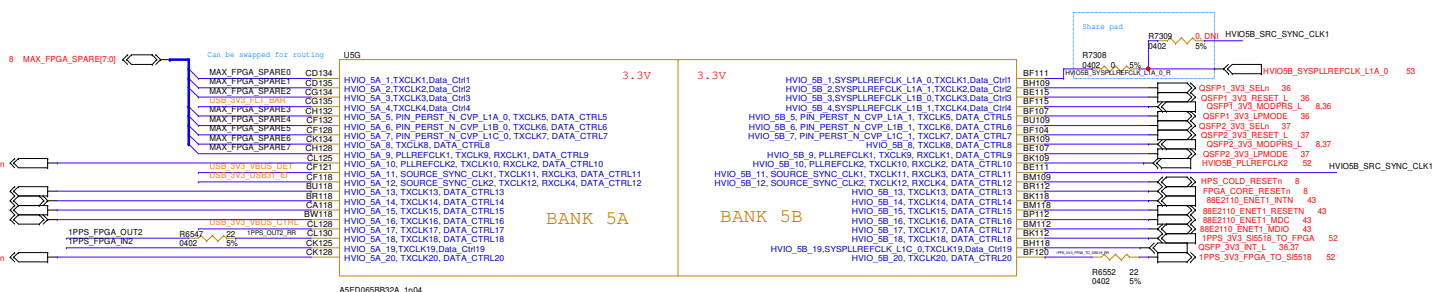
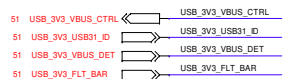
NOTES: Please check the detail restriction guide from IO Pinout Guideline Document if any of the FMC_V12_LA_* to be used as LVDS.



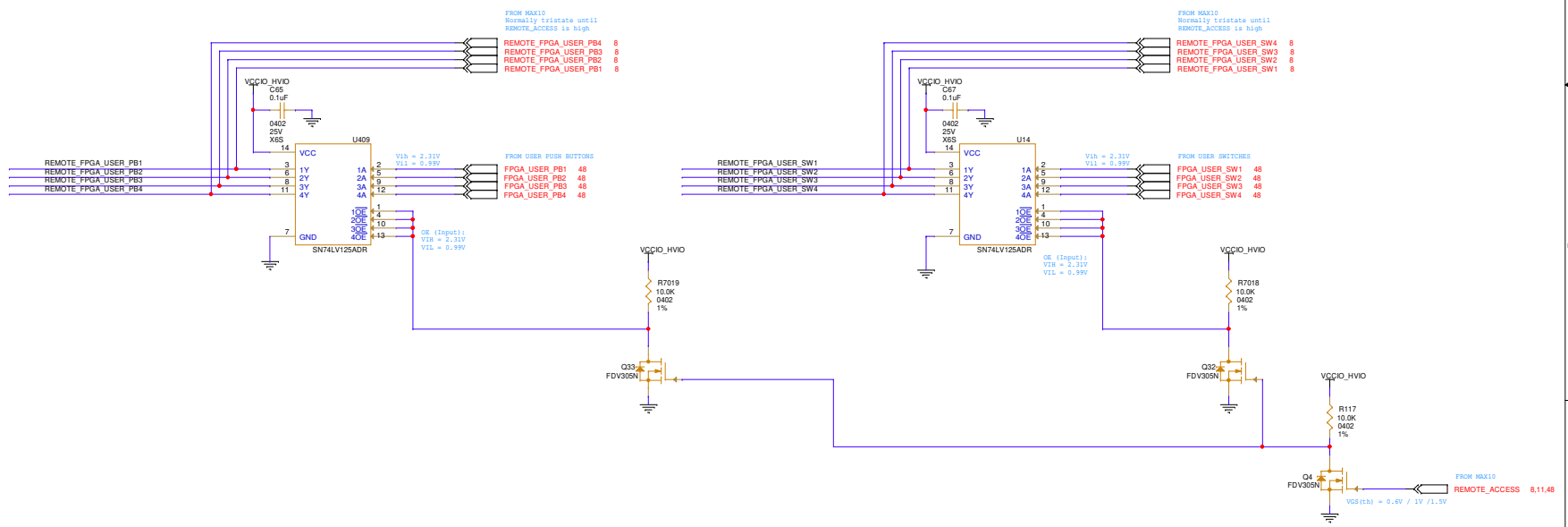
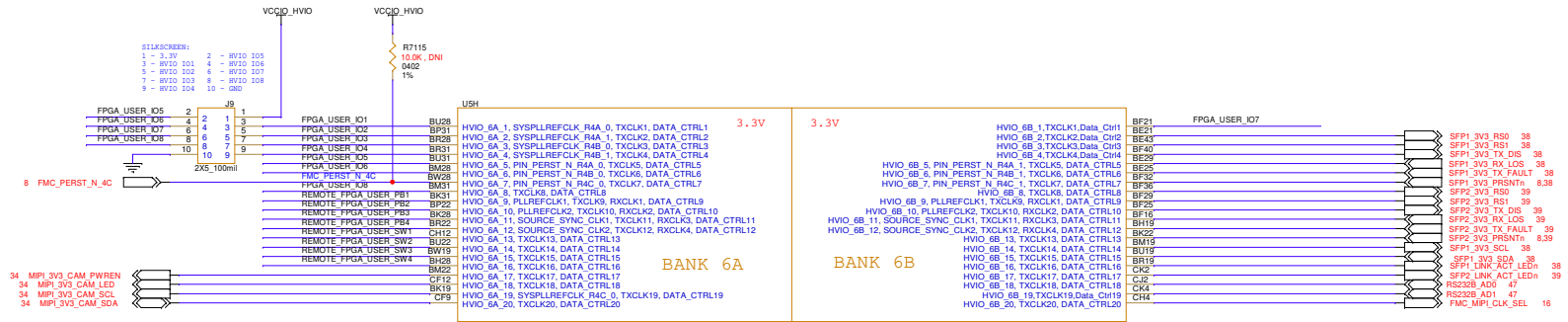
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THE AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size: Document Number: **180-0330713-A2**
 Date: Thursday, September 15, 2004 Sheet: 18 of 87

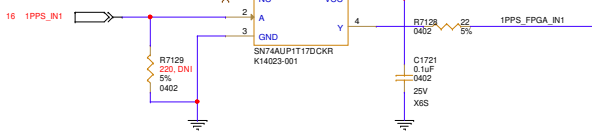
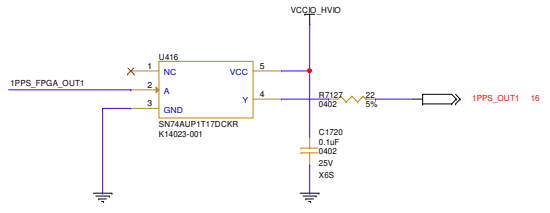
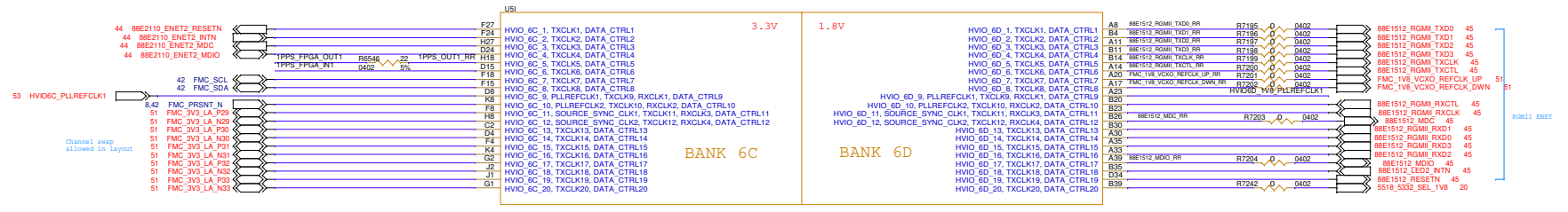
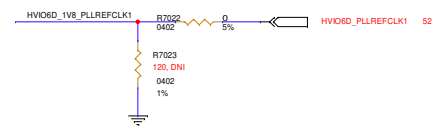
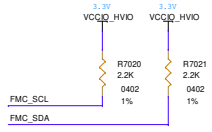
HVIO BANKS 5A AND 5B



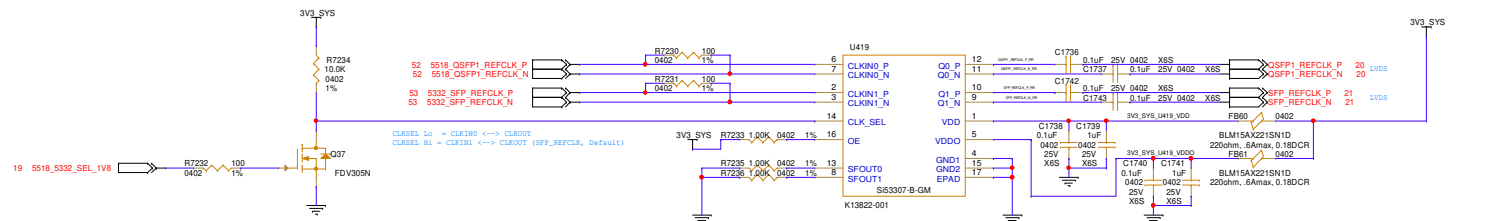
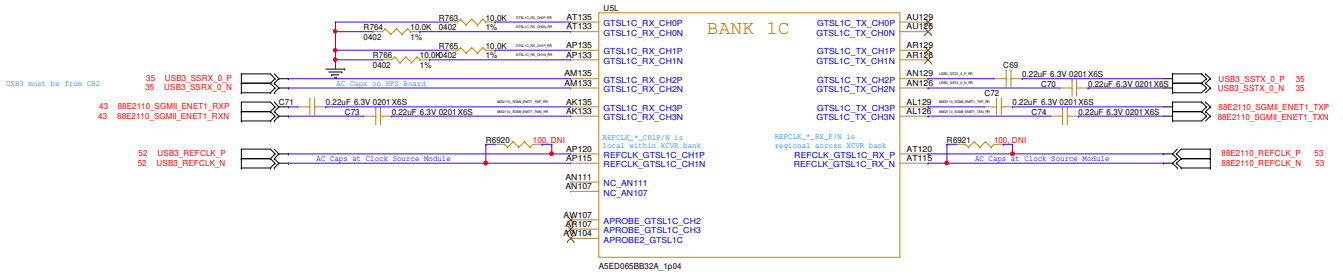
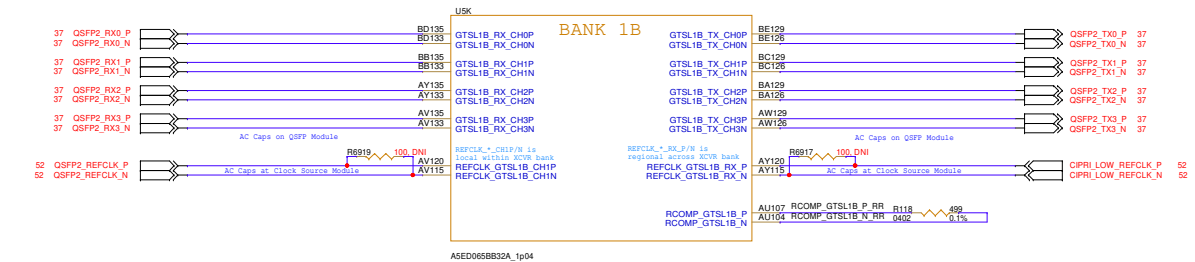
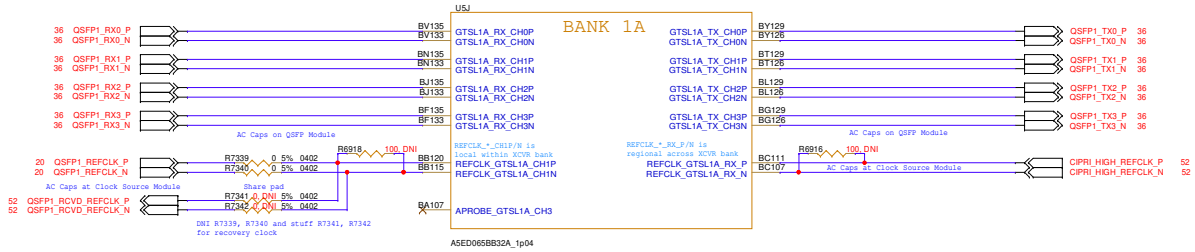
HVIO BANKS 6A AND 6B



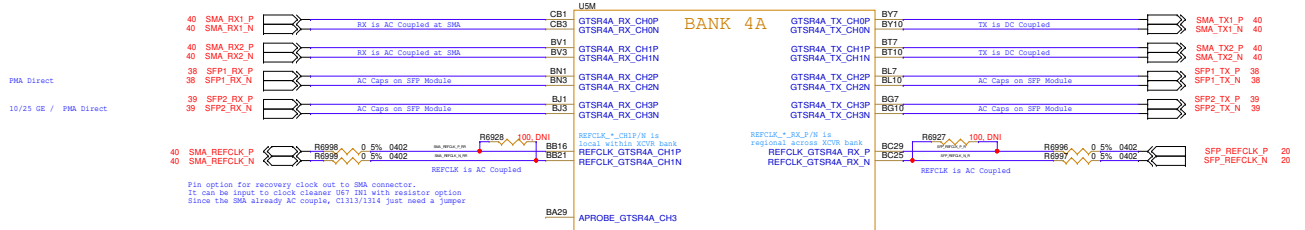
HVIO BANKS 6C AND 6D



XCVR BANKS 1A, 1B, 1C

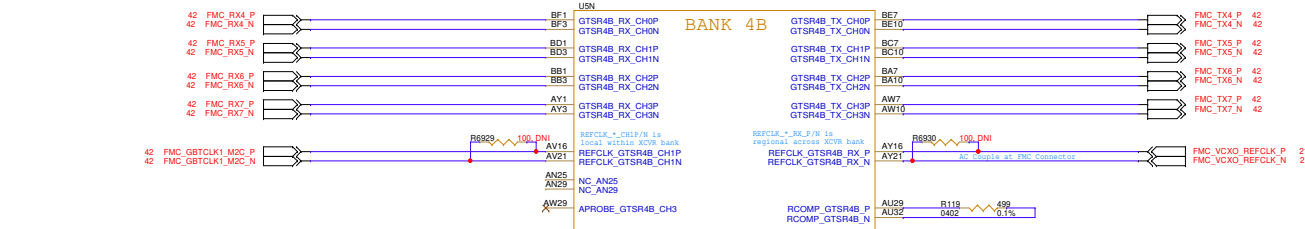


XCVR BANKS 4A, 4B, 4C

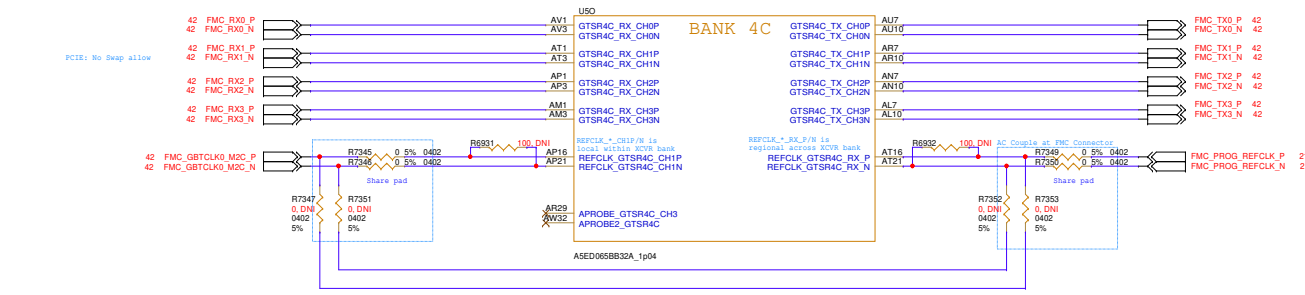


FMC 37.4 SPEC, Rule 3.1.1 9: If AC coupling is required for DP[0..31]_M00, DP[0..31]_M28 signals, this shall be provided on the mezzanine module.

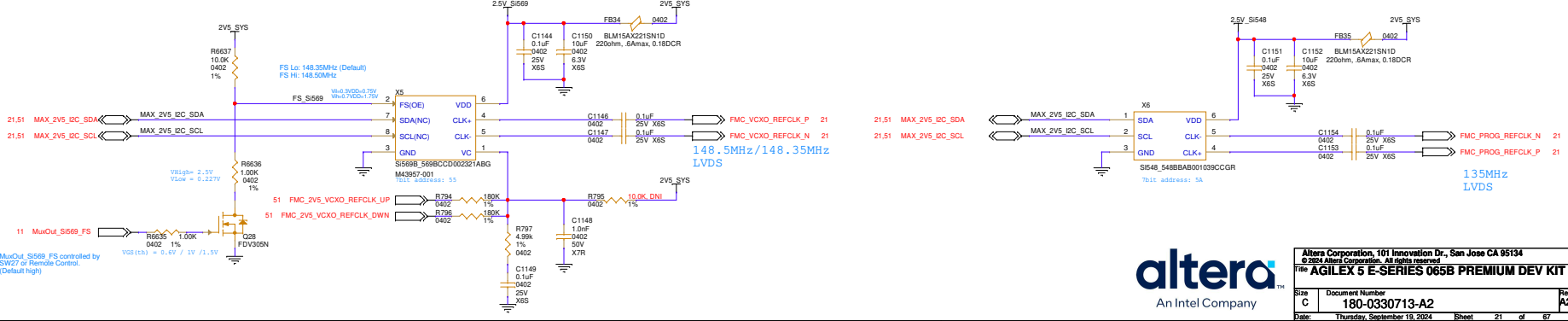
FMC 37.4 SPEC, Rule 3.1.1 9: If AC coupling is required for DP[0..31]_M00, DP[0..31]_M28 signals, this shall be provided on the mezzanine module.



PCIE: No Swap allow



For BRICK input to regional clock: Mount R7347, R7353, R7352, R7351. Suspend R7345, R7346, R7349, R7350.



DNU & NC PINS

USP

CL101	DNU_CL101
CL103	DNU_CK101
CL106	DNU_CK103
CL108	DNU_CL106

AM120	DNU_AM120
AL115	DNU_AL115
BD64	DNU_BD64
BD63	DNU_BD64
AL68	DNU_AL68
AL57	DNU_AL68
BD120	DNU_AL57
BC40	DNU_BD120
AL43	DNU_BC40
AK104	DNU_AL43
BA32	DNU_BA104
AK104	DNU_BA32
AK104	DNU_AH104
AK32	DNU_AK32
BD100	DNU_AK32
BD36	DNU_BD100
BD40	DNU_BC36
BD100	DNU_AH40
BC36	DNU_BC100
AK36	DNU_BC36
AK36	DNU_AK36

ASED065B32A_1p04

USX

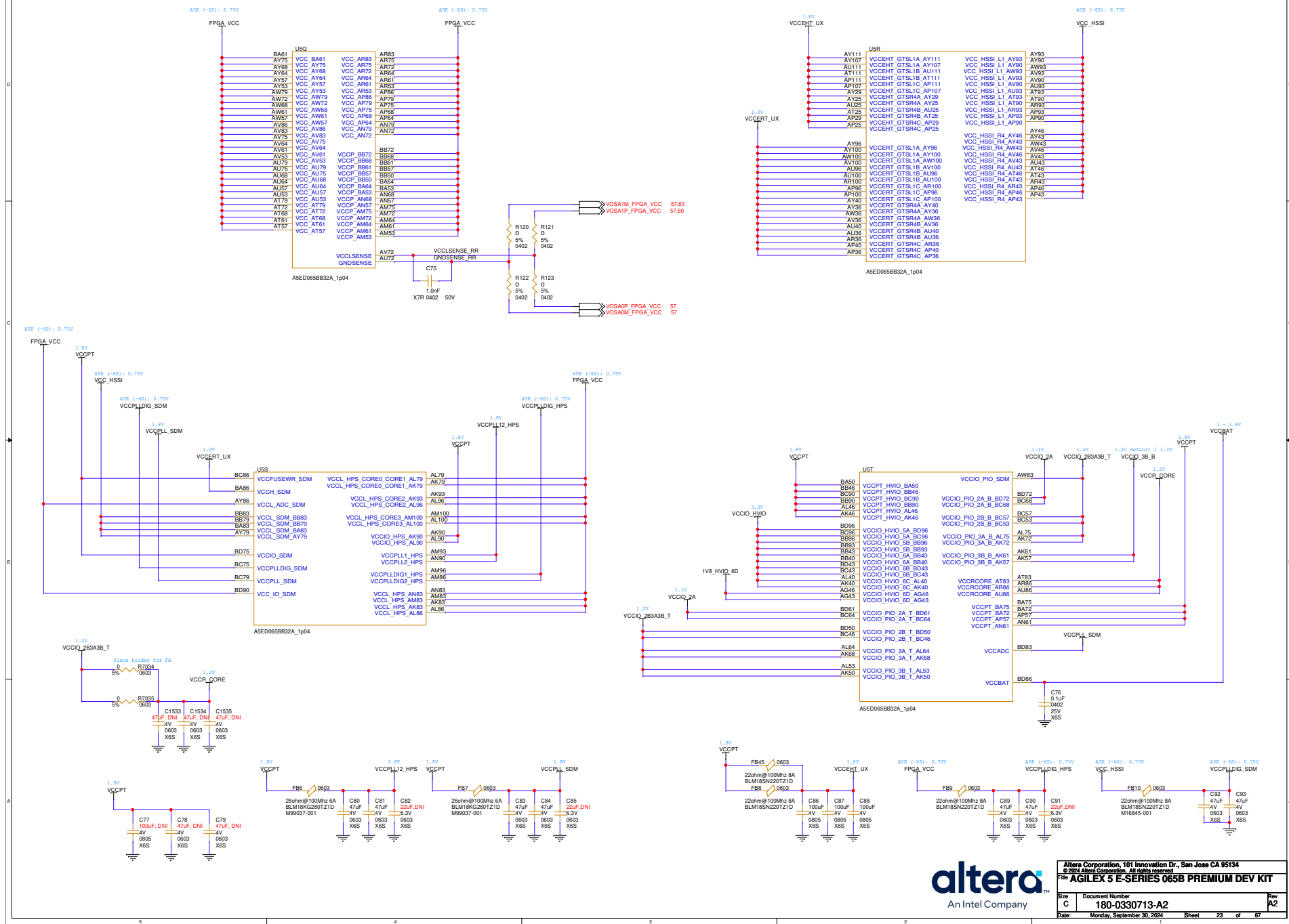
Y8	NC_Y8	NC_AW50	AW50
Y37	NC_Y4	NC_AP93	AP93
Y34	NC_Y37	NC_AP93	AP93
Y27	NC_Y34	NC_AN50	AN50
Y24	NC_Y27	NC_AM50	AM10
Y18	NC_Y24	NC_MM18	AL28
Y15	NC_Y18	NC_AL32	AL28
W2	NC_Y15	NC_AL28	AL28
W1	NC_W2	NC_AL28	AL28
V8	NC_W1	NC_AL16	AL16
V37	NC_V8	NC_AL10	AL16
V27	NC_V37	NC_AL104	AK32
V18	NC_V27	NC_AK32	AK32
U2	NC_V18	NC_AK25	AK25
U1	NC_U2	NC_AK16	AK16
T8	NC_U1	NC_AJ2	AJ2
T4	NC_T8	NC_AJ2	AJ2
T37	NC_T4	NC_AH	AH8
T34	NC_T37	NC_AH8	AH4
T27	NC_T34	NC_AH	AG40
T24	NC_T27	NC_AG40	AG40
T18	NC_T24	NC_AQ36	AG20
T15	NC_T18	NC_AQ28	AG20
T2	NC_T15	NC_AQ21	AG10
P4	NC_T2	NC_AQ12	AF2
P24	NC_P4	NC_AF2	AE4
P15	NC_P24	NC_AE4	AD2
N2	NC_P15	NC_AD2	AD1
M1	NC_N2	NC_AD1	AC40
M8	NC_M1	NC_AK40	AC40
M4	NC_M8	NC_AK40	AC36
M37	NC_M4	NC_AK36	AC36
M34	NC_M37	NC_AK36	AC36
M27	NC_M34	NC_AK36	AC36
M24	NC_M27	NC_AK36	AC36
M18	NC_M24	NC_AK36	AC36
M15	NC_M18	NC_AK36	AC36
L1	NC_M15	NC_AK36	AC36
K37	NC_L1	NC_AK36	AC36
K34	NC_K37	NC_AK36	AC36
K27	NC_K34	NC_AK36	AC36
K24	NC_K27	NC_AK36	AC36
K18	NC_K24	NC_AK36	AC36
K15	NC_K18	NC_AK36	AC36
H37	NC_K15	NC_AK36	AC36
F37	NC_H37	NC_AK36	AC36
F34	NC_F37	NC_AK36	AC36
BD16	NC_F34	NC_AK36	AC36
AY50	NC_BD16	NC_AK36	AC36
	NC_AY50	NC_AK36	AC36

ASED065B32A_1p04



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FPGA POWER



FPGA GND

Table listing ground connections for USJ and CH102. Columns include pin names (e.g., CK110, CH121) and their corresponding ground points (e.g., GND, GND_CK110).

A5ED0658B32A_1p04

Table listing ground connections for USV and BB36. Columns include pin names (e.g., BL5, BL13) and their corresponding ground points (e.g., GND, GND_BL5).

A5ED0658B32A_1p04

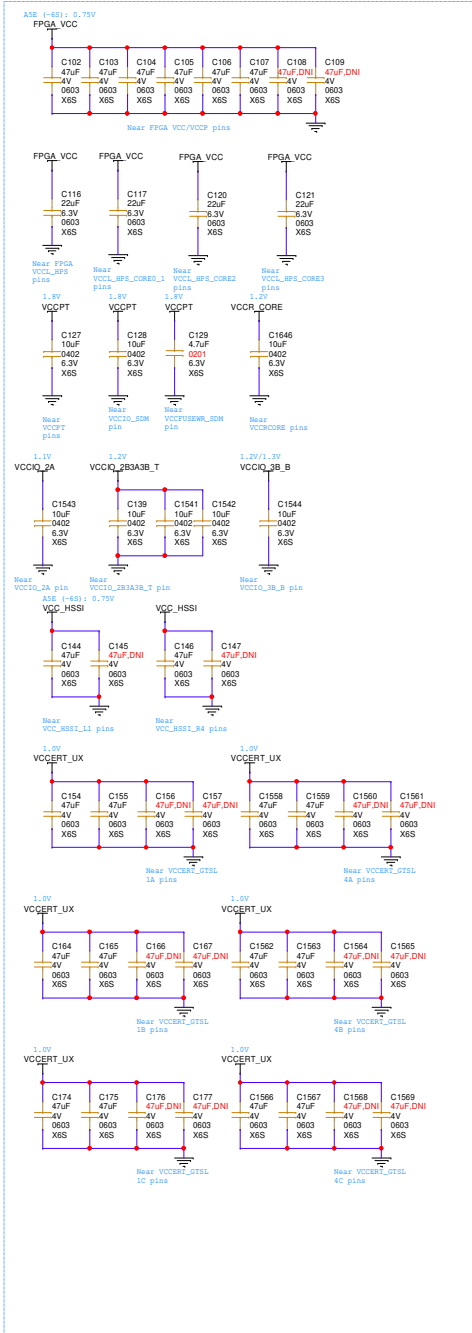
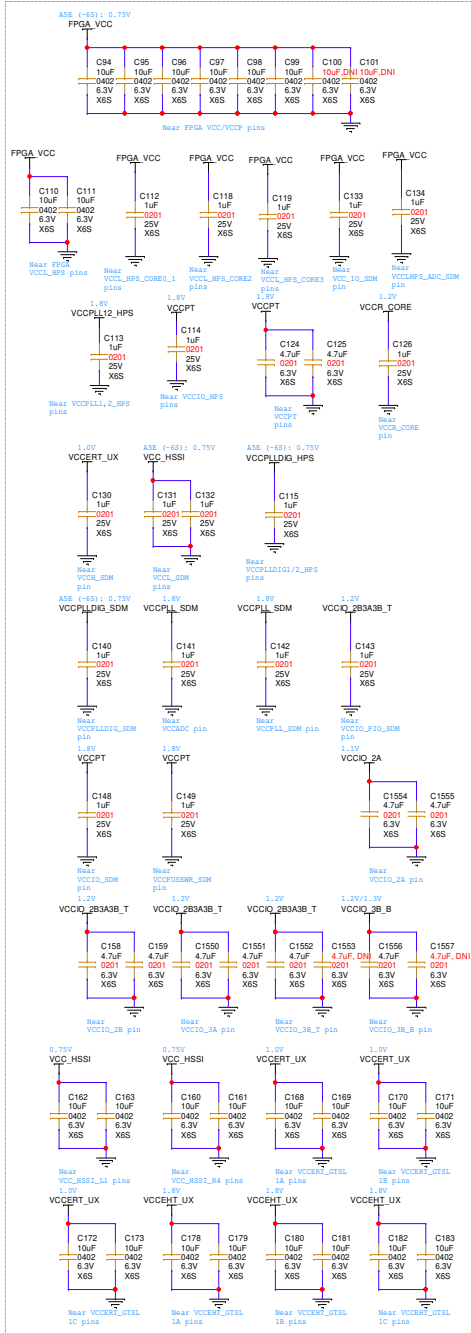
Table listing ground connections for USW and AN135. Columns include pin names (e.g., AV29, AV35) and their corresponding ground points (e.g., GND, GND_AV29).

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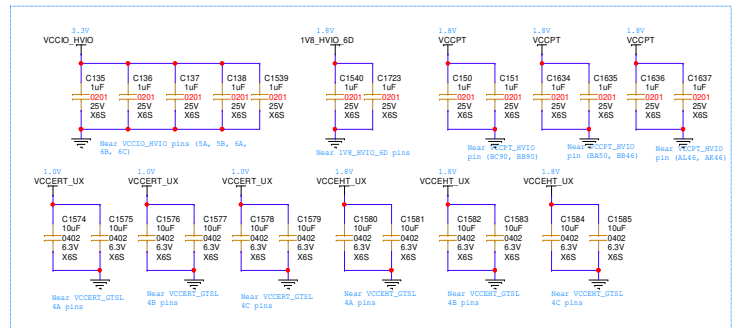
Altera logo and company information: Altera Corporation, 101 Innovation Dr., San Jose CA 95134. Includes document number 180-0330713-A2 and date Thursday, September 19, 2004.

Place bottom FPGA cavity

Place top FPGA periphery

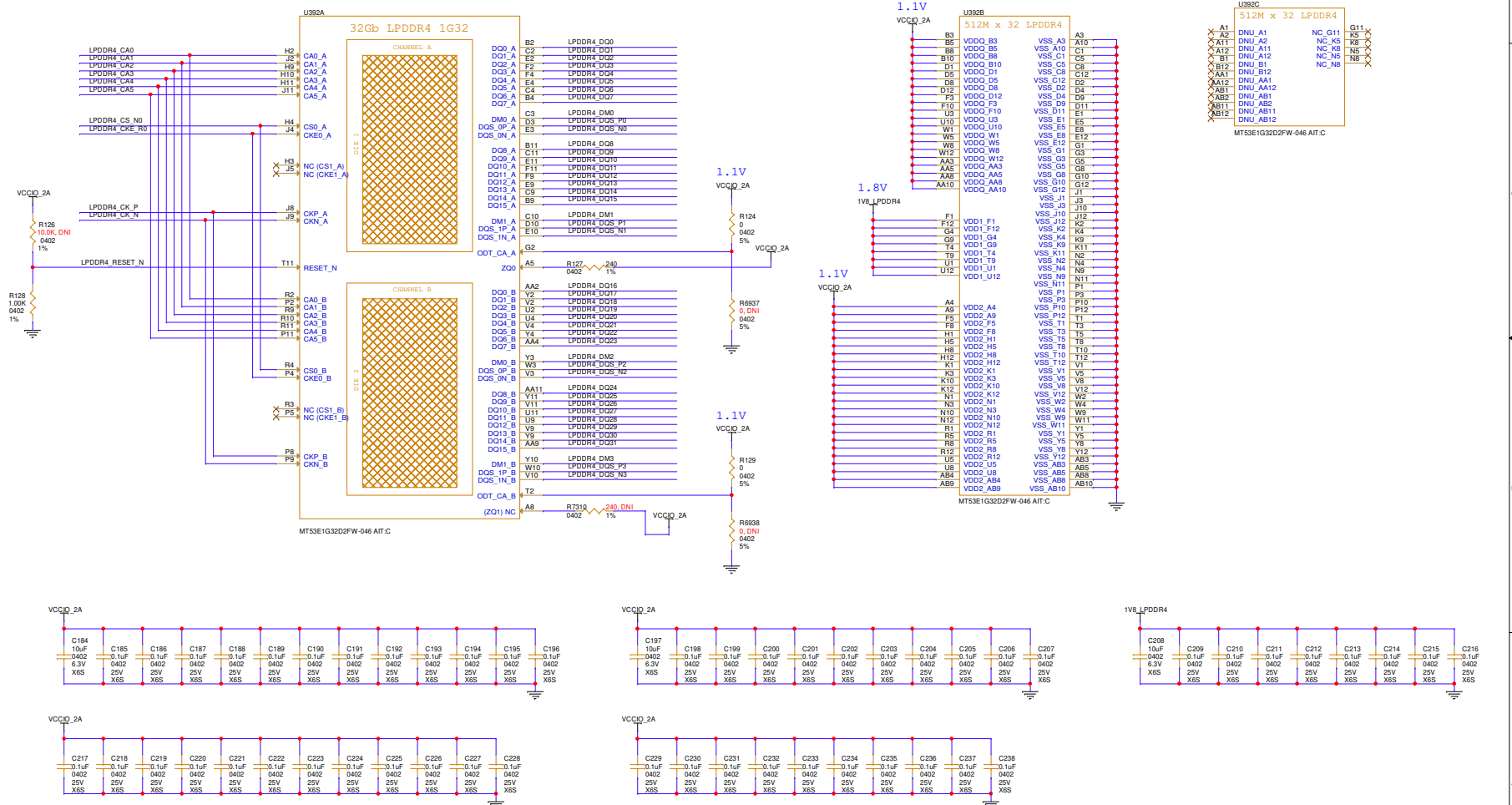


Place bottom FPGA cavity

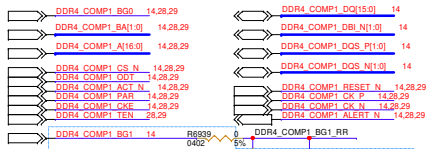


32-BIT LPDDR4

- LPDDR4_DQ[31:0] 13
- LPDDR4_DM[3:0] 13
- LPDDR4_DQS_P[3:0] 13
- LPDDR4_DQS_N[3:0] 13
- LPDDR4_CA[5:0] 13
- LPDDR4_CK_P 13
- LPDDR4_CK_N 13
- LPDDR4_RESET_N 13
- LPDDR4_CS_N0 13
- LPDDR4_CKE_B0 13

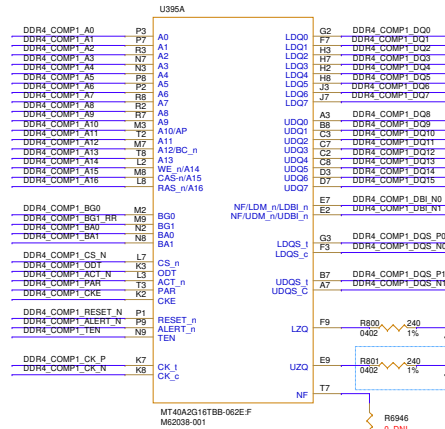


8GB DDR4 COMP1 BYTE 0-1

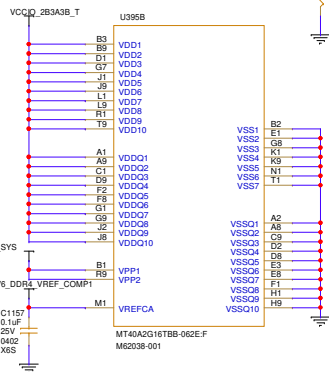


BOM NOTES:
Mono Die -> DNI
Twin Die -> stuff 0 Ohm

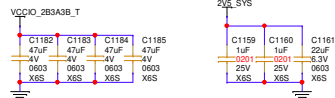
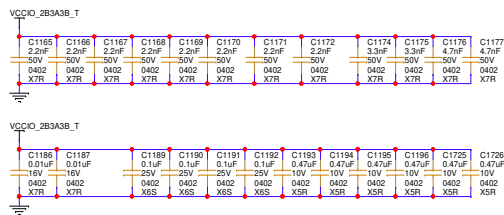
BOM NOTES:
Mono Die -> stuff 0 Ohm
Twin Die -> DNI



MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)
For Mono Die device, Pin E9 = GND; M9 = GND
For Twin Die device, Pin E9 = U2Q; M9 = BG1.

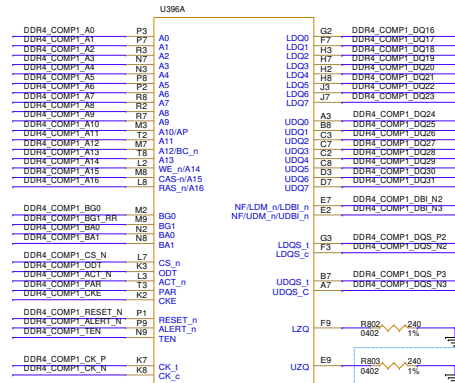
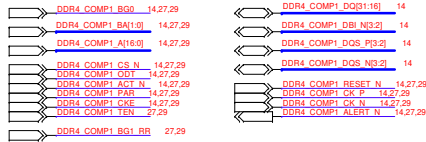


BOM NOTES:
Mono Die -> stuff 0 Ohm
Twin Die -> stuff 240 Ohm



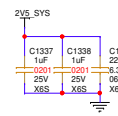
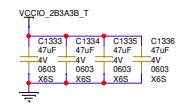
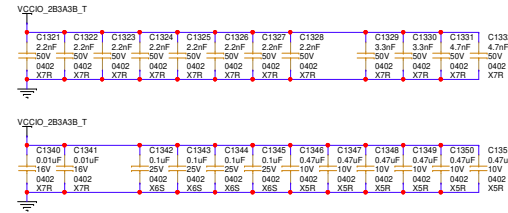
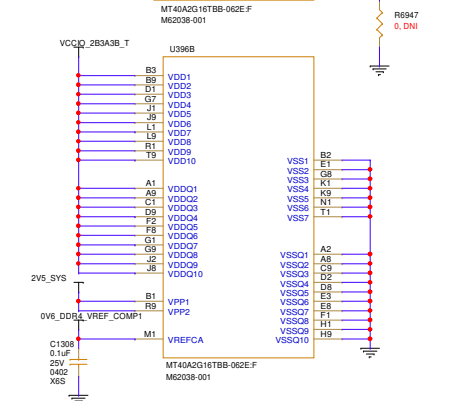
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8GB DDR4 COMP1 BYTE 2-3



MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)
 For Mono Die device, Pin E9 = GND; M9 = GND
 For Twin Die device, Pin E9 = U2G; M9 = BG1.

BOM NOTES:
 Mono Die -> stuff 0 Ohm
 Twin Die -> stuff 240 Ohm



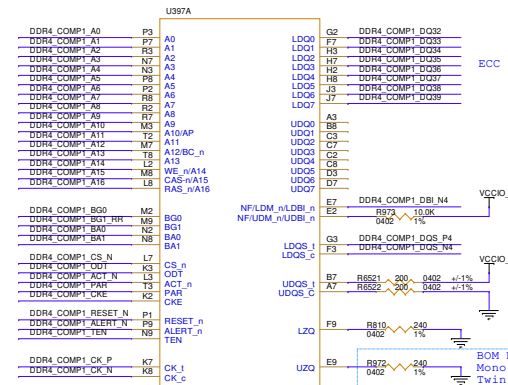
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Part # AGILEX 5 E-SERIES 065B PREMIUM DEV KIT			
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Date:	Thursday, September 18, 2014	Sheet	28 of 87

8GB DDR4 COMP1 BYTE ECC

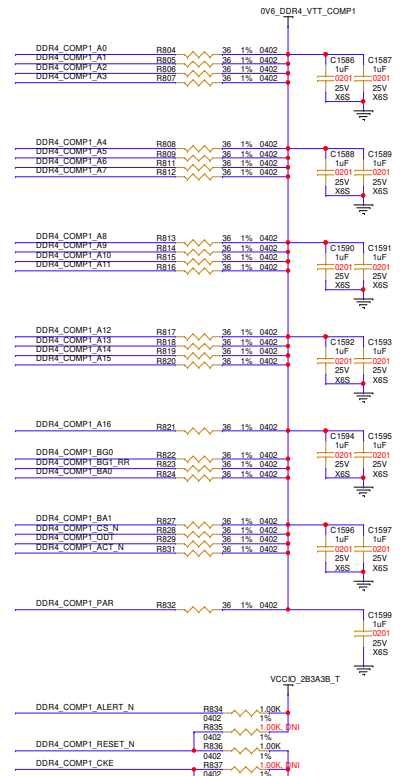
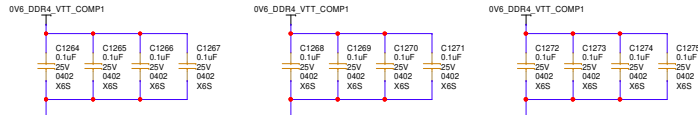
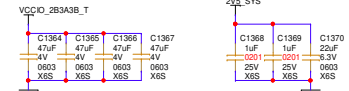
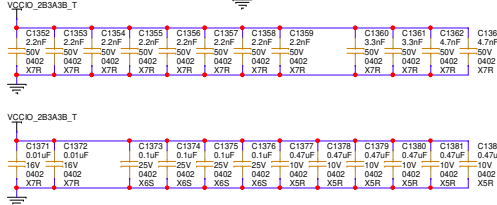
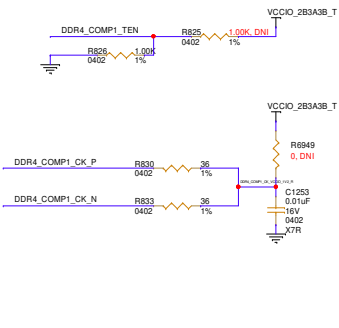
MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)

For Mono Die device, Pin E9 = GND; M9 = GND
For Twin Die device, Pin E9 = UZQ; M9 = BGL.

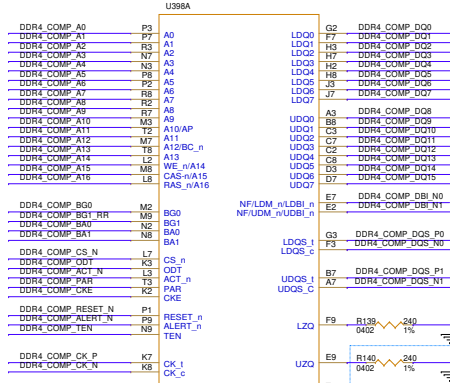
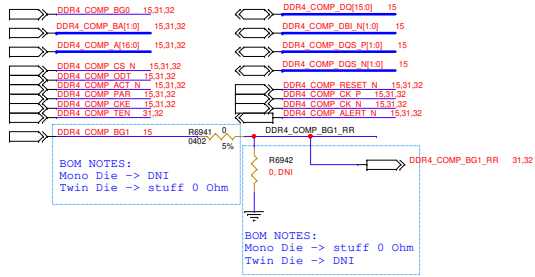
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- DDR4_COMP1_BA[1:0] 14,27,28
- DDR4_COMP1_A[16:0] 14,27,28
- DDR4_COMP1_CS_N 14,27,28
- DDR4_COMP1_ODT 14,27,28
- DDR4_COMP1_ACT_N 14,27,28
- DDR4_COMP1_PAR 14,27,28
- DDR4_COMP1_CKE 14,27,28
- DDR4_COMP1_BGL_RR 27,28
- DDR4_COMP1_DQ[3:32] 14
- DDR4_COMP1_DBI_N4 14
- DDR4_COMP1_DQS_P4 14
- DDR4_COMP1_DQS_N4 14
- DDR4_COMP1_RESET_N 14,27,28
- DDR4_COMP1_CK_P 14,27,28
- DDR4_COMP1_CK_N 14,27,28
- DDR4_COMP1_ALERT_N 14,27,28
- DDR4_COMP1_TEN 27,28



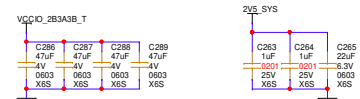
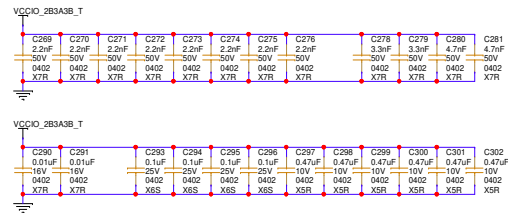
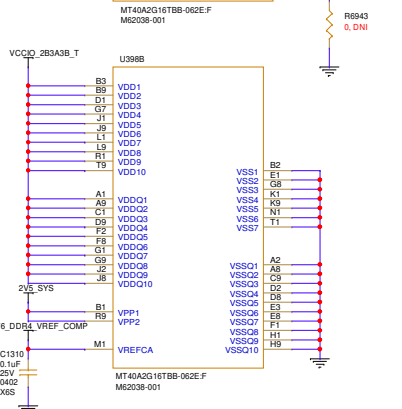
BOM NOTES:
Mono Die -> stuff 0 Ohm
Twin Die -> stuff 240 Ohm



HPS 8GB DDR4 COMPONENT BYTE 0-1



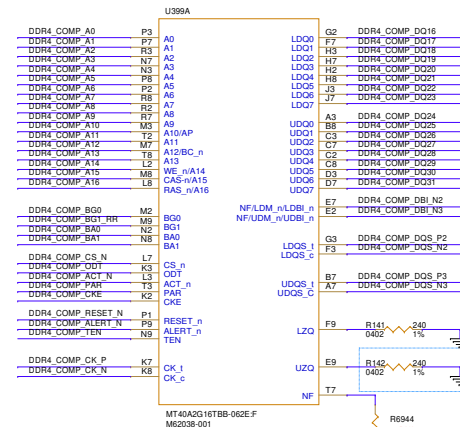
MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)
 For Mono Die device, Pin E9 = GND; M9 = GND
 For Twin Die device, Pin E9 = UZQ; M9 = BG1.



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C	180-0330713-A2	A2
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HPS 8GB DDR4 COMPONENT BYTE 2-3

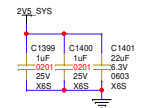
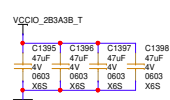
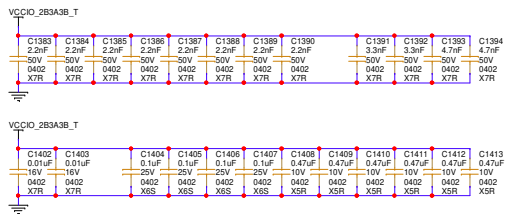
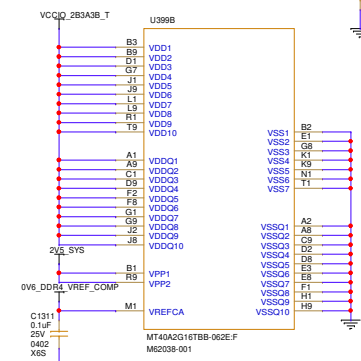
- DDR4_COMP_BG0 15,30,32
- DDR4_COMP_BA1[0] 15,30,32
- DDR4_COMP_A16[0] 15,30,32
- DDR4_COMP_CS_N 15,30,32
- DDR4_COMP_OBT 15,30,32
- DDR4_COMP_ACT_N 15,30,32
- DDR4_COMP_PAR 15,30,32
- DDR4_COMP_CKE 15,30,32
- DDR4_COMP_TEN 30,32
- DDR4_COMP_BG1_RR 30,32
- DDR4_COMP_DQ31[16] 15
- DDR4_COMP_DBI_N[3:2] 15
- DDR4_COMP_DQS_P[3:2] 15
- DDR4_COMP_DQS_N[3:2] 15
- DDR4_COMP_RESET_N 15,30,32
- DDR4_COMP_CK_P 15,30,32
- DDR4_COMP_CK_N 15,30,32
- DDR4_COMP_ALERT_N 15,30,32



MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)

For Mono Die device, Pin E9 = GND; M9 = GND.
For Twin Die device, Pin E9 = UZ0; M9 = BG1.

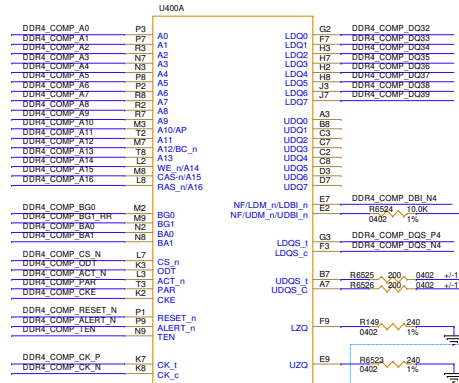
BOM NOTES:
Mono Die -> stuff 0 Ohm
Twin Die -> stuff 240 Ohm



HPS 8GB DDR4 COMPONENT BYTE ECC

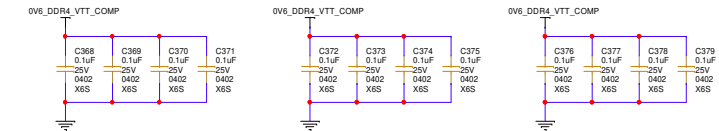
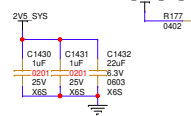
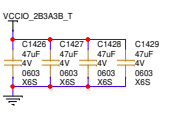
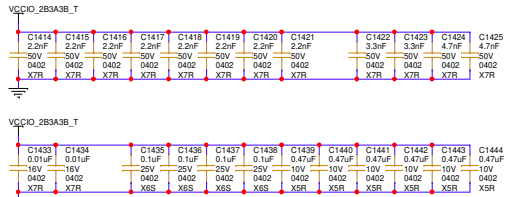
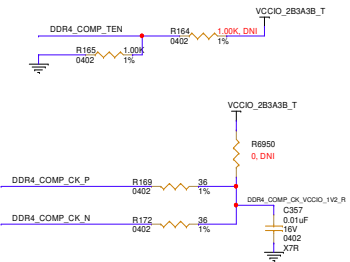
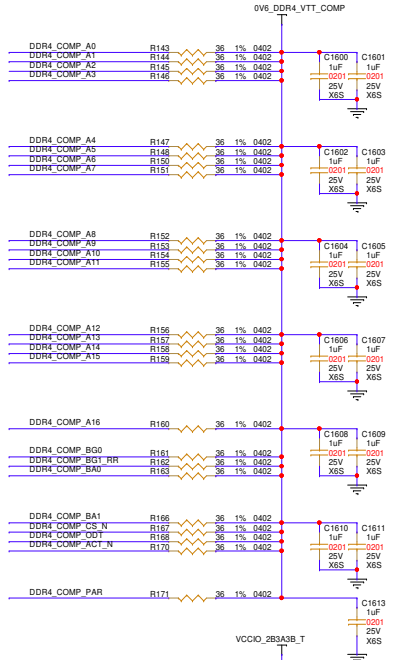
MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)
 For Mono Die device, Pin E9 = GND; M9 = GND
 For Twin Die device, Pin E9 = U2G; M9 = BGL

- DDR4_COMP_BG0 15,30,31
- DDR4_COMP_BA[1:0] 15,30,31
- DDR4_COMP_A[16:0] 15,30,31
- DDR4_COMP_CS_N 15,30,31
- DDR4_COMP_ODT 15,30,31
- DDR4_COMP_ACT_N 15,30,31
- DDR4_COMP_PAR 15,30,31
- DDR4_COMP_CKE 15,30,31
- DDR4_COMP_BGL_RR 30,31
- DDR4_COMP_DQ[9:3] 15
- DDR4_COMP_DBI_N4 15
- DDR4_COMP_DQS_P4 15
- DDR4_COMP_DQS_N4 15
- DDR4_COMP_RESET_N 15,30,31
- DDR4_COMP_CK_P 15,30,31
- DDR4_COMP_CK_N 15,30,31
- DDR4_COMP_ALERT_N 15,30,31
- DDR4_COMP_TEN 30,31



ECC

BOM NOTES:
 Mono Die -> stuff 0 Ohm
 Twin Die -> stuff 240 Ohm

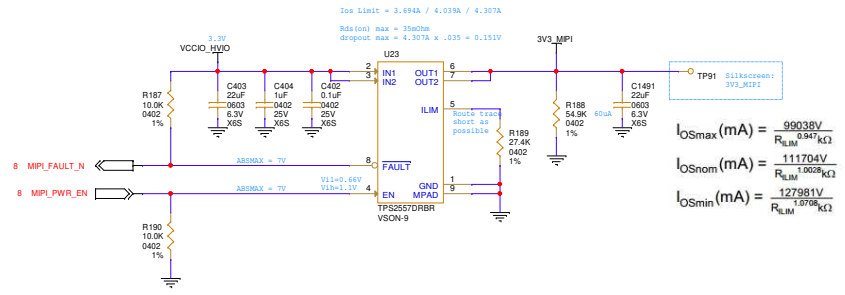


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The AGILEX 5 E-SERIES 06S6 PREMIUM DEV KIT		
Size	Document Number	Rev
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Date:	Thursday, September 19, 2014	Sheet 32 of 87

BLANK



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File: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT		
Size	Document Number	Rev
C	180-0330713-A2	A2
Date:	Thursday, September 19, 2024	Sheet 33 of 87

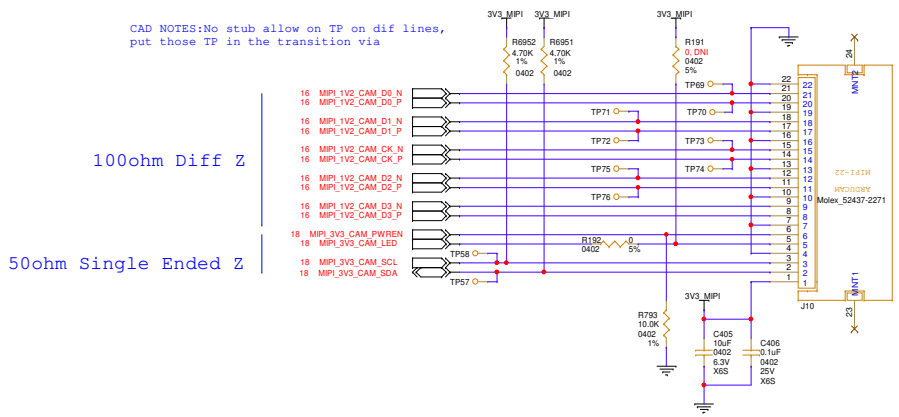


$$I_{OSmax} (mA) = \frac{99038V}{R_{LIM} 0.947 k\Omega}$$

$$I_{OSnom} (mA) = \frac{111704V}{R_{LIM} 7.068 k\Omega}$$

$$I_{OSmin} (mA) = \frac{127981V}{R_{LIM} 1.079 k\Omega}$$

CAD NOTES: No stub allow on TP on dif lines, put those TP in the transition via

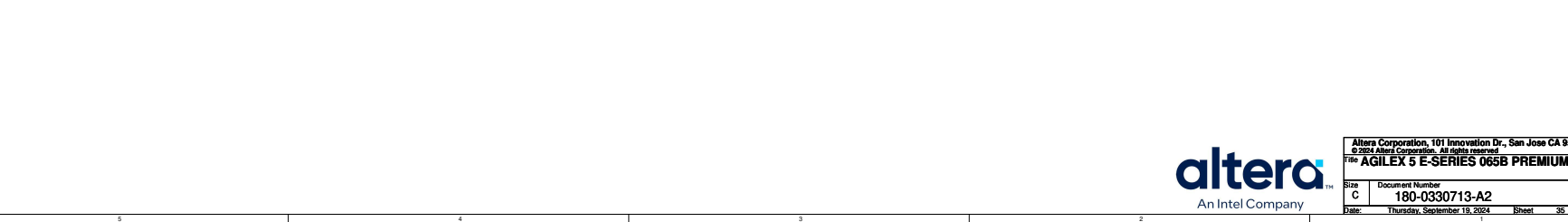
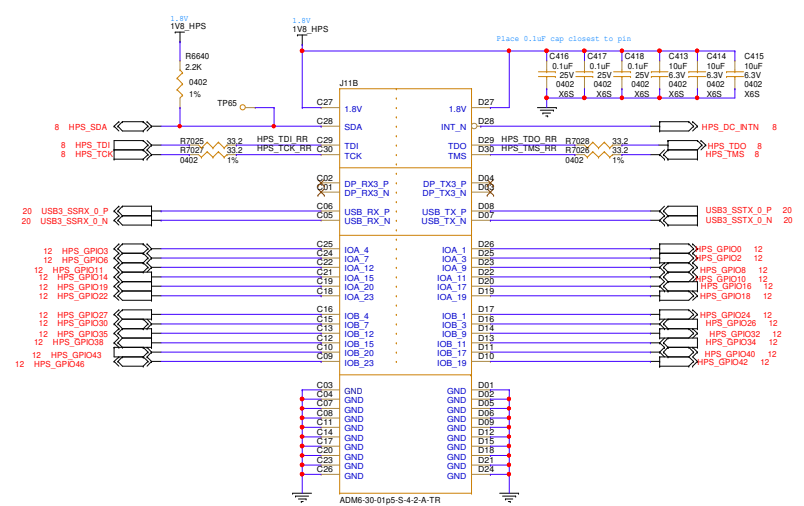
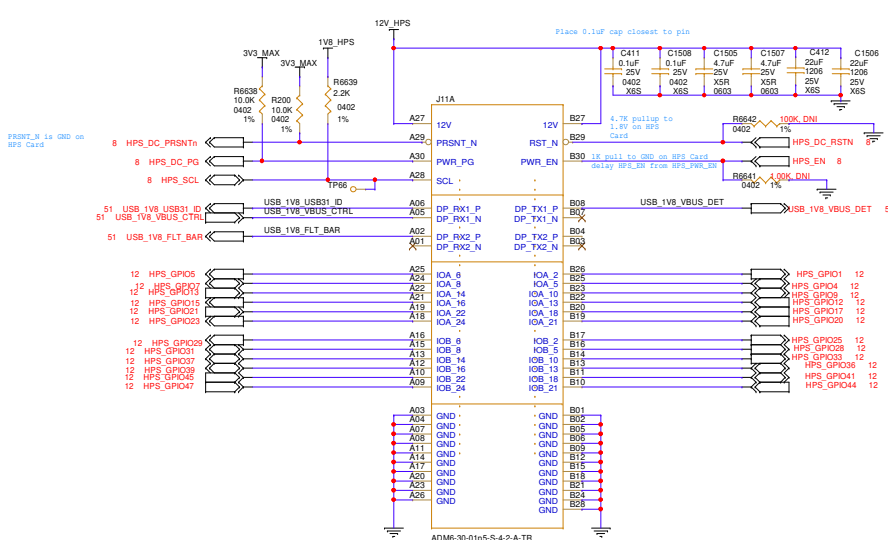
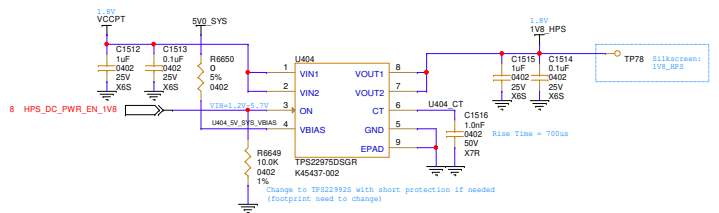
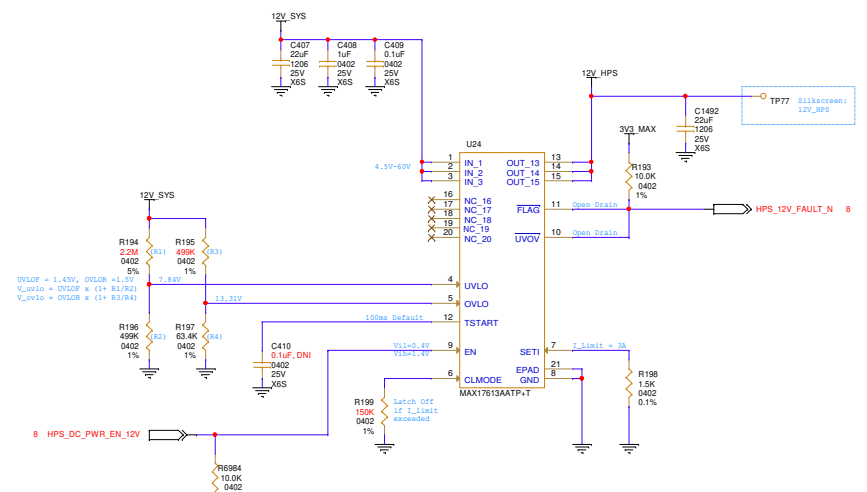


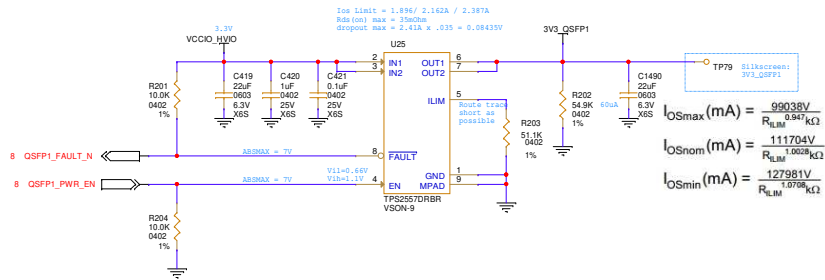
100ohm Diff Z

50ohm Single Ended Z



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Size	Document Number	Rev
C	180-0330713-A2	A2
Date:	Thursday, September 19, 2004	Sheet 34 of 87



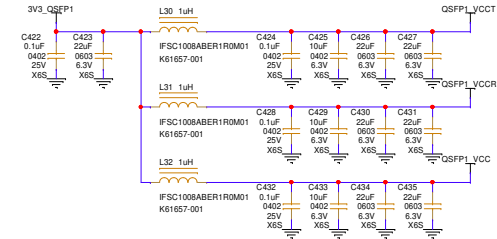


NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

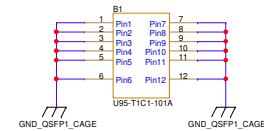
NOTE 2: QSFP 100-ohm termination is implemented via the FPGA on-chip termination.

NOTE 3: DC blocking capacitors are in the module for RX and TX.

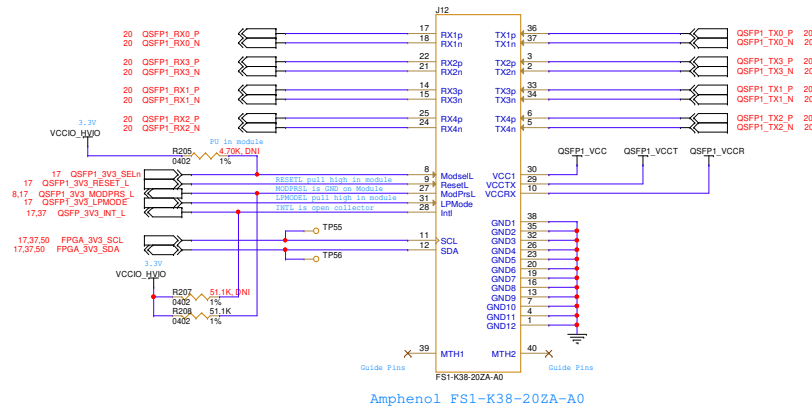
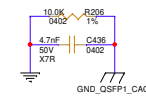
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



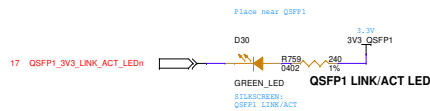
Place close to QSFP Connector

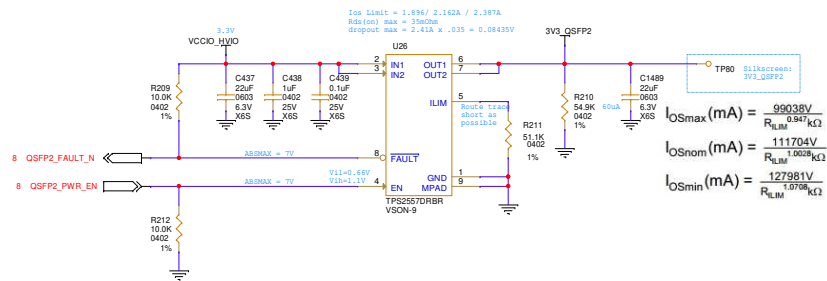


Amphenol U95-T1C1-101A



Amphenol FS1-K38-202A-A0



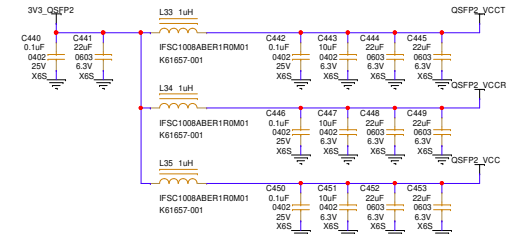


NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

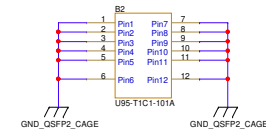
NOTE 2: zQSFP 100-ohm termination is implemented via the FPGA on-chip termination.

NOTE 3: DC blocking capacitors are in the module for RX and TX.

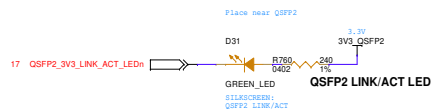
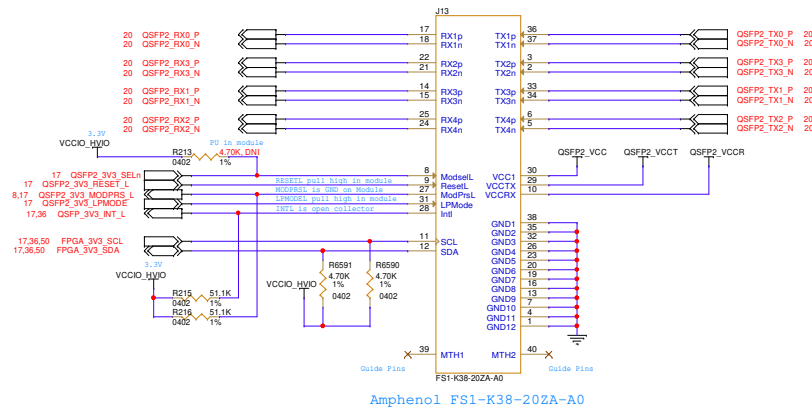
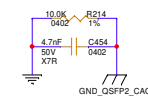
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.

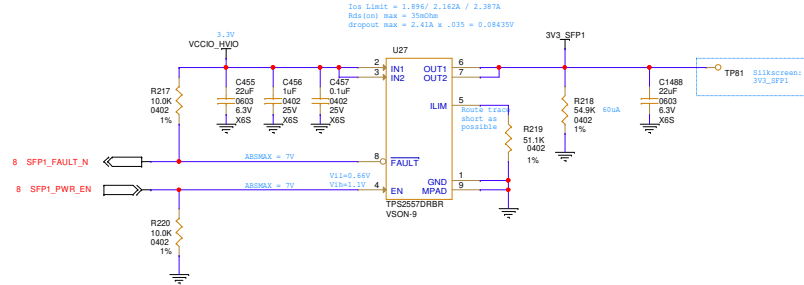


Place close to zQSFP Connector



Amphenol U95-T1C1-101A

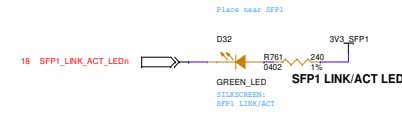
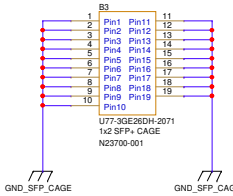
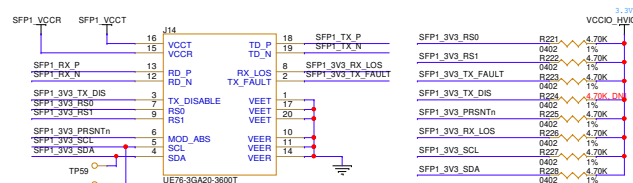
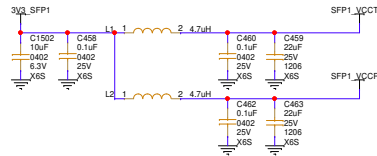




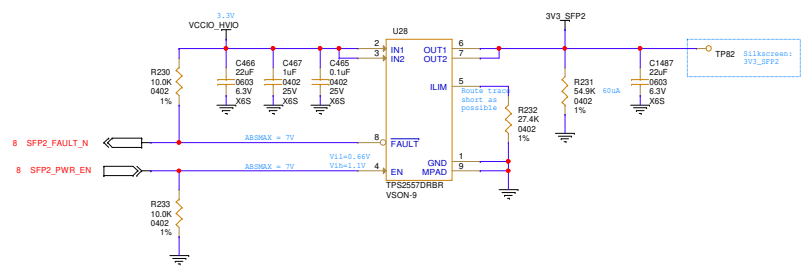
NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

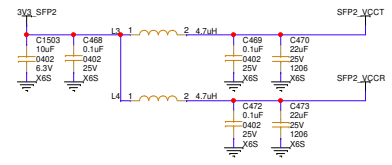
NOTE 3: DC blocking capacitors are in the module for RX and TX.



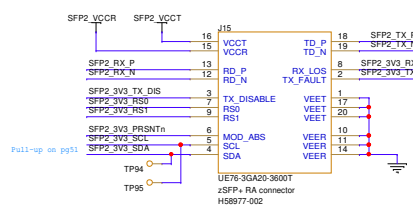
I_{oh} Limit = 1.896V / 2.162A / 2.387A
 R_{ds(on)} max = 350mΩ
 ΔV_{drop} max = 2.41A × .035 = 0.08435V



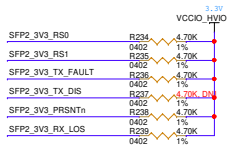
NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.
 NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.
 NOTE 3: DC blocking capacitors are in the module for RX and TX.



Level I power is < 1W (0.3 A)
 Level II power is < 1.5W (0.45 A)
 Level II Instantaneous peak current per rail 600mA

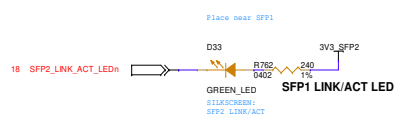


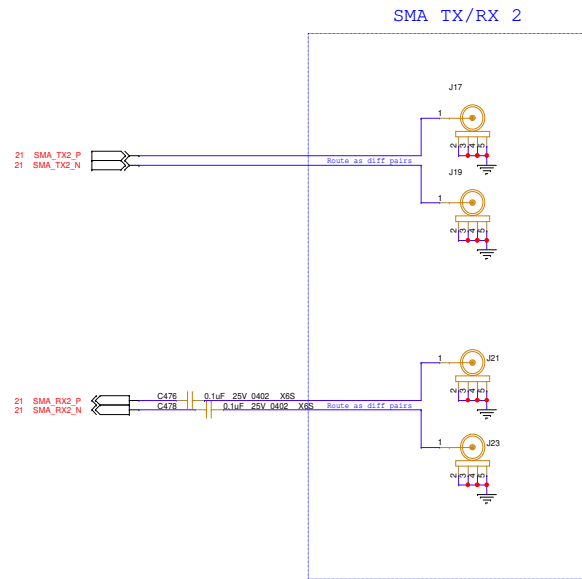
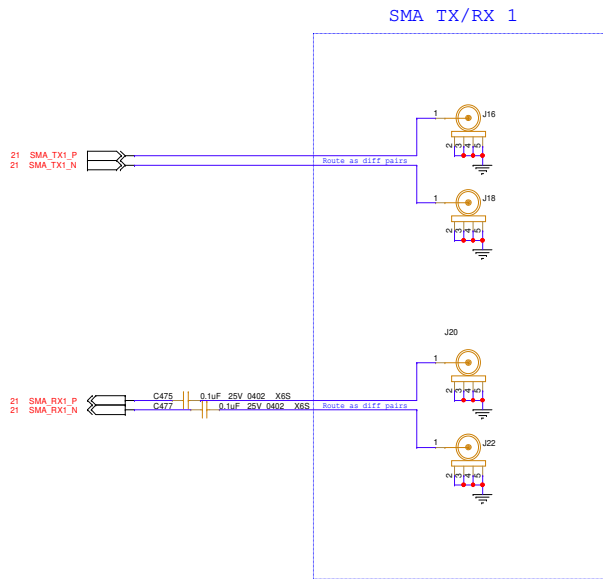
Optical (SFP+) Connector, case in page 38 B3



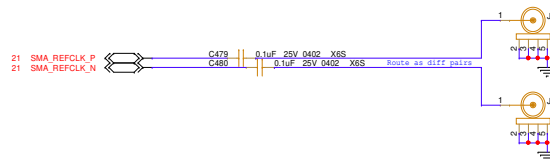
- 21 SFP2 TX_P
- 21 SFP2 TX_N
- 21 SFP2 RX_P
- 21 SFP2 RX_N
- 18 SFP2_3V3_RS0
- 18 SFP2_3V3_RS1
- 18 SFP2_3V3_TX_FAULT
- 18 SFP2_3V3_TX_DIS
- 18 SFP2_3V3_RX_LOS
- 18 SFP2_3V3_TX_FAULT
- 8,18 SFP2_3V3_PRSENtN
- 51 SFP2_3V3_SCL
- 51 SFP2_3V3_SDA

SFP modules have RS1 connected to GND.
 If using SFP+ Rate Select pin are defined as:
 RS1=0 -> TX datarates <= 4.25GB/s
 RS1=1 -> TX datarates > 4.25GB/s
 RS0=0 -> RX datarates <= 4.25GB/s
 RS0=1 -> RX datarates > 4.25GB/s





SMA XCVR REFCLK IN



FMC+ Connector (Vita 57.4) Complete Pin Table

FMC Connector (Vita 57.1) Complete Pin Table

14 x 40	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRRNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSN2_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	GND	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N	GND
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	GND	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	GND	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND

FMC+ Voltage Specification

Voltage Supply	Allowable Voltage Range	No Pins	Max Amps	Tolerance	Max Capacitive Load
VADJ	0 - 3.3V	4	4	+/- 5%	1000 uF
VIO_B_M2C	0 - VADJ	2	1.15	+/- 5%	500 uF
VREF_A_M2C	0 - VADJ	1	1mA	+/- 2%	10 uF
VREF_B_M2C	0 - VIO_B_M2C	1	1mA	+/- 2%	10 uF
3P3VAUX	3.3V	1	20mA	+/- 5%	150 uF
3P3V	3.3V	5	3	+/- 5%	1000 uF
12P0V	12V	5	1	+/- 5%	1000 uF

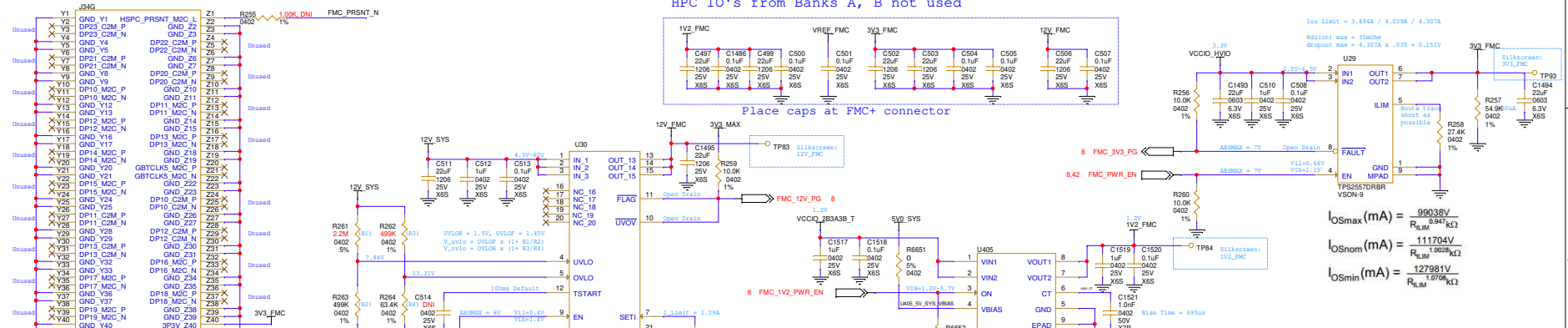
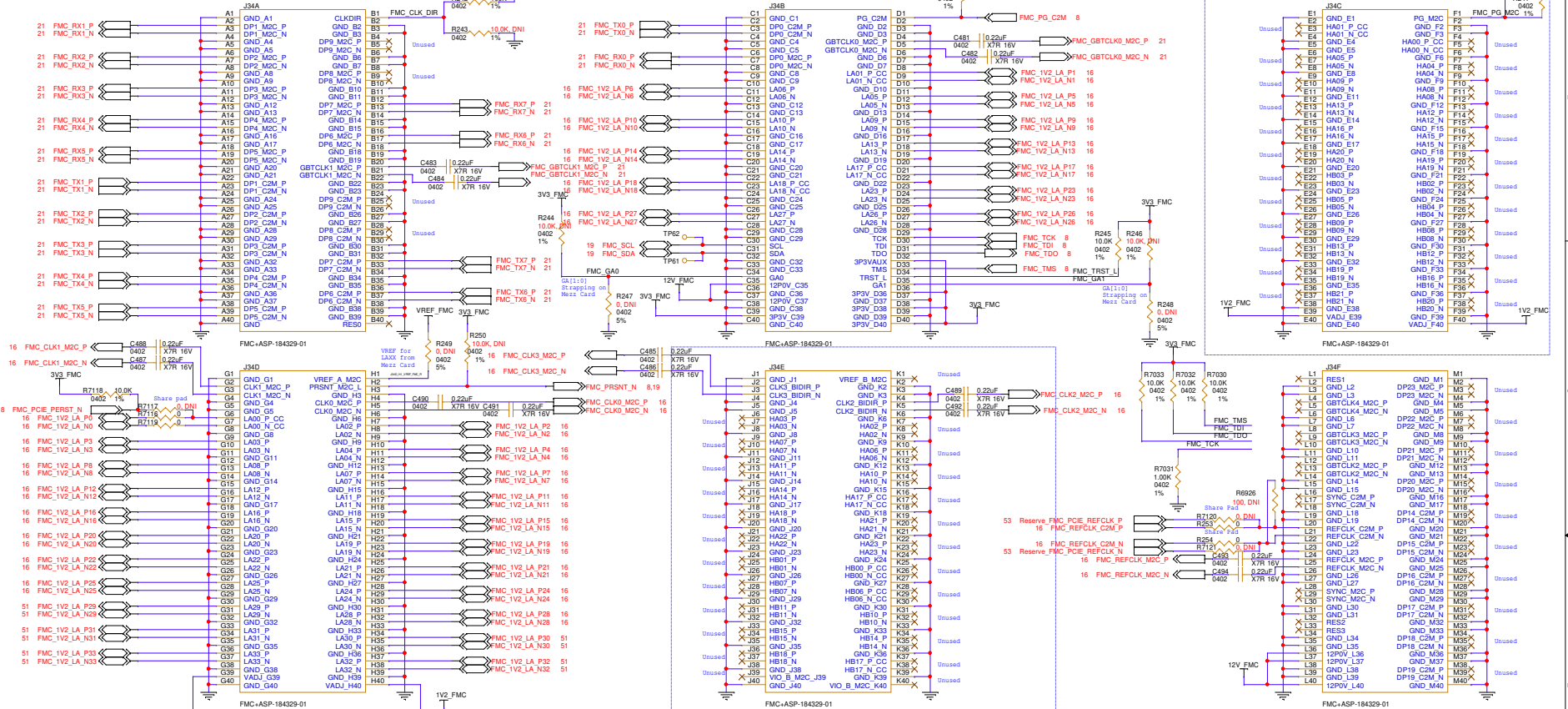
Supported FMC Cards:

1. FMC+ PCIe Gen4 x16 RootPort Card (HighTech Global)
- ** Note: Only support PCIe Gen4 x4 **
2. FMC+ HDMI 2.1 Card Rev9 (Bitec)
3. FMC+ DP 1.4 Rev12 (Bitec)



Only Serdes TX / RX Channels [7:0] are available, Channels [23:8] are unused.

FMC+ Connector



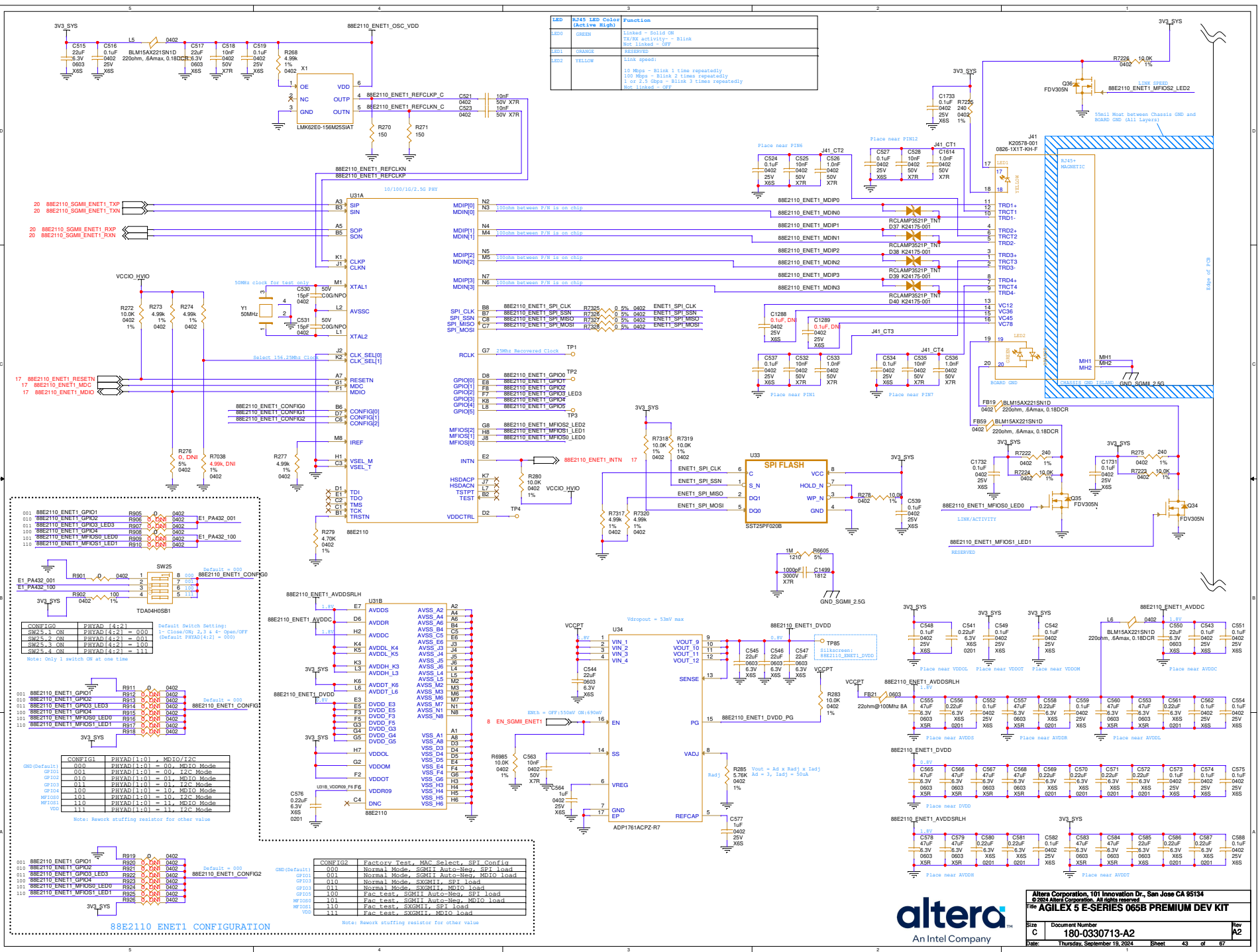
$I_{OSmax} (mA) = \frac{99038V}{R_{LIM} \cdot 0.947k\Omega}$
 $I_{OSnom} (mA) = \frac{111704V}{1.000k\Omega}$
 $I_{OSmin} (mA) = \frac{127581V}{R_{LIM} \cdot 0.978k\Omega}$

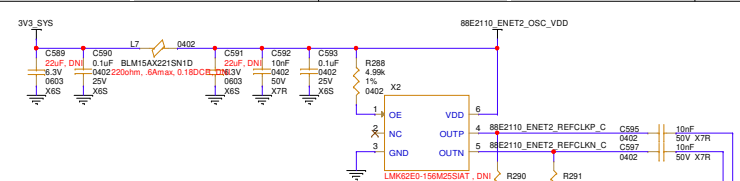
Rise Time = 495ns
 Change to 70025022 with short protection if not (footprint need to change)

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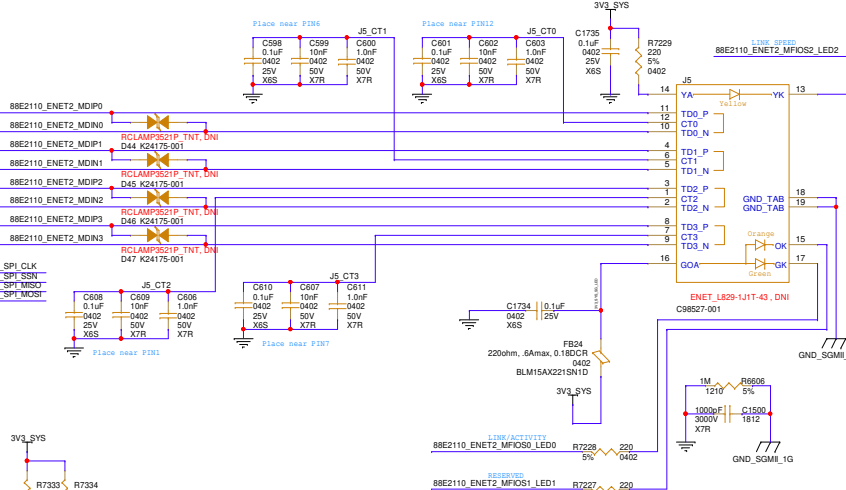
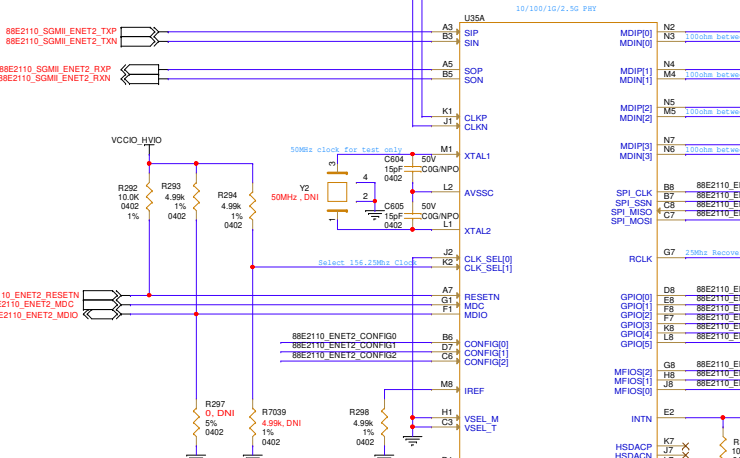
Size: 180-0330713-A2
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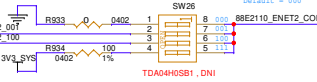


LED	RJ45 LED Color (Active High)	Function
LED0	GREEN	Linker - Solid ON TX/RX activity - Blink No Linked - Off
LED1	ORANGE	RESERVED
LED2	YELLOW	Link Speed.

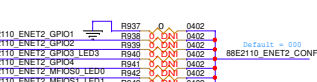
10 Mbps - Blink 1 time repeatedly
100 Mbps - Blink 2 times repeatedly
1 Gbps - Blink 3 times repeatedly
No Linked - Off



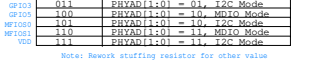
Pin	88E2110 ENET2	Component	Value	Notes
001	88E2110 ENET2 GPIO1	R927	0 0402	E2_PA432_001
010	88E2110 ENET2 GPIO2	R928	0 0402	E2_PA432_001
101	88E2110 ENET2 GPIO3	R929	0 0402	E2_PA432_100
102	88E2110 ENET2 GPIO4	R930	0 0402	E2_PA432_100
103	88E2110 ENET2 MFIOS2_0	R931	0 0402	E2_PA432_100
110	88E2110 ENET2 MFIOS2_1	R932	0 0402	E2_PA432_100



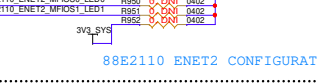
COMP100	PRIVAD1 [4:2]	Default	Default Settings
SW25_2_ON	PRIVAD1[4:2] = 000	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_3_ON	PRIVAD1[4:2] = 001	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_4_ON	PRIVAD1[4:2] = 111	0	1- Close/000, 2, 3 & 4 - Open/0FF



COMP100	PRIVAD1 [4:2]	Default	Default Settings
SW25_2_ON	PRIVAD1[4:2] = 000	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_3_ON	PRIVAD1[4:2] = 001	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_4_ON	PRIVAD1[4:2] = 111	0	1- Close/000, 2, 3 & 4 - Open/0FF

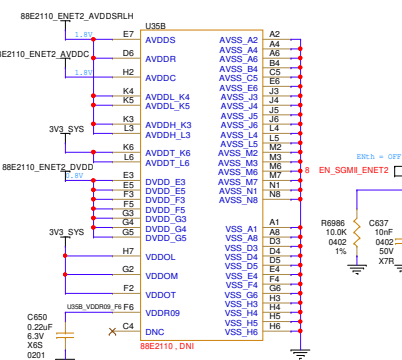


COMP100	PRIVAD1 [4:2]	Default	Default Settings
SW25_2_ON	PRIVAD1[4:2] = 000	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_3_ON	PRIVAD1[4:2] = 001	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_4_ON	PRIVAD1[4:2] = 111	0	1- Close/000, 2, 3 & 4 - Open/0FF

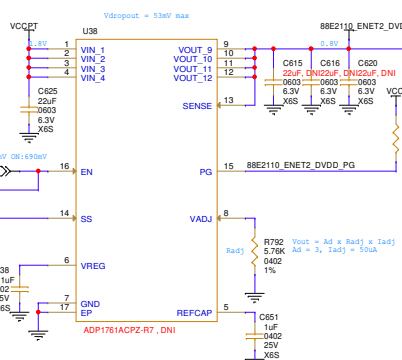


COMP100	PRIVAD1 [4:2]	Default	Default Settings
SW25_2_ON	PRIVAD1[4:2] = 000	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_3_ON	PRIVAD1[4:2] = 001	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_4_ON	PRIVAD1[4:2] = 111	0	1- Close/000, 2, 3 & 4 - Open/0FF

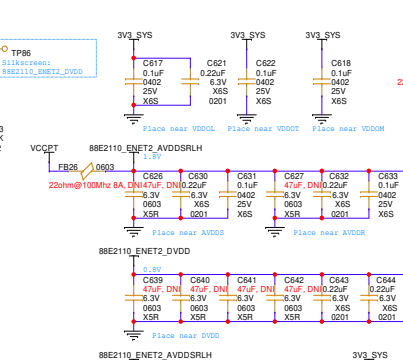
88E2110 ENET2 CONFIGURATION



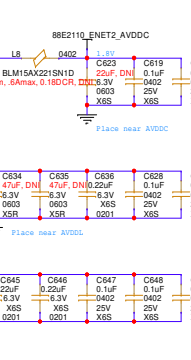
COMP100	PRIVAD1 [4:2]	Default	Default Settings
SW25_2_ON	PRIVAD1[4:2] = 000	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_3_ON	PRIVAD1[4:2] = 001	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_4_ON	PRIVAD1[4:2] = 111	0	1- Close/000, 2, 3 & 4 - Open/0FF



COMP100	PRIVAD1 [4:2]	Default	Default Settings
SW25_2_ON	PRIVAD1[4:2] = 000	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_3_ON	PRIVAD1[4:2] = 001	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_4_ON	PRIVAD1[4:2] = 111	0	1- Close/000, 2, 3 & 4 - Open/0FF



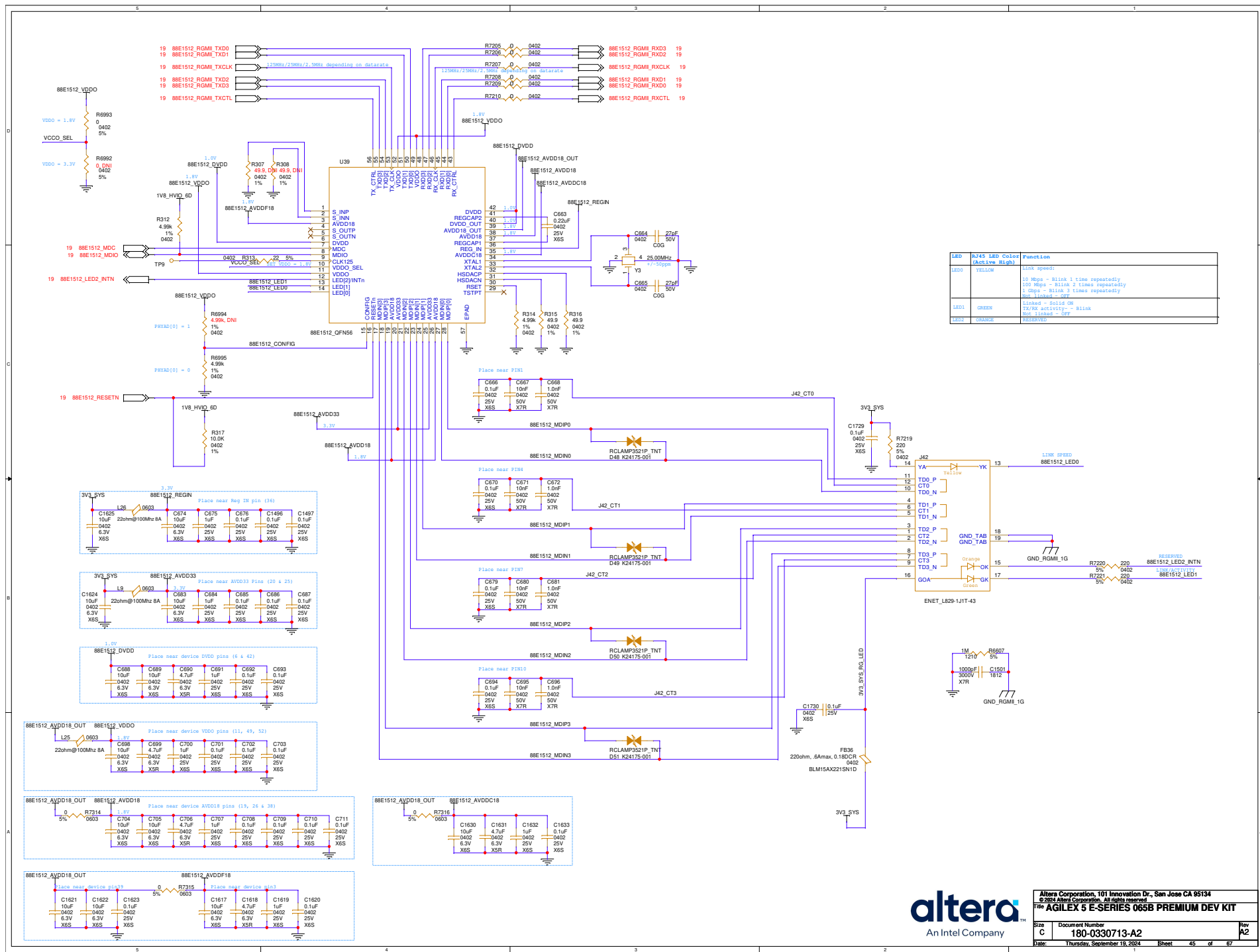
COMP100	PRIVAD1 [4:2]	Default	Default Settings
SW25_2_ON	PRIVAD1[4:2] = 000	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_3_ON	PRIVAD1[4:2] = 001	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_4_ON	PRIVAD1[4:2] = 111	0	1- Close/000, 2, 3 & 4 - Open/0FF



COMP100	PRIVAD1 [4:2]	Default	Default Settings
SW25_2_ON	PRIVAD1[4:2] = 000	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_3_ON	PRIVAD1[4:2] = 001	0	1- Close/000, 2, 3 & 4 - Open/0FF
SW25_4_ON	PRIVAD1[4:2] = 111	0	1- Close/000, 2, 3 & 4 - Open/0FF

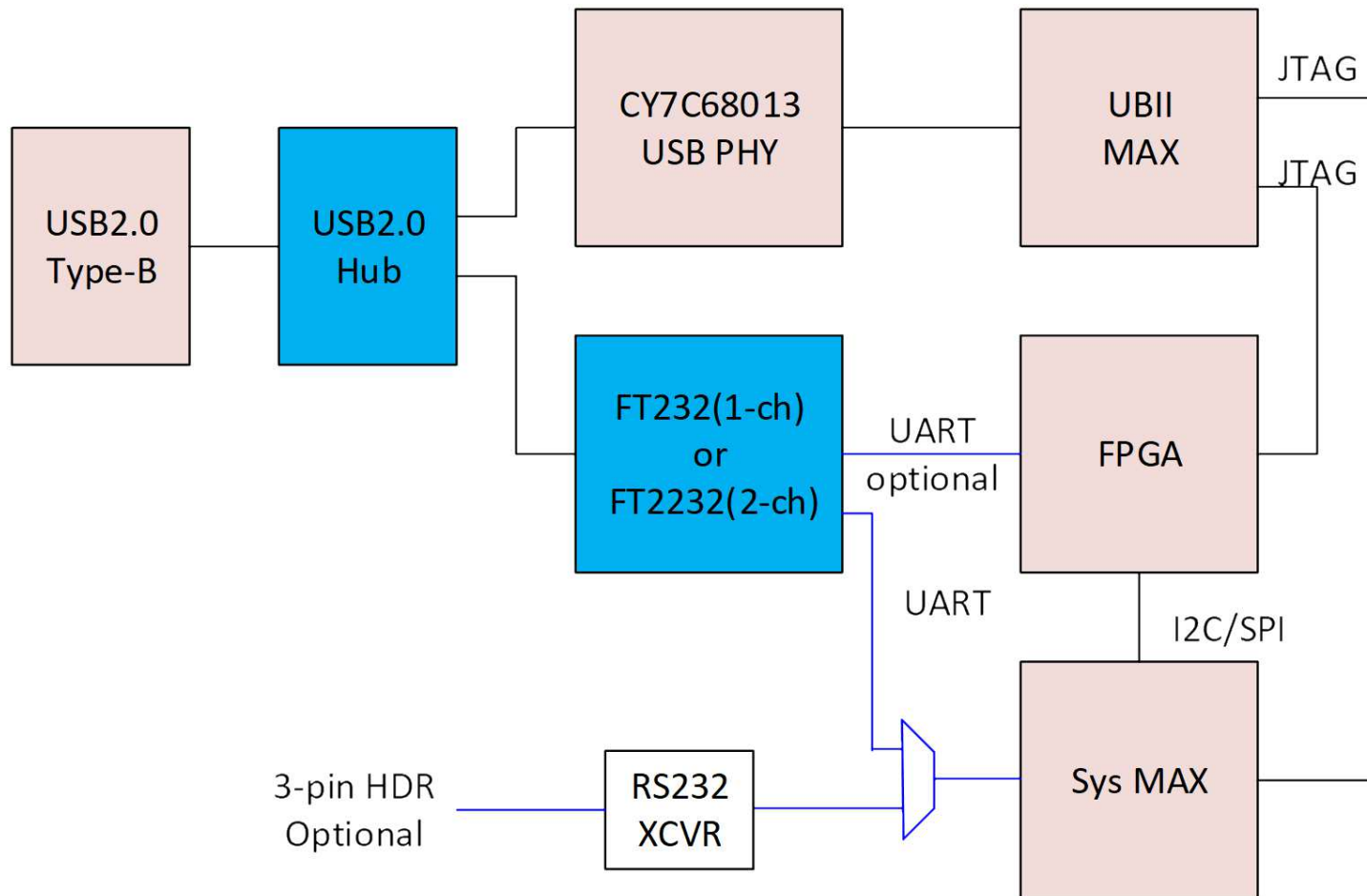
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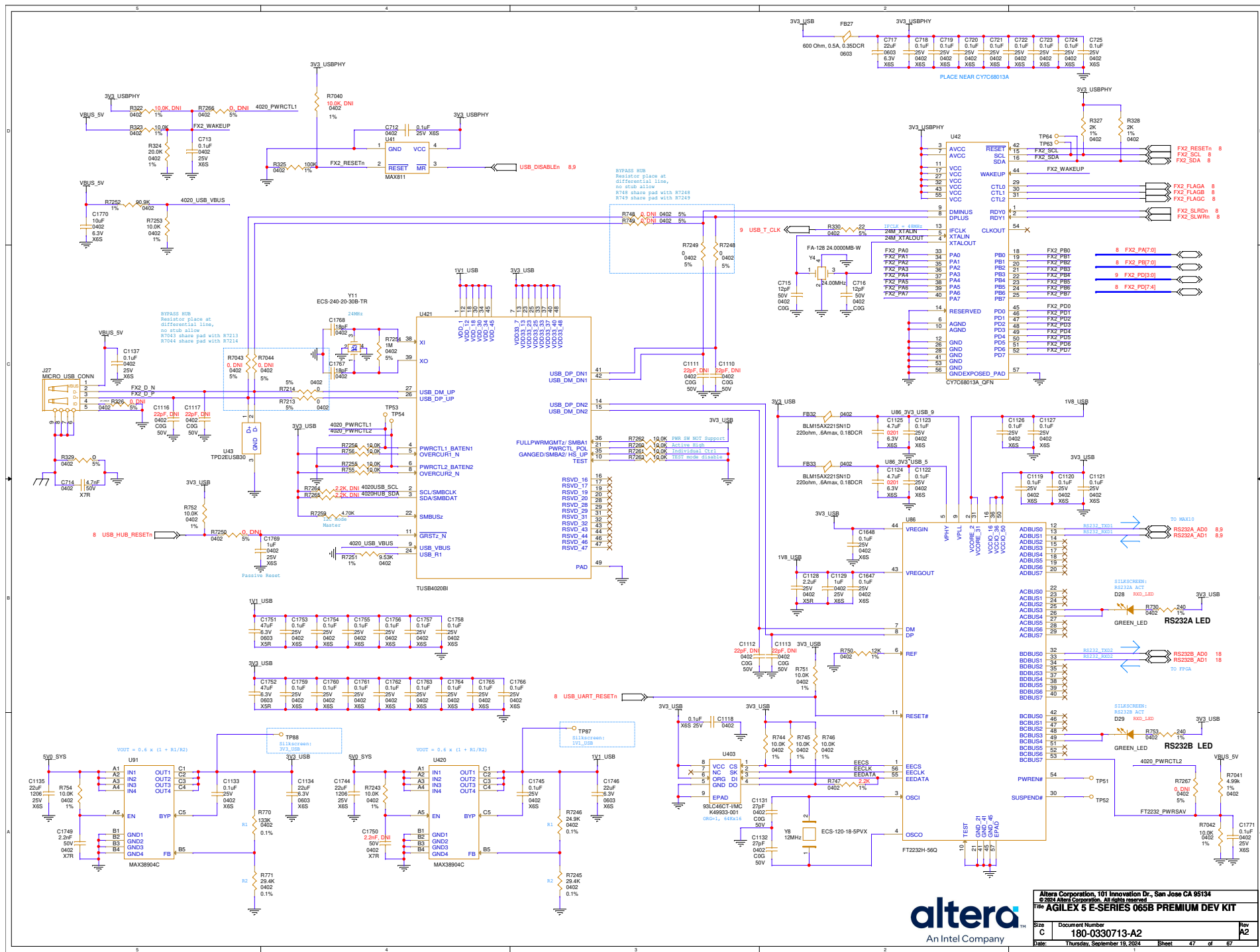
Size: Document Number: 180-0330713-A2
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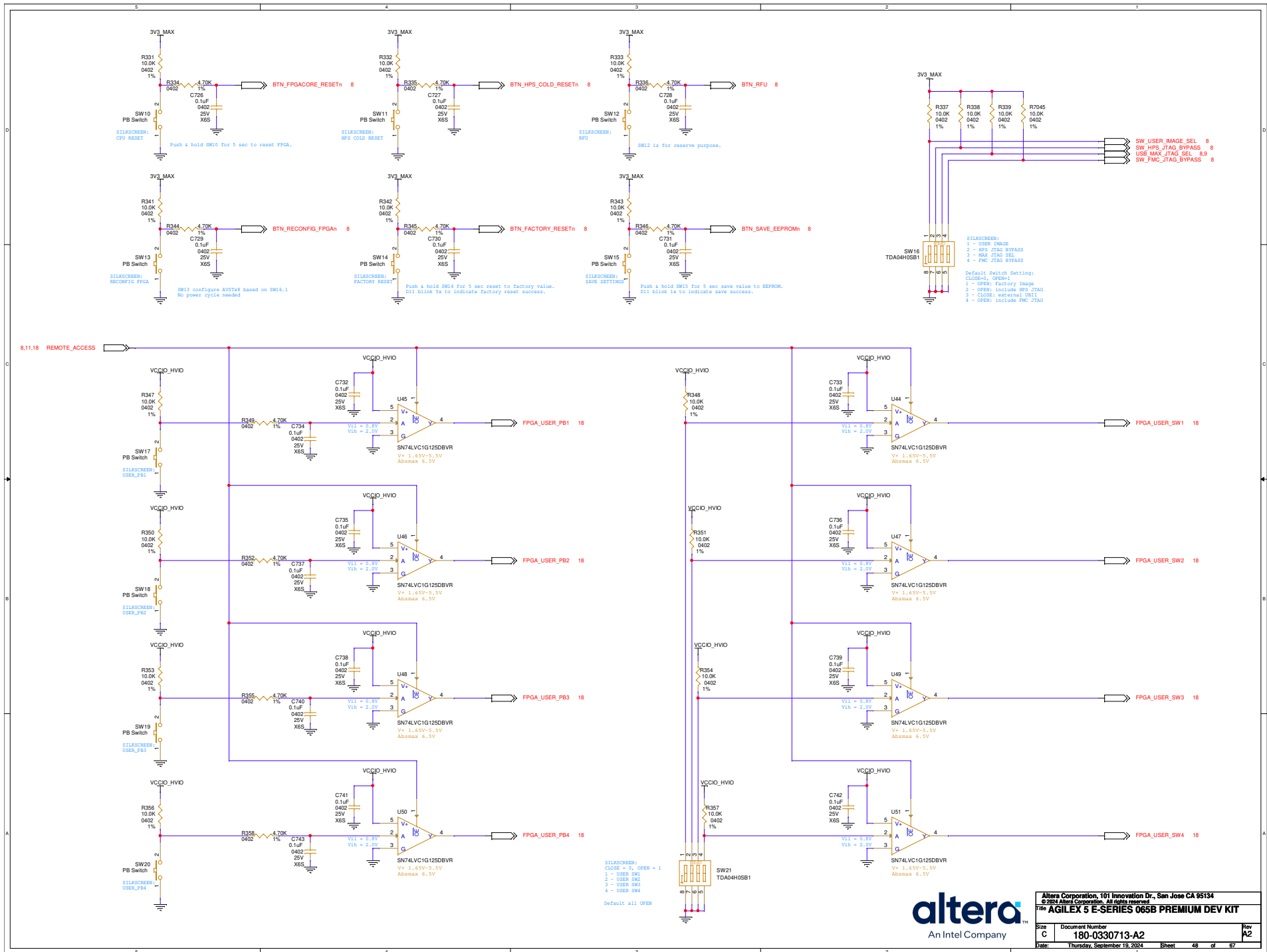


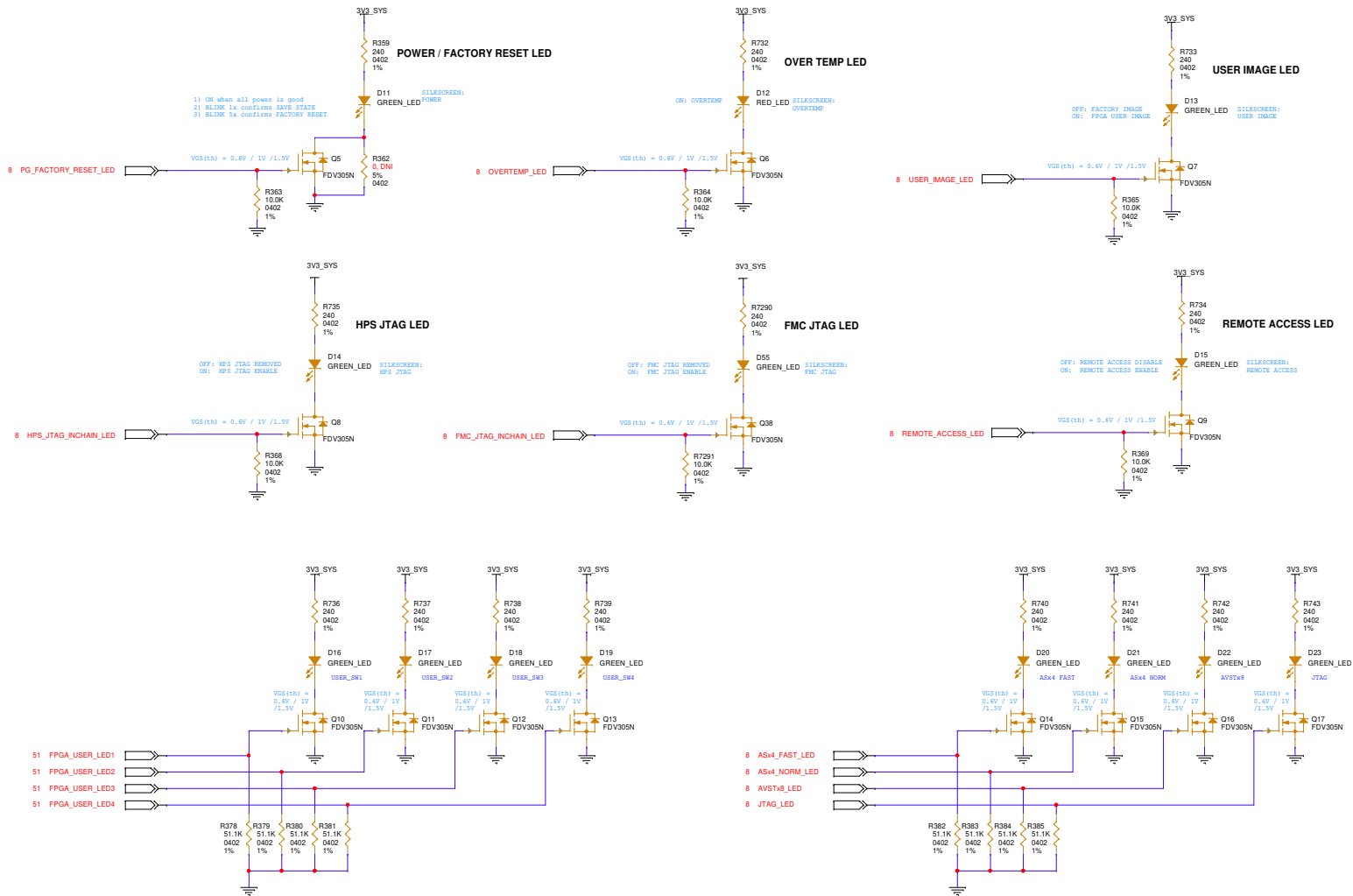
LED	LED Color (Relative to Board)	Function
LED0	YELLOW	LINK SPEED: 10 Mbps - Blink 1 time repeatedly 100 Mbps - Blink 2 times repeatedly 1 Gbps - Blink 3 times repeatedly Not linked - OFF
LED1	GREEN	Linked - Solid ON Link Activity - Blink Not linked - OFF
LED2	ORANGE	RESERVED



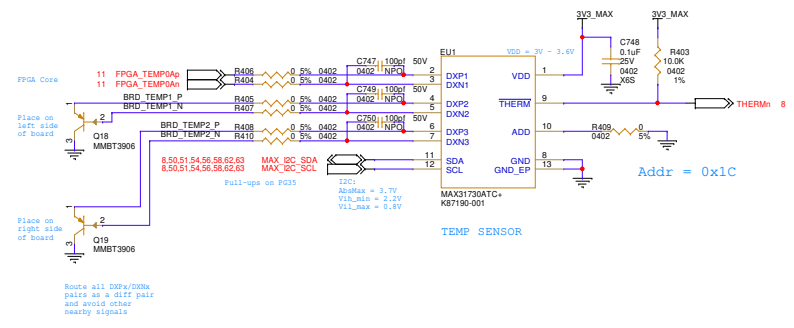
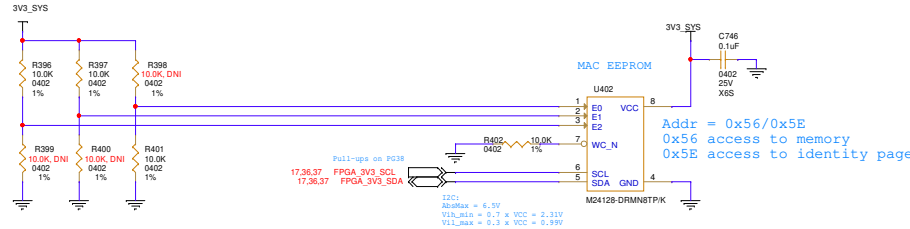
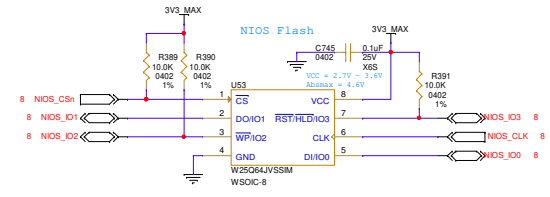
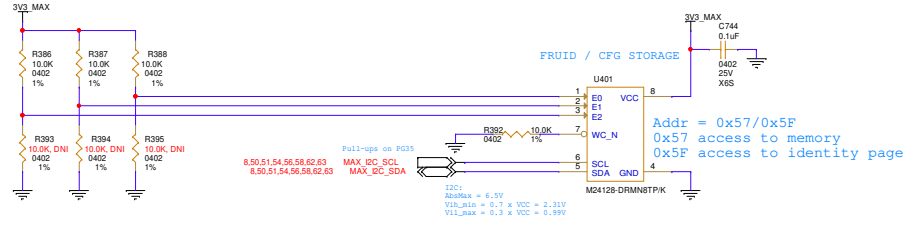




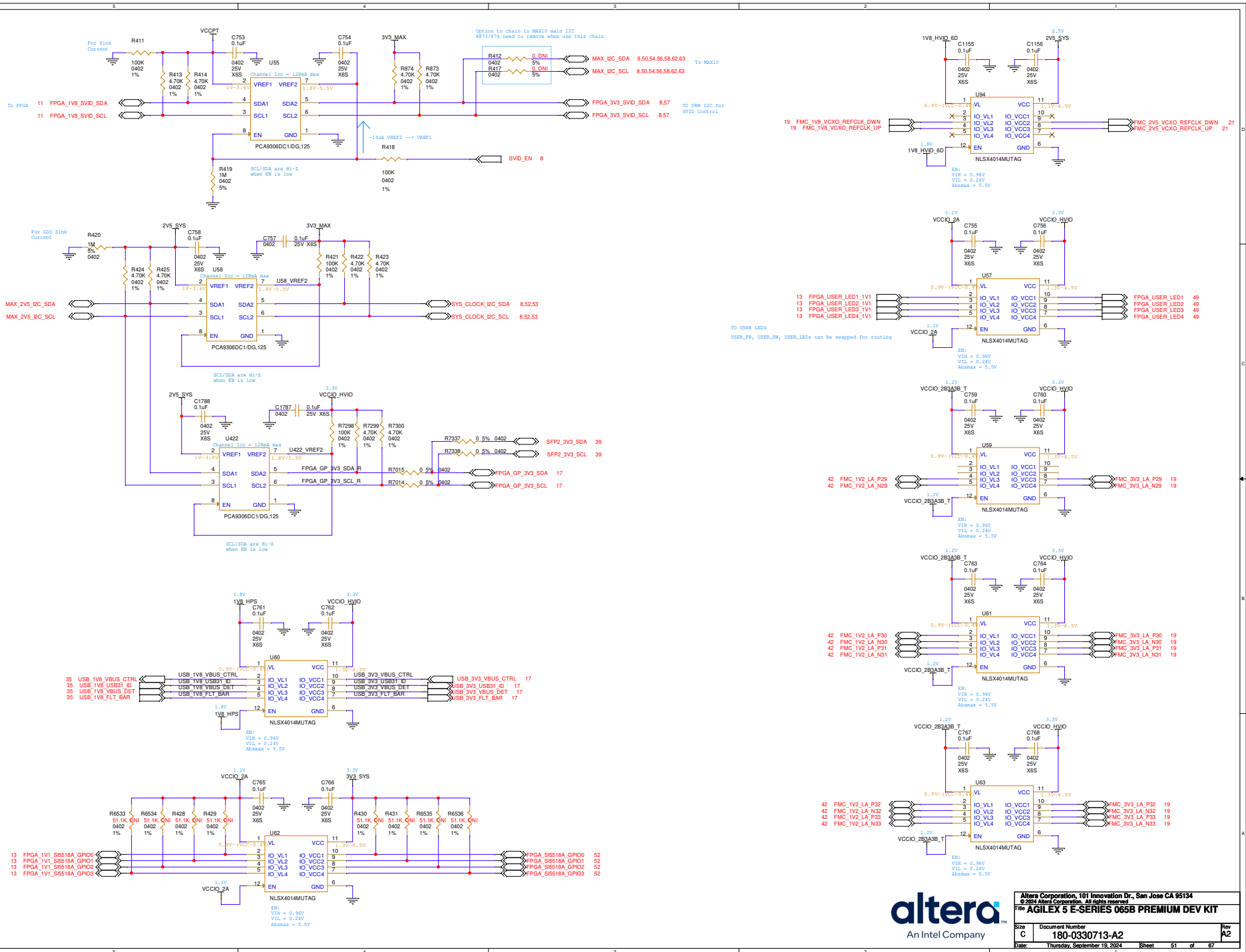


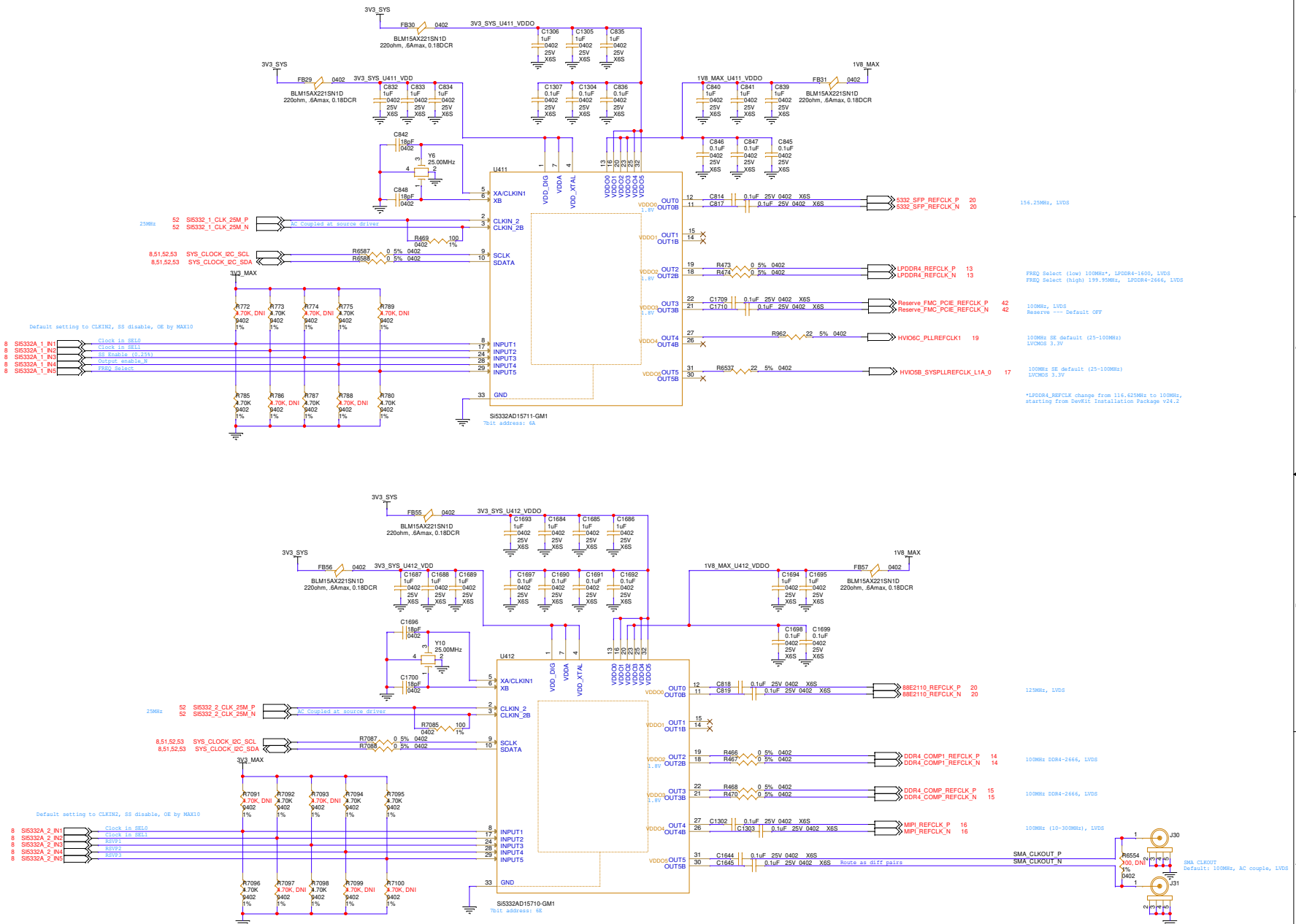


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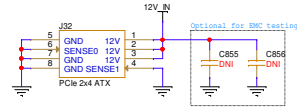


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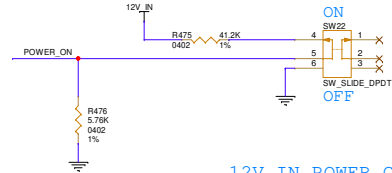




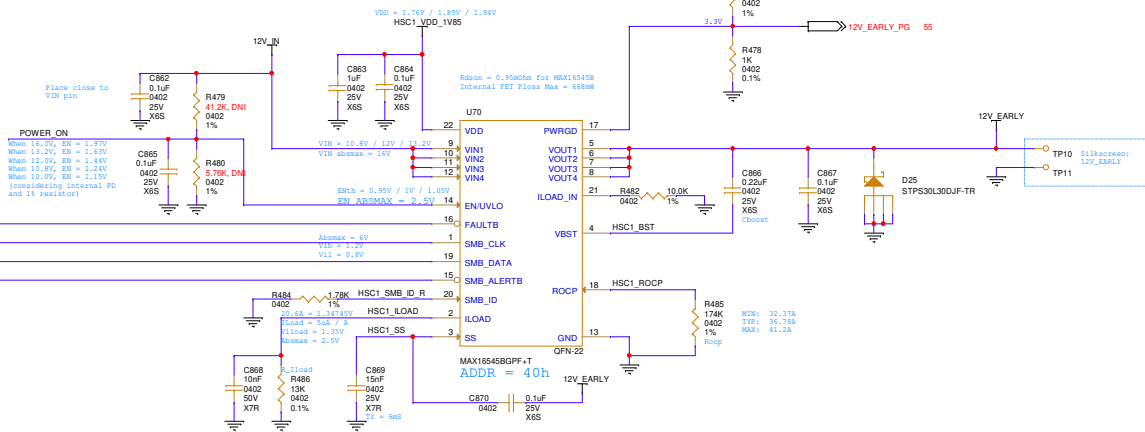
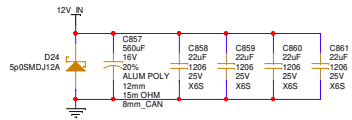
Power On Switch



150W 2x4 ATX AUX
INPUT POWER
CONNECTOR



12V_IN POWER CONDITIONER
(MAX10 POWER DOMAIN)



Pull-ups on PG8

8.50.51.56.58.62.63 MAX_IC_SCL

8.50.51.56.58.62.63 MAX_IC_SDA

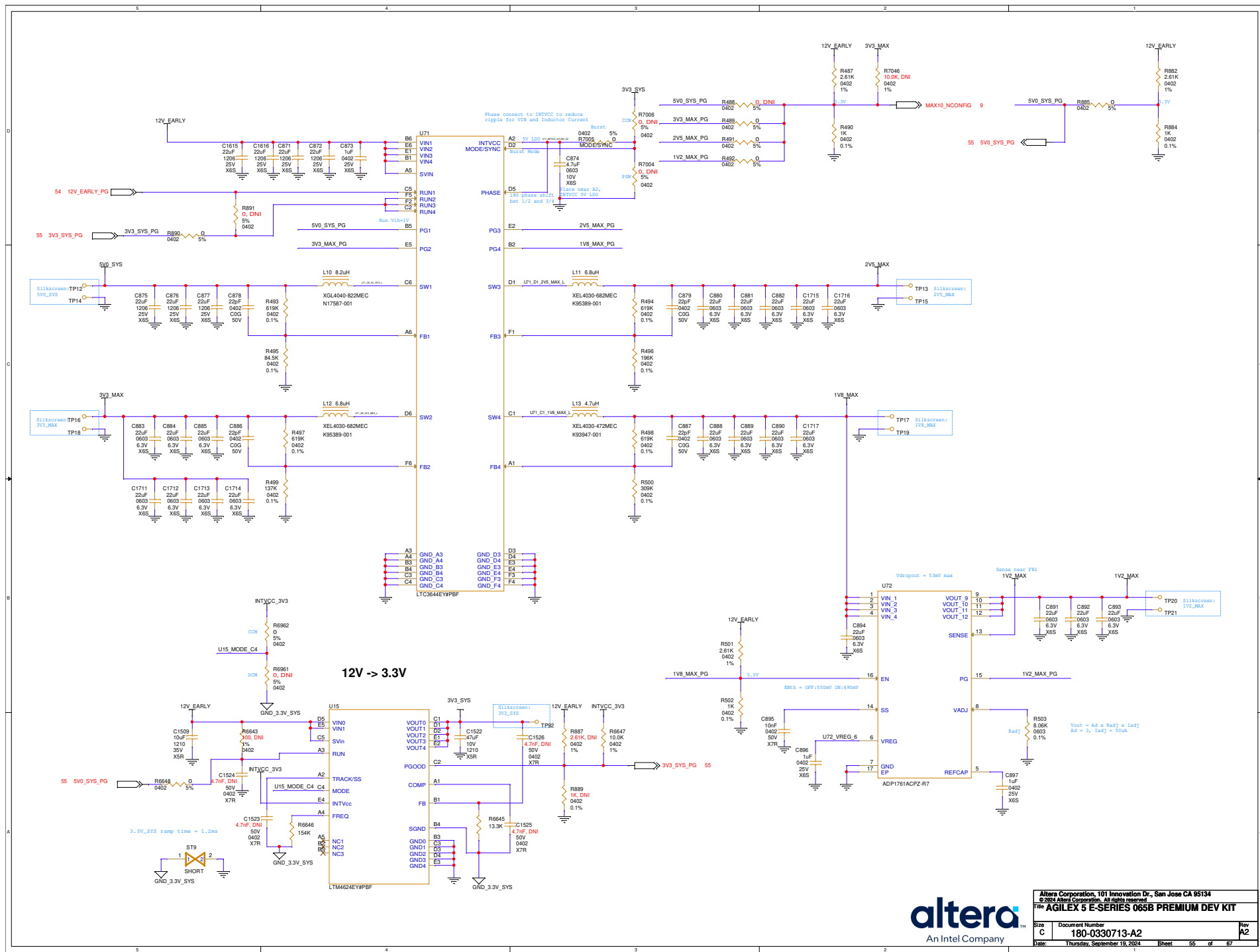
8 HSC1_ALERTN

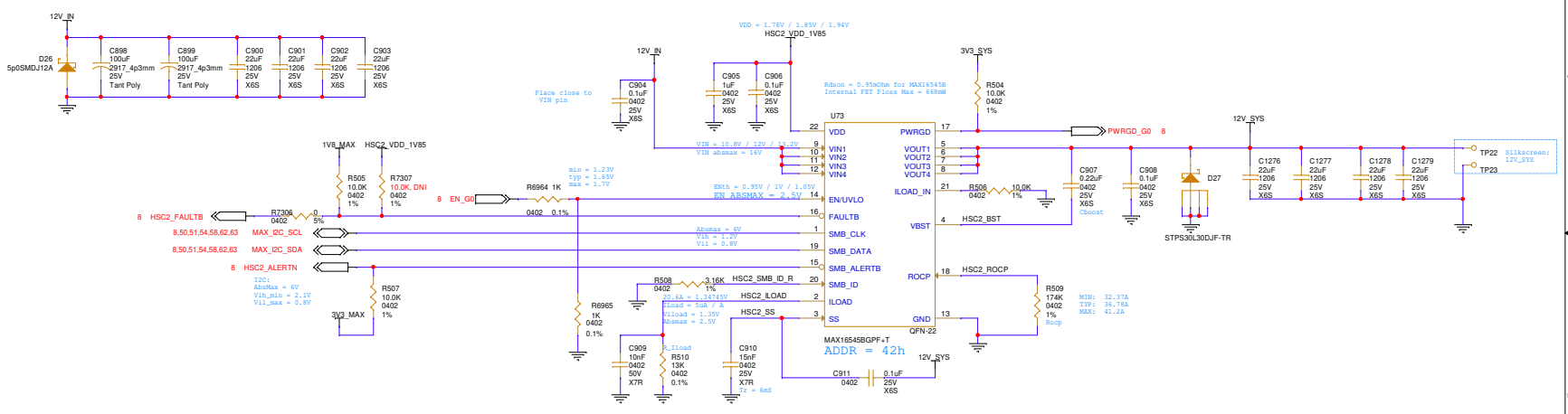
I2C1

Vih_max = 6V

Vih_min = 2.1V

Vil_max = 0.8V

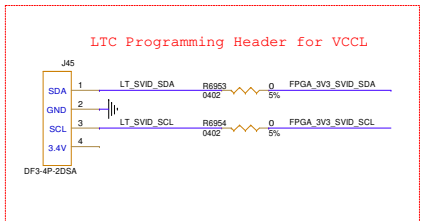
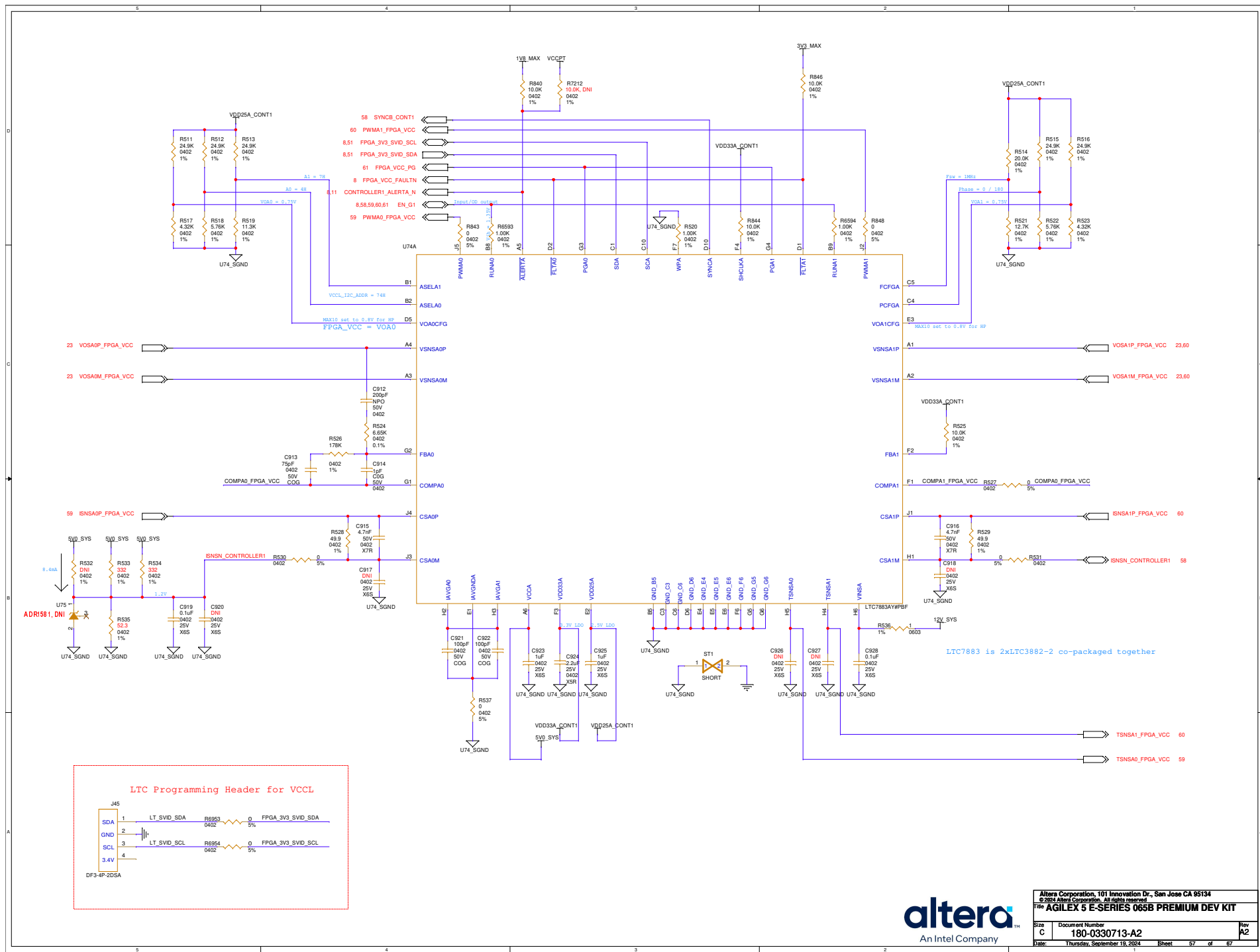




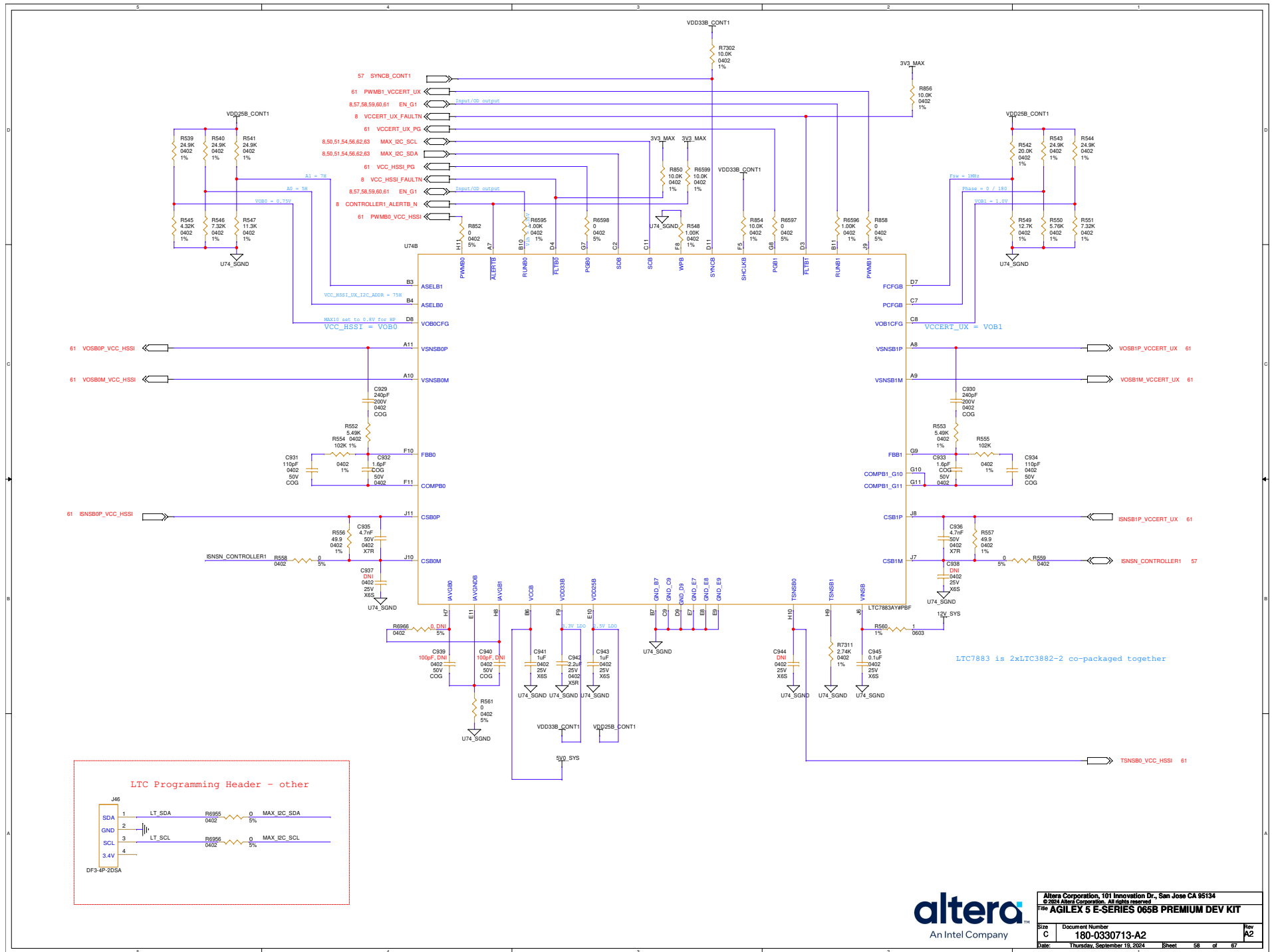
12V_SYS POWER CONDITIONER
(FPGA POWER DOMAIN)

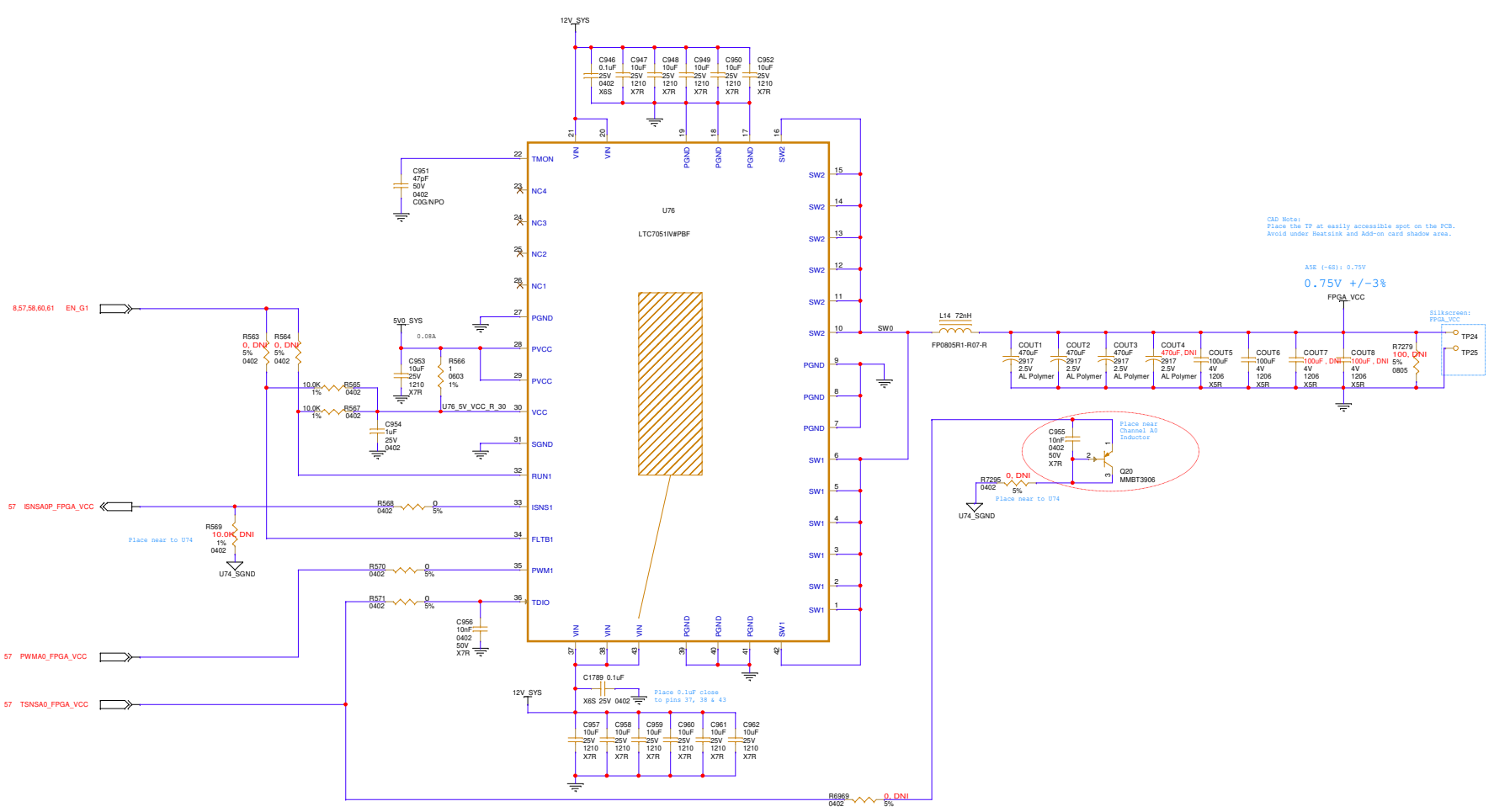


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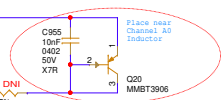




CAD Note:
Place the TP at easily accessible spot on the PCB.
Avoid under Heatstik and Add-on card shadow area.

ASE (-60) 0.75V
0.75V +/-3%

TP25
TP24



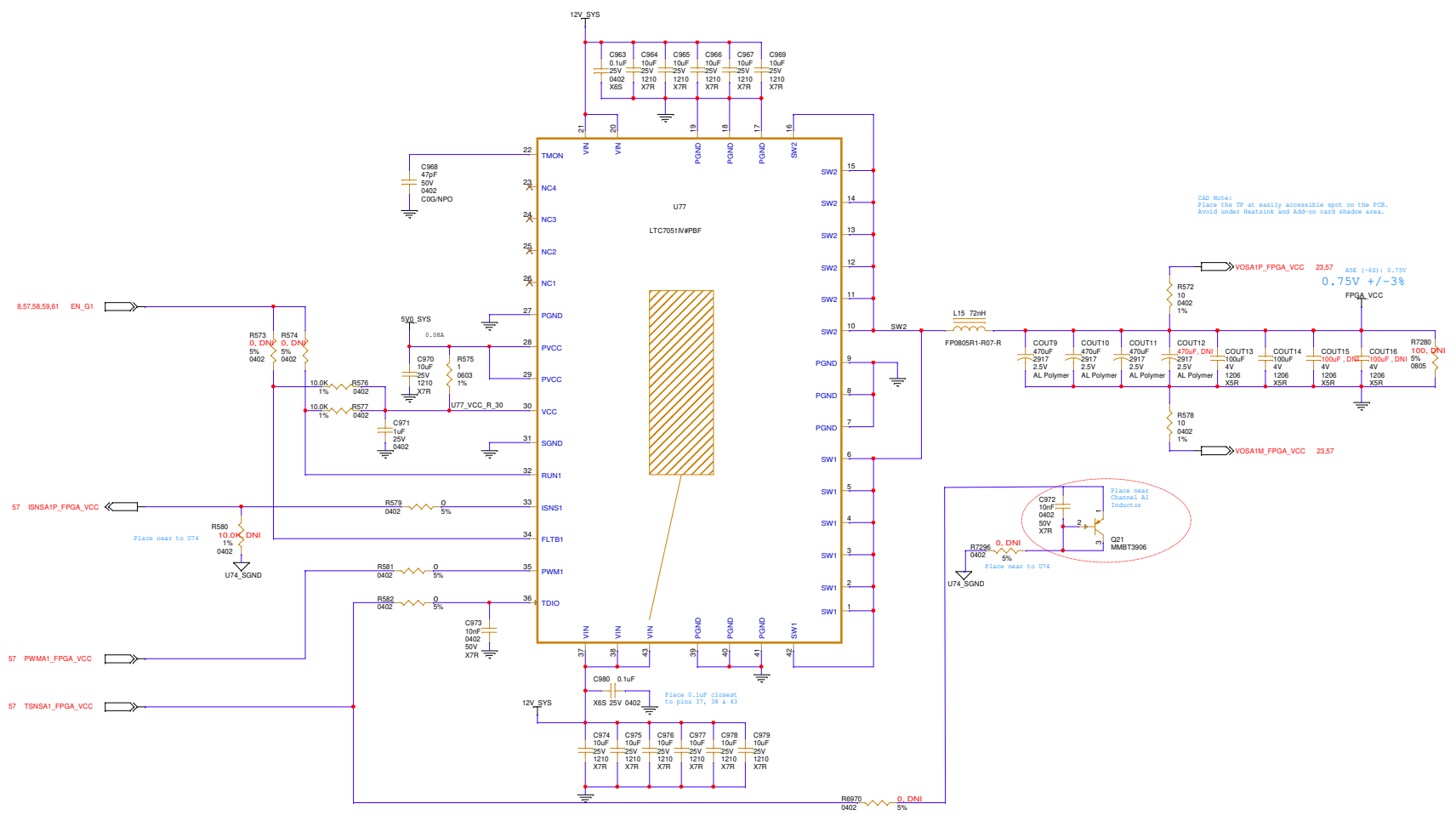
Place near Channel A0 Inductor.

Place near to U74

Place 0.1uF close to pins 37, 38 & 43



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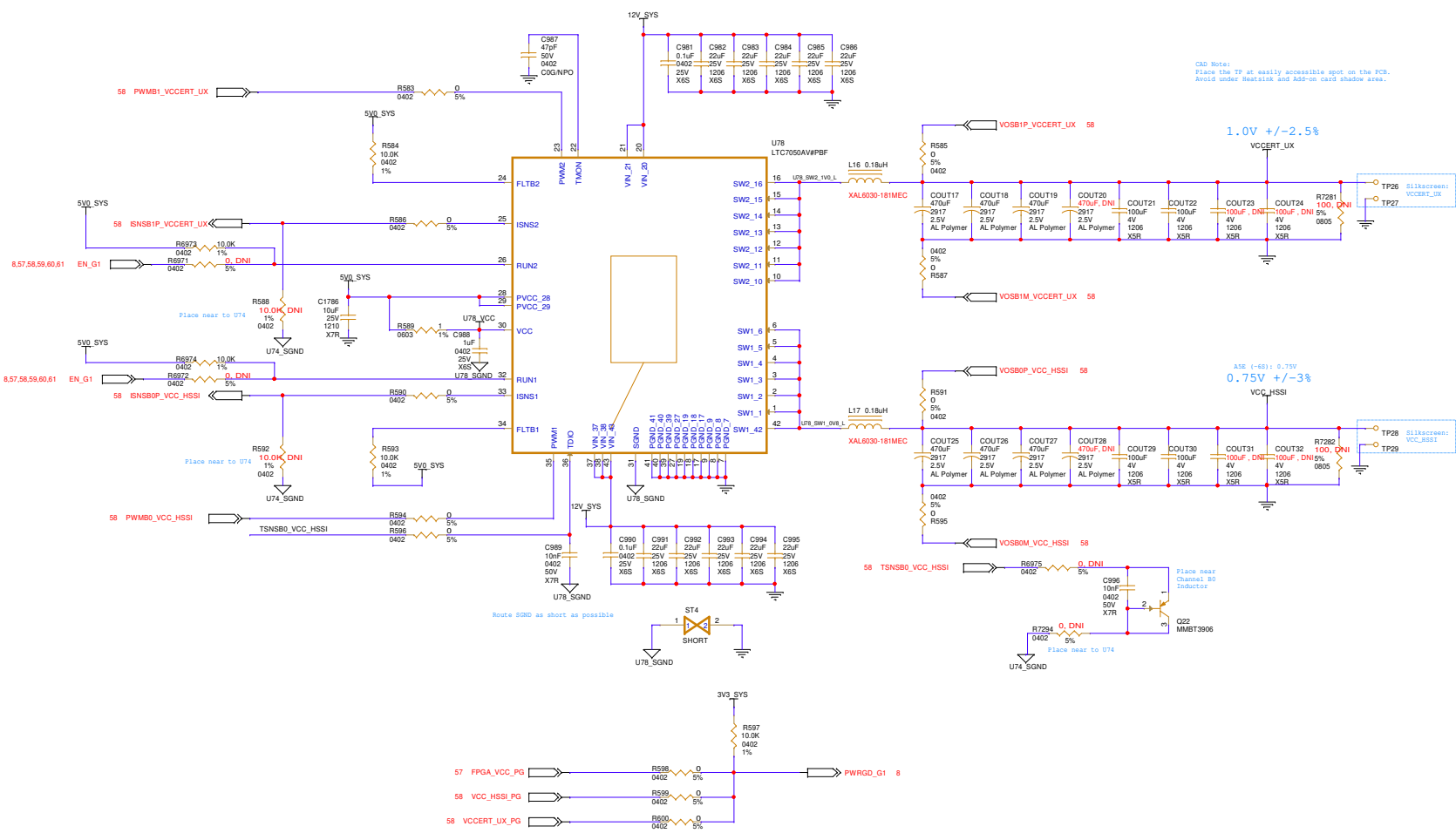


CAD Note:
Place the TP at easily accessible spot on the PCB.
Avoid under heatstink and avoid dark shadow area.

VOSA1P_FPGA_VCC 23.57 $ASR: (+23): 0.75V$
 $0.75V \pm/-3\%$
FPGA_VCC

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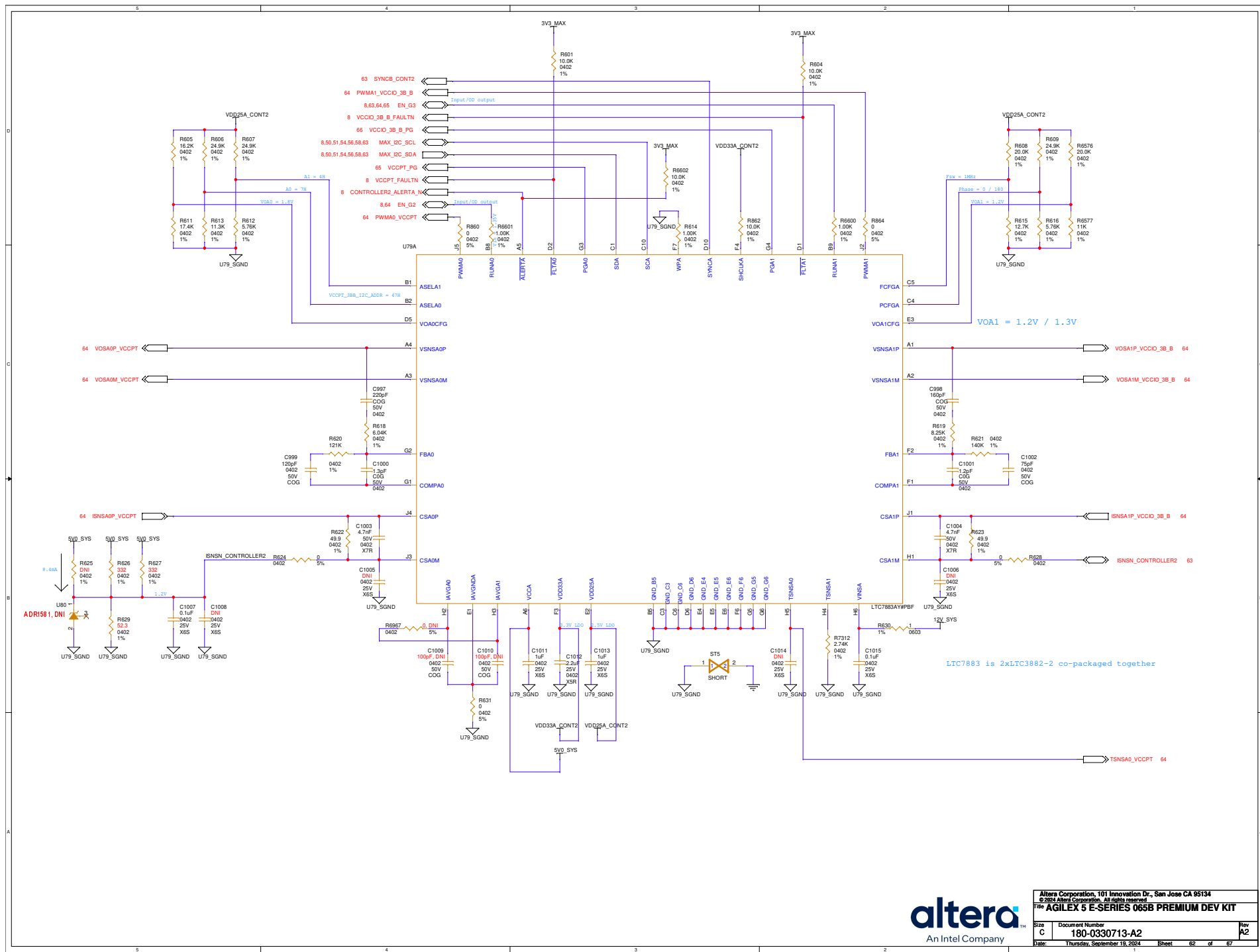
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File: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT		
Size: 0	Document Number: 180-0330713-A2	Rev: A2
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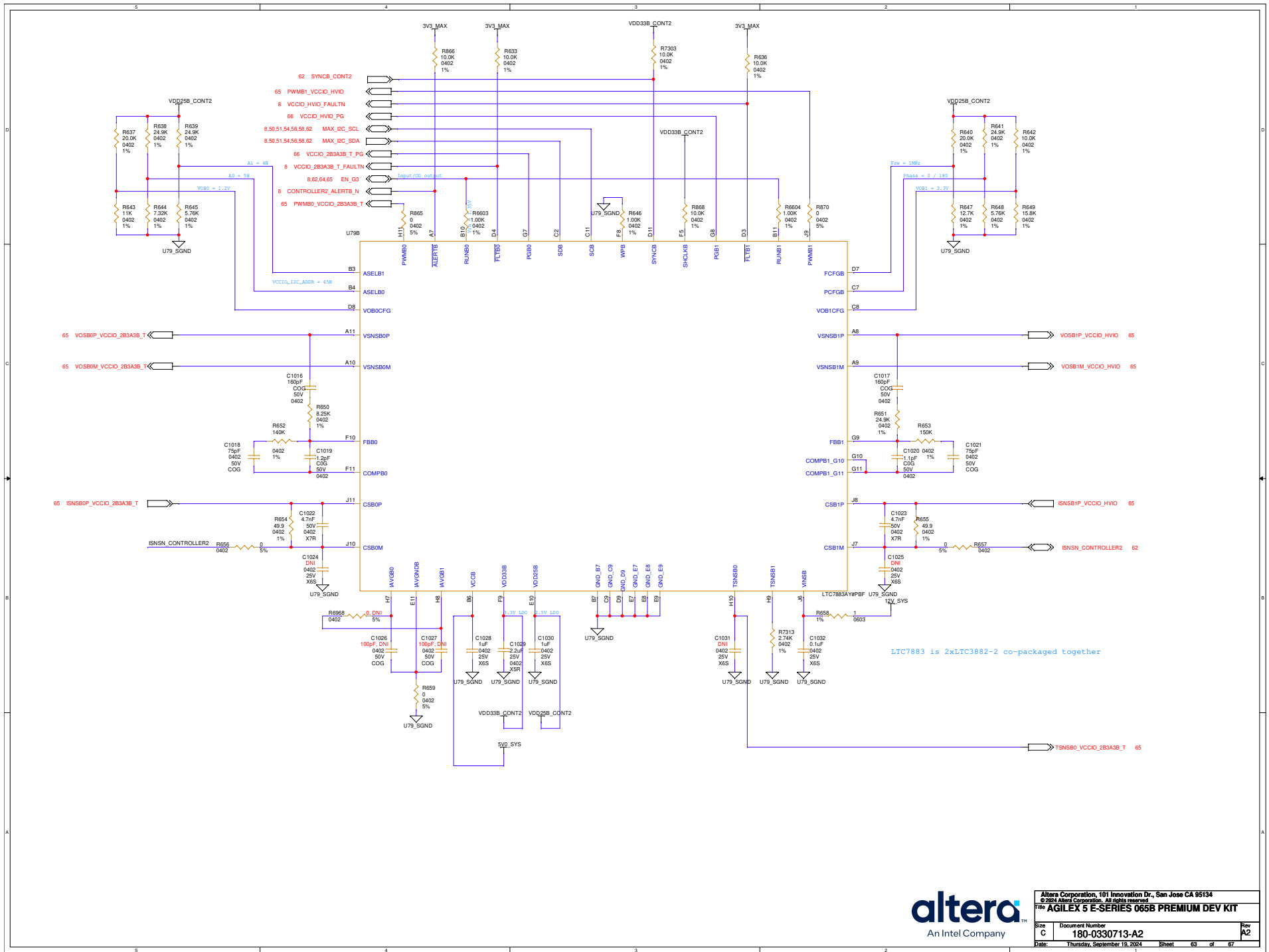
CAD Note:
Place the TP at easily accessible spot on the PCB.
Avoid under Restraint and Add-no card shadow area.

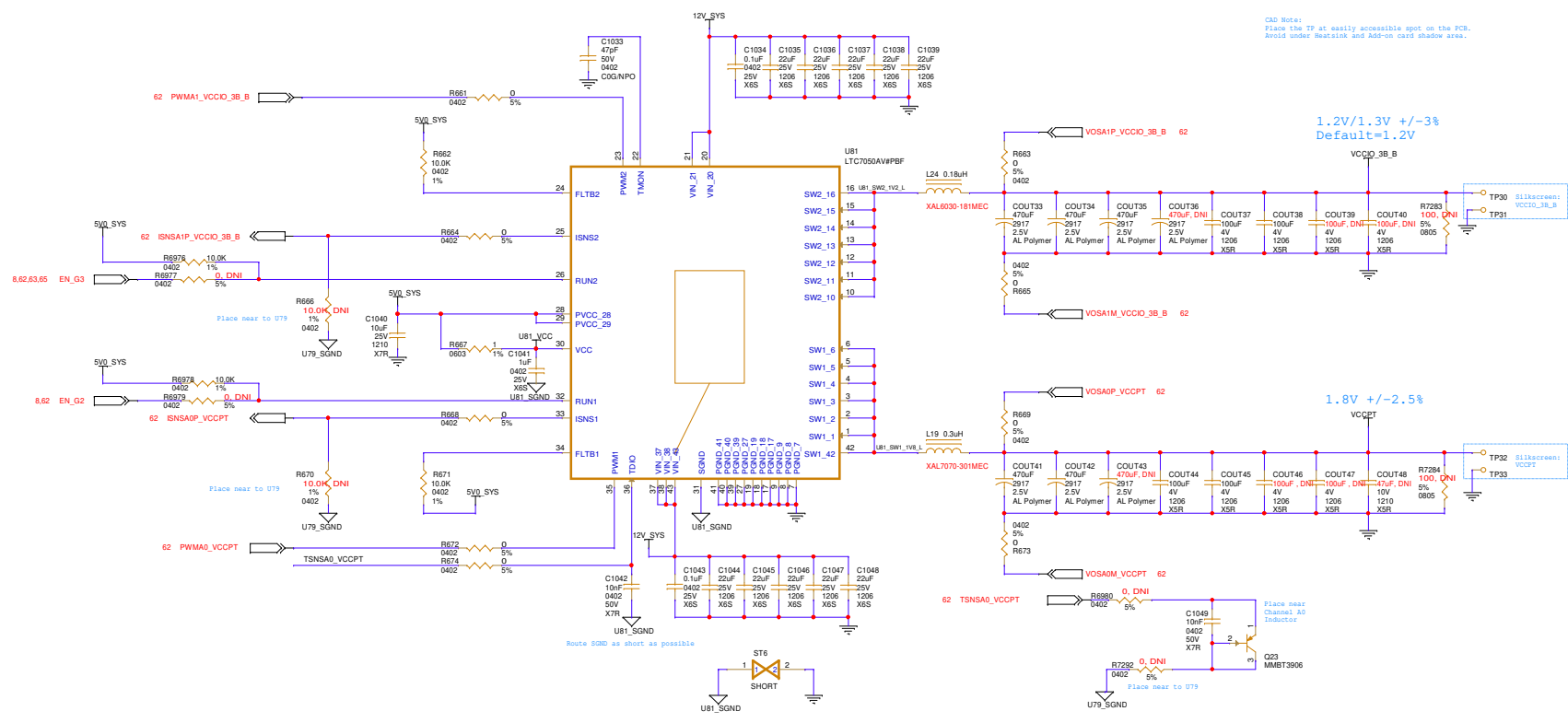


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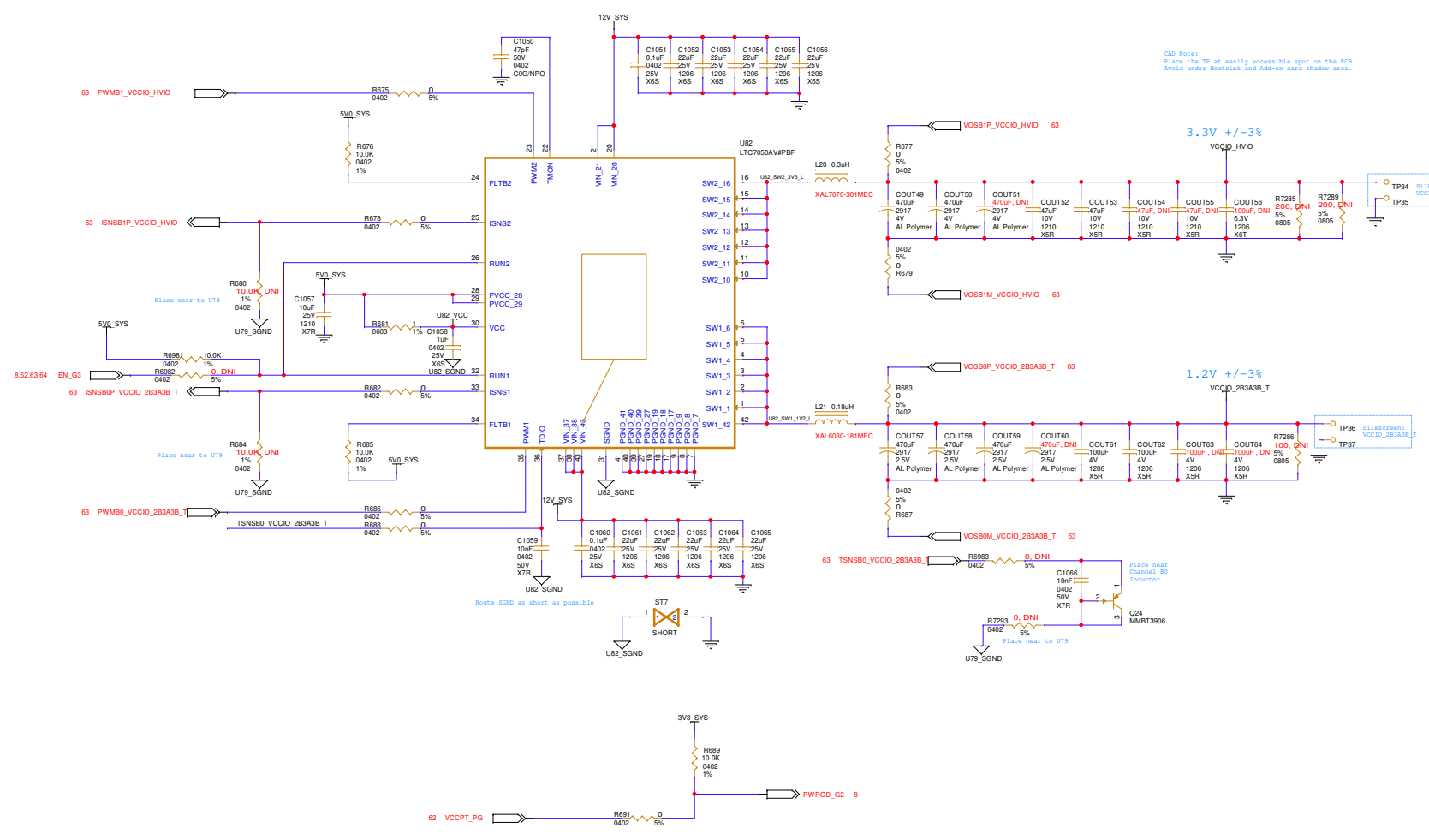




CAD Note:
Place the TP at easily accessible spot on the PCB.
Avoid under Heatsink and Add-on card shadow area.



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Old Note:
Place the TP at easily accessible spot on the PCB.
Avoid under heatlink and Add-on card shadow area.

Place near to U79

Place near to U79

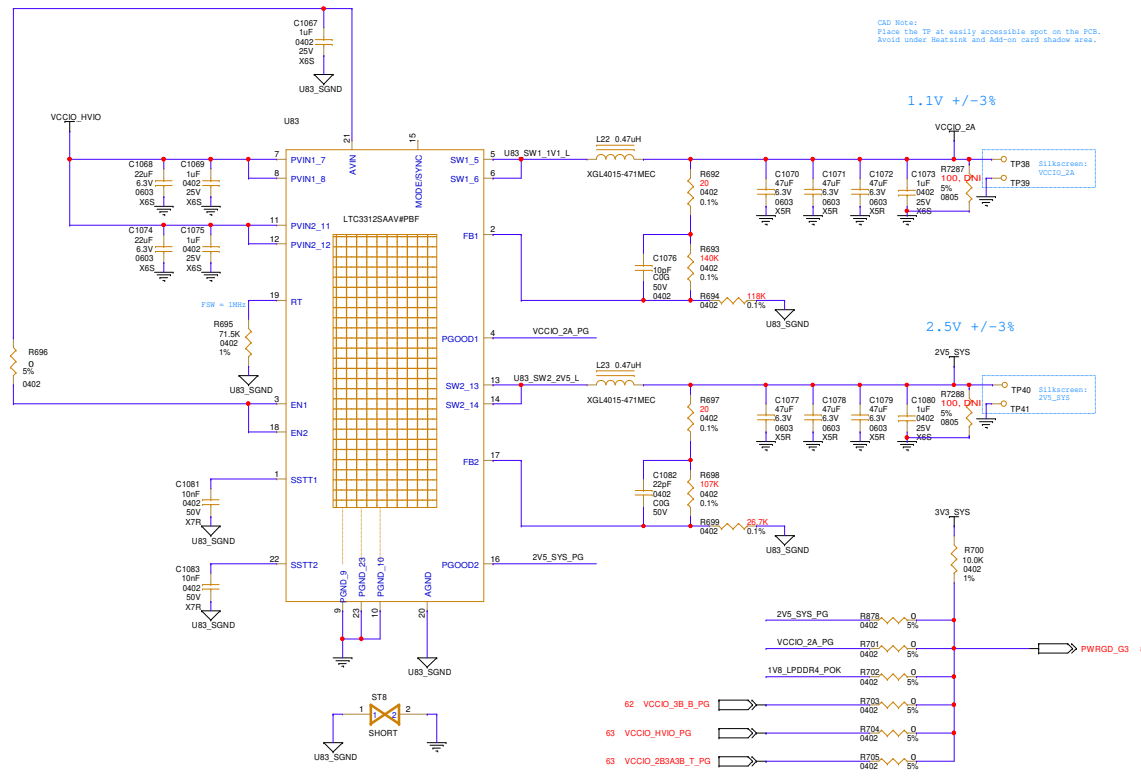
Route S0B0 as short as possible

Place near Chained 50 Inductor

Place near to U79



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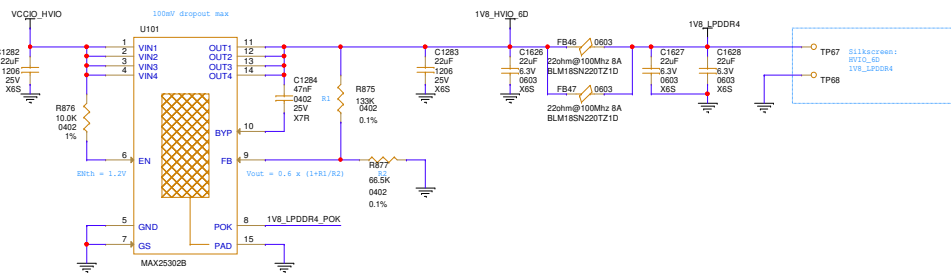


CAD Note:
Place the TP at easily accessible spot on the PCB.
Avoid under heatsink and Add-on card shadow area.

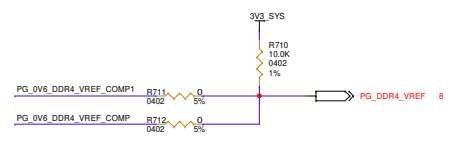
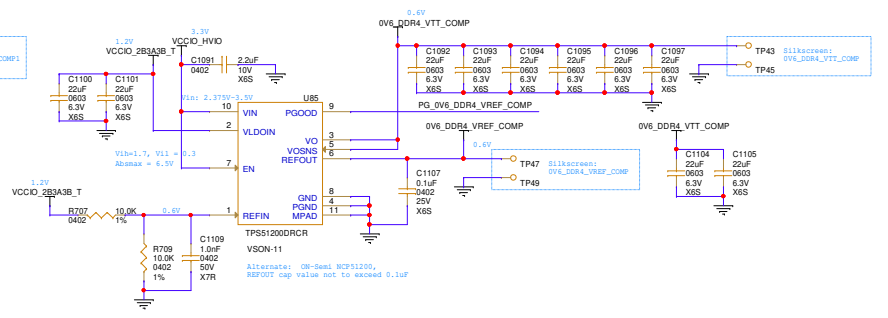
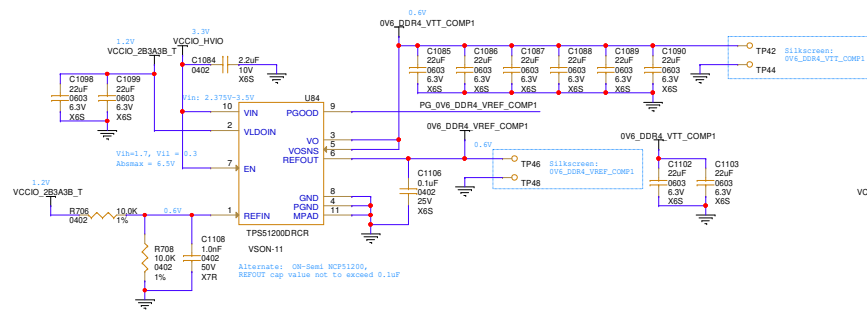
1.1V +/-3%

2.5V +/-3%

1.8V +/-3%



GD Note:
Place the TP at easily accessible spot on the PCB.
Avoid under Resistor and Add-on card shadow area.



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