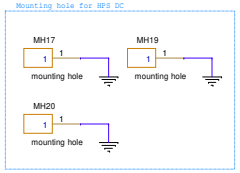
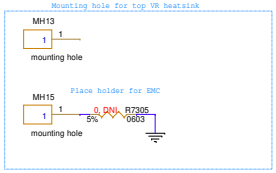
AGILEX™ 5 FPGA E-SERIES 065B PREMIUM DEVELOPMENT KIT

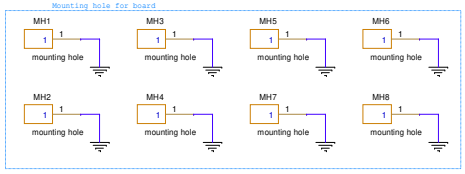
REV	DATE	PAGES	DESCRIPTION
A1	05/30/2024	All	Initial Release
A2	09/23/2024	All	Update to Altera logo, and Altera copy right declaration
B1			

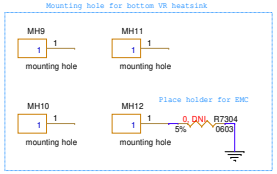
MMID --- 99CA36
Board OPN --- DK- A5E065BB32AES1
TA N20886-002

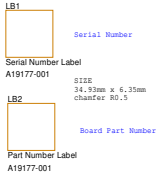
PBA N11816-101
PB N18468-002
PCB MPN 100-0330713-A2











Pin information reference:
A5ED065 ES Device
B32A Version: 2023-07-03

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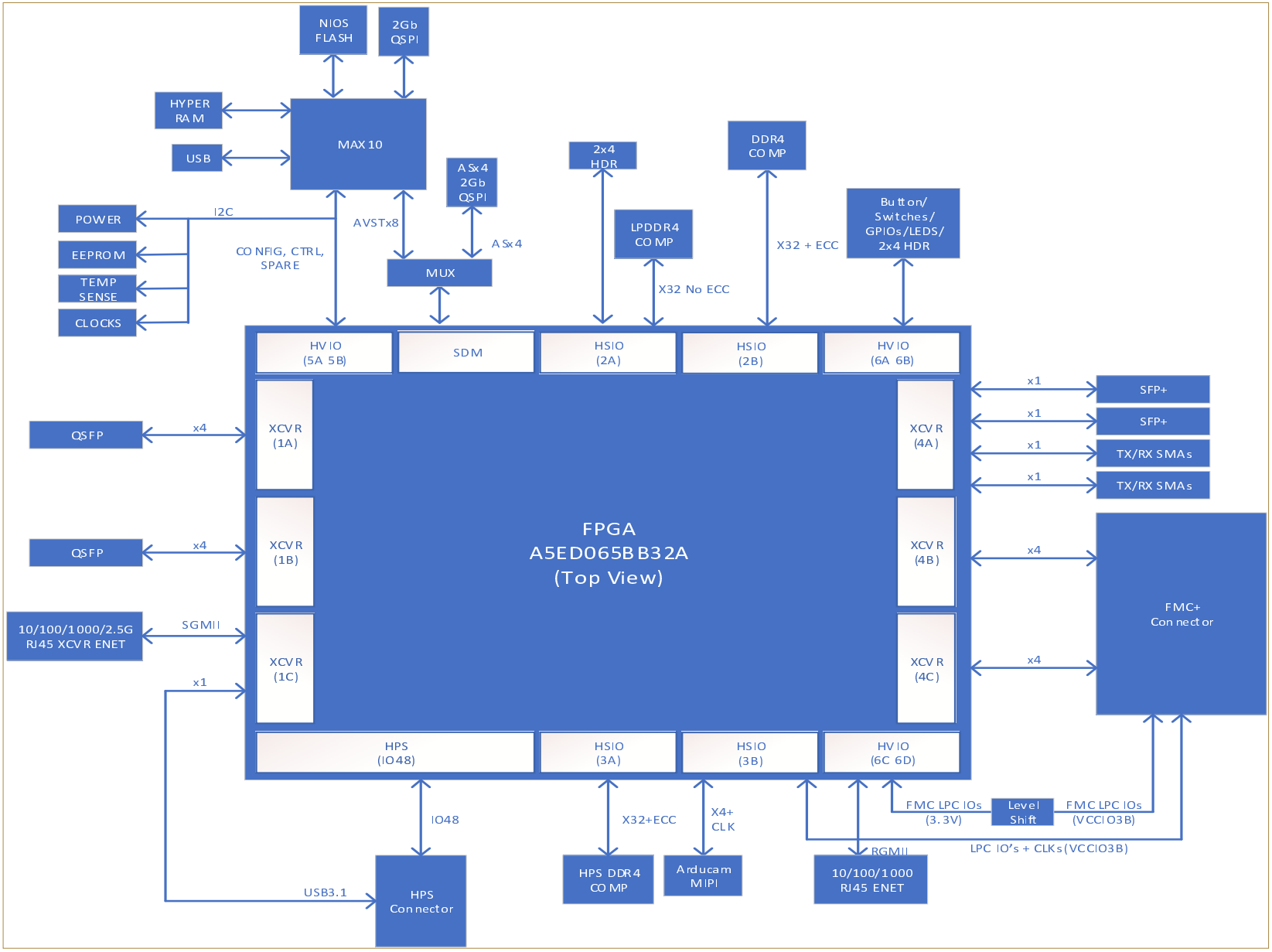
Title	AGILEX 5 E-SERIES 065B PREMIUM DEV KIT	
Size C	Document Number 180-0330713-A2	Rev A2
Date: Monday, September 23, 2024	Sheet 1 of 67	



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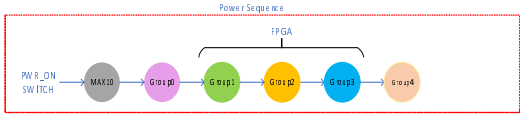
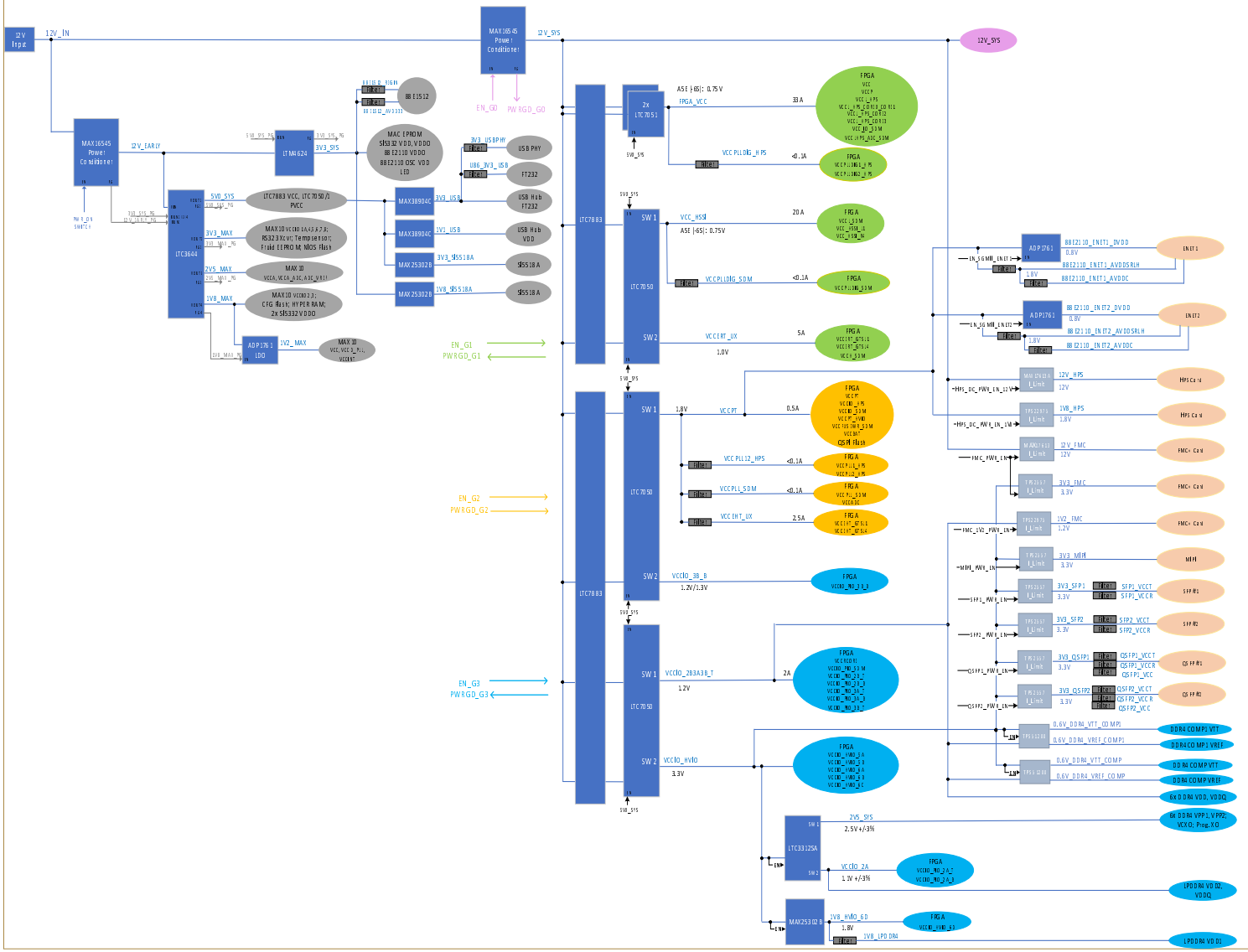
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 2 of 67

Recommendation:
Dev Kit power tree design are for reference.
Recommend customer to scale power solution based on design requirements





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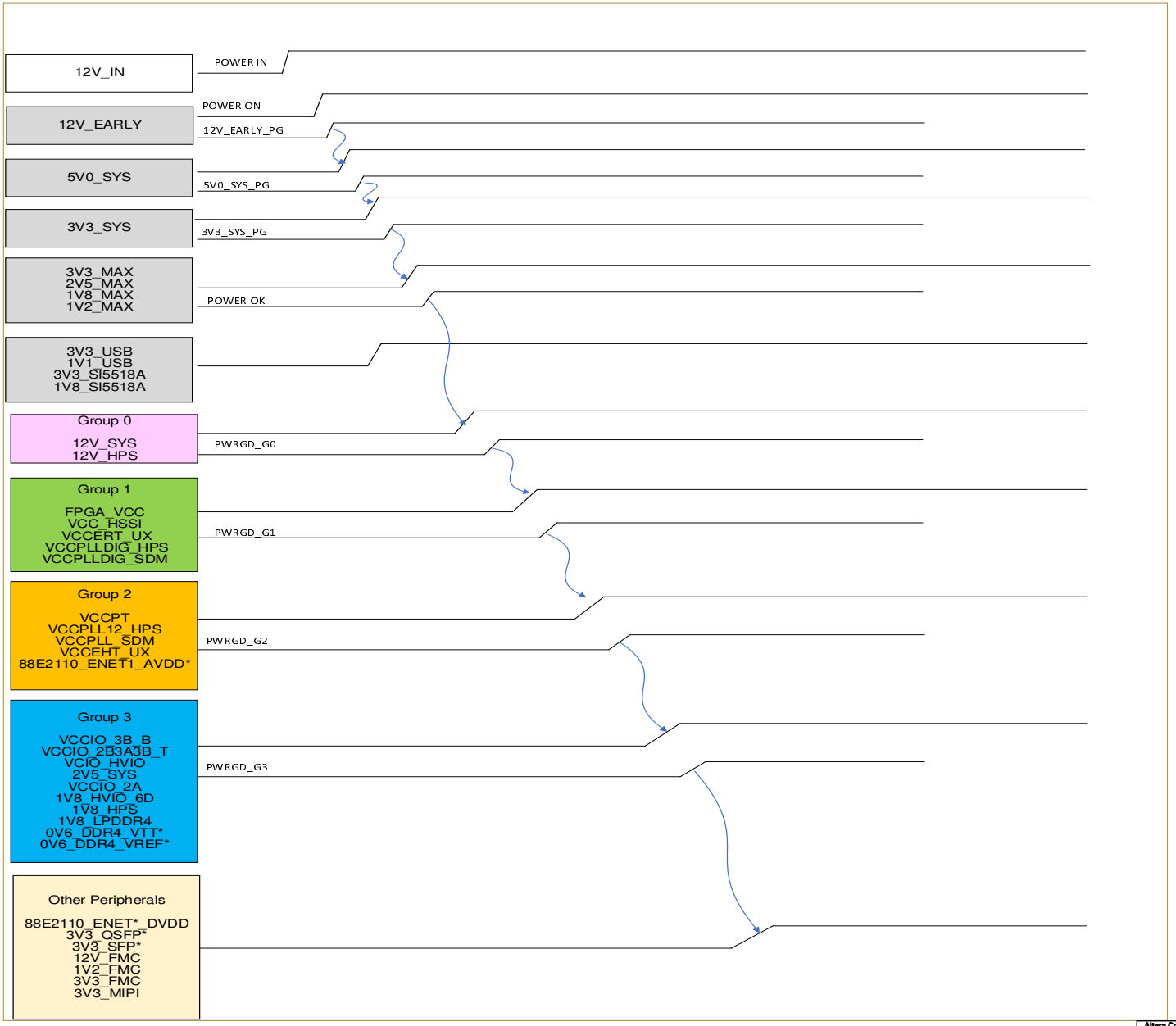
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 3 of 67



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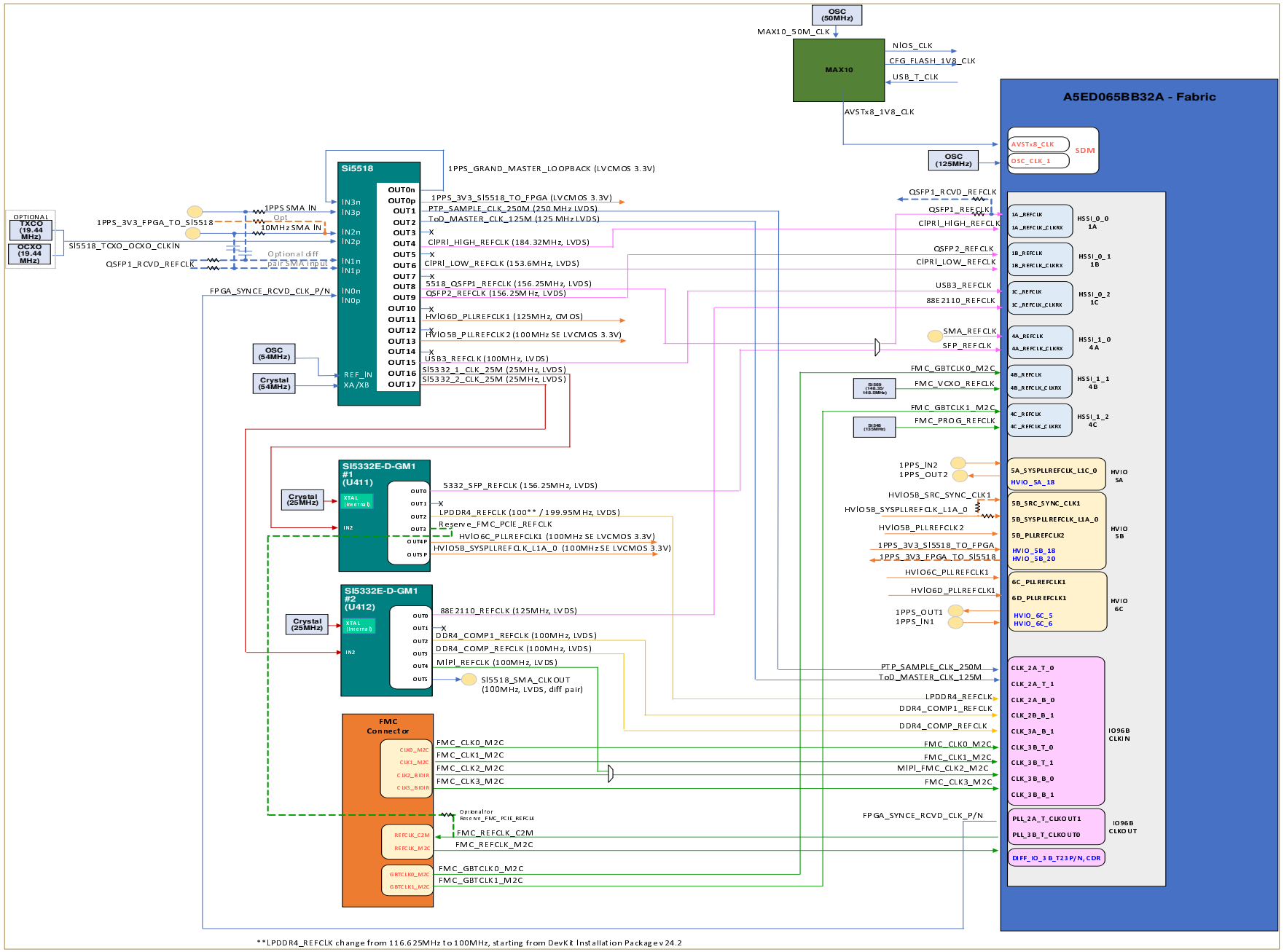
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

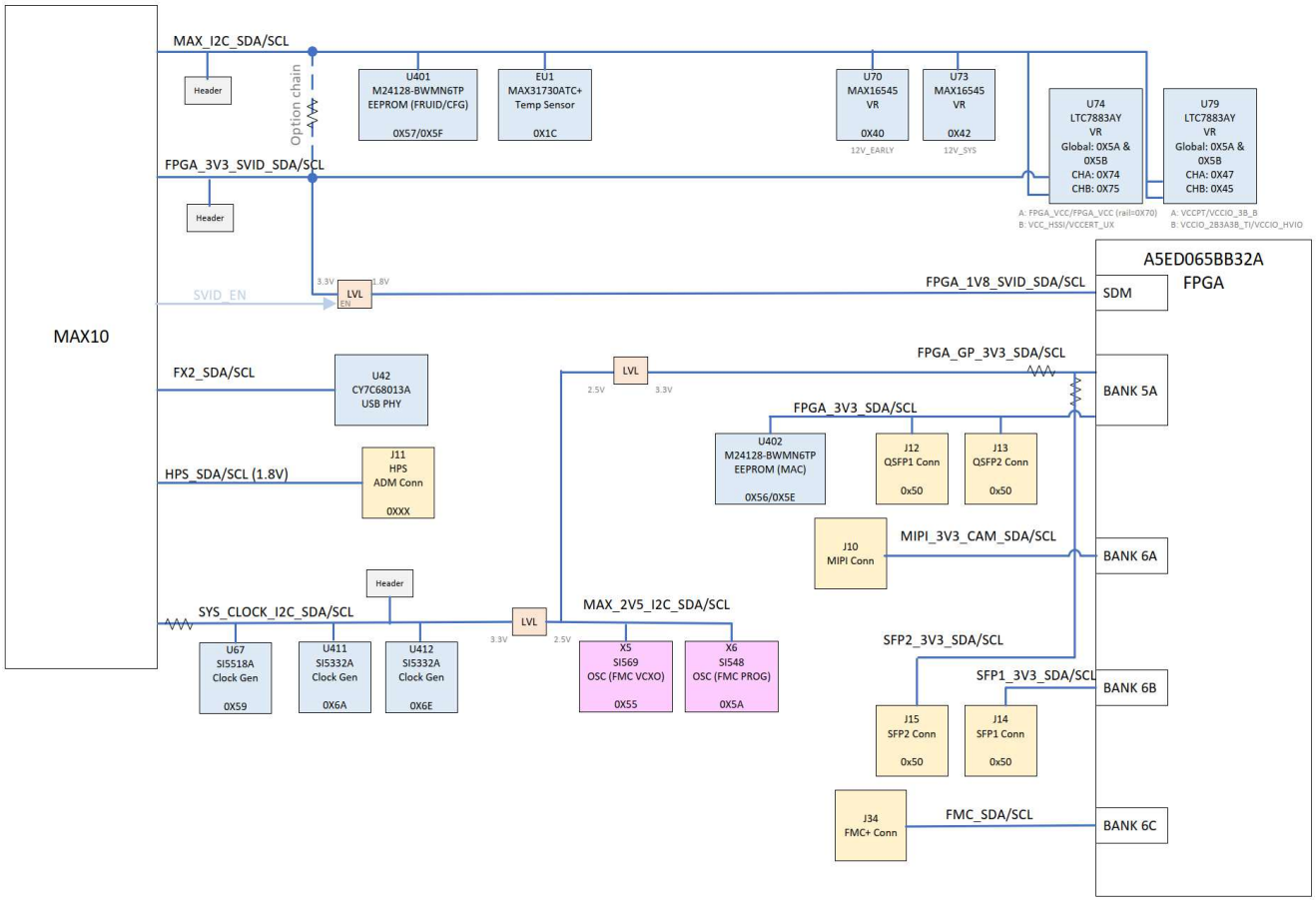
Date: Thursday, September 19, 2024 Sheet 4 of 67



Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 5 of 67



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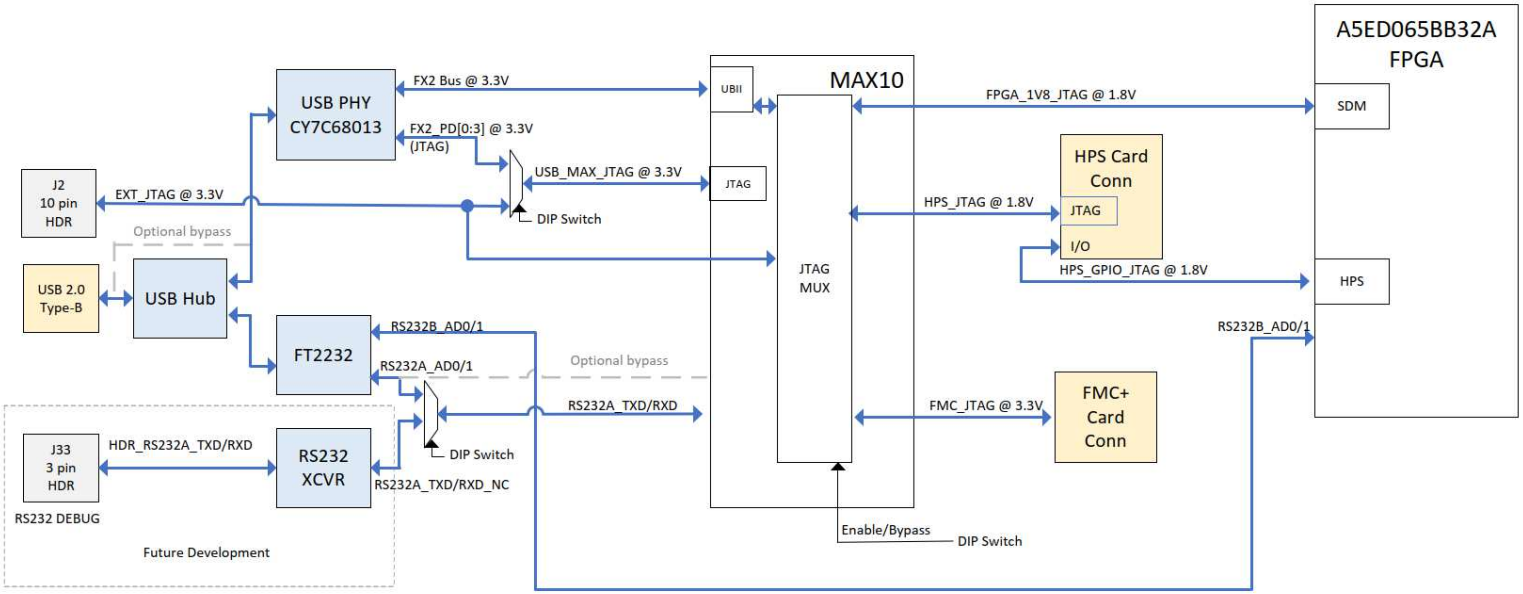
Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 6 of 67



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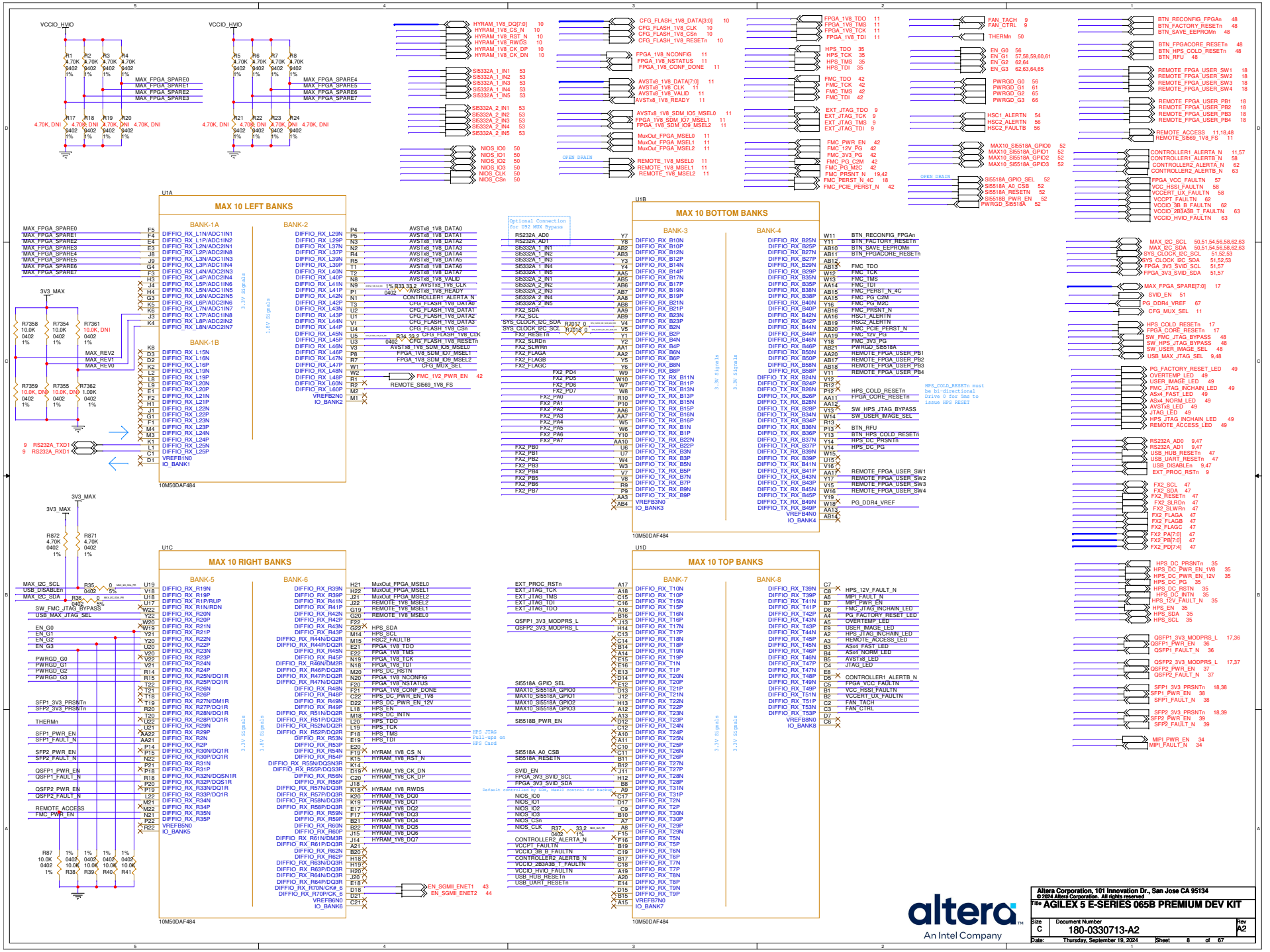
Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 7 of 67


MAX 10 LEFT BANKS
MAX 10 BOTTOM BANKS
MAX 10 RIGHT BANKS
MAX 10 TOP BANKS
BANK-1A
BANK-1B
BANK-2
BANK-3
BANK-4
BANK-5
BANK-6
BANK-7
BANK-8
U1A
U1B
U1C
U1D
10M50DAF484
VCCIO_HVIO
3V3_MAX
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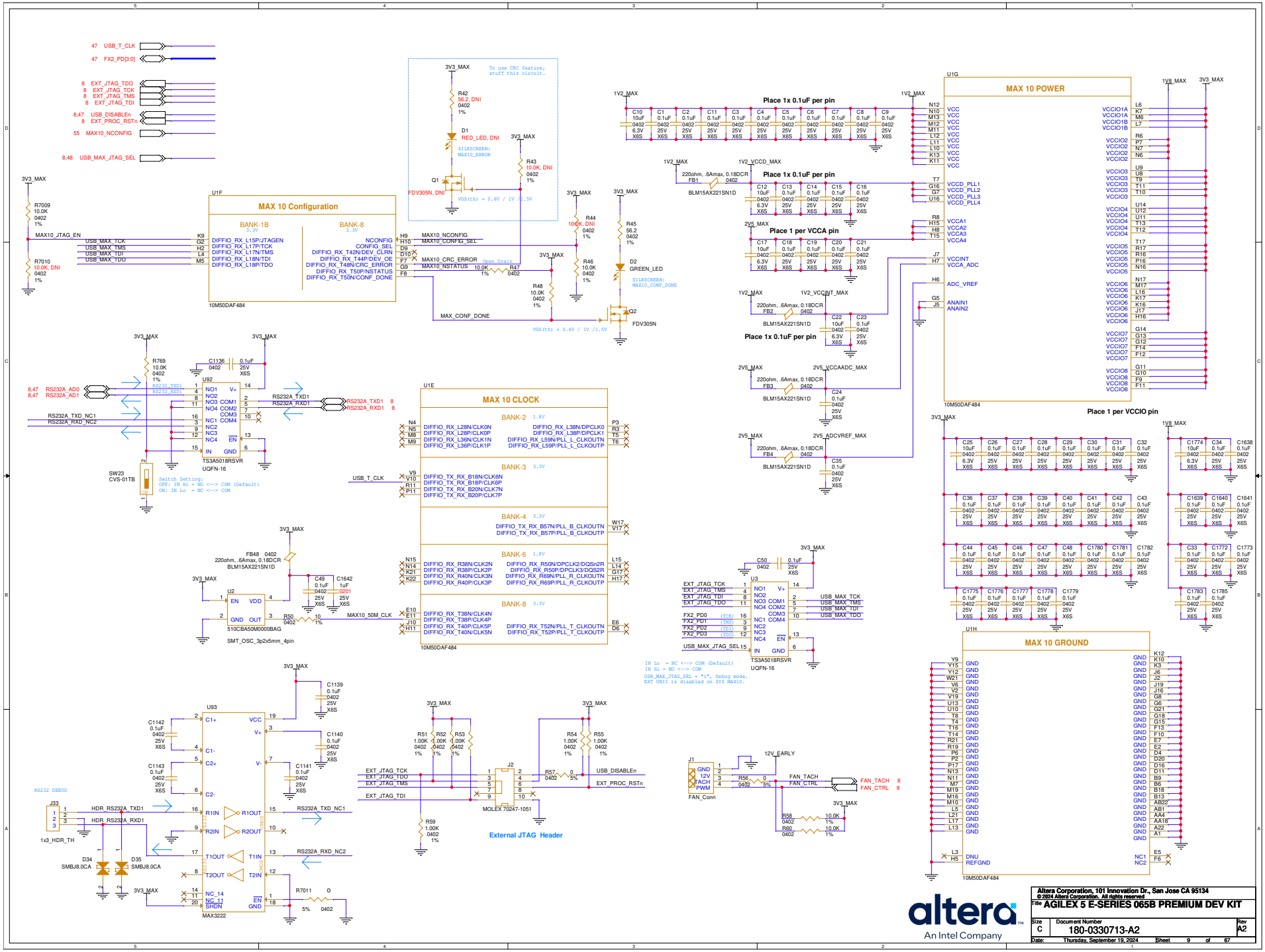
Size C
Document Number 180-0330713-A2
Rev A2
Date: Thursday, September 19, 2024
Sheet 8 of 67


MAX 10 Configuration
MAX 10 CLOCK
MAX 10 POWER
MAX 10 GROUND
External JTAG Header
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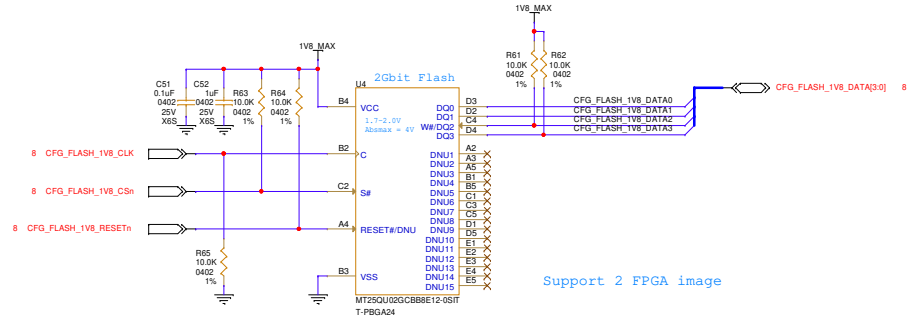
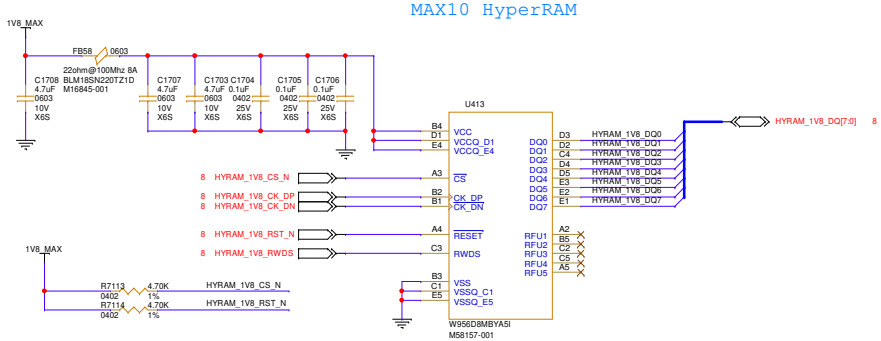
Document Number 180-0330713-A2
Rev A2
Thursday, September 19, 2024
Sheet 9 of 67

AVST CFG Flash



Support 2 FPGA image

MAX10 HyperRAM



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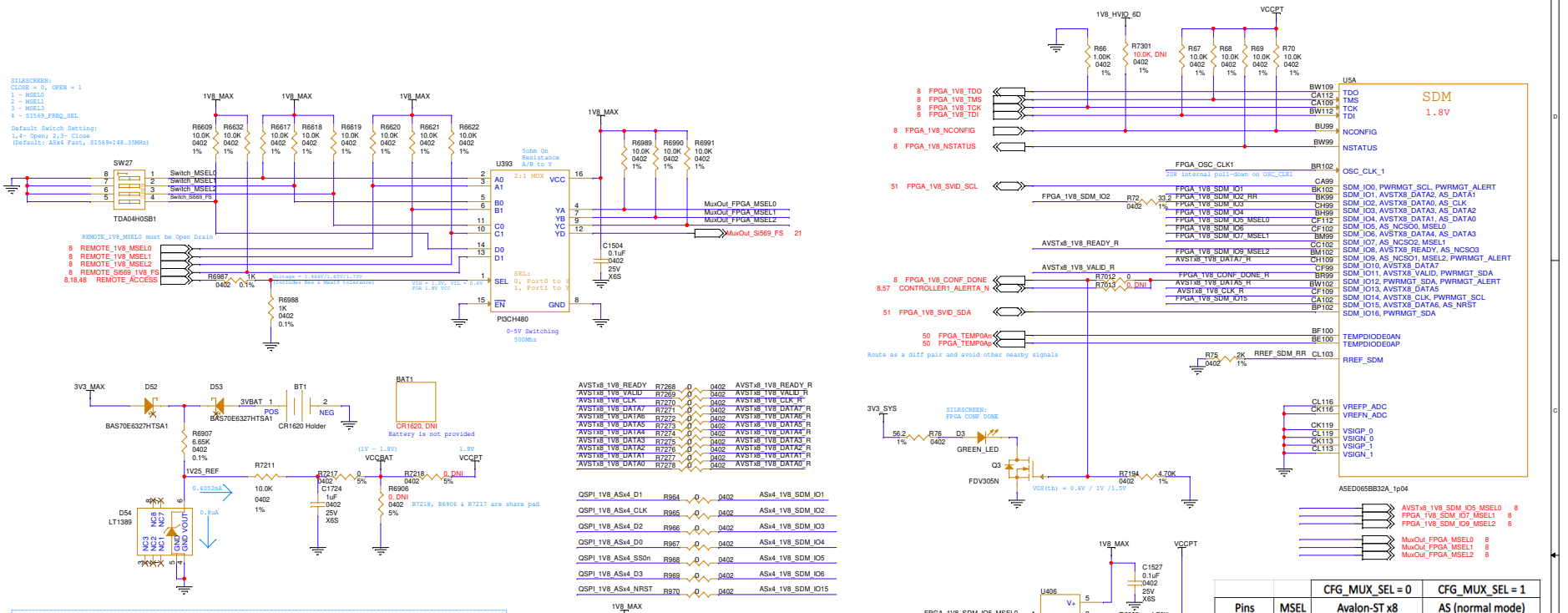
Title	AGILEX 5 E-SERIES 065B PREMIUM DEV KIT
Size: C	Document Number: 180-0330713-A2
Rev: A2	
Date: Thursday, September 19, 2024	Sheet 10 of 67

SDM CONFIGURATION



		CFG_MUX_SEL = 0	CFG_MUX_SEL = 1
Pins	MSEL	Avalon-ST x8	AS (normal mode)
SDM_IO0		PWR_SCL	PWR_SCL
SDM_IO1		AVSTx8_DATA2	AS_DATA1
SDM_IO2		AVSTx8_DATA0	AS_CLK
SDM_IO3		AVSTx8_DATA3	AS_DATA2
SDM_IO4		AVSTx8_DATA1	AS_DATA0
SDM_IO5	MSEL0		AS_nCSO0
SDM_IO6		AVSTx8_DATA4	AS_DATA3
SDM_IO7	MSEL1	HPS_COLD_nRESET	AS_nCSO2
SDM_IO8		AVST_READY	AS_nCSO3
SDM_IO9	MSEL2		AS_nCSO1
SDM_IO10		AVSTx8_DATA7	
SDM_IO11		AVSTx8_VALID	HPS_COLD_nRESET
SDM_IO12		CONF_DONE	CONF_DONE
SDM_IO13		AVSTx8_DATA5	
SDM_IO14		AVSTx8_CLK	
SDM_IO15		AVSTx8_DATA6	AS_nRST
SDM_IO16		PWR_SDA	PWR_SDA

CONFIG MODE	MSEL2	MSEL1	MSEL0
ASx4 FAST Default	0	0	1
ASx4 NORM	0	1	1
AVSTx8	1	1	0
JTAG	1	1	1

Note: MSEL0 is shared with QSPI_CSn which has a pull-up. MAX10 should make MSEL0 Open Drain.

Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size: C | Document Number: 180-0330713-A2 | Rev: A2

Date: Thursday, September 19, 2024 | Sheet 11 of 67

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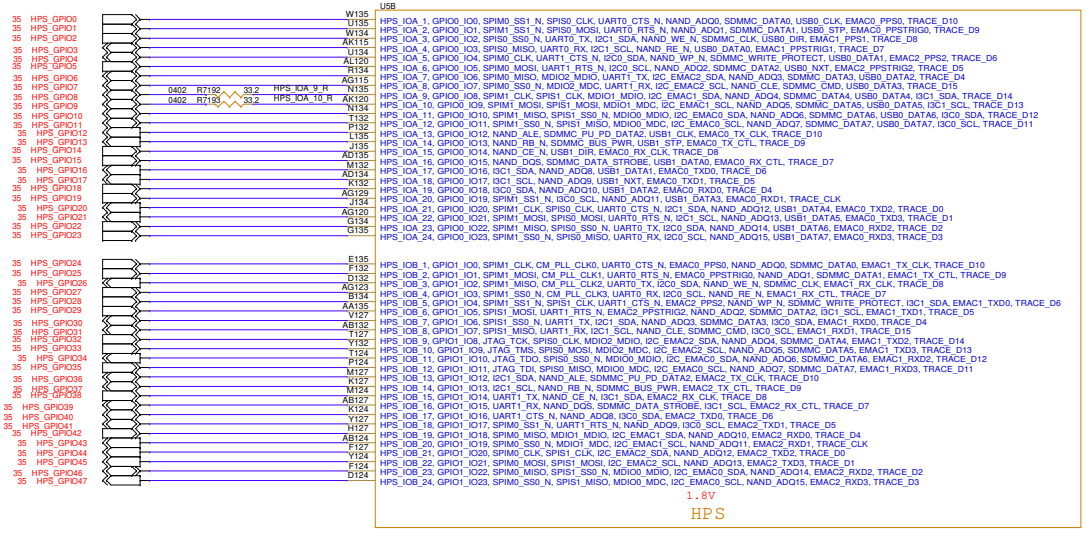
HPS BANK IO48



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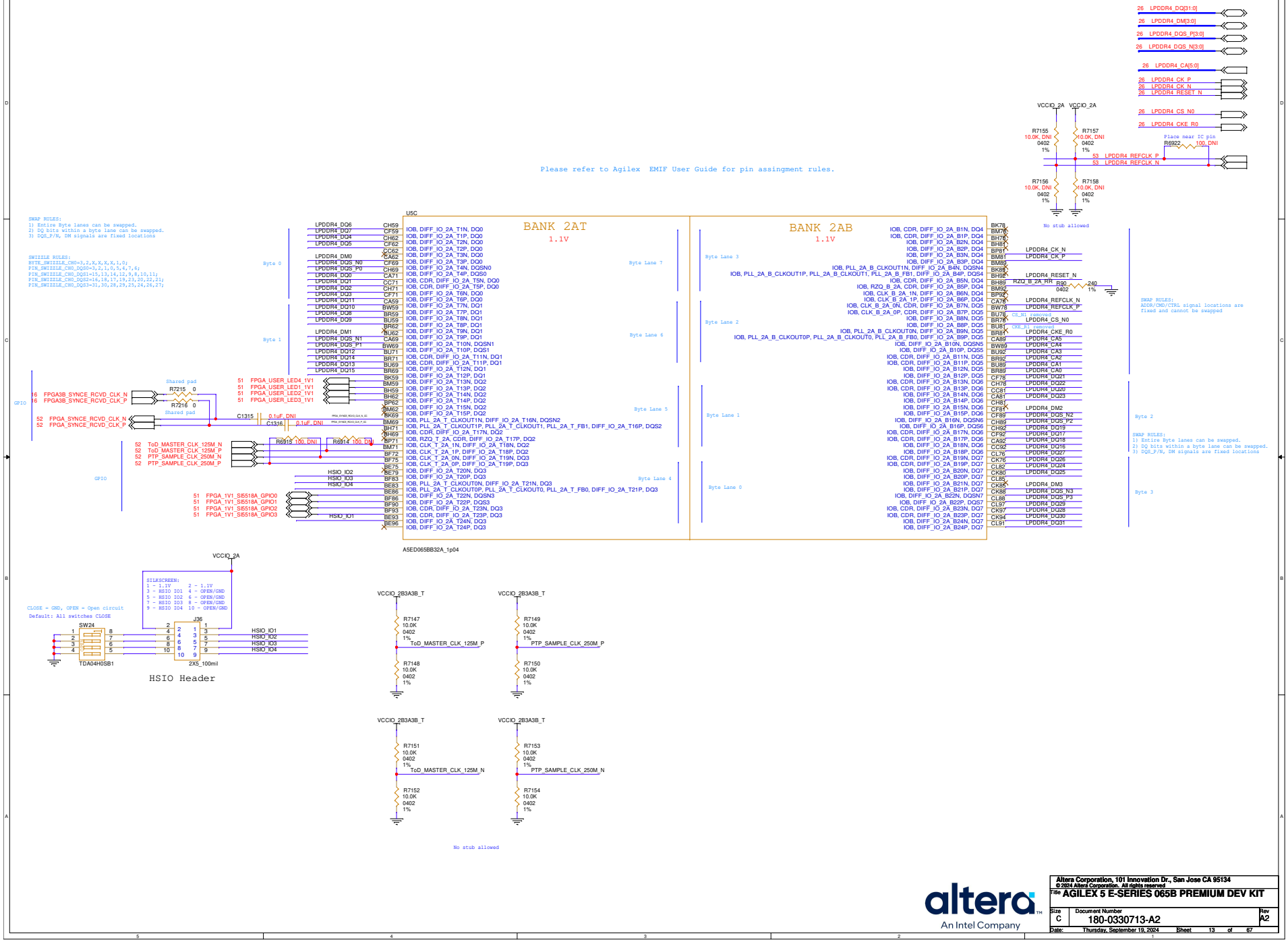
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 12 of 67

HSIO BANKS 2AL AND 2AR

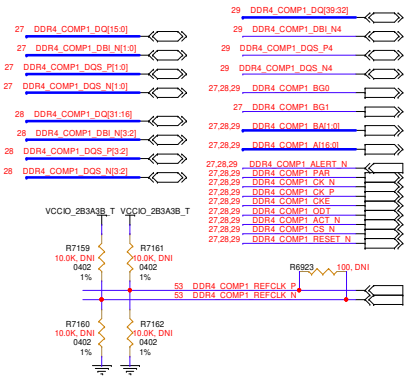


Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

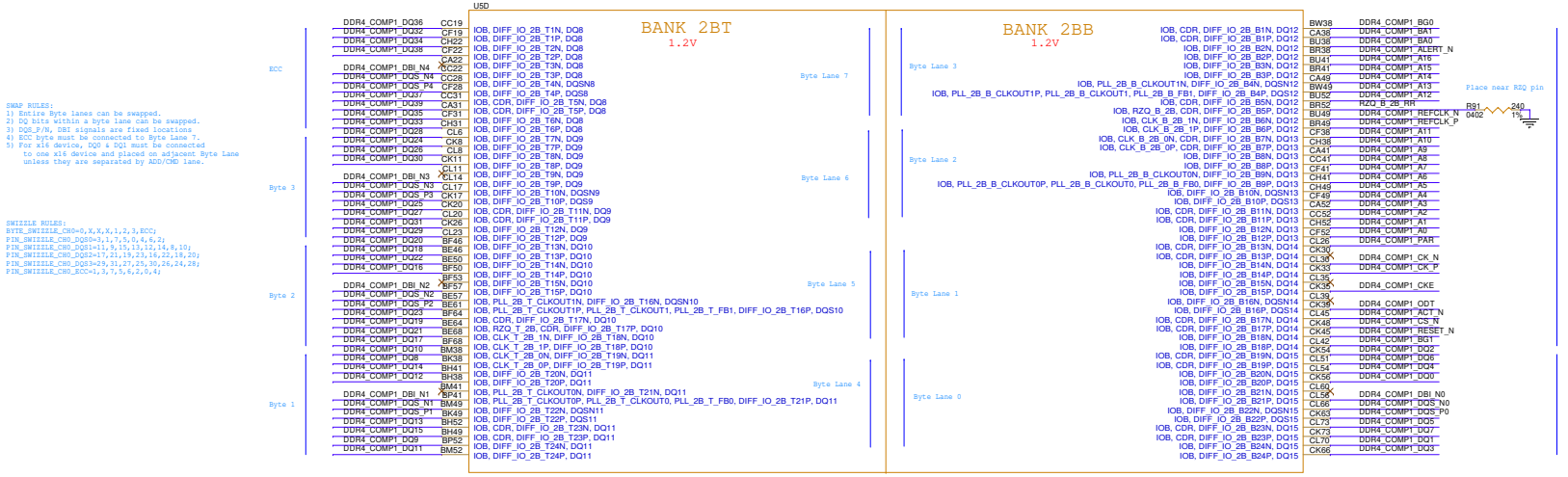
Date: Thursday, September 19, 2024 Sheet 13 of 67

HSIO BANKS 2BL AND 2BR



Please refer to Agilex EMIF User Guide for pin assignment rules.

U5D



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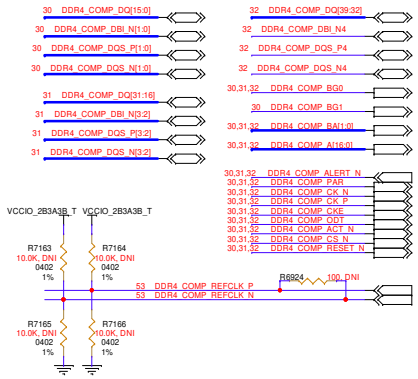
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

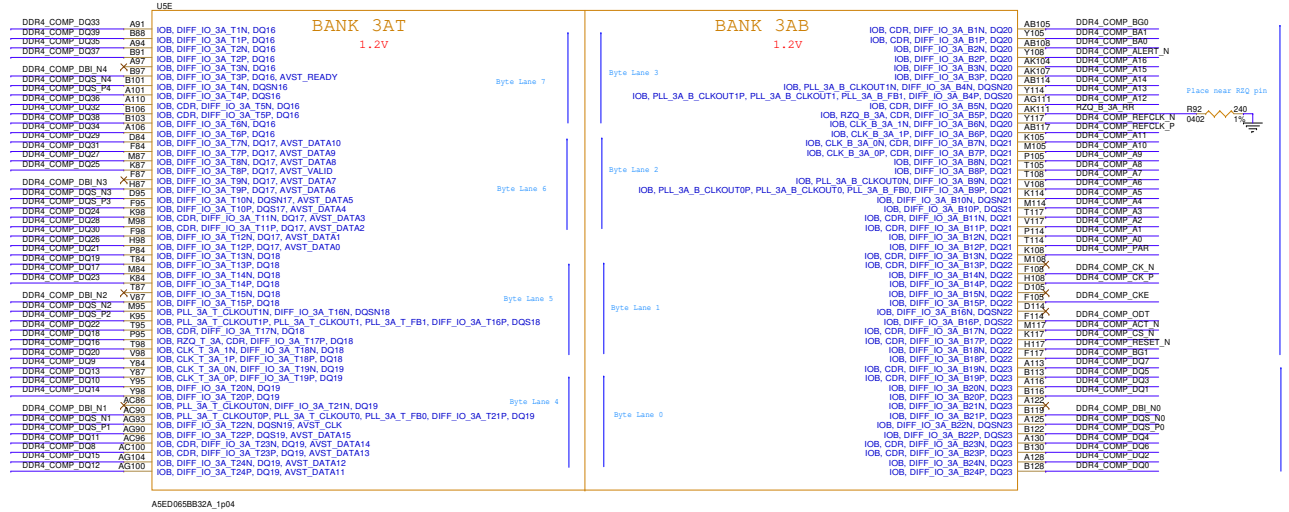
Date: Thursday, September 19, 2024 Sheet 14 of 67

HSIO BANKS 3AL AND 3AR



Please refer to Agilex EMIF User Guide for pin assignment rules.

U5E



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Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 15 of 67

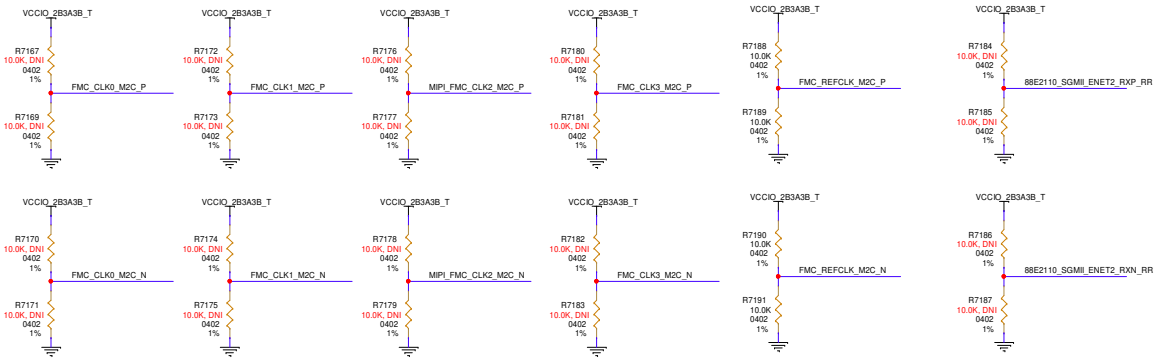
Pin placement restriction for MIPI & LVDS mixing with LVCMOS:

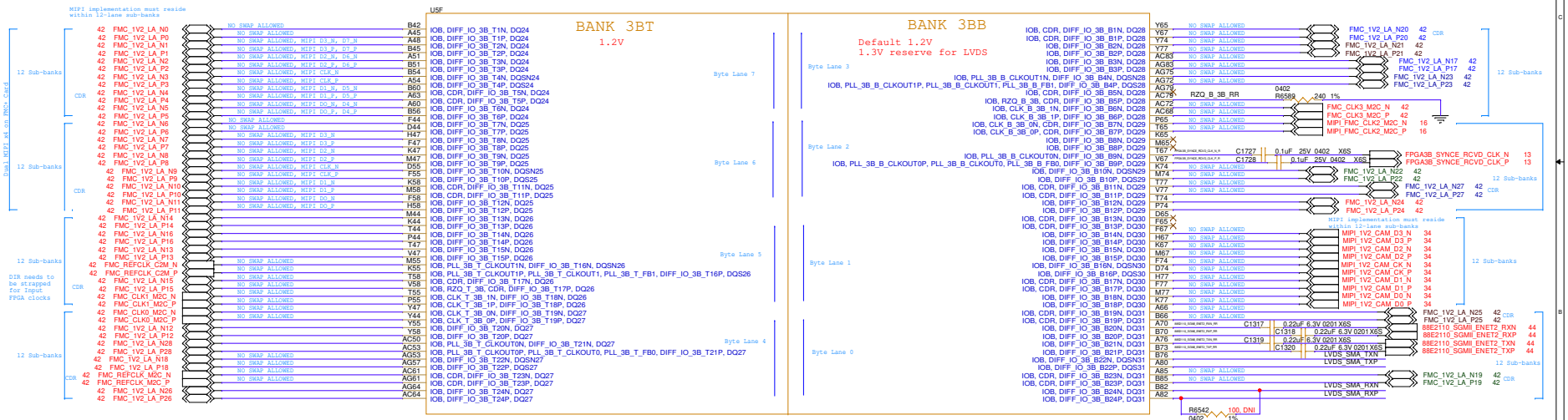
IO Lane Used for MIPI	Width	Restricted Pin Used As LVCMOS	
		Pin Index	Pin Number
IO Lane 1	1 data + 1 clock	P26	V77
	2 data + 1 clock	P26	V77
	4 data + 1 clock	P26 , P10	V77, B66
IO Lane 6	1 data + 1 clock	P75 , P87	K58, B60
	2 data + 1 clock	P87	B60
	4 data + 1 clock	P87, P70 , P82	B60, K44, D44
IO Lane 7	1 data + 1 clock	P86 ; P2 from Bank 3A	A63, B130
	2 data + 1 clock	P77 ; P2 from Bank 3A	D55, B130
	4 data + 1 clock	P77, P83,P94 ; P2 from Bank 3A	D55, F44, A45, B130
IO Lane 6 and 7	8 data + 1 clock	P70, P82, P83, P89 ,P94	K44, D44,F44,B54,A45

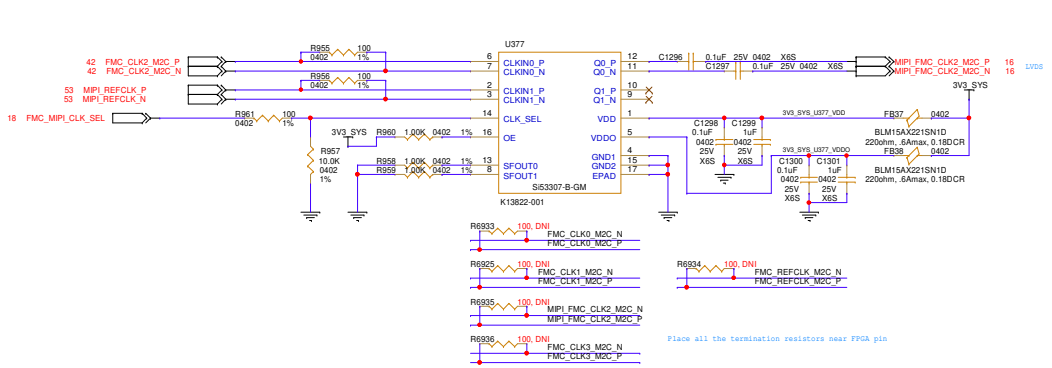
IO Lane Used for LVDS	Function	Restricted Pin Used As LVCMOS	
		Pin Index	Pin Number
IO Lane 0	LVDS_SMA_RX	P3	A85
	LVDS_SMA_TX	-	-
IO Lane 2	FPGA3B_SYNCE_RCVD_CLK	-	-
	MIPI_FMC_CLK2_M2C	P43	AC83
IO Lane 3	FMC_CLK3_M2C	P38, P41	AC79 (RZQ), AG75
IO Lane 4	FMC_REFCLK_M2C	P40, P48	AG72, AC64
	FMC_CLK0_M2C	P57, P67	Y55, T47
IO Lane 5	FMC_CLK1_M2C	P62	V58
	FMC_REFCLK_C2M	P74	M58

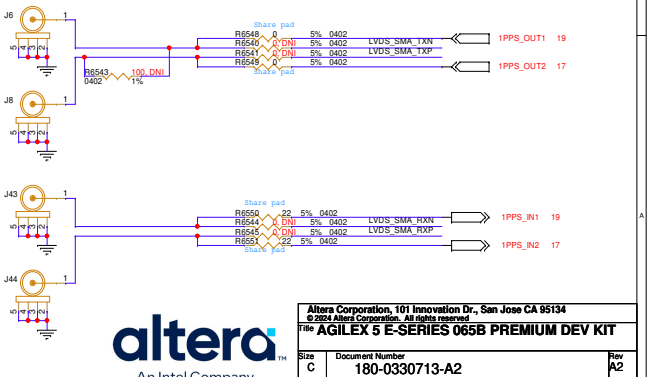
NOTES: Please check the detail restriction guide from IO Pinout Guideline Document if any of the FMC_1V2_LA_* to be used as LVDS.

HSIO BANKS 3BL AND 3BR









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Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 16 of 67

HVIO BANKS 5A AND 5B

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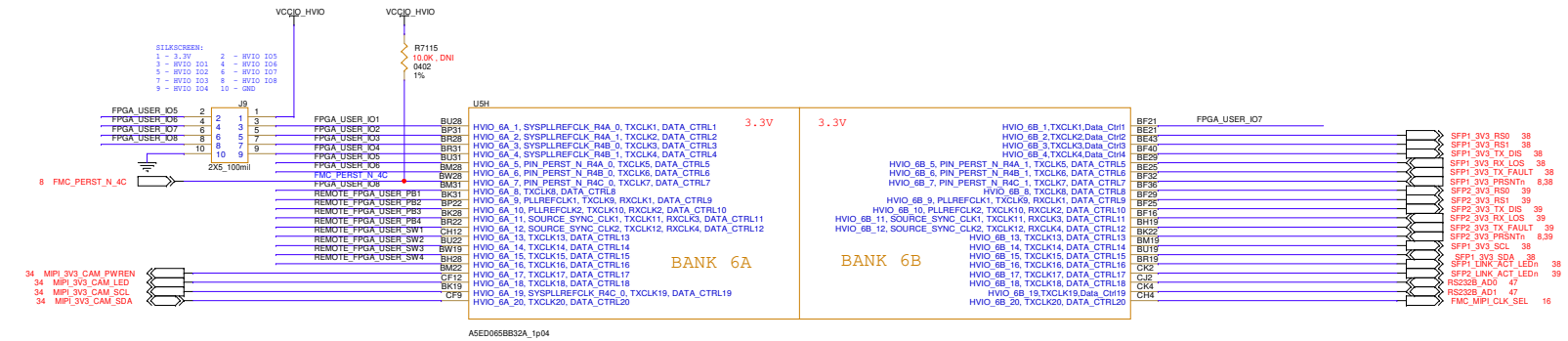
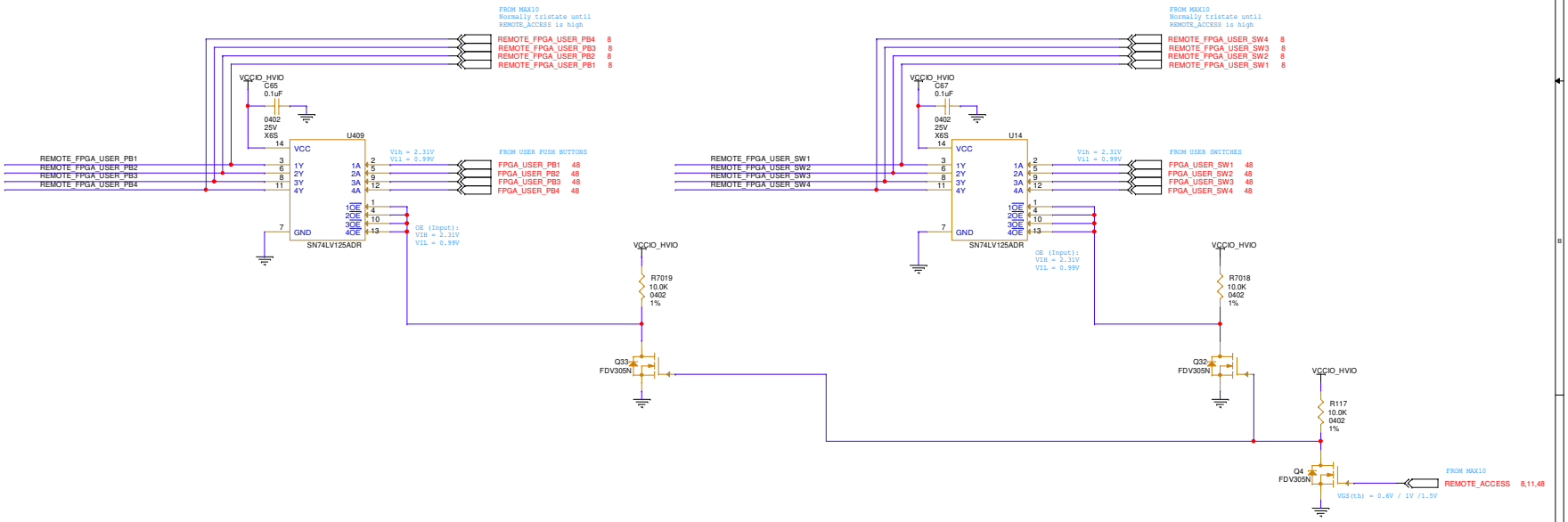
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 17 of 67

HVIO BANKS 6A AND 6B





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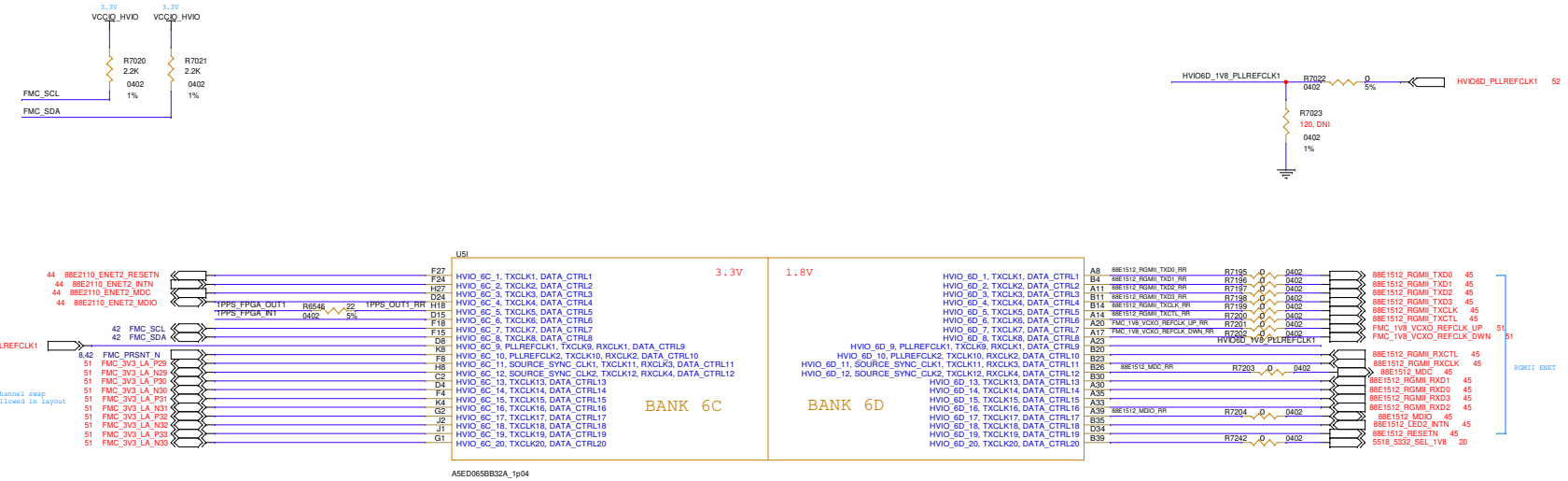
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 18 of 67

HVIO BANKS 6C AND 6D

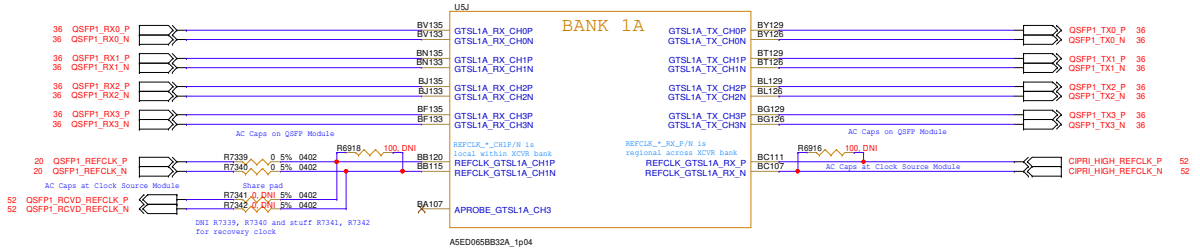


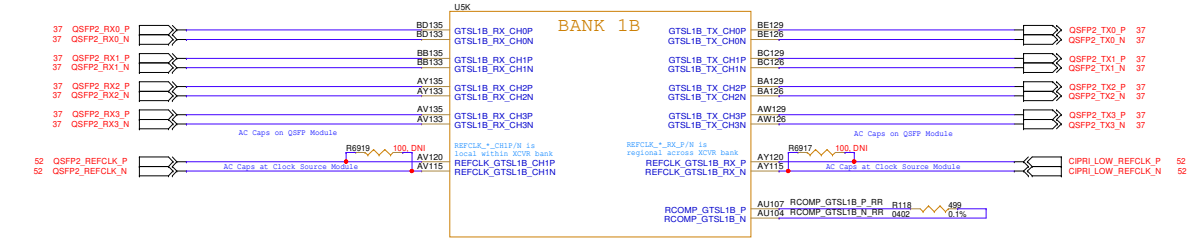
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

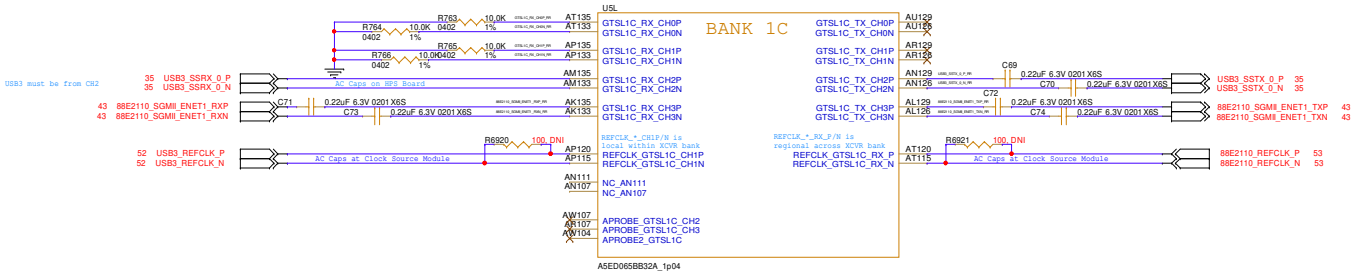
Size	Document Number	Rev
C	180-0330713-A2	A2

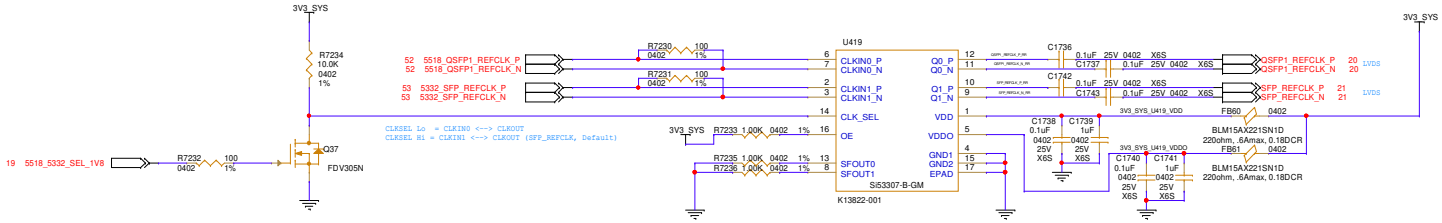
Date: Thursday, September 19, 2024 Sheet 19 of 67

XCVR BANKS 1A, 1B, 1C







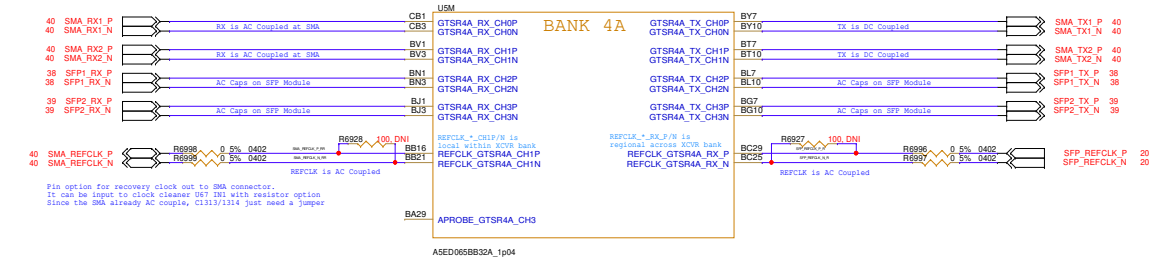


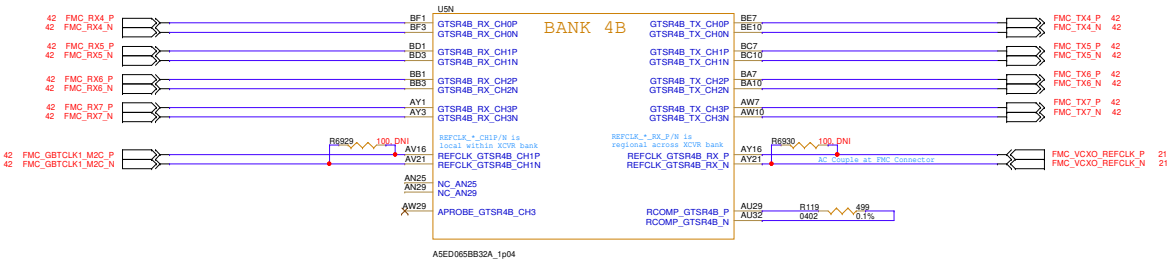
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

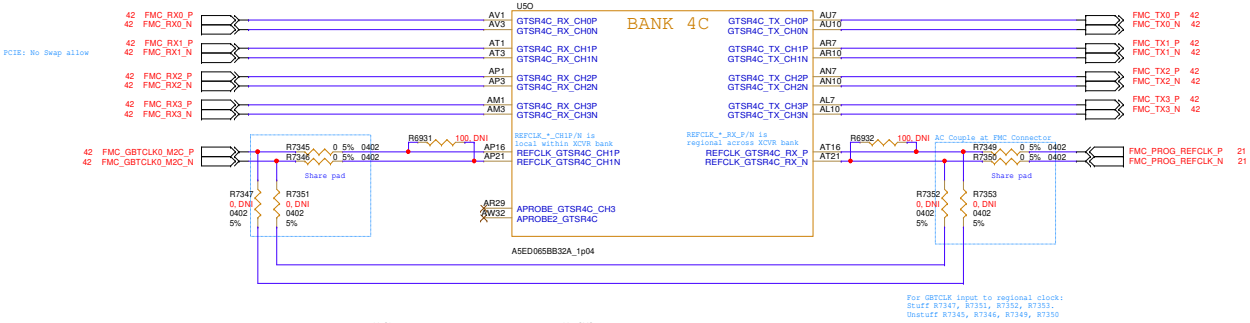
Size	Document Number	Rev
C	180-0330713-A2	A2

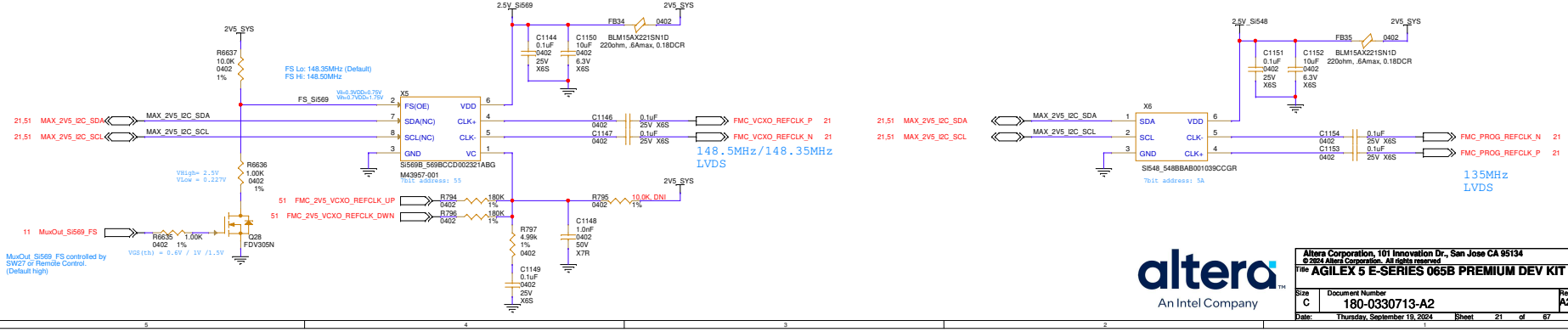
Date: Thursday, September 19, 2024 Sheet 20 of 67

XCVR BANKS 4A, 4B, 4C







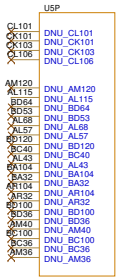


Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 21 of 67

DNU & NC PINS



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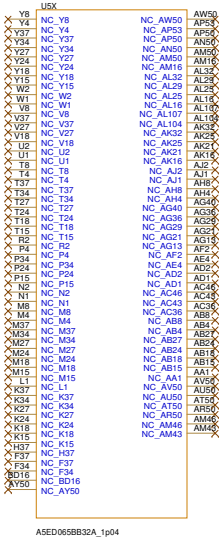

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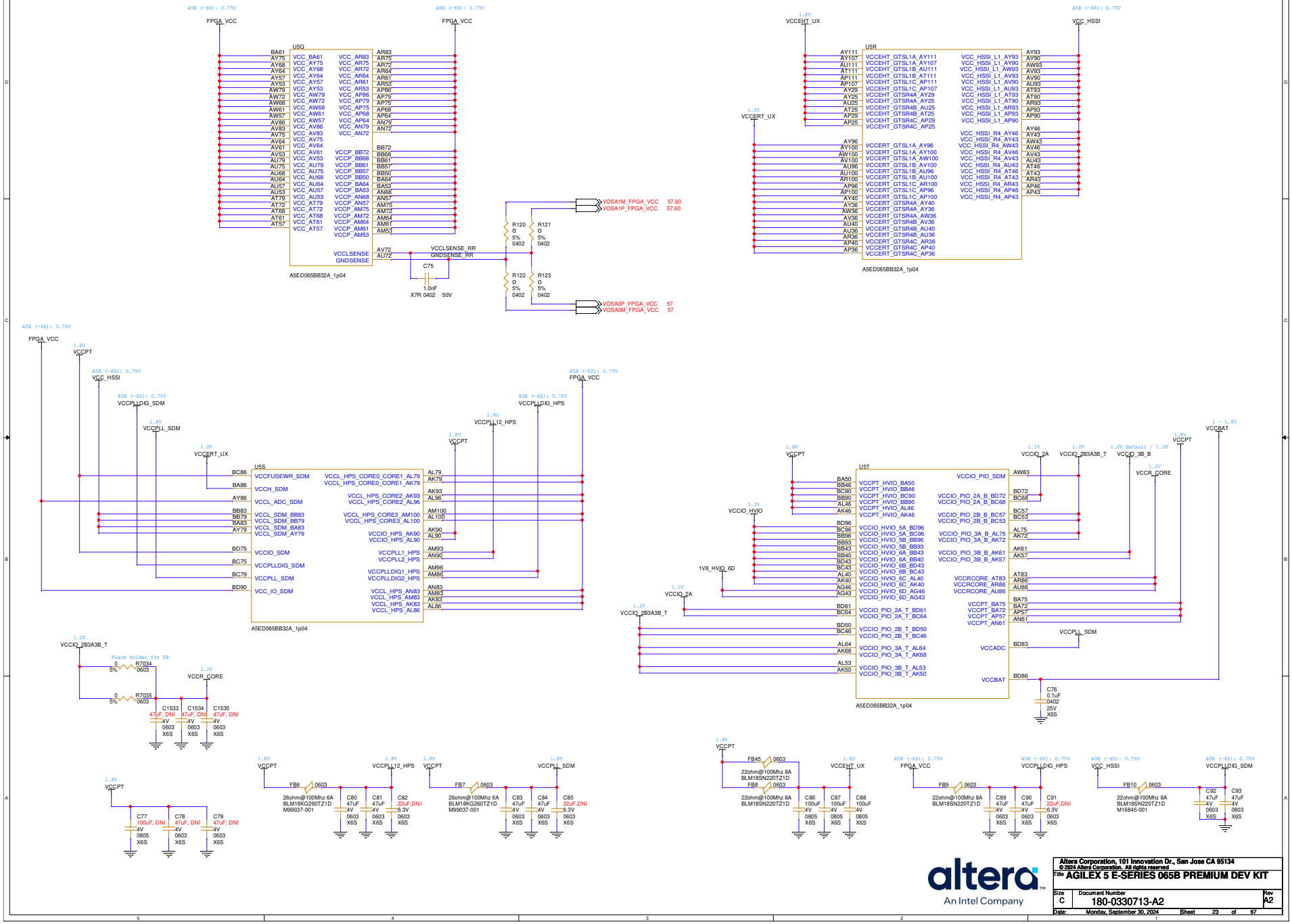
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 22 of 67

FPGA POWER

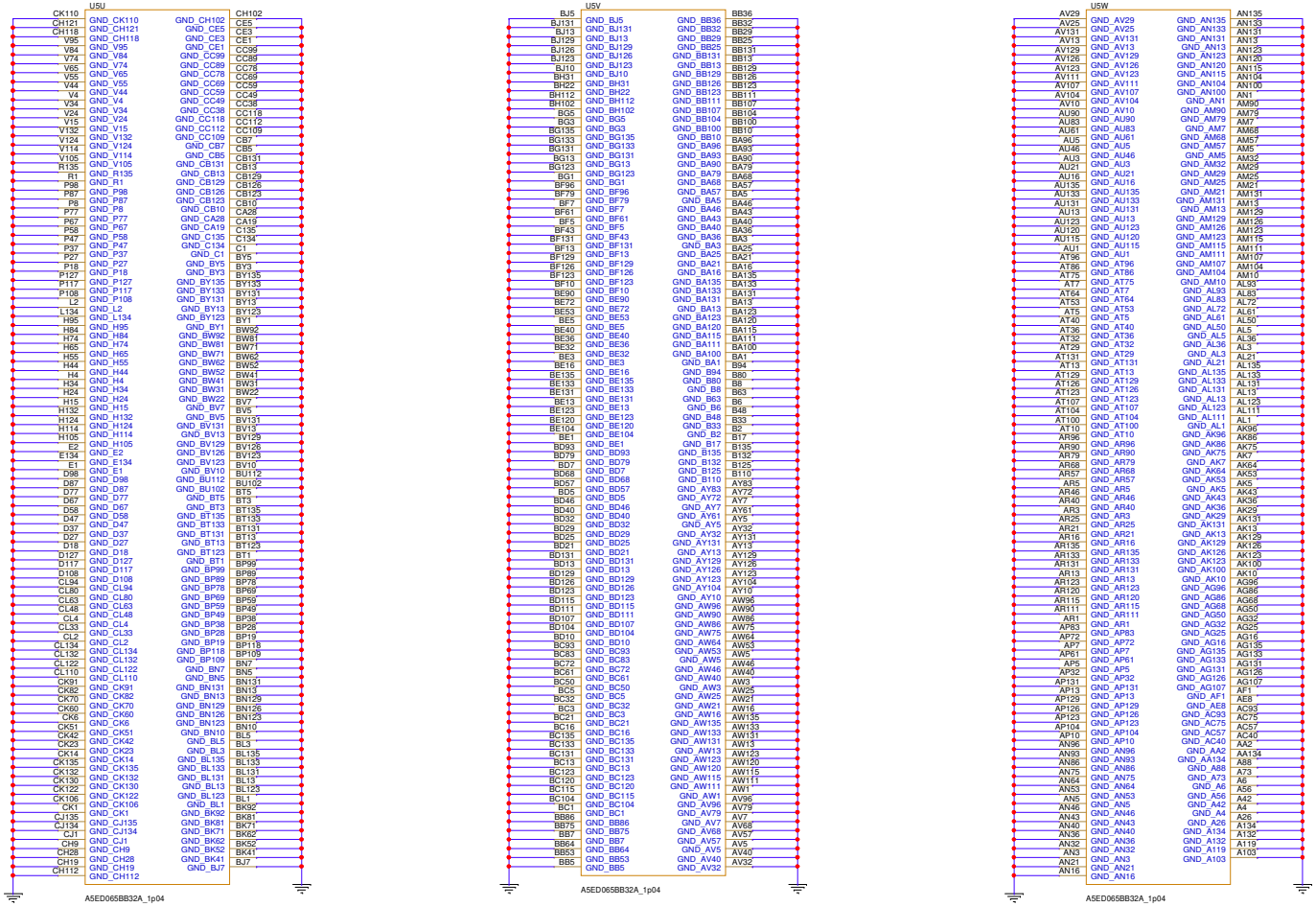


Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Monday, September 30, 2024 Sheet 23 of 67

FPGA GND



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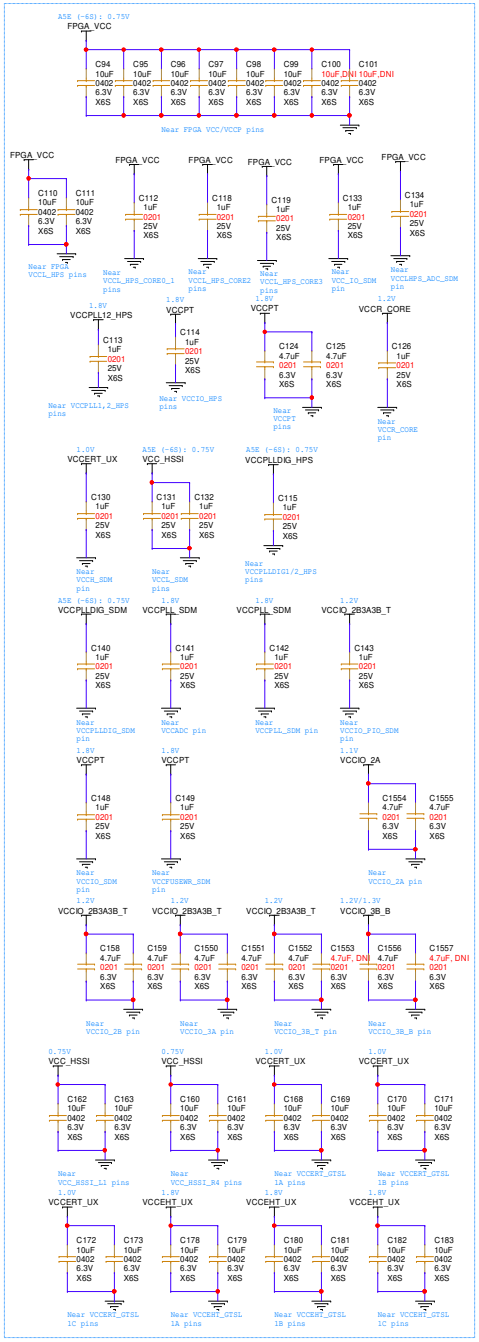
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

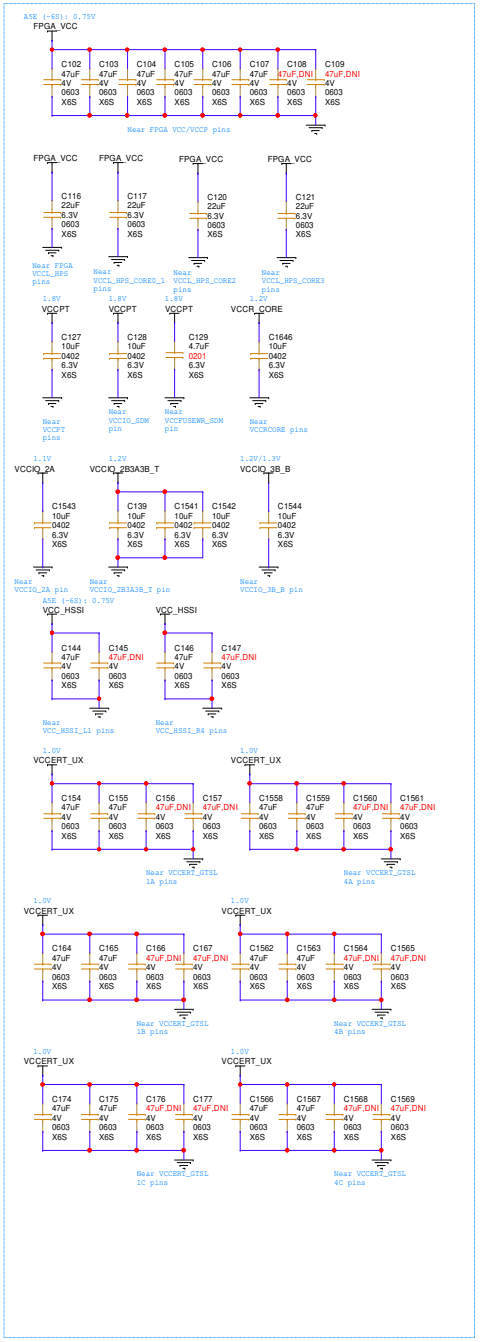
Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 24 of 67

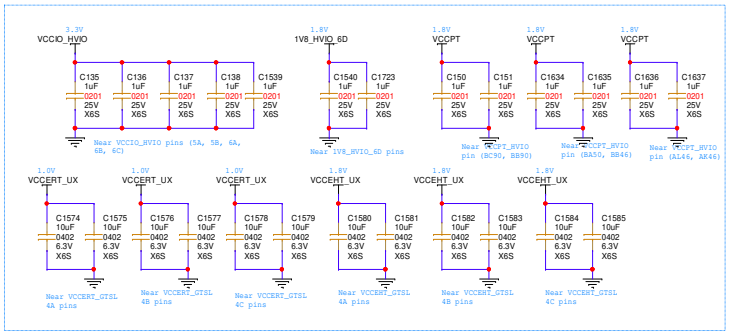
Place bottom FPGA cavity



Place top FPGA periphery



Place bottom FPGA cavity

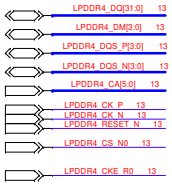


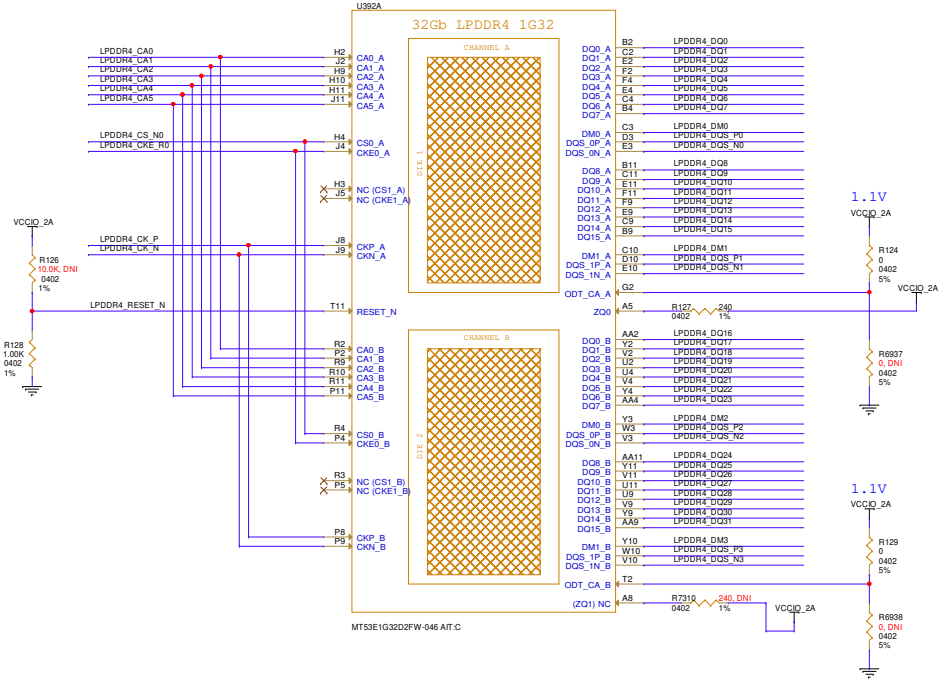
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

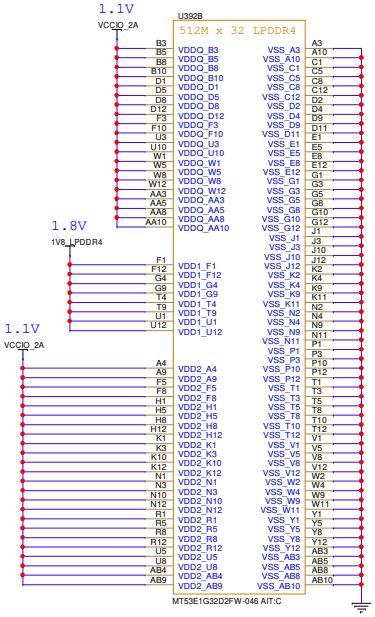
Size	Document Number	Rev
C	180-0330713-A2	A2

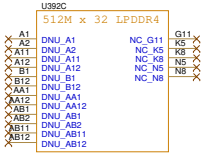
Date: Thursday, September 19, 2024 Sheet 25 of 67

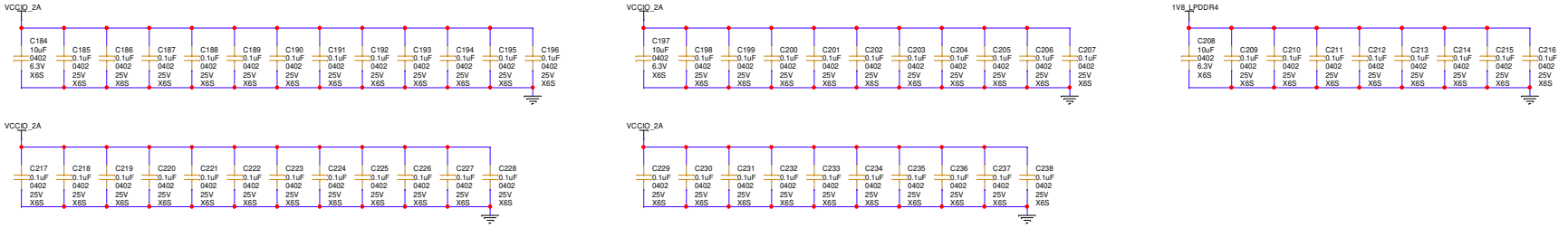
32-BIT LPDDR4









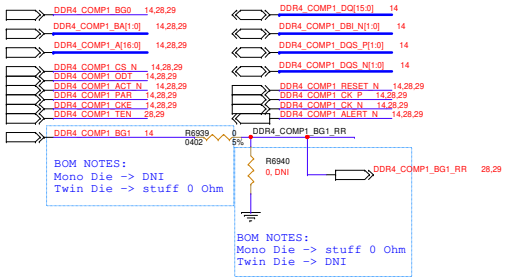


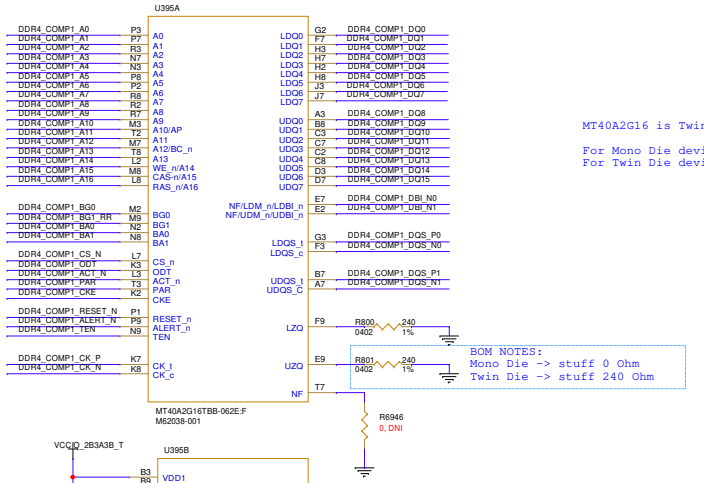
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 26 of 67

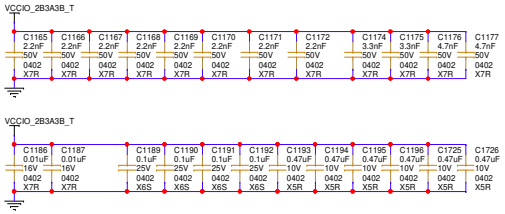
8GB DDR4 COMP1 BYTE 0-1

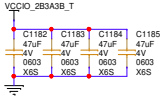


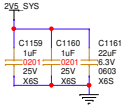


MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)

For Mono Die device, Pin E9 = GND; M9 = GND
For Twin Die device, Pin E9 = UZQ; M9 = BG1.







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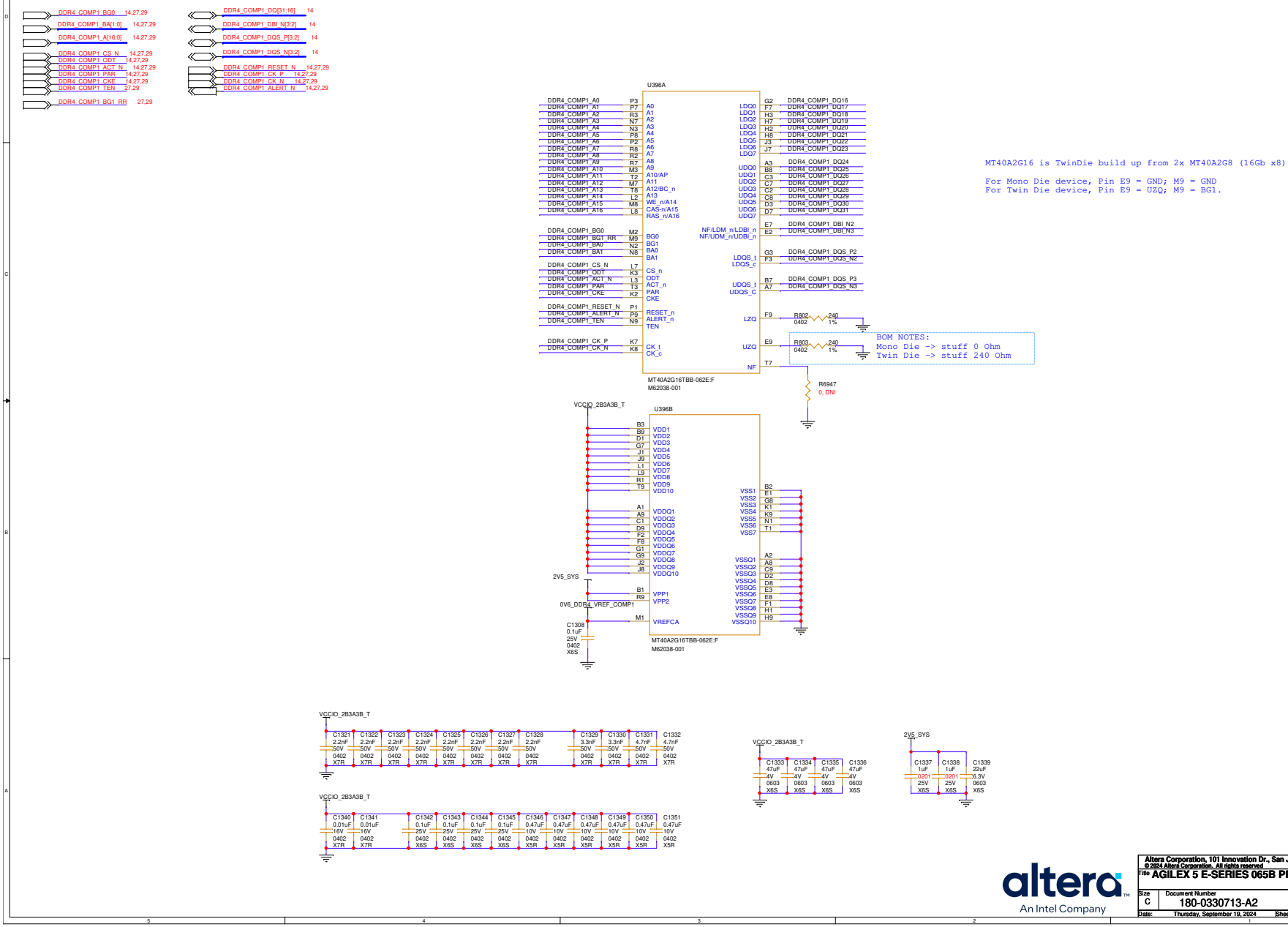
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 27 of 67

8GB DDR4 COMP1 BYTE 2-3



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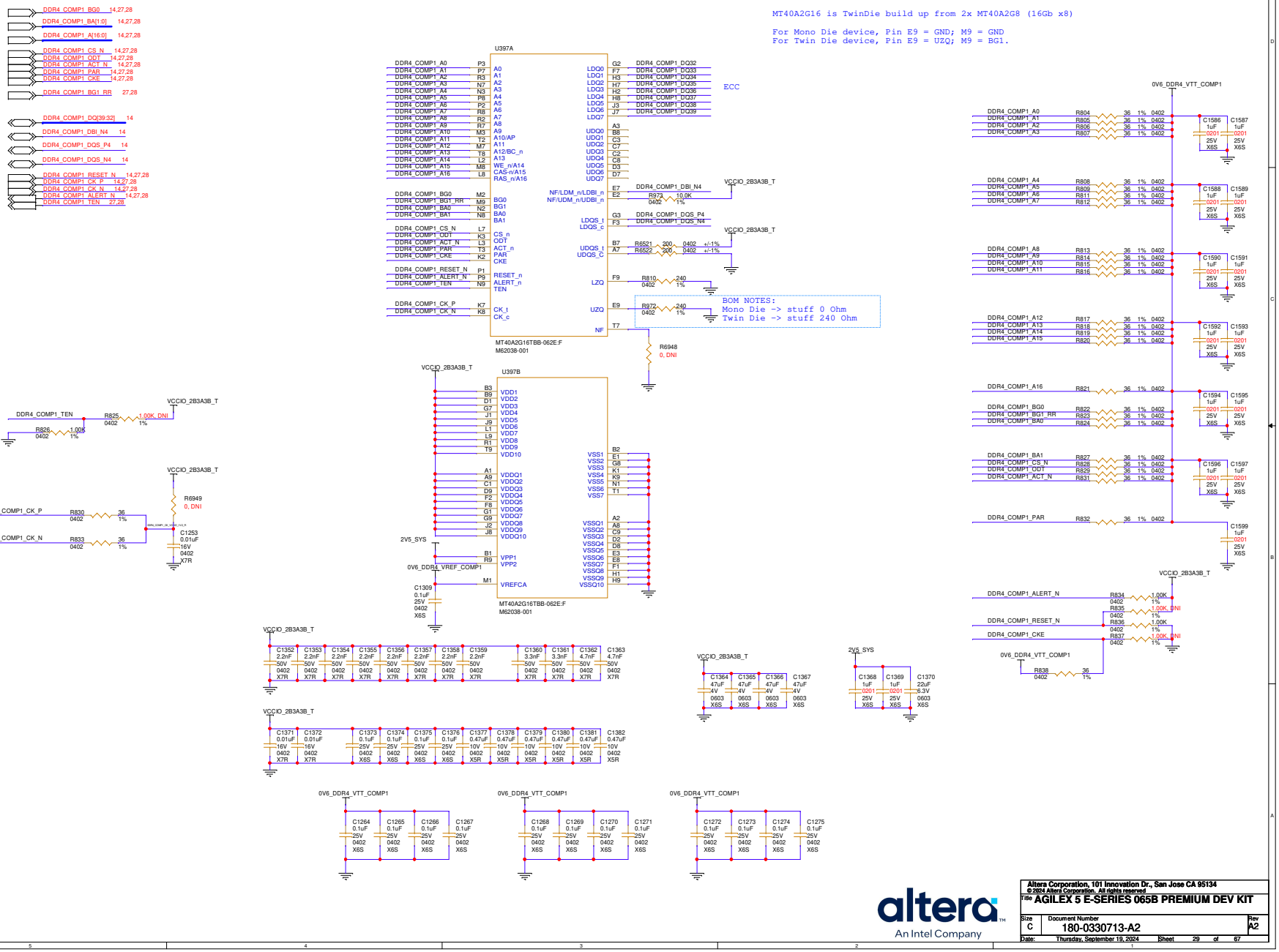
Title	AGILEX 5 E-SERIES 065B PREMIUM DEV KIT	
Size C	Document Number 180-0330713-A2	Rev A2
Date: Thursday, September 19, 2024	Sheet 28 of 67	

8GB DDR4 COMP1 BYTE ECC



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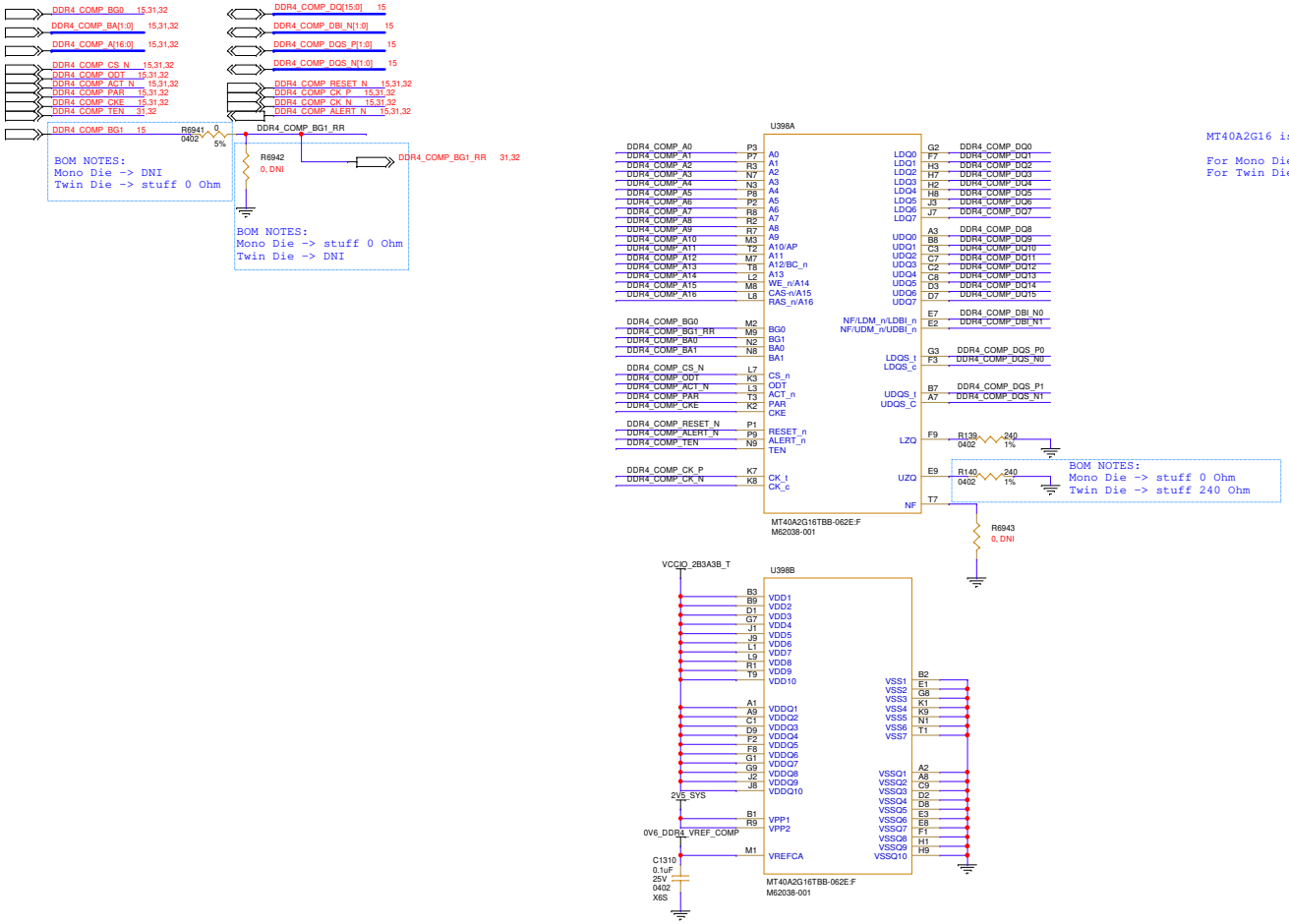
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

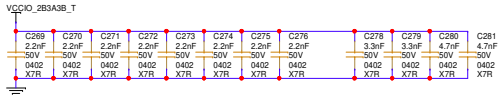
Date: Thursday, September 19, 2024 Sheet 29 of 67

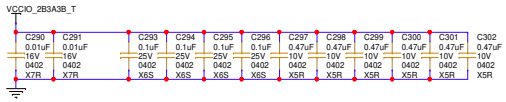
HPS 8GB DDR4 COMPONENT BYTE 0-1

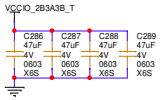


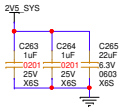
MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)

For Mono Die device, Pin E9 = GND; M9 = GND
For Twin Die device, Pin E9 = UZQ; M9 = BG1.









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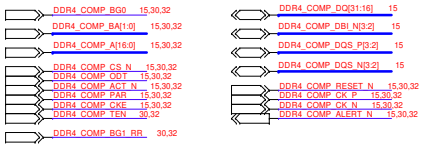
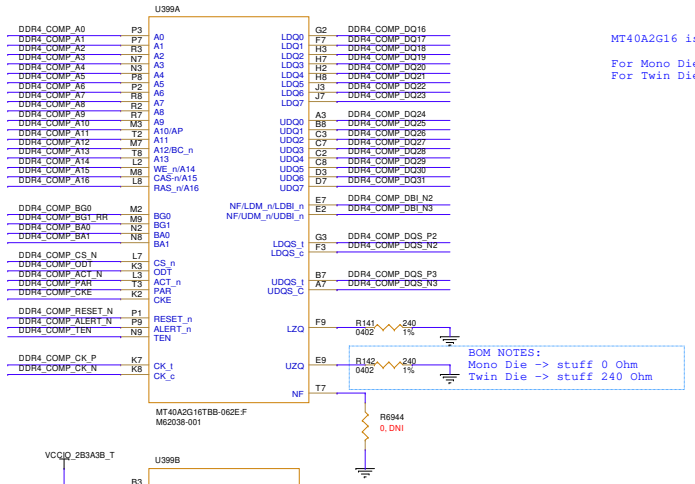
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

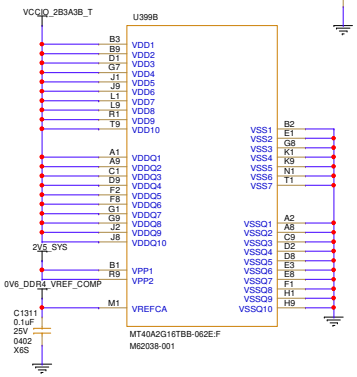
Size	Document Number	Rev
C	180-0330713-A2	A2

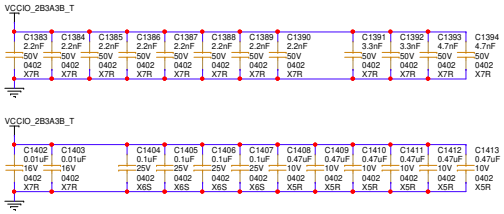
Date: Thursday, September 19, 2024 Sheet 30 of 67

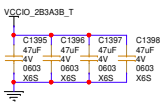
HPS 8GB DDR4 COMPONENT BYTE 2-3

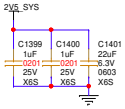












Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 31 of 67

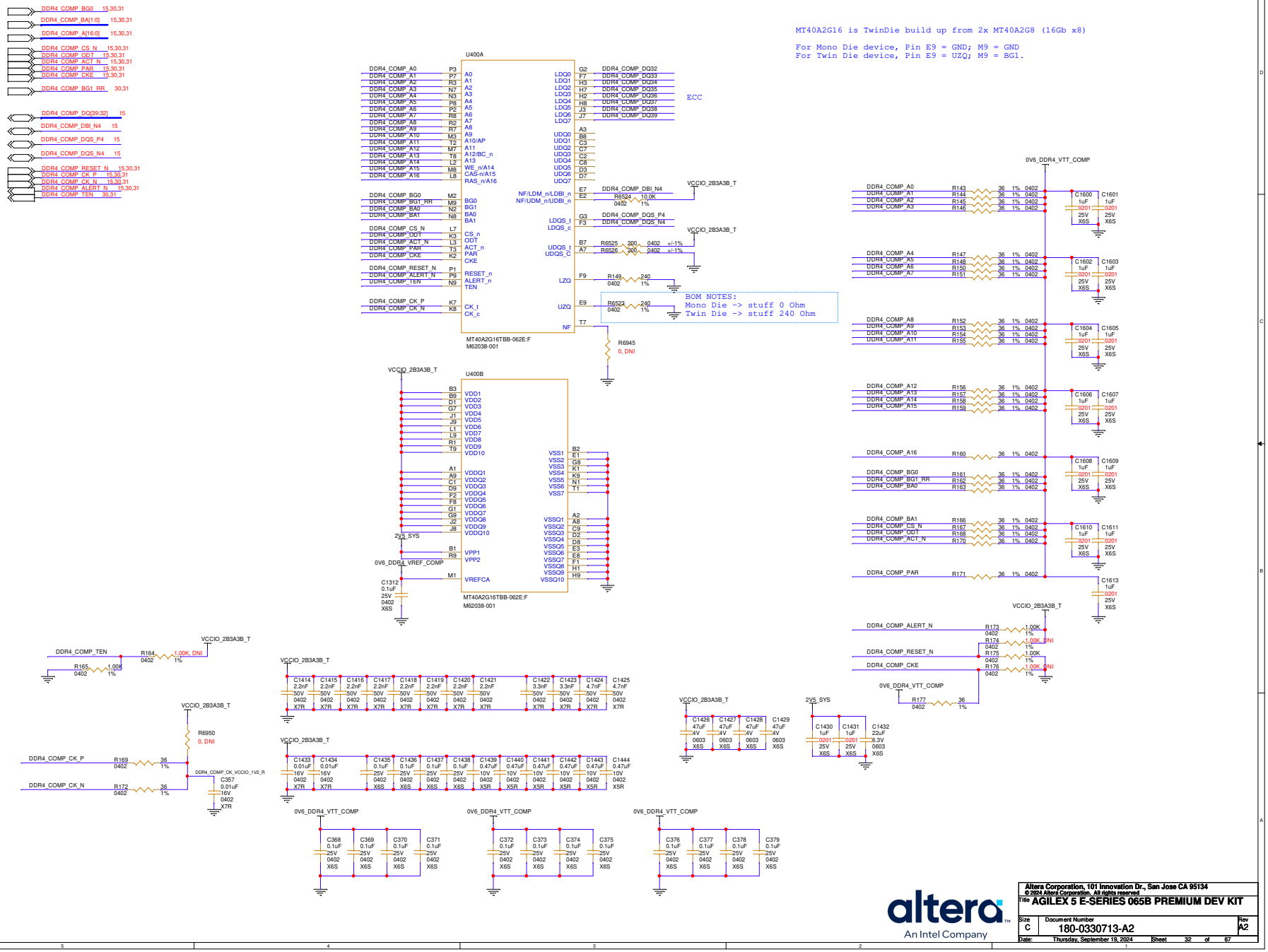
HPS 8GB DDR4 COMPONENT BYTE ECC

MT40A2G16 is TwinDie build up from 2x MT40A2G8 (16Gb x8)

For Mono Die device, Pin E9 = GND; M9 = GND
For Twin Die device, Pin E9 = UZQ; M9 = BG1.

BOM NOTES:
Mono Die -> stuff 0 Ohm
Twin Die -> stuff 240 Ohm

ECC



Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 32 of 67

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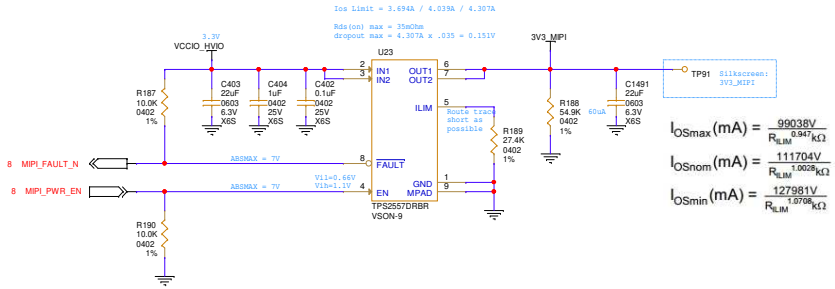
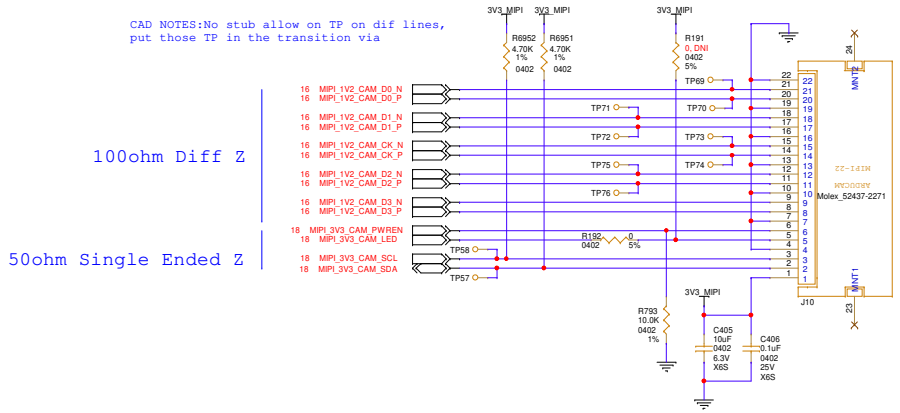
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 33 of 67





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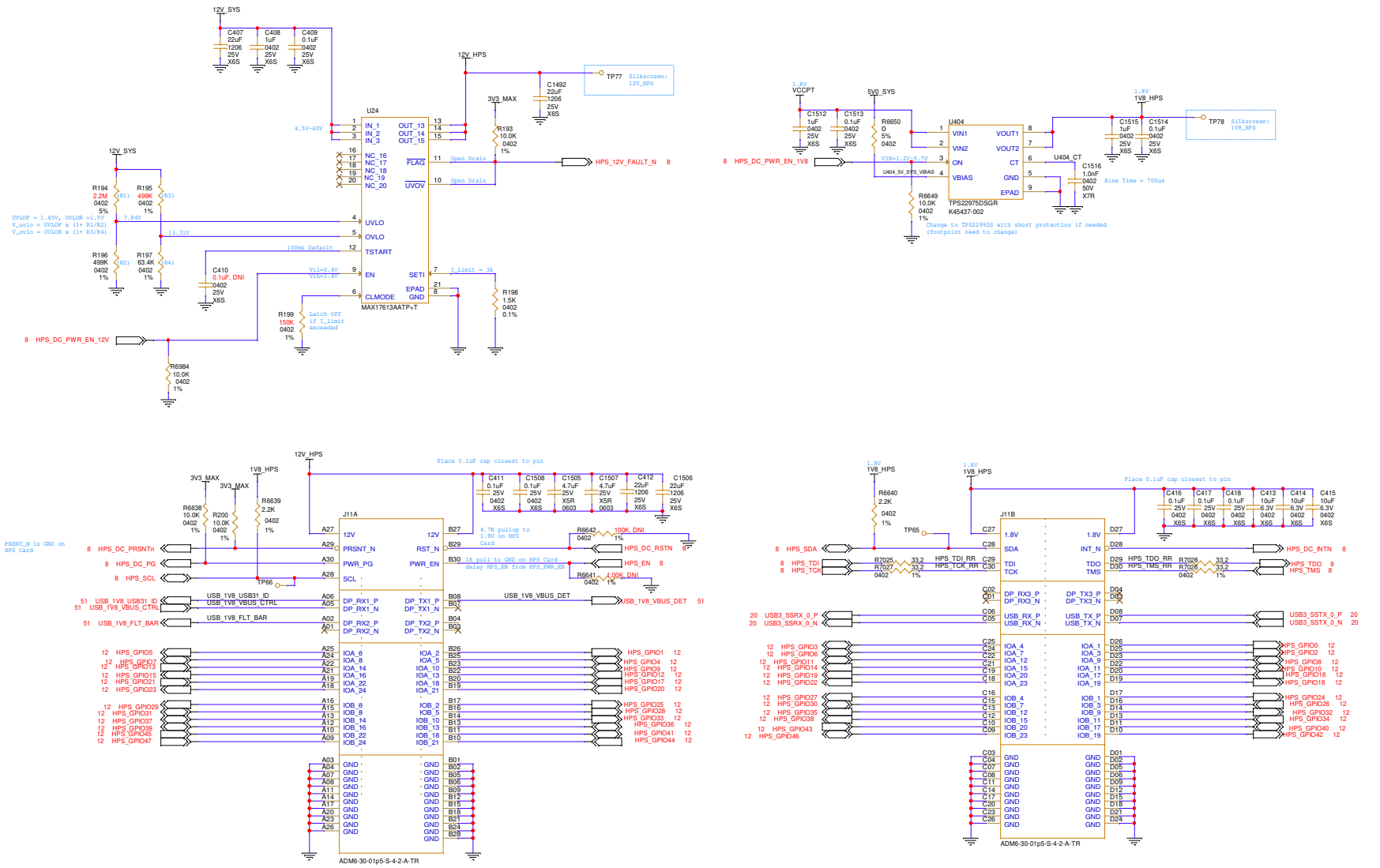
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

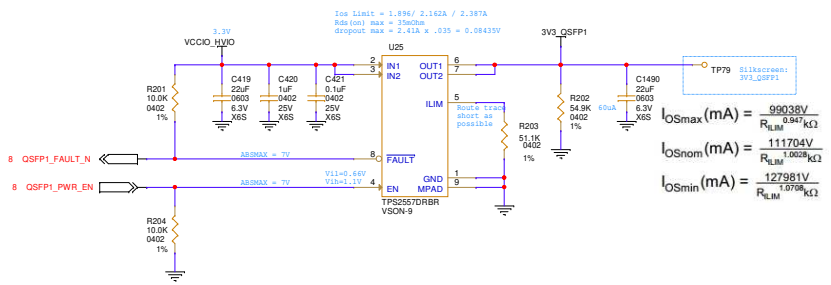
Date: Thursday, September 19, 2024 Sheet 34 of 67



Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 35 of 67

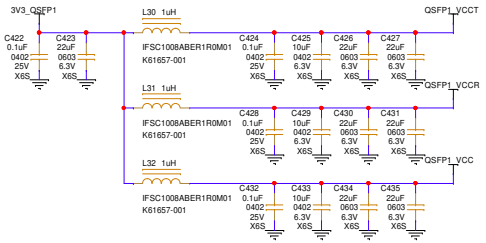


NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

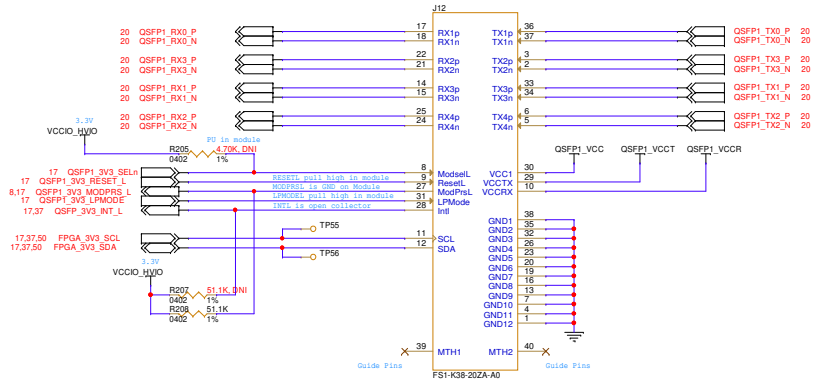
NOTE 2: QSFP 100-ohm termination is implemented via the FPGA on-chip termination.

NOTE 3: DC blocking capacitors are in the module for RX and TX.

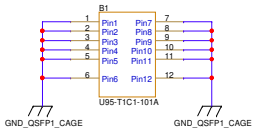
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



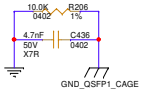
Place close to QSFP Connector

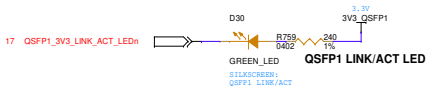


Amphenol FS1-K38-20ZA-A0



Amphenol U95-T1C1-101A

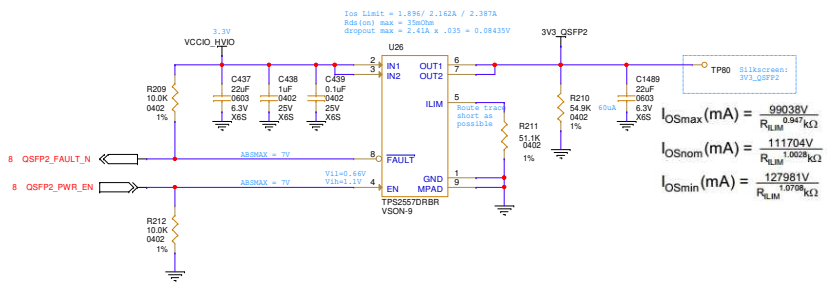




Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 36 of 67

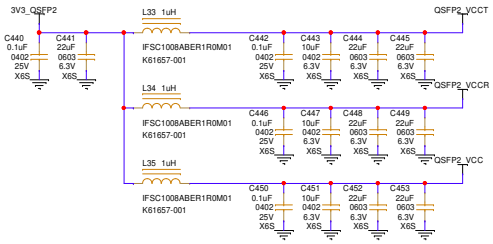


NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

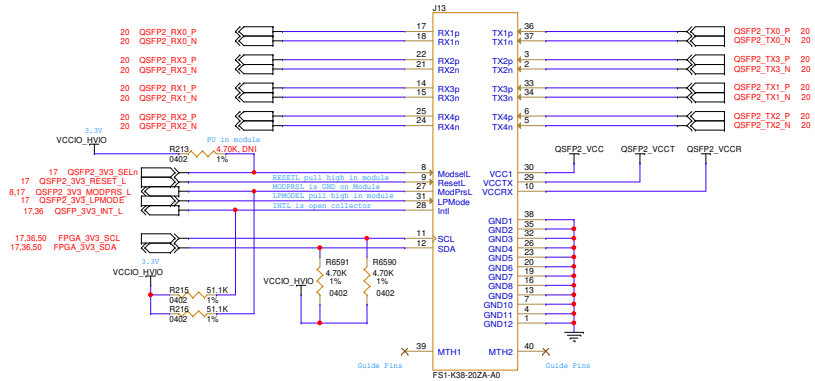
NOTE 2: zQSFP 100-ohm termination is implemented via the FPGA on-chip termination.

NOTE 3: DC blocking capacitors are in the module for RX and TX.

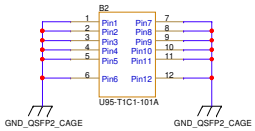
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



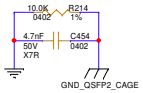
Place close to zQSFP Connector

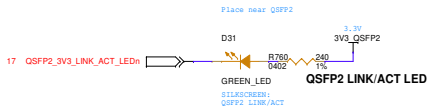


Amphenol FS1-K38-20ZA-A0



Amphenol U95-T1C1-101A





QSFP2 LINK/ACT LED

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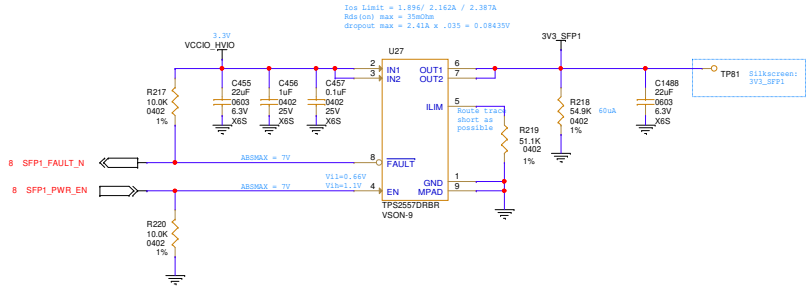
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

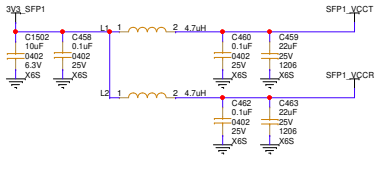
Date: Thursday, September 19, 2024 Sheet 37 of 67

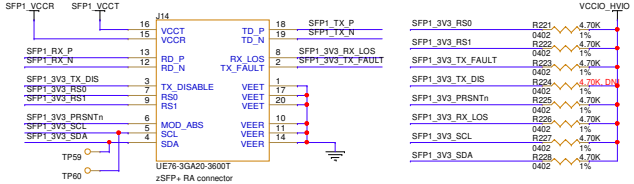


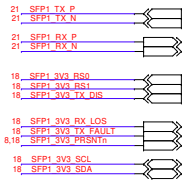
NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

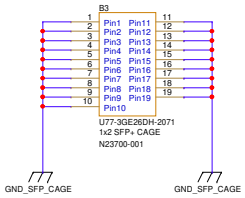
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

NOTE 3: DC blocking capacitors are in the module for RX and TX.





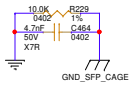


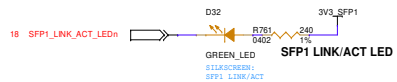


Optical (SFP+) Transceiver Cage 1x2

SFP modules have RS1 connected to GND.
If using SFP+ Rate Select pin are defined as:
RS1=0 -> TX datarates <= 4.25GB/s
RS1=1 -> TX datarates > 4.25GB/s

RS0=0 -> RX datarates <= 4.25GB/s
RS0=1 -> RX datarates > 4.25GB/s



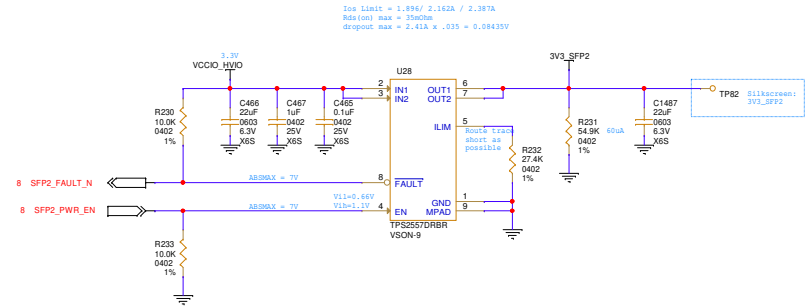


SFP1 LINK/ACT LED

Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

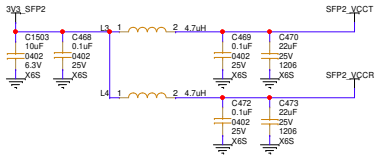
Date: Thursday, September 19, 2024 Sheet 38 of 67



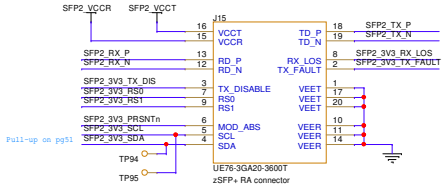
NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

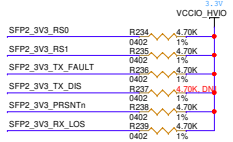
NOTE 3: DC blocking capacitors are in the module for RX and TX.



Level I power is < 1W (0.3 A)
Level II power is < 1.5W (0.45 A)
Level II Instantaneous peak current per rail 600mA

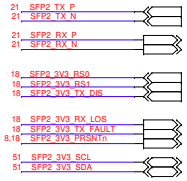


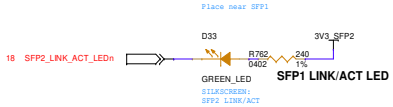
Optical (SFP+) Connector, case in page 38 B3



SFP modules have RS1 connected to GND.
If using SFP+ Rate Select pin are defined as:
RS1=0 -> TX datarates <= 4.25GB/s
RS1=1 -> TX datarates > 4.25GB/s

RS0=0 -> RX datarates <= 4.25GB/s
RS0=1 -> RX datarates > 4.25GB/s





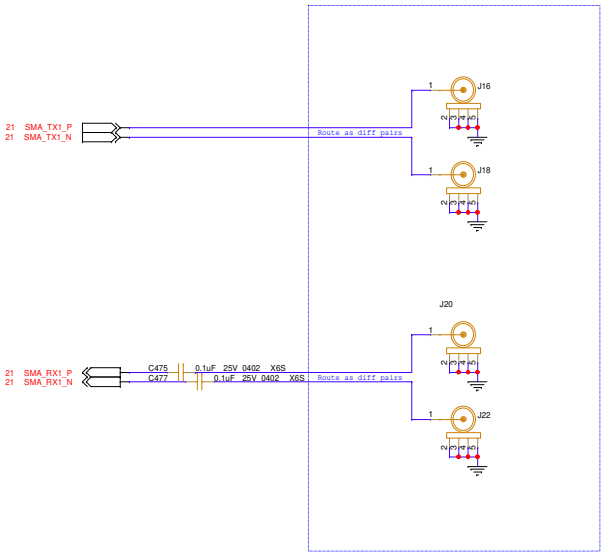
SFP1 LINK/ACT LED

Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

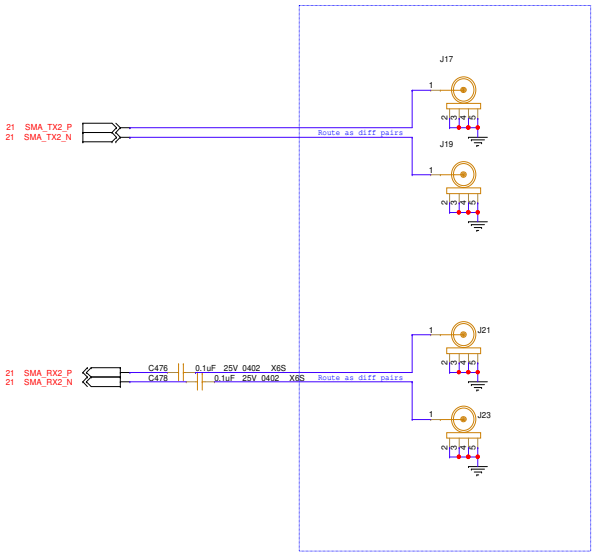
Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 39 of 67

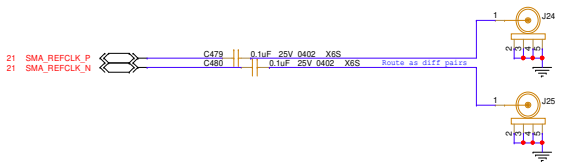
SMA TX/RX 1



SMA TX/RX 2



SMA XCVR REFCLK IN



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Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 40 of 67

FMC+ Connector (Vita 57.4) Complete Pin Table

FMC Connector (Vita 57.1) Complete Pin Table

14 x 40	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND

FMC+ Voltage Specification

Voltage Supply	Allowable Voltage Range	No Pins	Max Amps	Tolerance	Max Capacitive Load
VADJ	0 – 3.3V	4	4	+/- 5%	1000 uF
VIO_B_M2C	0 – VADJ	2	1.15	+/- 5%	500 uF
VREF_A_M2C	0 – VADJ	1	1mA	+/- 2%	10 uF
VREF_B_M2C	0 – VIO_B_M2C	1	1mA	+/- 2%	10 uF
3P3VAUX	3.3V	1	20mA	+/- 5%	150 uF
3P3V	3.3V	5	3	+/- 5%	1000 uF
12P0V	12V	5	1	+/- 5%	1000 uF

Supported FMC Cards:

1. FMC+ PCIe Gen4 x16 RootPort Card (HighTech Global)
** Note: Only support PCIe Gen4 x4 **
2. FMC+ HDMI 2.1 Card Rev9 (Bitec)
3. FMC+ DP 1.4 Rev12 (Bitec)

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Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size: C | Document Number: 180-0330713-A2 | Rev: A2

Date: Thursday, September 19, 2024 | Sheet 41 of 67

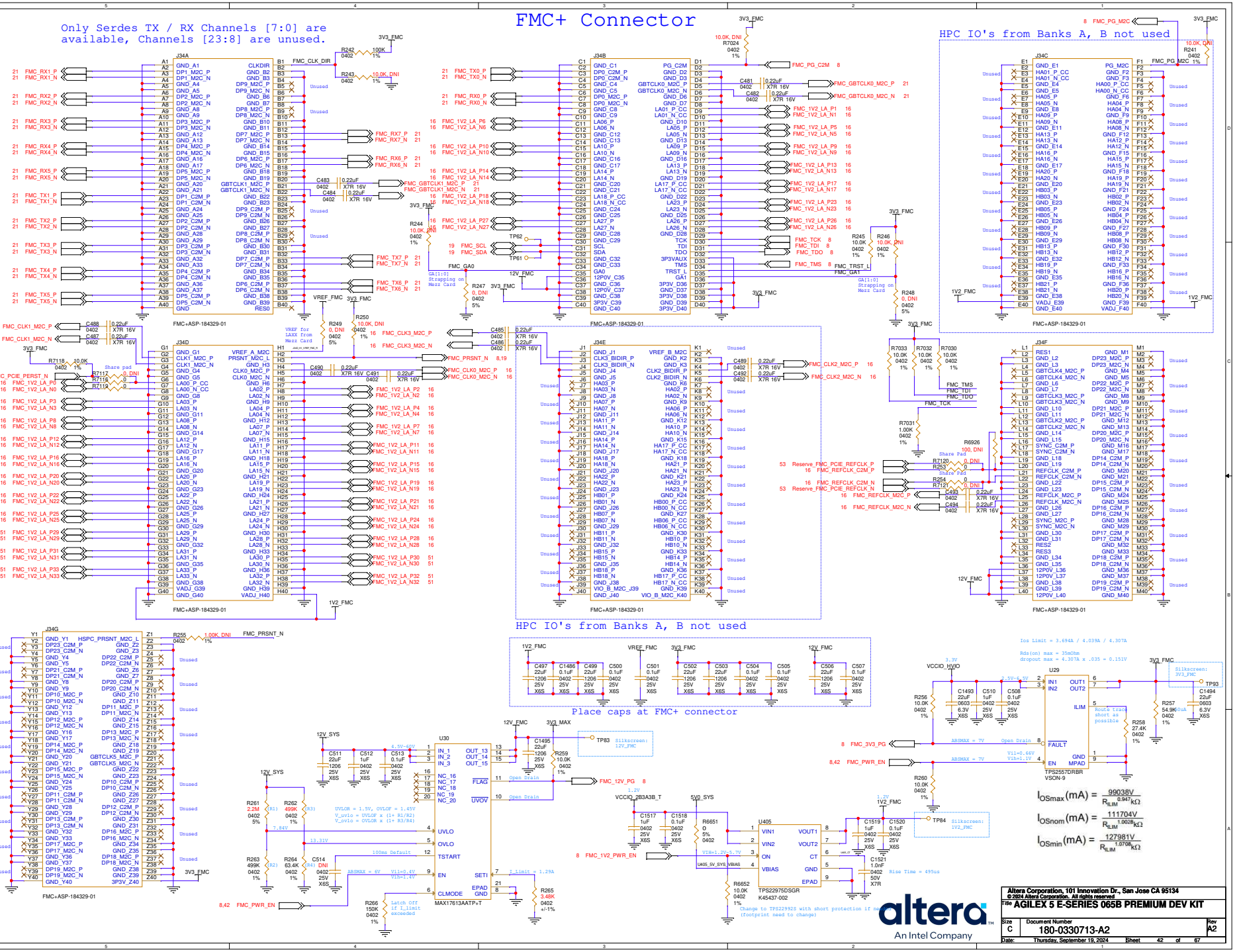
FMC+ Connector

Only Serdes TX / RX Channels [7:0] are available, Channels [23:8] are unused.

HPC IO's from Banks A, B not used

HPC IO's from Banks A, B not used

Place caps at FMC+ connector



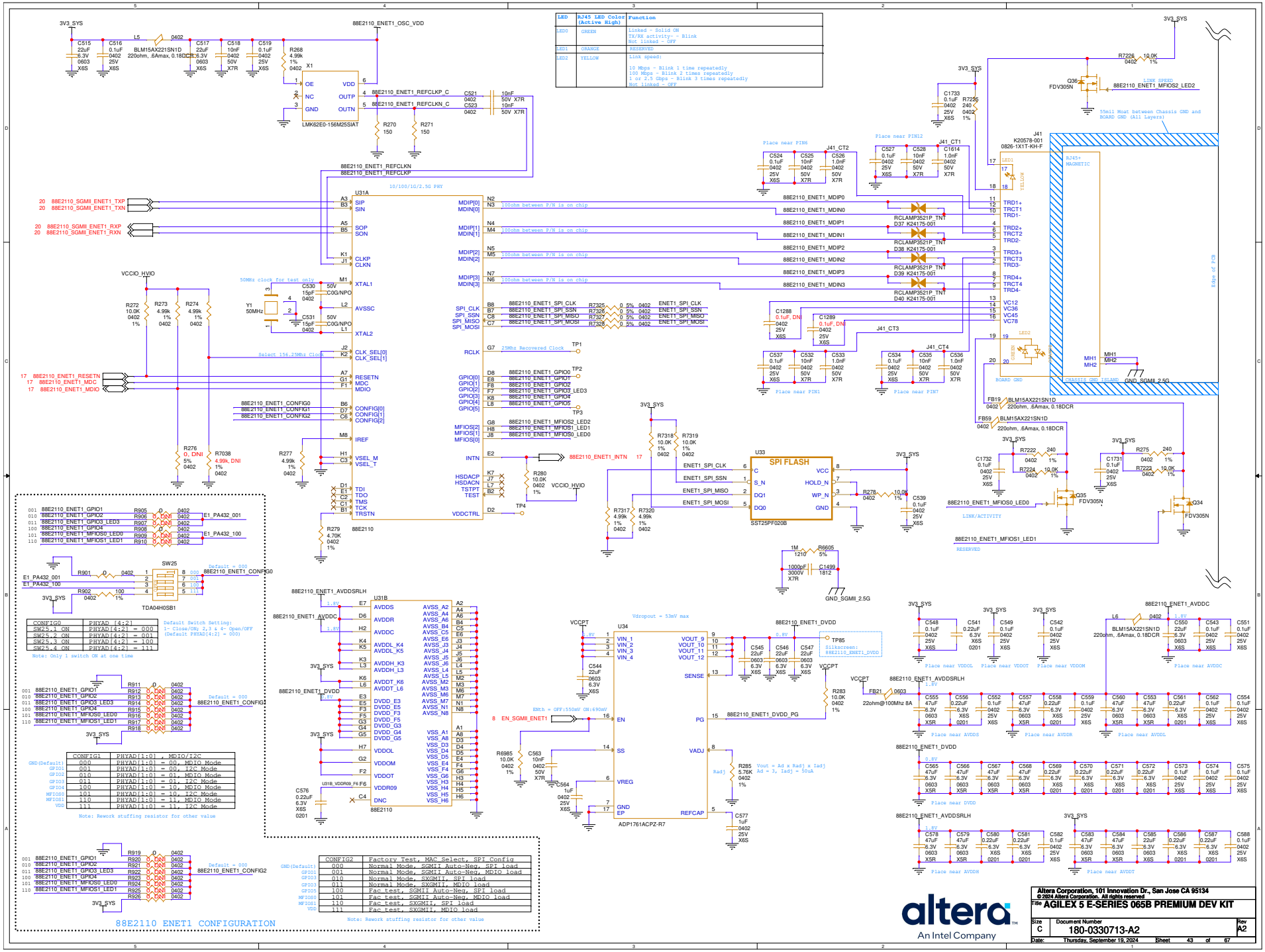
$$I_{OSmax}(mA) = \frac{99038V}{R_{ILIM}(k\Omega)} - 0.947$$

$$I_{OSnom}(mA) = \frac{111704V}{R_{ILIM}(k\Omega)} - 1.0028$$

$$I_{OSmin}(mA) = \frac{127981V}{R_{ILIM}(k\Omega)} - 1.0708$$

Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2
Date: Thursday, September 19, 2024	Sheet 42 of 67	


88E2110_ENET1_OSC_VDD
LMK62E0-156M25SIAT
88E2110_ENET1_REFCLKP
88E2110_ENET1_REFCLKN
88E2110_ENET1_REFCLKP_C
88E2110_ENET1_REFCLKN_C
10/100/1G/2.5G PHY
U31A
U31B
88E2110
VCCIO_HVIO
50MHz clock for test only
Select 156.25Mhz Clock
25Mhz Recovered Clock
88E2110_ENET1_INTN
88E2110_ENET1_RESETN
88E2110_ENET1_MDC
88E2110_ENET1_MDIO
88E2110_ENET1_SPI_CLK
88E2110_ENET1_SPI_SSN
88E2110_ENET1_SPI_MISO
88E2110_ENET1_SPI_MOSI
88E2110_ENET1_MDIP0
88E2110_ENET1_MDIN0
88E2110_ENET1_MDIP1
88E2110_ENET1_MDIN1
88E2110_ENET1_MDIP2
88E2110_ENET1_MDIN2
88E2110_ENET1_MDIP3
88E2110_ENET1_MDIN3
100ohm between P/N is on chip
RCLAMP3521P_TNT
J41
K20578-001
0826-1X1T-KH-F
RJ45+ MAGNETIC
SPI FLASH
SST25PF020B
ENET1_SPI_CLK
ENET1_SPI_SSN
ENET1_SPI_MISO
ENET1_SPI_MOSI
88E2110_ENET1_MFIOS2_LED2
88E2110_ENET1_MFIOS0_LED0
88E2110_ENET1_MFIOS1_LED1
LINK SPEED
LINK/ACTIVITY
RESERVED
55mil Moat between Chassis GND and BOARD GND (All Layers)
Place near PIN1
Place near PIN6
Place near PIN7
Place near PIN12
BOARD GND
CHASSIS GND_ISLAND
GND_SGMII_2.5G
88E2110_ENET1_AVDDSRLH
88E2110_ENET1_AVDDC
88E2110_ENET1_DVDD
88E2110_ENET1_DVDD_PG
ADP1761ACPZ-R7
Vdropout = 52mV max
ENth = OFF:550mV ON:690mV
Vout = Ad x Radj x Iadj
Ad = 3, Iadj = 50uA
88E2110 ENET1 CONFIGURATION
CONFIG0
CONFIG1
CONFIG2
Factory Test, MAC Select, SPI Config
Normal Mode, SGMII Auto-Neg, SPI load
Normal Mode, SGMII Auto-Neg, MDIO load
Normal Mode, SXGMII, SPI load
Normal Mode, SXGMII, MDIO load
Fac test, SGMII Auto-Neg, SPI load
Fac test, SGMII Auto-Neg, MDIO load
Fac test, SXGMII, SPI load
Fac test, SXGMII, MDIO load
Note: Rework stuffing resistor for other value
Default Switch Setting:
1- Close/ON; 2,3 & 4- Open/OFF
(Default PHYAD[4:2] = 000)
TDA04H0SB1
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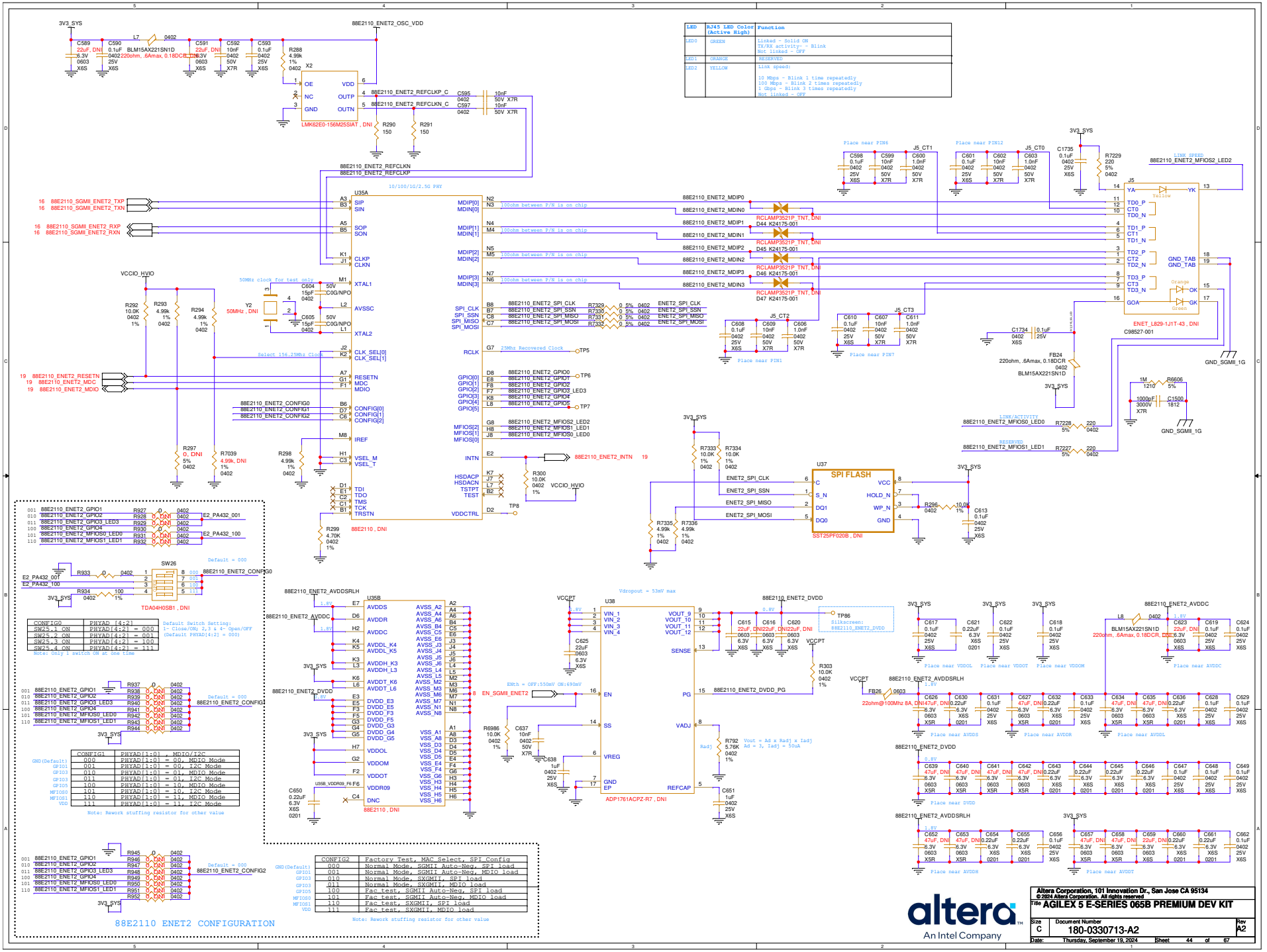
Title AGILEX 5 E-SERIES 065B PREMIUM DEV KIT
Size C
Document Number 180-0330713-A2
Rev A2
Date: Thursday, September 19, 2024
Sheet 43 of 67


88E2110 ENET2 CONFIGURATION
SPI FLASH
SST25PF020B , DNI
ADP1761ACPZ-R7 , DNI
LMK82E0-156M25SIAT , DNI
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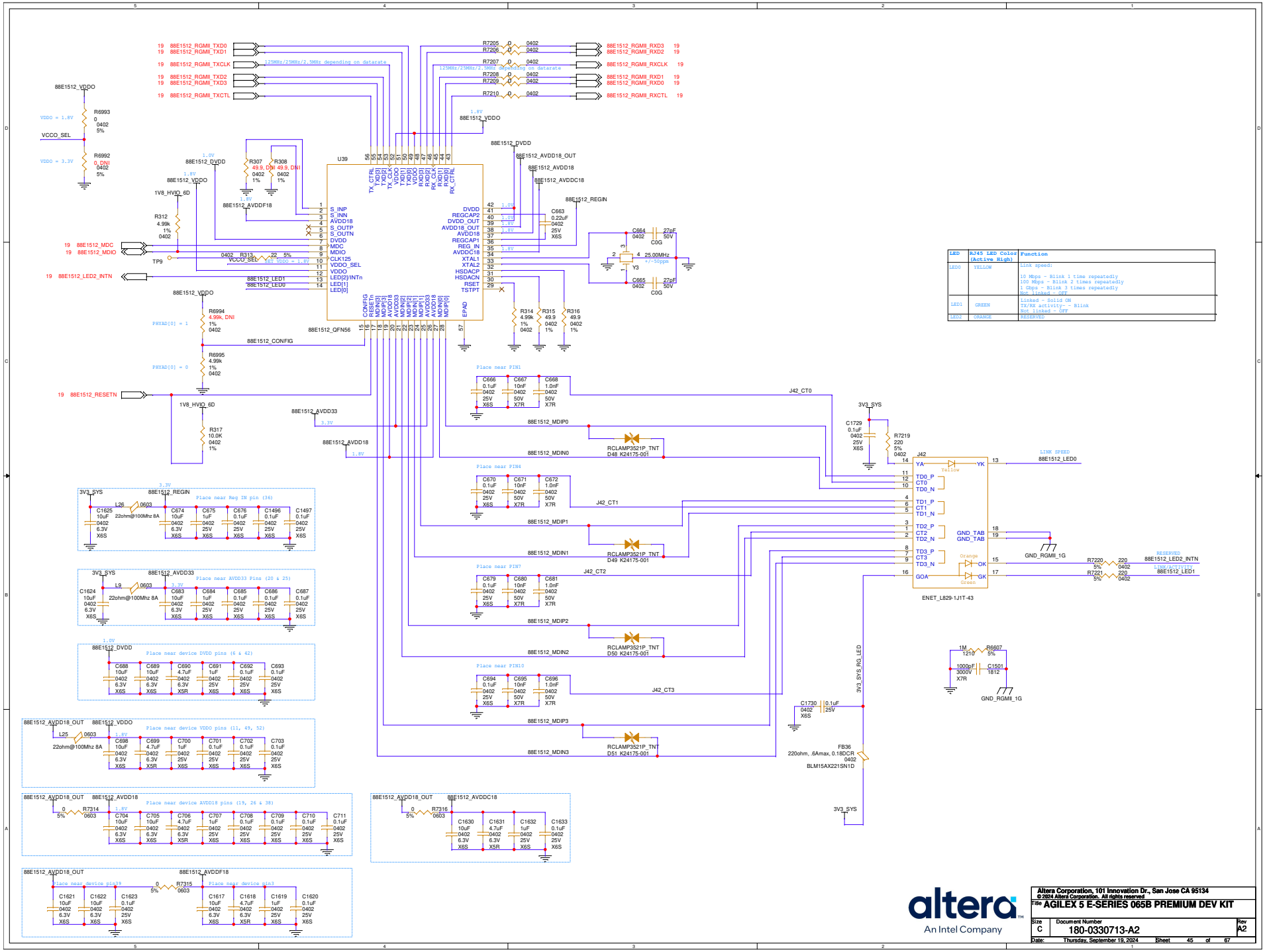
AGILEX 5 E-SERIES 065B PREMIUM DEV KIT
Document Number 180-0330713-A2
Rev A2
Date: Thursday, September 19, 2024
Sheet 44 of 67



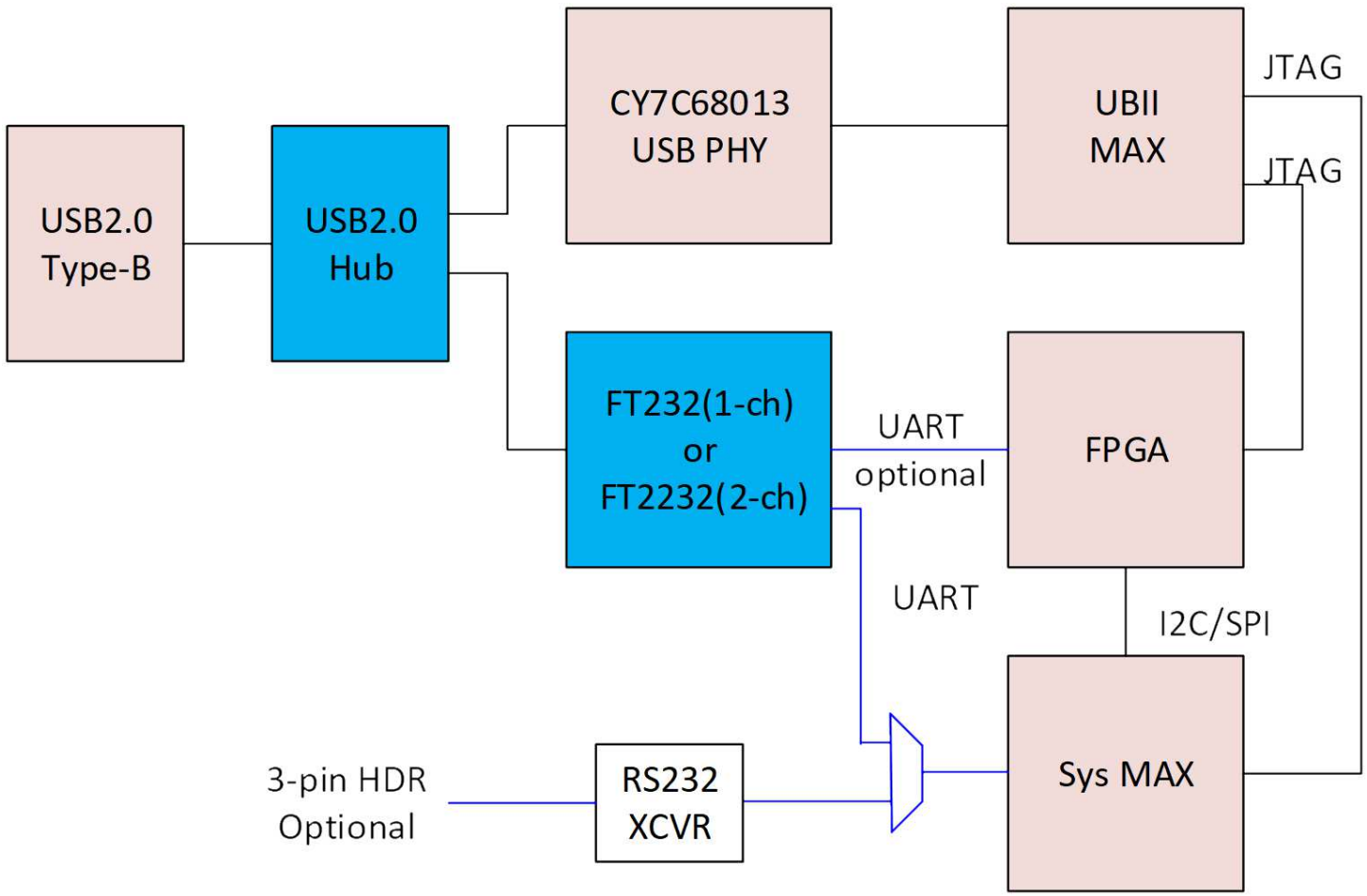
LED	RJ45 LED Color (Active High)	Function
LED0	YELLOW	Link speed: 10 Mbps - Blink 1 time repeatedly 100 Mbps - Blink 2 times repeatedly 1 Gbps - Blink 3 times repeatedly Not linked - OFF
LED1	GREEN	Linked - Solid ON TX/RX activity- - Blink Not linked - OFF
LED2	ORANGE	RESERVED

Altera Corporation, 101 Innovation Dr., San Jose CA 95134

Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

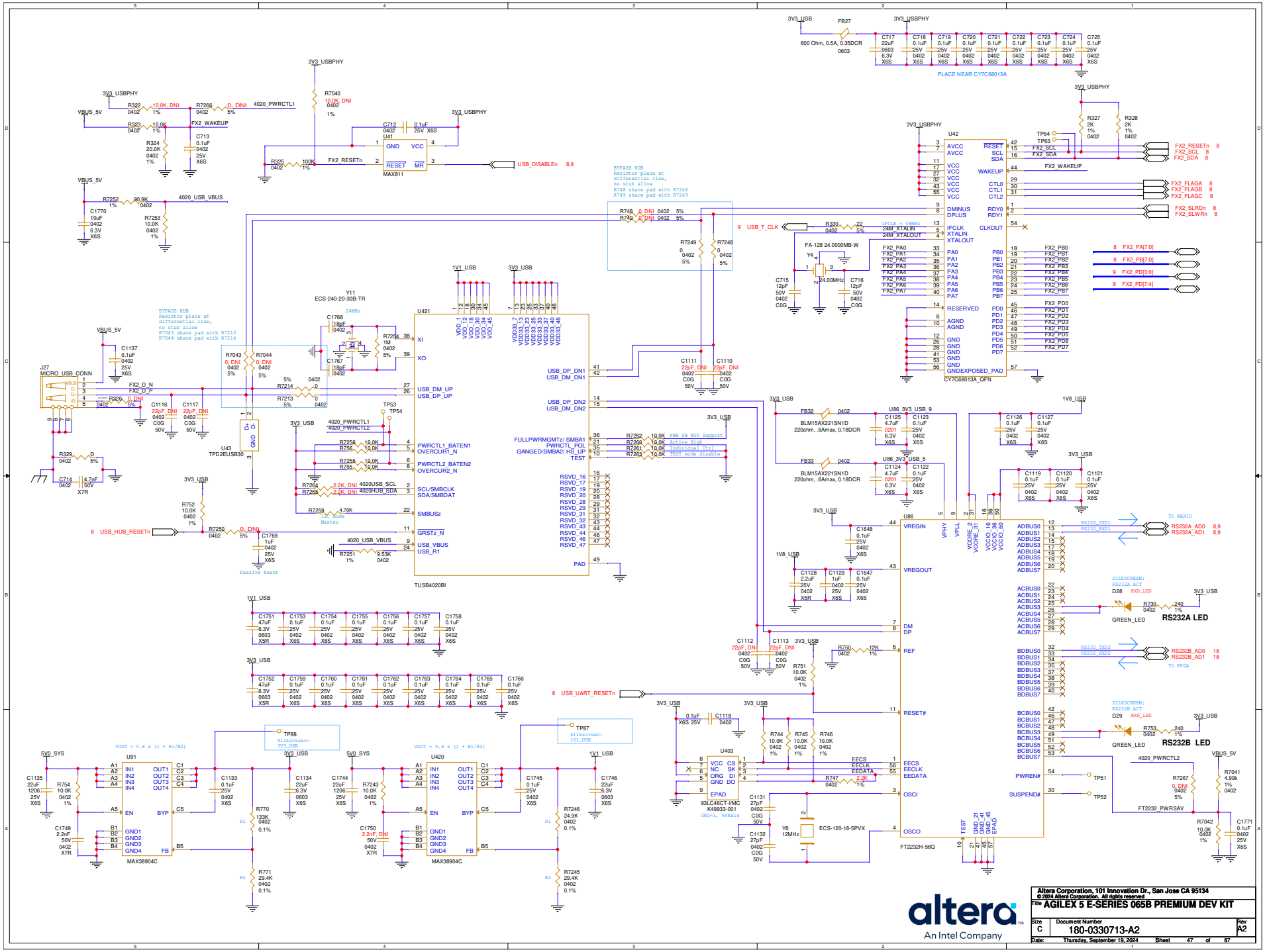
Date: Thursday, September 19, 2024 Sheet 45 of 67



Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 46 of 67



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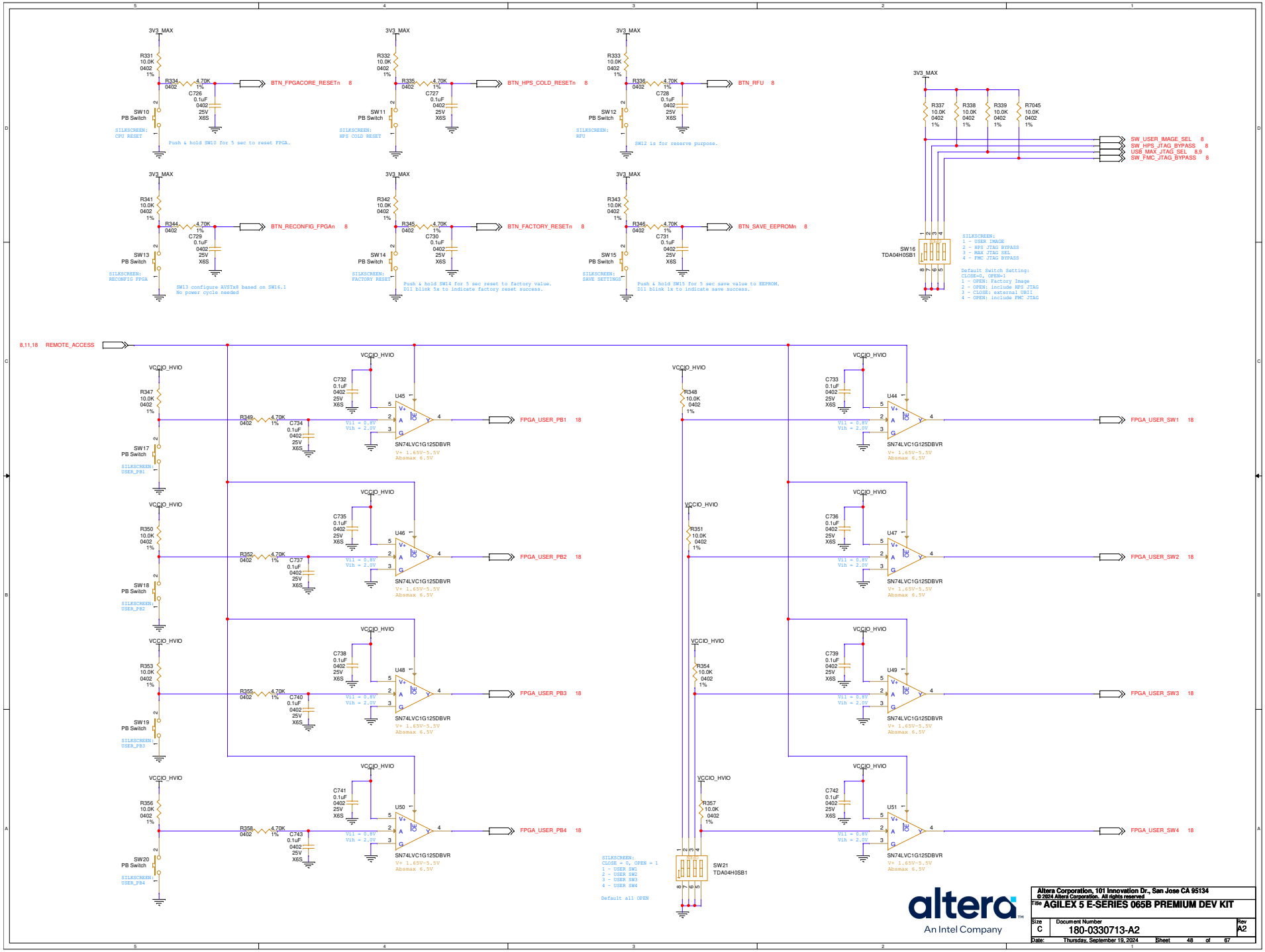
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 47 of 67


3V3_MAX
R331 10.0K 0402 1%
R334 0402 4.70K 1%
C726 0.1uF 0402 25V X6S
SW10 PB Switch
SILKSCREEN: CPU RESET
BTN_FPGACORE_RESETn 8
Push & hold SW10 for 5 sec to reset FPGA.
R332 10.0K 0402 1%
R335 0402 4.70K 1%
C727 0.1uF 0402 25V X6S
SW11 PB Switch
SILKSCREEN: HPS COLD RESET
BTN_HPS_COLD_RESETn 8
R333 10.0K 0402 1%
R336 0402 4.70K 1%
C728 0.1uF 0402 25V X6S
SW12 PB Switch
SILKSCREEN: RFU
BTN_RFU 8
SW12 is for reserve purpose.
R337 10.0K 0402 1%
R338 10.0K 0402 1%
R339 10.0K 0402 1%
R7045 10.0K 0402 1%
SW_USER_IMAGE_SEL 8
SW_HPS_JTAG_BYPASS 8
USB_MAX_JTAG_SEL 8,9
SW_FMC_JTAG_BYPASS 8
SW16 TDA04H0SB1
SILKSCREEN:
1 - USER IMAGE
2 - HPS JTAG BYPASS
3 - MAX JTAG SEL
4 - FMC JTAG BYPASS
Default Switch Setting:
CLOSE=0, OPEN=1
1 - OPEN: Factory Image
2 - OPEN: Include HPS JTAG
3 - CLOSE: external UBII
4 - OPEN: include FMC JTAG
R341 10.0K 0402 1%
R344 0402 4.70K 1%
C729 0.1uF 0402 25V X6S
SW13 PB Switch
SILKSCREEN: RECONFIG FPGA
BTN_RECONFIG_FPGAn 8
SW13 configure AVSTx8 based on SW16.1
No power cycle needed
R342 10.0K 0402 1%
R345 0402 4.70K 1%
C730 0.1uF 0402 25V X6S
SW14 PB Switch
SILKSCREEN: FACTORY RESET
BTN_FACTORY_RESETn 8
Push & hold SW14 for 5 sec reset to factory value.
D11 blink 5x to indicate factory reset success.
R343 10.0K 0402 1%
R346 0402 4.70K 1%
C731 0.1uF 0402 25V X6S
SW15 PB Switch
SILKSCREEN: SAVE SETTINGS
BTN_SAVE_EEPROMn 8
Push & hold SW15 for 5 sec save value to EEPROM.
D11 blink 1x to indicate save success.
8,11,18 REMOTE_ACCESS
VCCIO_HVIO
R347 10.0K 0402 1%
R349 0402 4.70K 1%
C732 0.1uF 0402 25V X6S
C734 0.1uF 0402 25V X6S
SW17 PB Switch
SILKSCREEN: USER_PB1
U45
SN74LVC1G125DBVR
V+ 1.65V-5.5V
Absmax 6.5V
Vil = 0.8V
Vih = 2.0V
FPGA_USER_PB1 18
R350 10.0K 0402 1%
R352 0402 4.70K 1%
C735 0.1uF 0402 25V X6S
C737 0.1uF 0402 25V X6S
SW18 PB Switch
SILKSCREEN: USER_PB2
U46
FPGA_USER_PB2 18
R353 10.0K 0402 1%
R355 0402 4.70K 1%
C738 0.1uF 0402 25V X6S
C740 0.1uF 0402 25V X6S
SW19 PB Switch
SILKSCREEN: USER_PB3
U48
FPGA_USER_PB3 18
R356 10.0K 0402 1%
R358 0402 4.70K 1%
C741 0.1uF 0402 25V X6S
C743 0.1uF 0402 25V X6S
SW20 PB Switch
SILKSCREEN: USER_PB4
U50
FPGA_USER_PB4 18
R348 10.0K 0402 1%
C733 0.1uF 0402 25V X6S
U44
FPGA_USER_SW1 18
R351 10.0K 0402 1%
C736 0.1uF 0402 25V X6S
U47
FPGA_USER_SW2 18
R354 10.0K 0402 1%
C739 0.1uF 0402 25V X6S
U49
FPGA_USER_SW3 18
R357 10.0K 0402 1%
C742 0.1uF 0402 25V X6S
U51
FPGA_USER_SW4 18
SW21 TDA04H0SB1
SILKSCREEN:
CLOSE = 0, OPEN = 1
1 - USER SW1
2 - USER SW2
3 - USER SW3
4 - USER SW4
Default all OPEN
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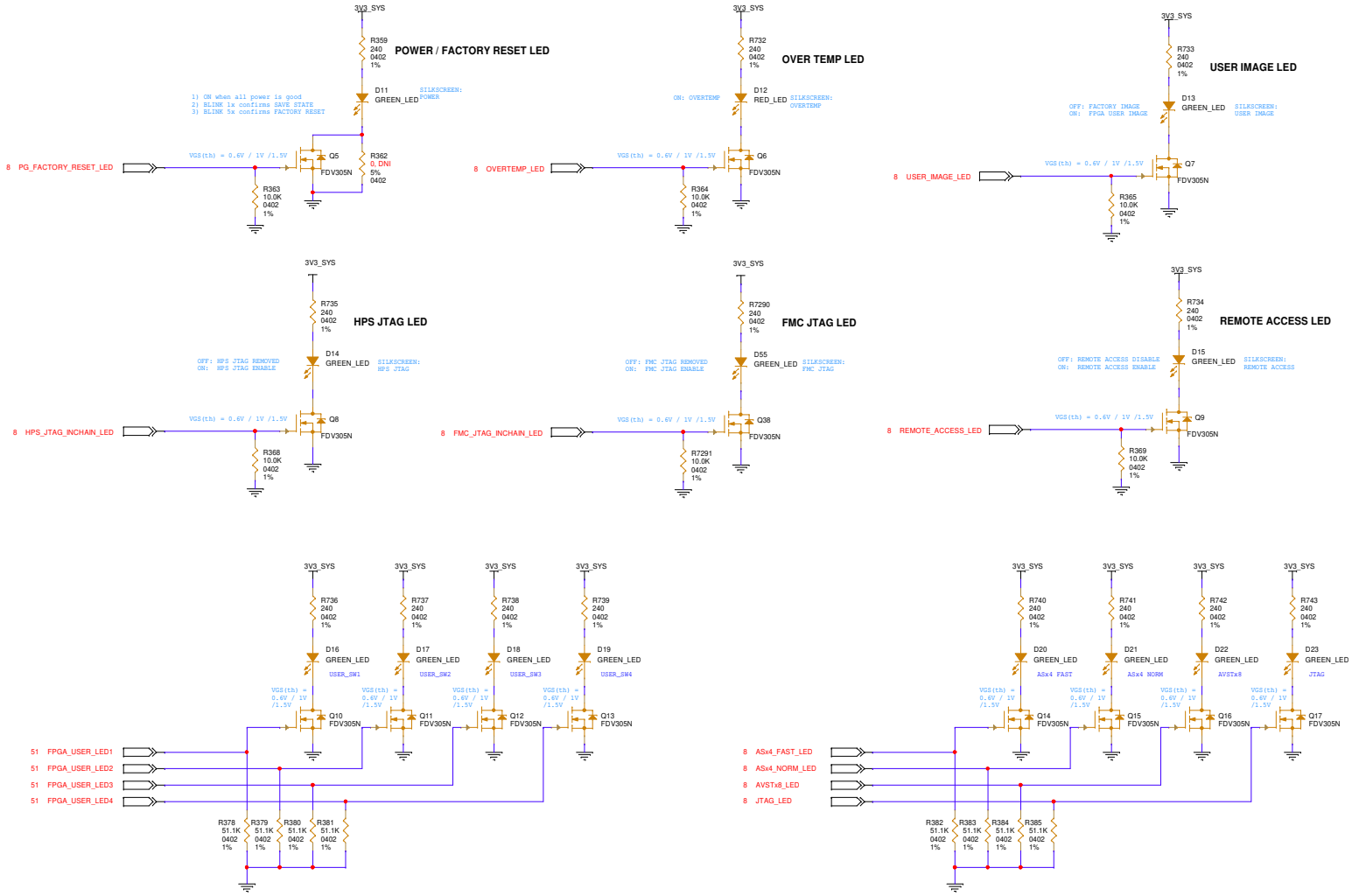
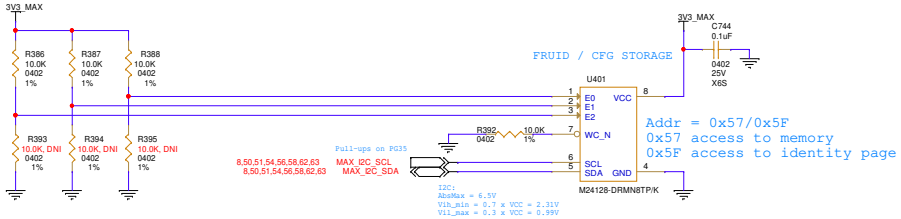
Title AGILEX 5 E-SERIES 065B PREMIUM DEV KIT
Size C
Document Number 180-0330713-A2
Rev A2
Date: Thursday, September 19, 2024
Sheet 48 of 67

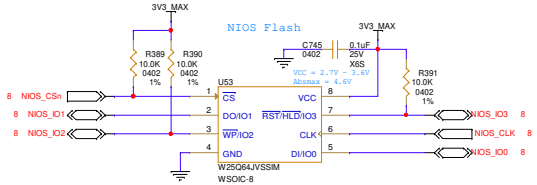


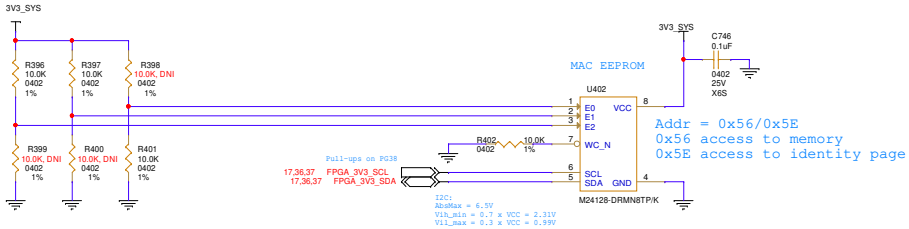
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

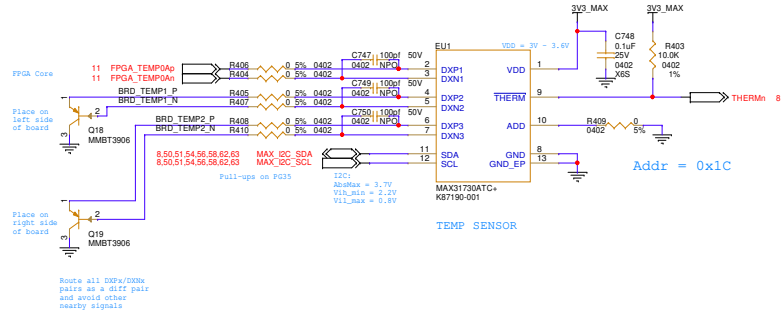
Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 49 of 67





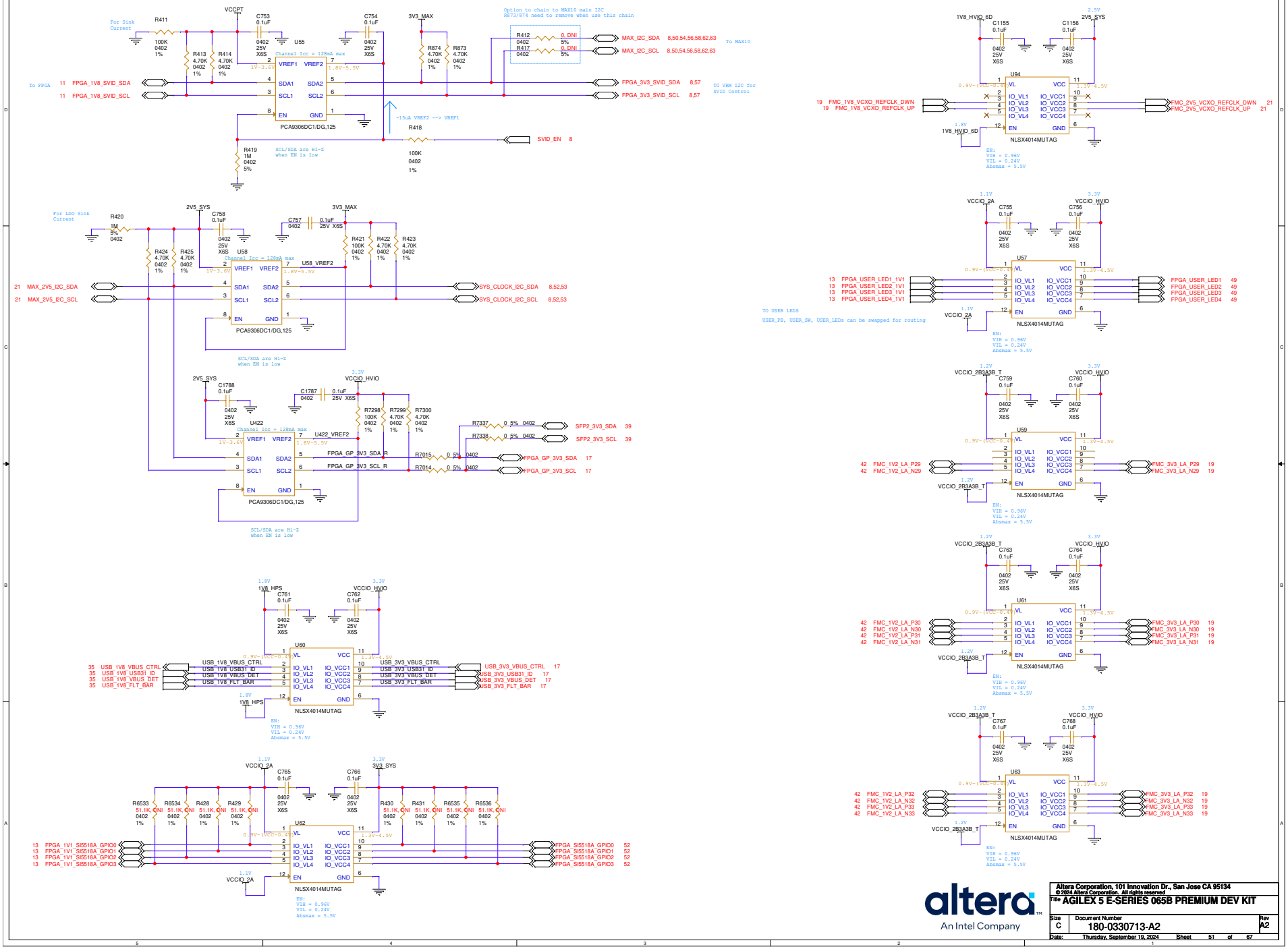




Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 50 of 67



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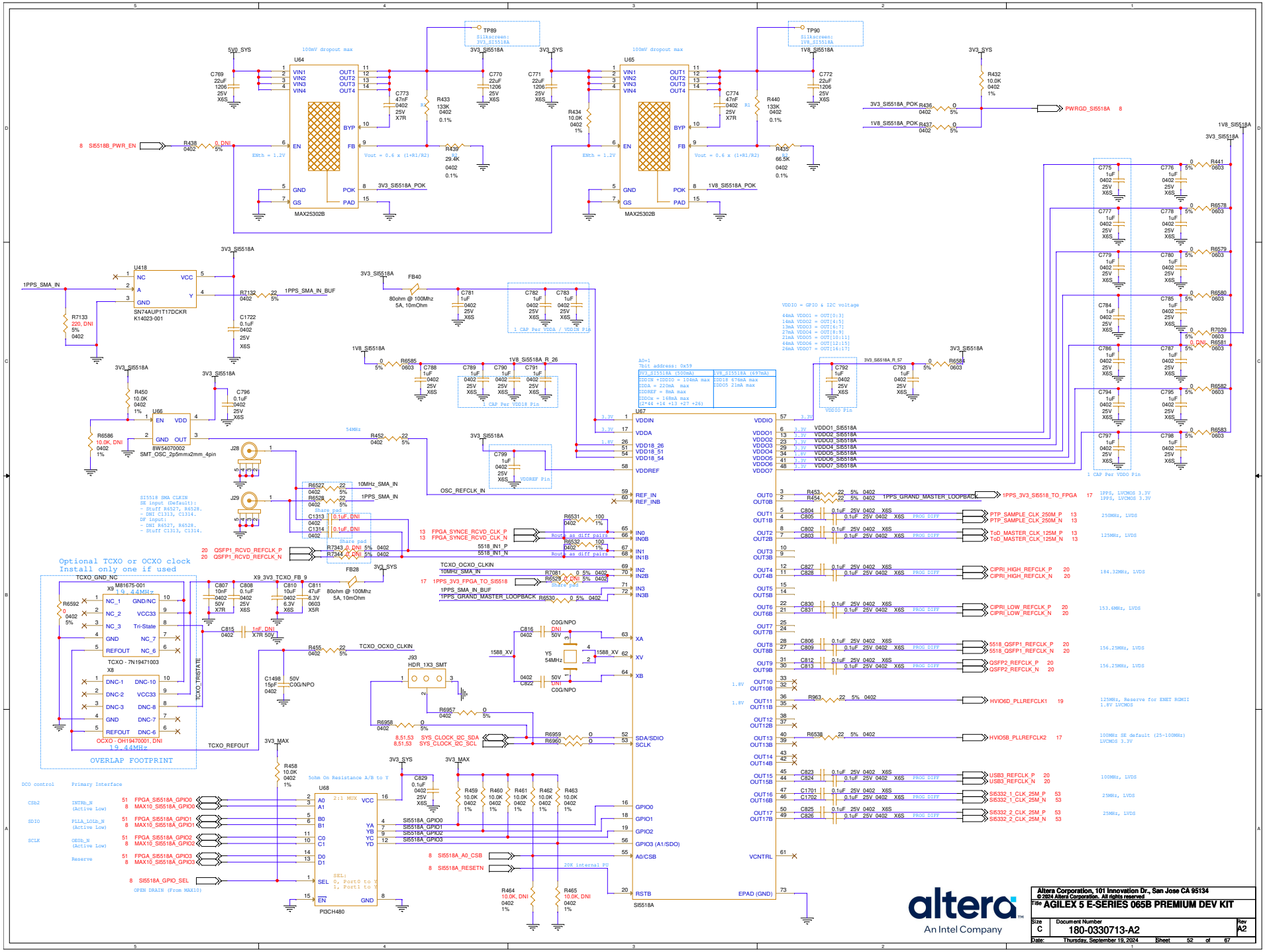
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 51 of 67


5V0_SYS
3V3_SYS
1V8_SI5518A
100mV dropout max
U64
U65
MAX25302B
TP89
TP90
Silkscreen: 3V3_SI5518A
Silkscreen: 1V8_SI5518A
VIN1
VIN2
VIN3
VIN4
OUT1
OUT2
OUT3
OUT4
BYP
FB
EN
GND
GS
POK
PAD
ENth = 1.2V
Vout = 0.6 x (1+R1/R2)
3V3_SI5518A_POK
1V8_SI5518A_POK
PWRGD_SI5518A
SI5518B_PWR_EN
1PPS_SMA_IN
1PPS_SMA_IN_BUF
SN74AUP1T17DCKR
K14023-001
U418
U66
SMT_OSC_2p5mmx2mm_4pin
54MHz
10MHz_SMA_IN
1PPS_SMA_IN
OSC_REFCLK_IN
U67
VDDIN
VDDA
VDD18_26
VDD18_51
VDD18_54
VDDREF
REF_IN
REF_INB
IN0B
IN1B
IN2B
IN3B
SDA/SDIO
SCLK
GPIO0
GPIO1
GPIO2
GPIO3 (A1/SDO)
A0/CSB
RSTB
VCNTRL
EPAD (GND)
SI5518A
VDDIO
VDDO1
VDDO2
VDDO3
VDDO4
VDDO5
VDDO6
VDDO7
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
OUT9
OUT10
OUT11
OUT12
OUT13
OUT14
OUT15
OUT16
OUT17
1 CAP Per VDDO Pin
1 CAP Per VDDA / VDDIN Pin
1 CAP Per VDD18 Pin
VDDREF Pin
VDDIO = GPIO & I2C voltage
44mA VDDO1 = OUT[0:3]
14mA VDDO2 = OUT[4:5]
13mA VDDO3 = OUT[6:7]
27mA VDDO4 = OUT[8:9]
21mA VDDO5 = OUT[10:11]
44mA VDDO6 = OUT[12:15]
26mA VDDO7 = OUT[16:17]
A0=1
7bit address: 0x59
3V3_SI5518A (500mA)
IVDDIN +IVDDIO = 176mA max
IVDDA = 220mA max
IVDDREF = 6mA max
IVDDx = 16mA max
(2*44 +14 +13 +27 +26)
1V8_SI5518A (697mA)
IVDD18 676mA max
IVDDO5 21mA max
SI5518 SMA CLKIN
SE input (Default):
- Stuff R6527, R6528.
- DNI C1313, C1314.
DF input:
- DNI R6527, R6528.
- Stuff C1313, C1314.
Share pad
Route as diff pairs
FPGA_SYNCE_RCVD_CLK_P
FPGA_SYNCE_RCVD_CLK_N
QSFP1_RCVD_REFCLK_P
QSFP1_RCVD_REFCLK_N
5518_IN1_P
5518_IN1_N
TCXO_OCXO_CLKIN
1PPS_3V3_FPGA_TO_SI5518
1PPS_GRAND_MASTER_LOOPBACK
Optional TCXO or OCXO clock
Install only one if used
TCXO_GND_NC
M81675-001
19.44MHz
TCXO - 7N19471003
OCXO - OH19470001, DNI
OVERLAP FOOTPRINT
TCXO_TRISTATE
TCXO_REFOUT
X9_3V3_TCXO_FB_9
FB28
80ohm @ 100Mhz
5A, 10mOhm
J93
HDR_1X3_SMT
Y5
54MHz
1588_XV
XA
XV
XB
C0G/NPO
3V3_MAX
U68
PI3CH480
2:1 MUX
SEL: 0, Port0 to Y; 1, Port1 to Y
50ohm On Resistance A/B to Y
20K internal PU
SI5518A_GPIO0
SI5518A_GPIO1
SI5518A_GPIO2
SI5518A_GPIO3
SI5518A_A0_CSB
SI5518A_RESETN
SI5518A_GPIO_SEL
OPEN DRAIN (From MAX10)
DCO control
Primary Interface
CSb2
SDIO
SCLK
Reserve
INTRb_N (Active Low)
PLLA_LOLb_N (Active Low)
OEOb_N (Active Low)
FPGA_SI5518A_GPIO0
MAX10_SI5518A_GPIO0
FPGA_SI5518A_GPIO1
MAX10_SI5518A_GPIO1
FPGA_SI5518A_GPIO2
MAX10_SI5518A_GPIO2
FPGA_SI5518A_GPIO3
MAX10_SI5518A_GPIO3
SYS_CLOCK_I2C_SCL
SYS_CLOCK_I2C_SDA
PTP_SAMPLE_CLK_250M_P
PTP_SAMPLE_CLK_250M_N
ToD_MASTER_CLK_125M_P
ToD_MASTER_CLK_125M_N
CIPRI_HIGH_REFCLK_P
CIPRI_HIGH_REFCLK_N
CIPRI_LOW_REFCLK_P
CIPRI_LOW_REFCLK_N
5518_QSFP1_REFCLK_P
5518_QSFP1_REFCLK_N
QSFP2_REFCLK_P
QSFP2_REFCLK_N
HVIO6D_PLLREFCLK1
HVIO5B_PLLREFCLK2
USB3_REFCLK_P
USB3_REFCLK_N
SI5332_1_CLK_25M_P
SI5332_1_CLK_25M_N
SI5332_2_CLK_25M_P
SI5332_2_CLK_25M_N
PROG DIFF
1PPS_GRAND_MASTER_LOOPBACK
1PPS_3V3_SI5518_TO_FPGA
1PPS, LVCMOS 3.3V
250MHz, LVDS
125MHz, LVDS
184.32MHz, LVDS
153.6MHz, LVDS
156.25MHz, LVDS
125MHz, Reserve for ENET RGMII 1.8V LVCMOS
100MHz SE default (25-100MHz) LVCMOS 3.3V
100MHz, LVDS
25MHz, LVDS
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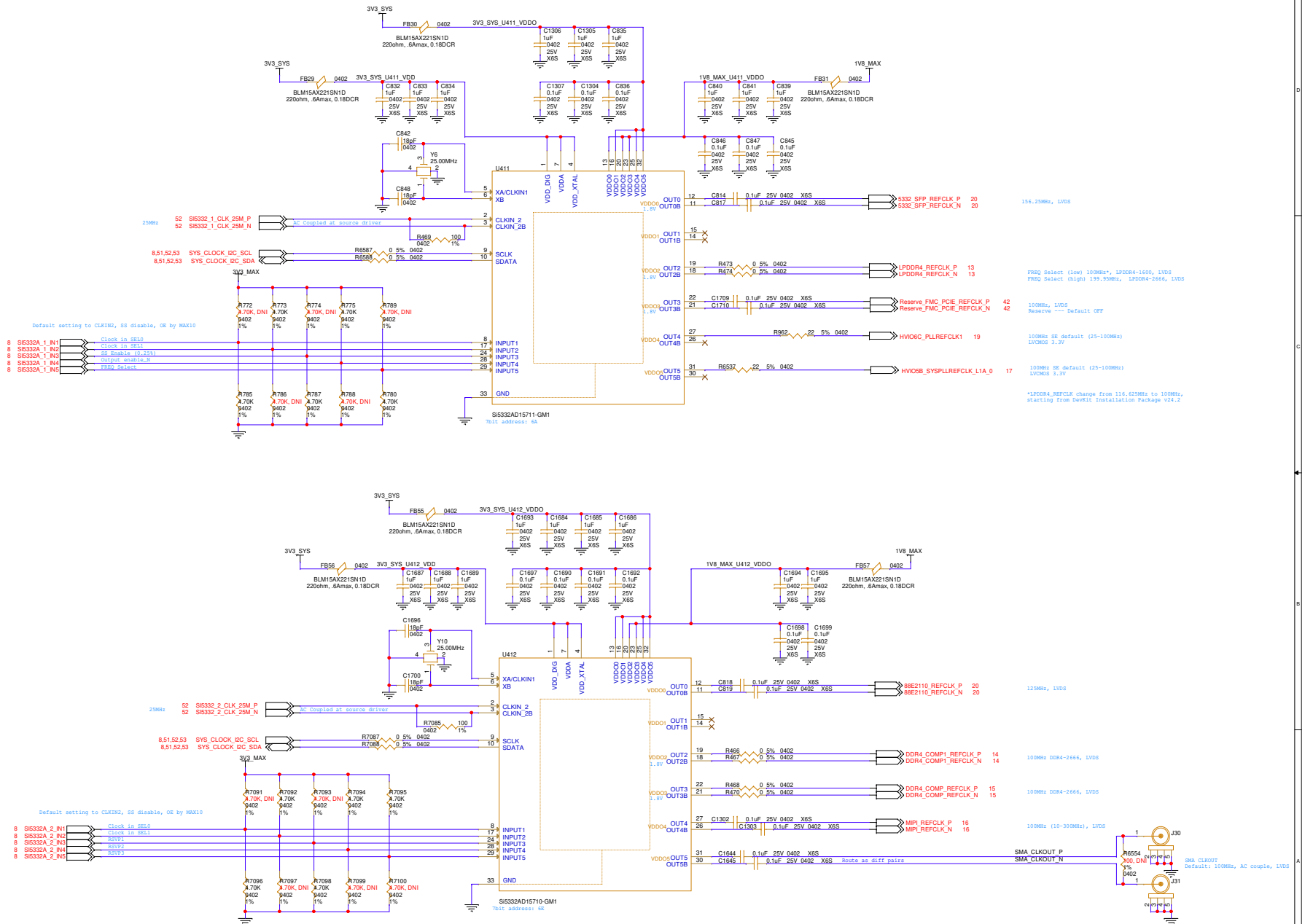
Title AGILEX 5 E-SERIES 065B PREMIUM DEV KIT
Size C
Document Number 180-0330713-A2
Rev A2
Date: Thursday, September 19, 2024
Sheet 52 of 67



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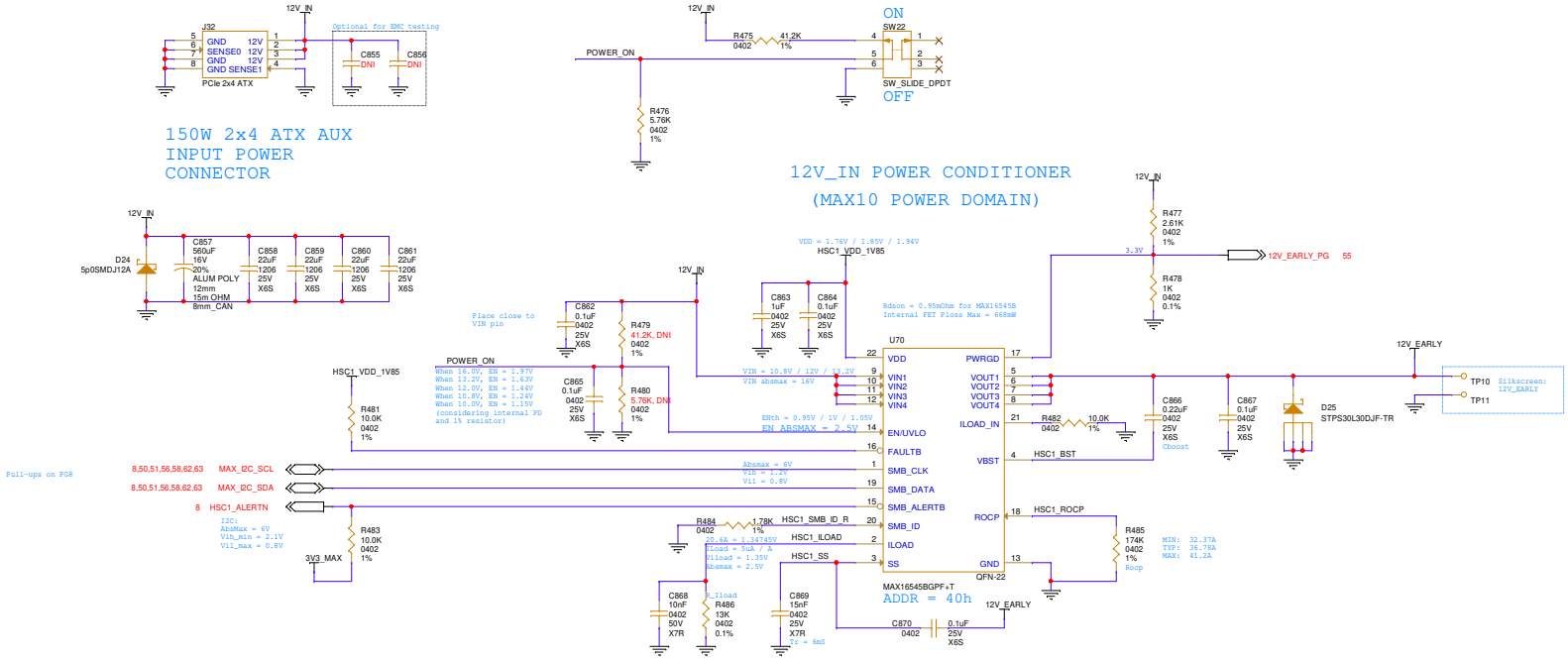
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 53 of 67

Power On Switch



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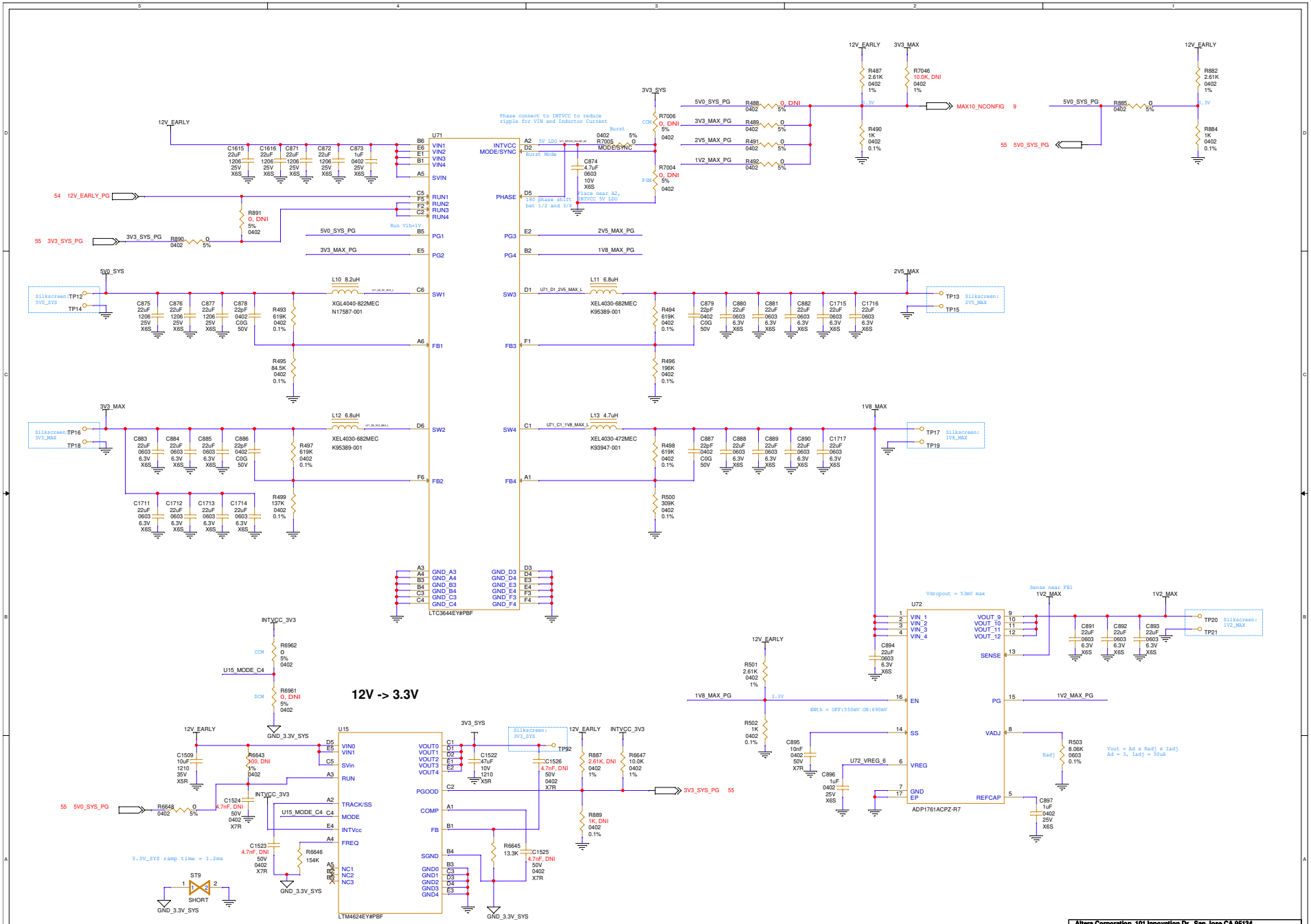
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT		
Size: C	Document Number: 180-0330713-A2	Rev: A2
Date: Thursday, September 19, 2024	Sheet 54 of 67	



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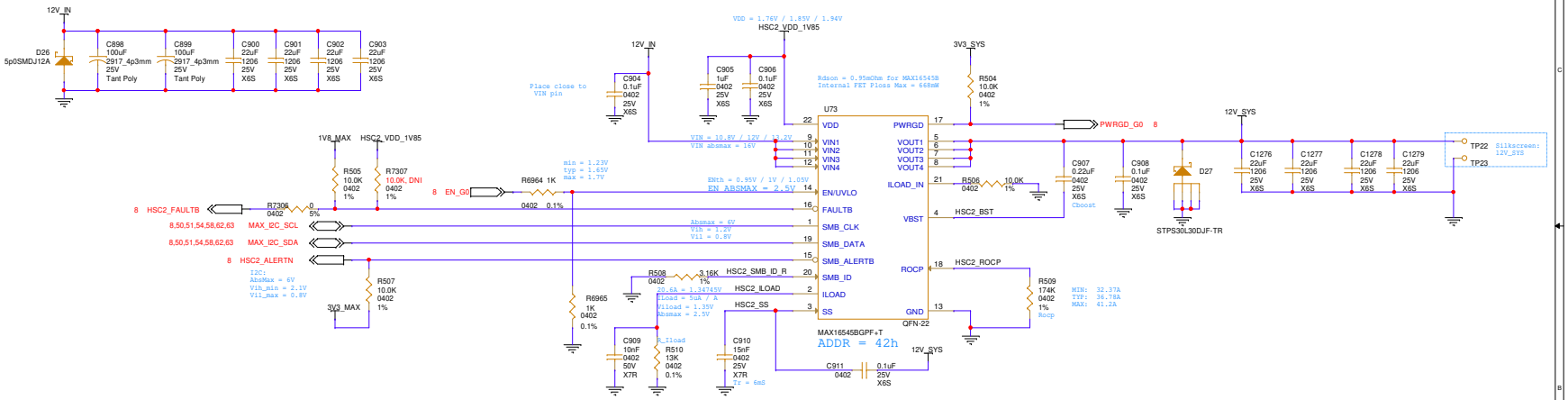
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 55 of 67



12V_SYS POWER CONDITIONER
(FPGA POWER DOMAIN)

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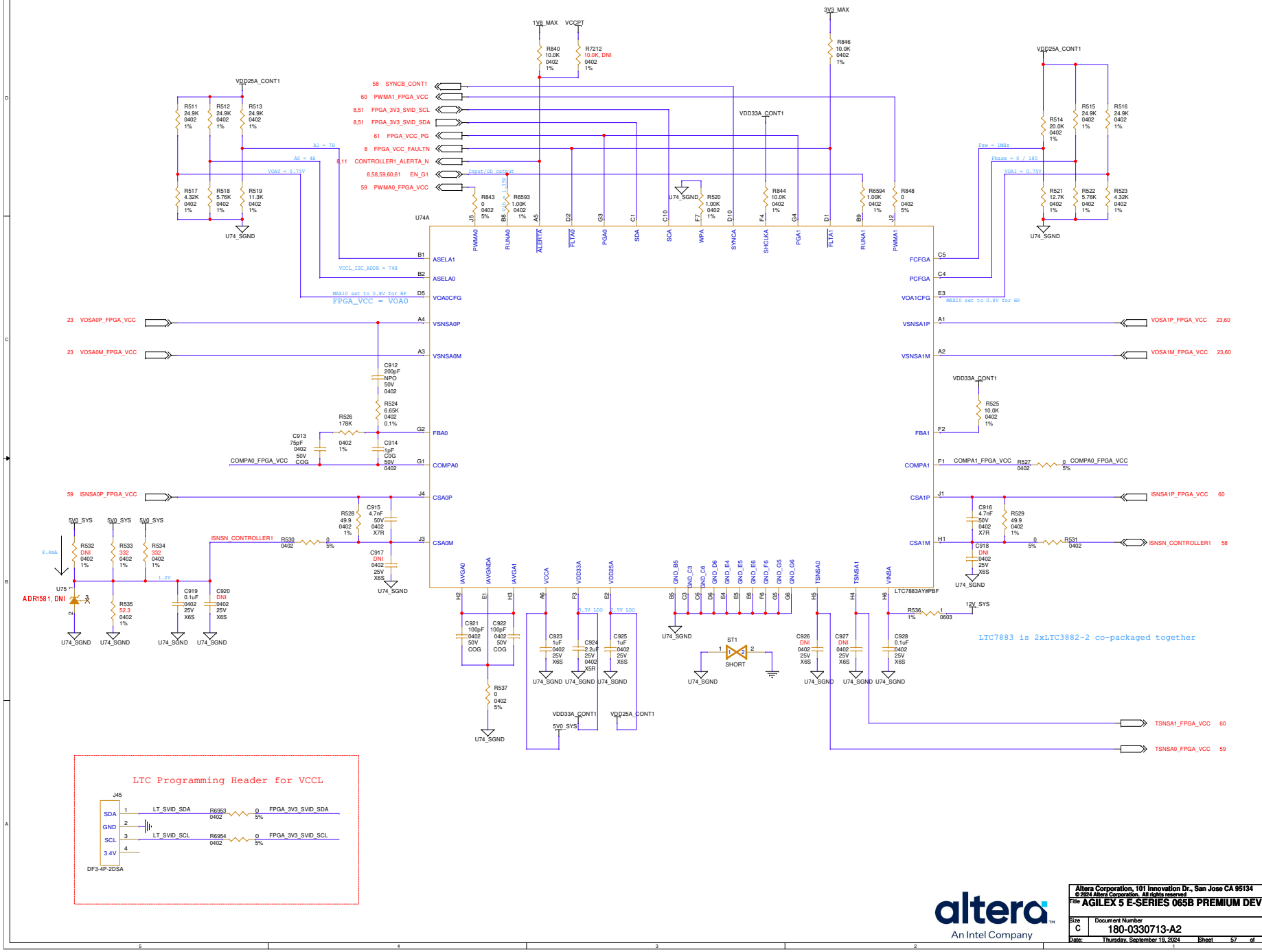
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 56 of 67


LTC Programming Header for VCCL
J45
SDA
GND
SCL
3.4V
DF3-4P-2DSA
LT_SVID_SDA
LT_SVID_SCL
R6953 0402 0 5%
R6954 0402 0 5%
FPGA_3V3_SVID_SDA
FPGA_3V3_SVID_SCL
U74A
LTC7883AY#PBF
LTC7883 is 2xLTC3882-2 co-packaged together
FPGA_VCC = VOA0
ADR1581, DNI
SHORT
ST1
U74_SGND
VDD25A_CONT1
VDD33A_CONT1
3V3_MAX
1V8_MAX
VCCPT
5V0_SYS
12V_SYS
VOSA0P_FPGA_VCC
VOSA0M_FPGA_VCC
VOSA1P_FPGA_VCC
VOSA1M_FPGA_VCC
ISNSA0P_FPGA_VCC
ISNSA1P_FPGA_VCC
ISNSN_CONTROLLER1
TSNSA1_FPGA_VCC
TSNSA0_FPGA_VCC
COMPA0_FPGA_VCC
COMPA1_FPGA_VCC
SYNCB_CONT1
PWMA1_FPGA_VCC
FPGA_3V3_SVID_SCL
FPGA_3V3_SVID_SDA
FPGA_VCC_PG
FPGA_VCC_FAULTN
CONTROLLER1_ALERTA_N
EN_G1
PWMA0_FPGA_VCC
VCCL_I2C_ADDR = 74H
MAX10 set to 0.8V for HP
Fsw = 1MHz
Phase = 0 / 180
VOA0 = 0.75V
VOA1 = 0.75V
A1 = 7H
A0 = 4H
Input/OD output
ASELA1
ASELA0
VOA0CFG
VOA1CFG
VSNSA0P
VSNSA0M
VSNSA1P
VSNSA1M
FBA0
FBA1
COMPA0
COMPA1
CSA0P
CSA0M
CSA1P
CSA1M
FCFGA
PCFGA
PWMA0
RUNA0
ALERTA
FLTA0
PGA0
SDA
SCA
WPA
SYNCA
SHCLKA
PGA1
FLTA1
RUNA1
PWMA1
AVGA0
AVGNDA
AVGA1
VCCA
VDD33A
VDD25A
GND_B5
GND_C3
GND_C5
GND_D6
GND_E4
GND_E5
GND_E6
GND_F6
GND_G5
GND_G6
TSNSA0
TSNSA1
VINSA
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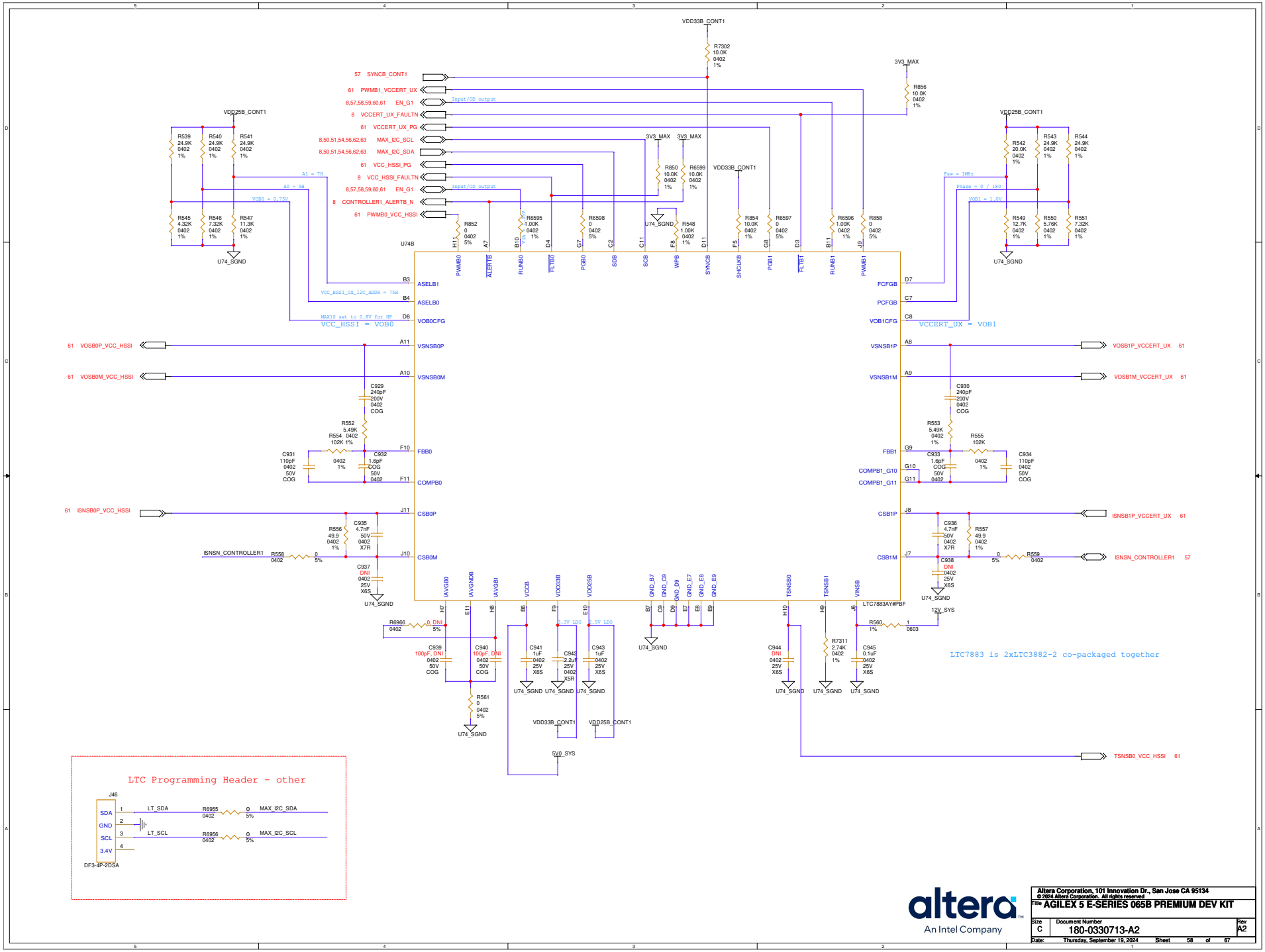
Title AGILEX 5 E-SERIES 065B PREMIUM DEV KIT
Size C
Document Number 180-0330713-A2
Rev A2
Date: Thursday, September 19, 2024
Sheet 57 of 67



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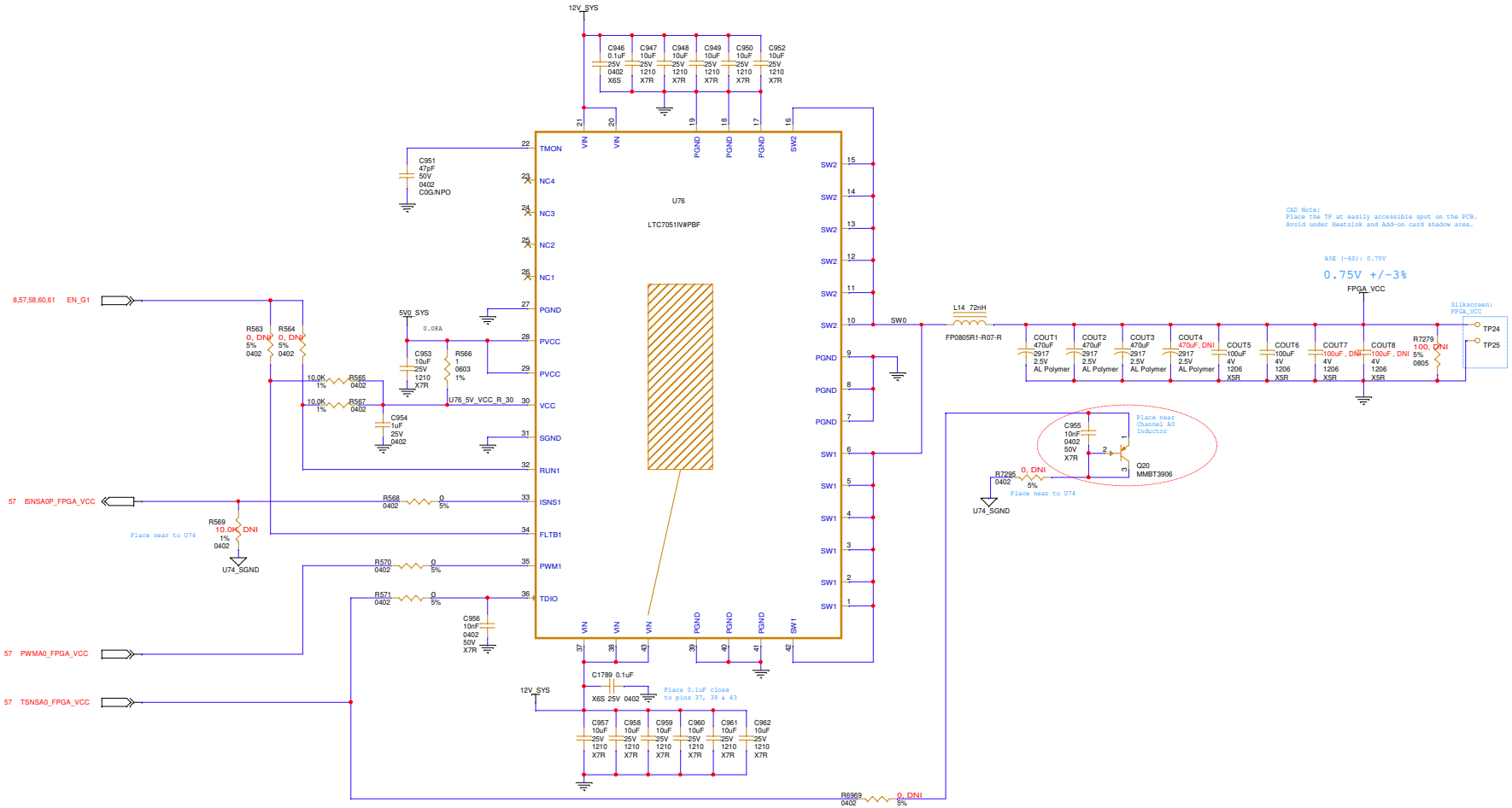
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 58 of 67



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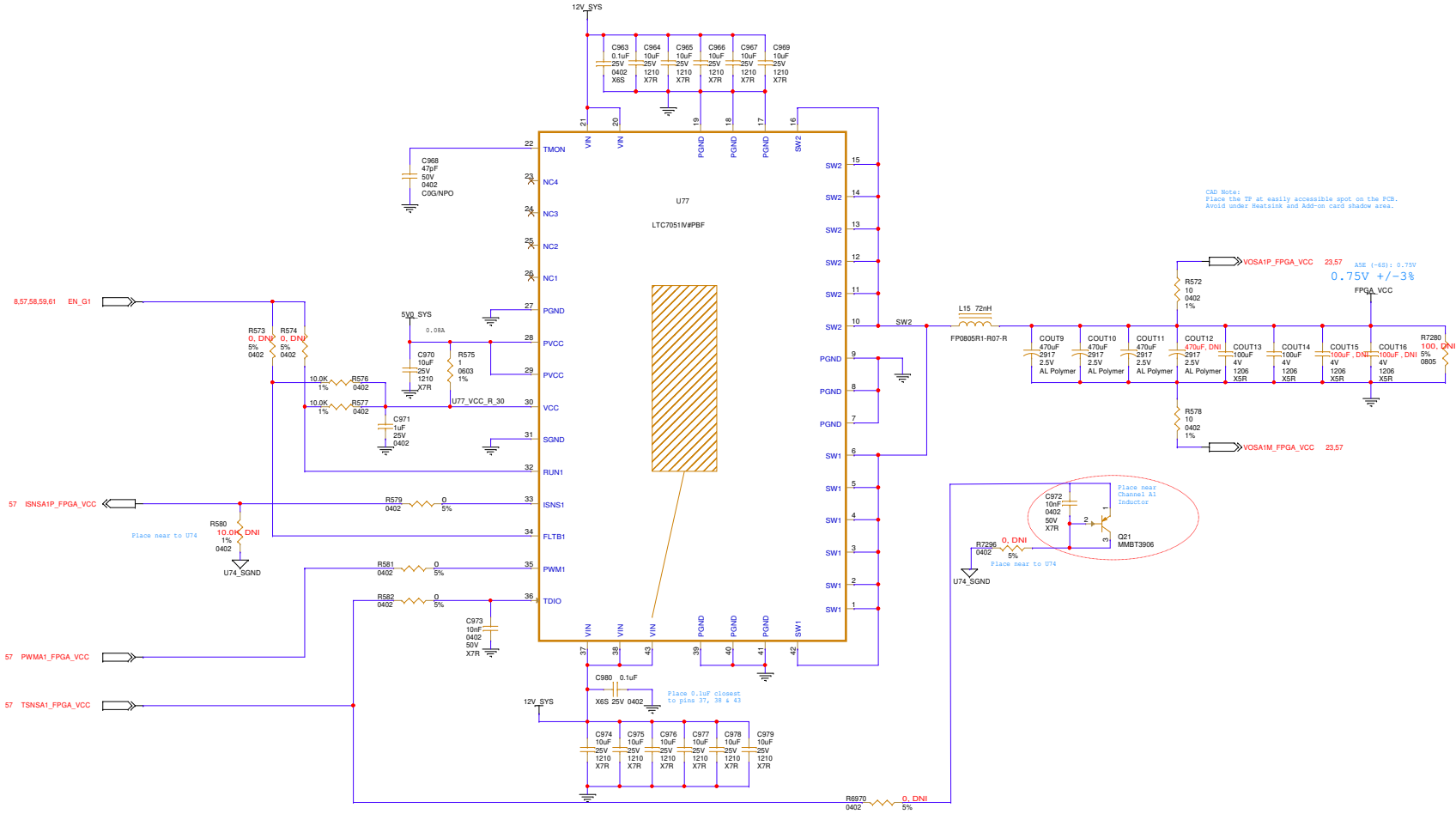
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 59 of 67



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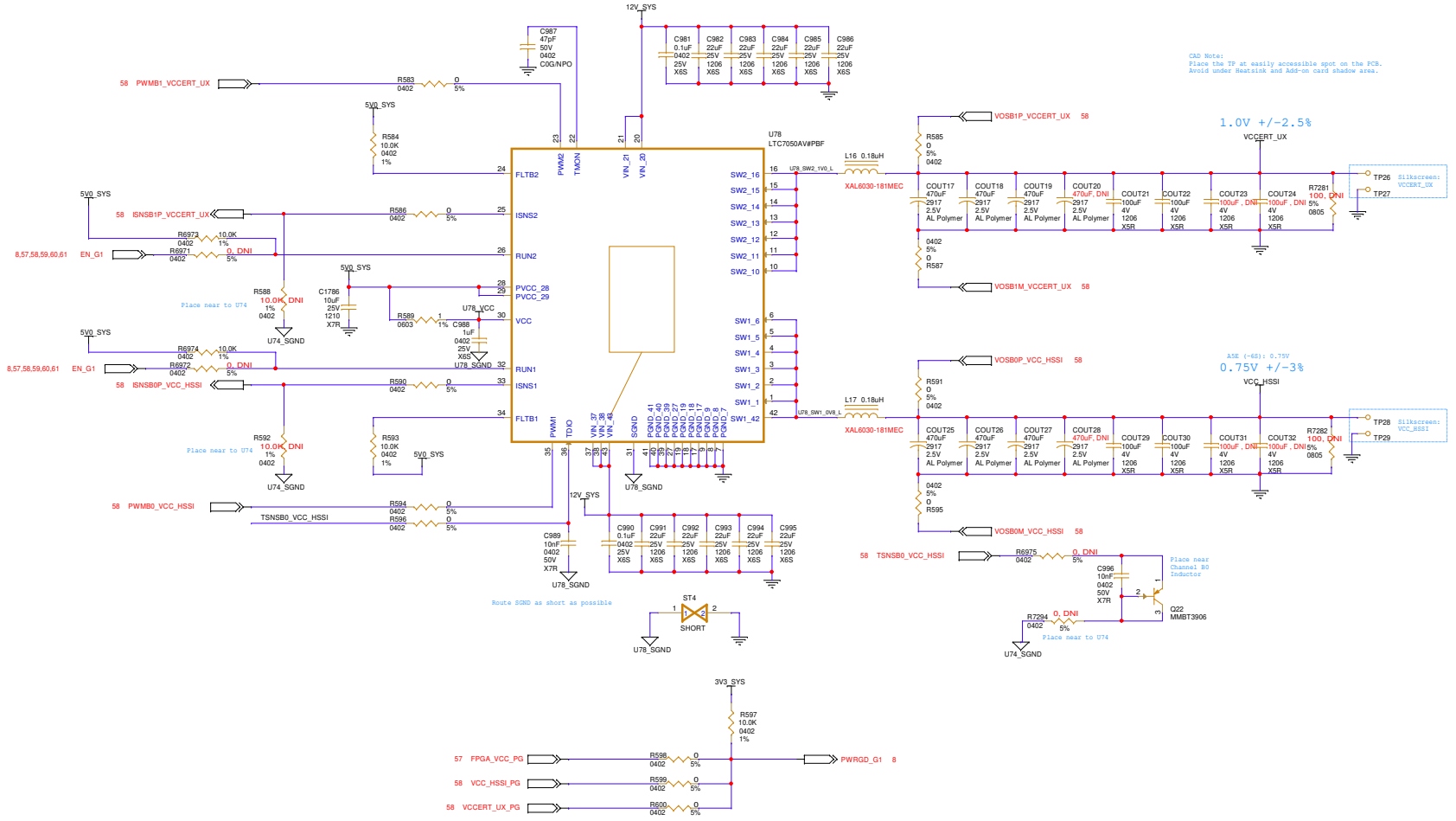
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

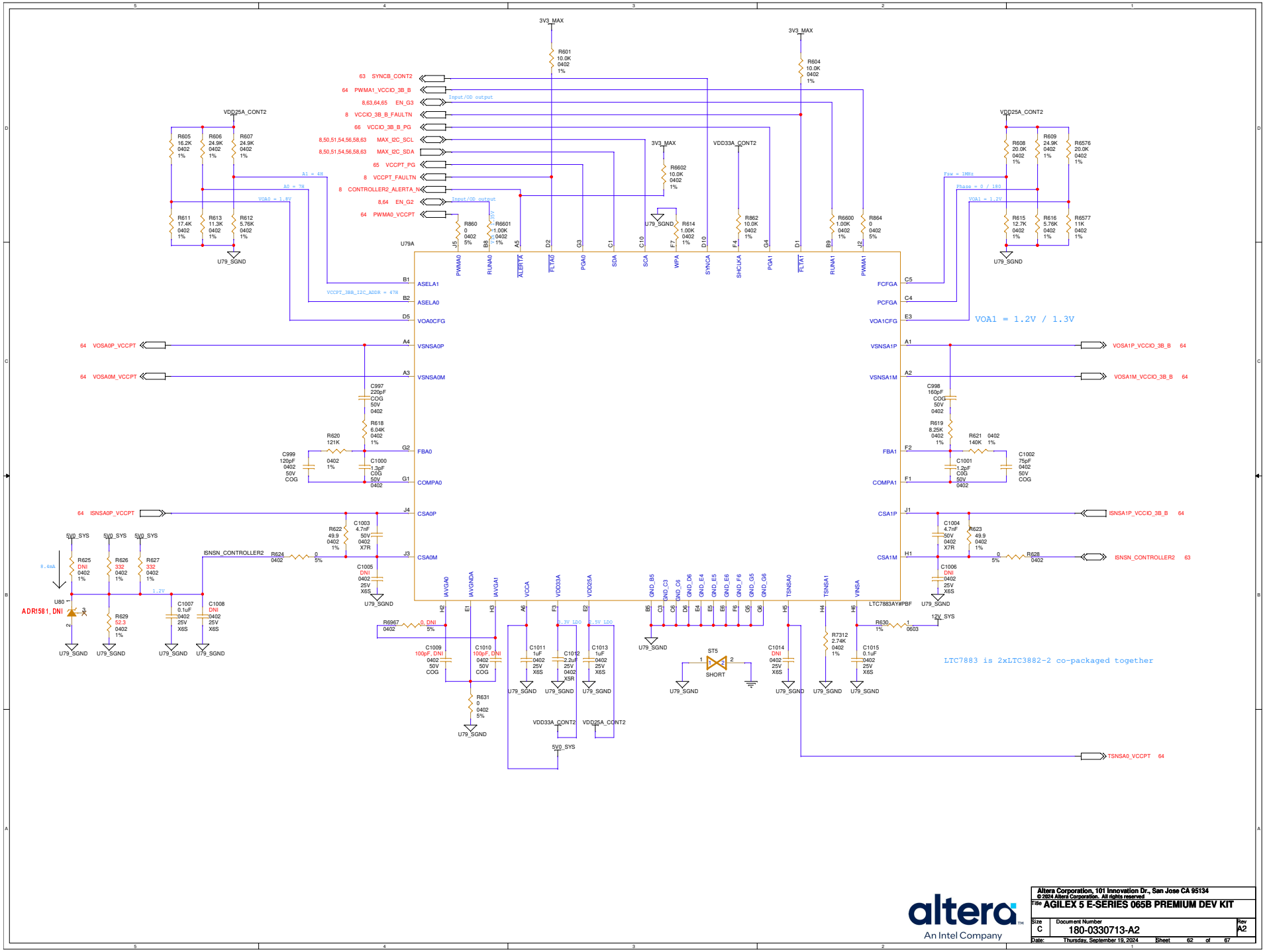
Date: Thursday, September 19, 2024 Sheet 60 of 67



Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 61 of 67



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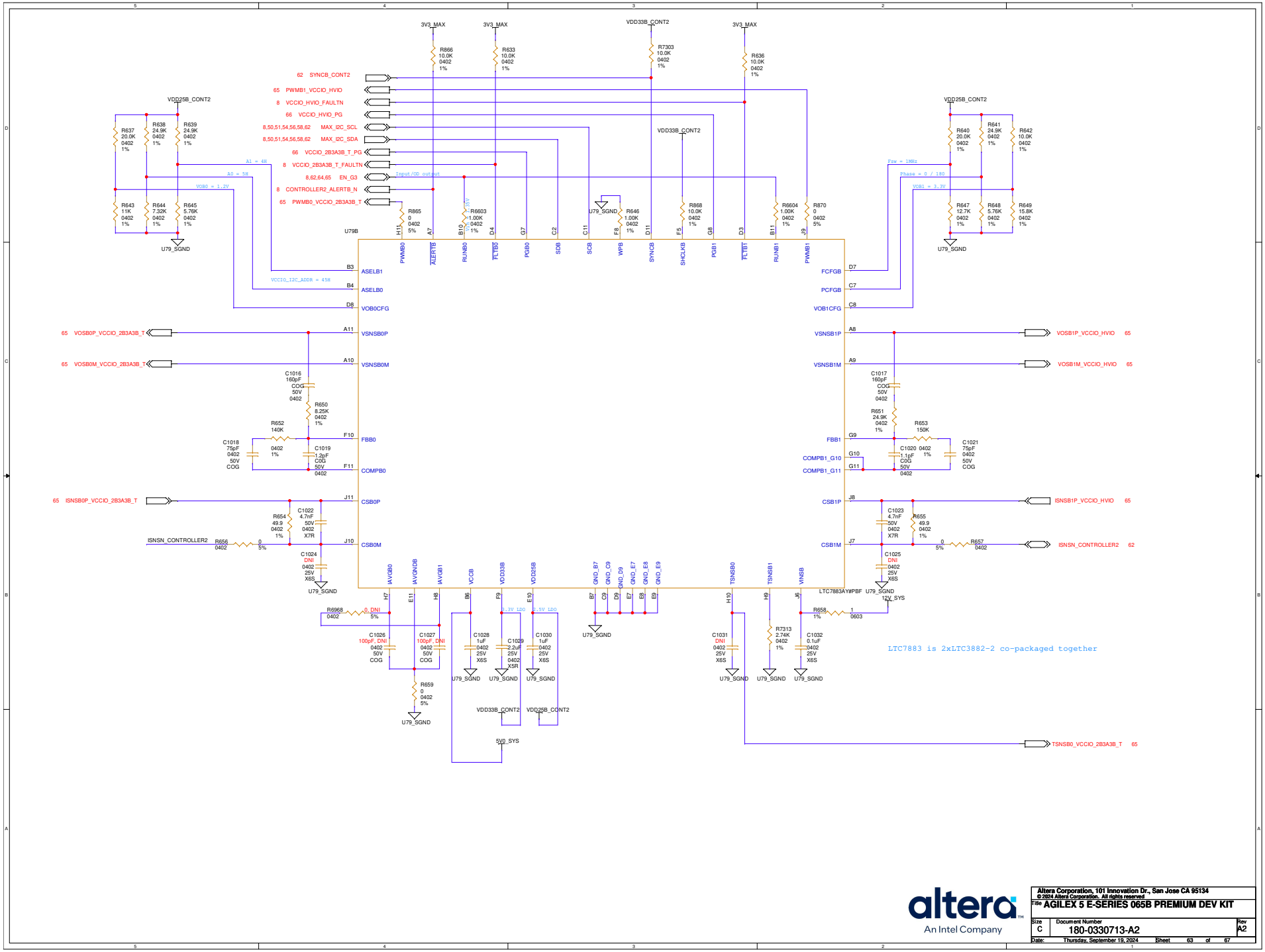
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 62 of 67



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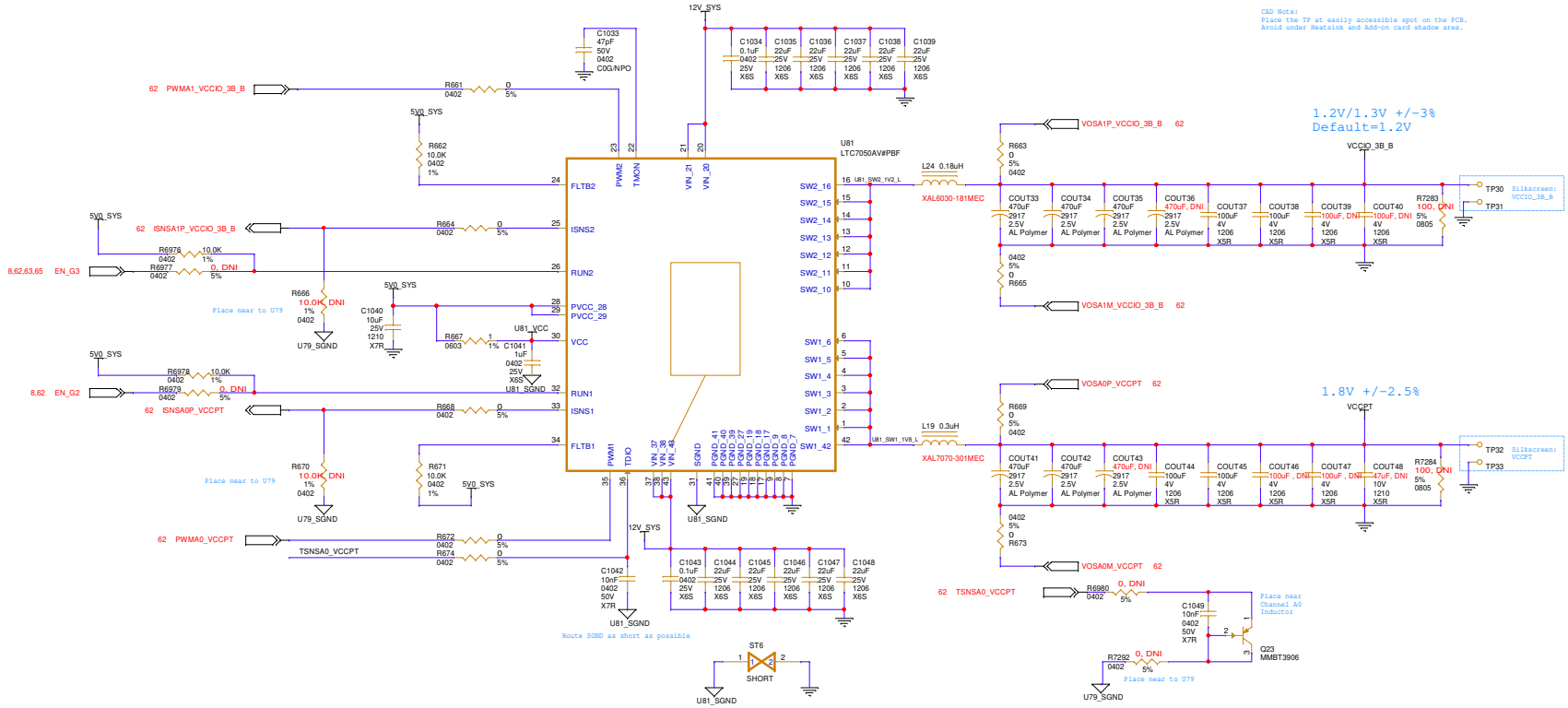
Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 63 of 67



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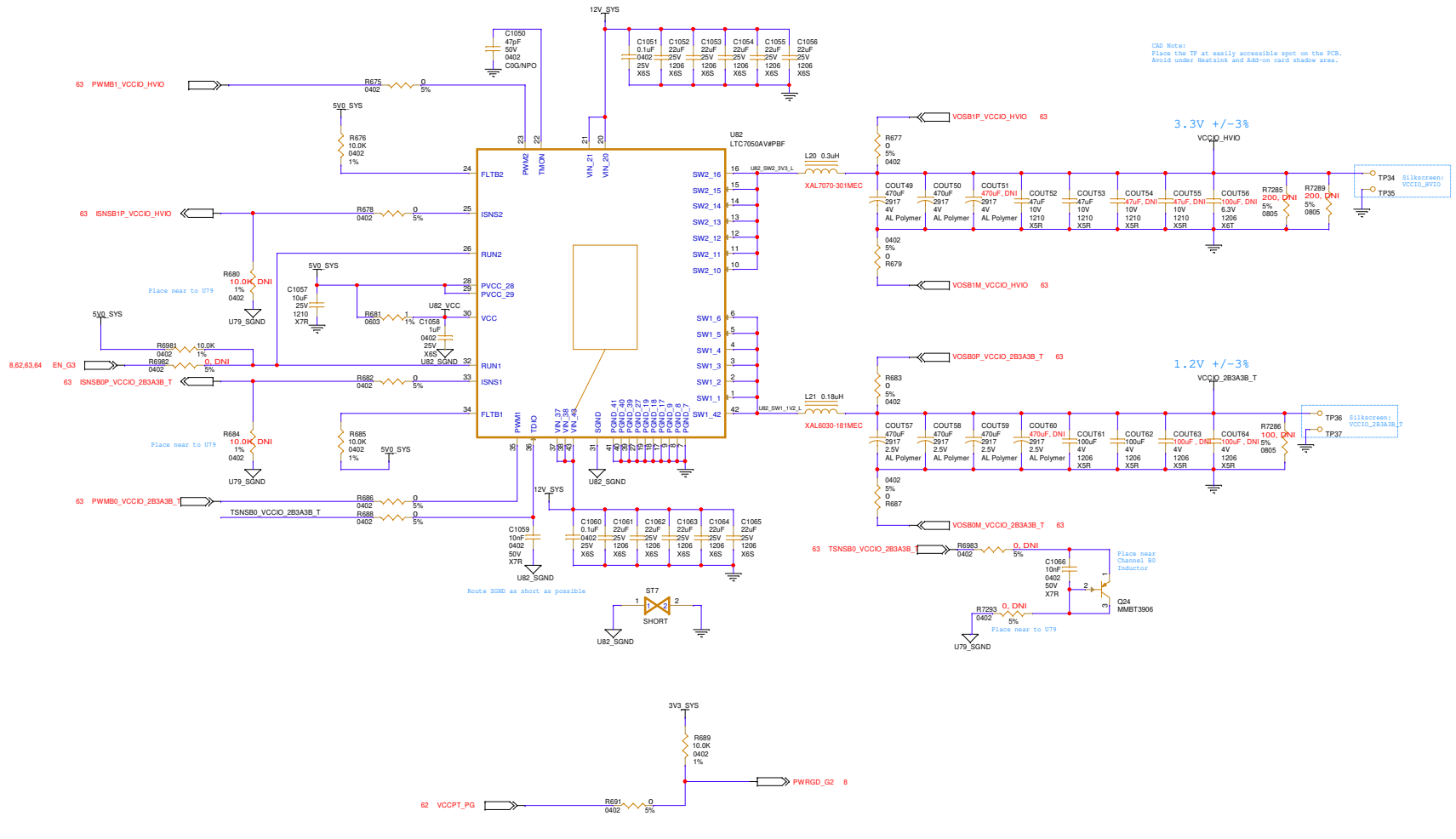
Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 64 of 67



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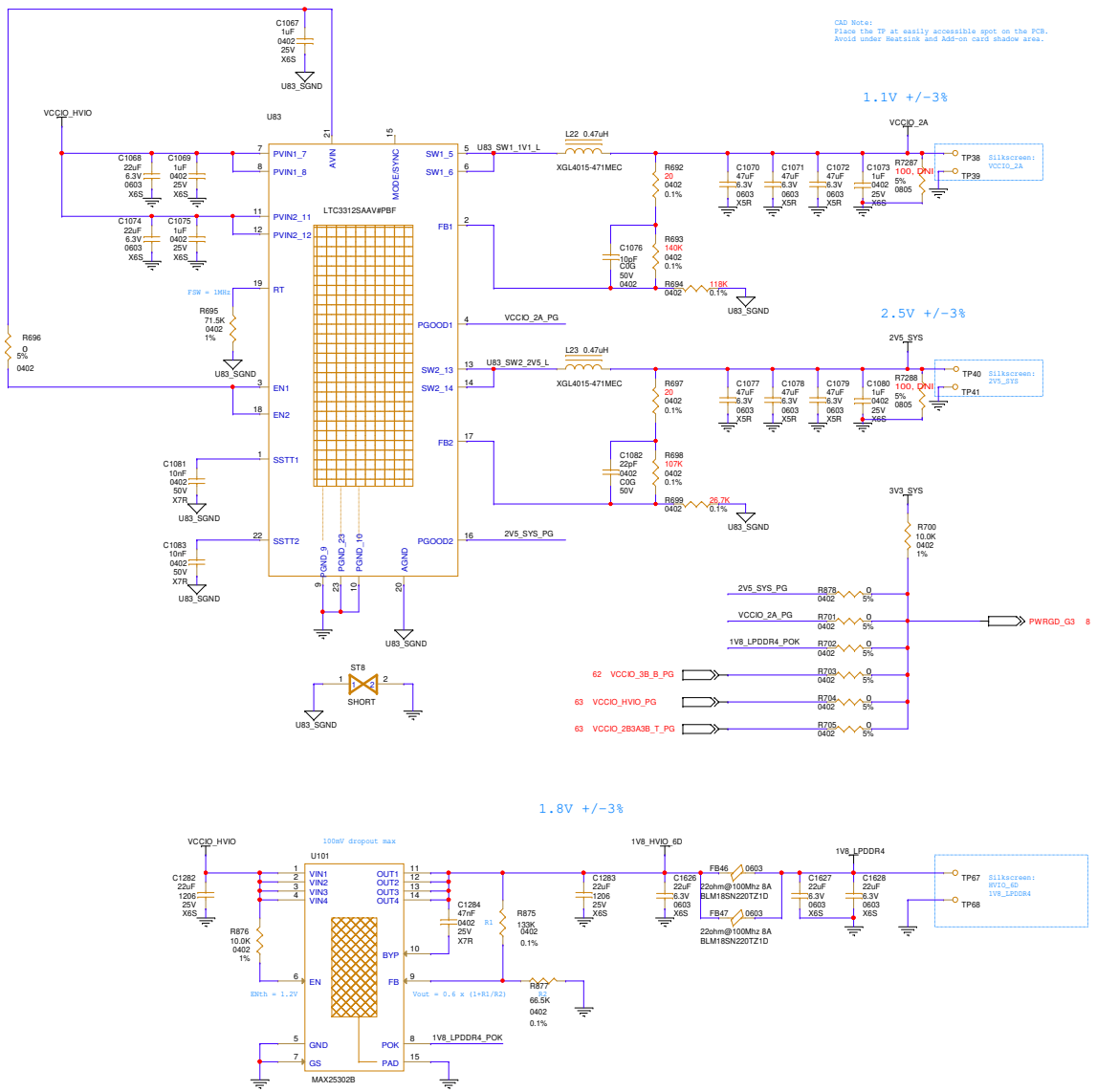
Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 65 of 67

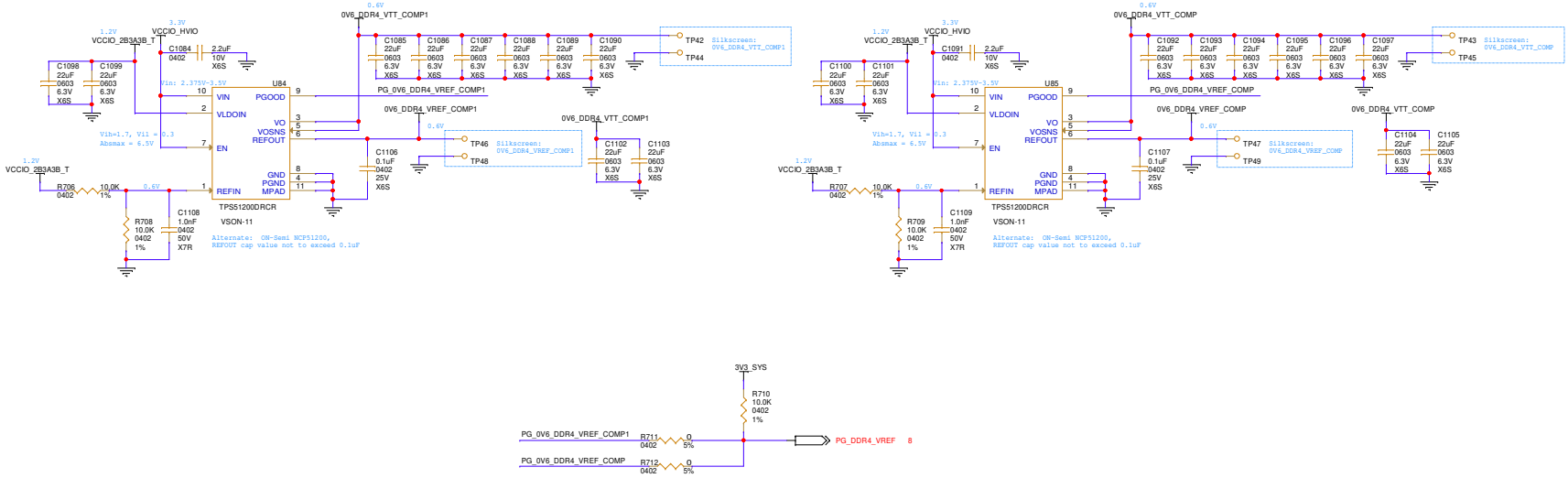


Title: AGILEX 5 E-SERIES 065B PREMIUM DEV KIT

Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 66 of 67

CAD Note:
Place the TP at easily accessible spot on the PCB.
Avoid under Heatsink and Add-on card shadow area.



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Size	Document Number	Rev
C	180-0330713-A2	A2

Date: Thursday, September 19, 2024 Sheet 67 of 67