Intel® Core™ Ultra Processors (Series 2)

Specification Update

Supporting Intel® Core™ Ultra 200S, 200HX, 200H, and 200U Series Processors, formerly known as Arrow Lake

Revision 004

January 2025

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Contents

Tables

Figures

Revision History

Document Number	Revision Number	Description	Revision Date
834774	001	Initial Revision – Includes errata ARL001-ARL018	October 2024
	002	Added Erratum: ARL019	November 2024
	003	Added Errata: ARL020, ARL021, ARL022 Removed Erratum ARL003	December 2024
	004	Added S 6+8, HX, H and U series processors Added Errata: ARL023, ARL024, ARL025, ARL026, ARL027	January 2025

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1 Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this updated document and are no longer published in other documents. This document may also contain information that has not been previously published.

1.1 Affected Documents

Document Title	Document Number
Intel® Core™ Ultra 200S and 200HX Series Processor Datasheet, Volume 1 of 2	832586
Intel® Core™ Ultra 200S and 200HX Series Processor Datasheet, Volume 2 of 2	834966
Intel® Core™ Ultra 200H and 200U Series Processor Datasheet, Volume 1 of 2	842704
Intel® Core™ Ultra 200H and 200U Series Processor Datasheet, Volume 2 of 2	844261

1.2 Related Documents

Document Title	Document Number/Location
AP-485, Intel® Processor Identification and the CPUID Instruction	http://www.intel.com/design/processor/applnots/241618.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference Manual A-M Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference Manual N-Z Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide Intel® 64 and IA-32 Intel® Architecture Optimization Reference Manual	http://www.intel.com/products/processor/manuals/index.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes	http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	D51397-001
ACPI Specifications	www.acpi.info

1.3 Nomenclature

Errata – These are design defects or errors. Errata may cause the processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes – These are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications – These describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes – These include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle or until a stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update, when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.)

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2 Identification Information

2.1 Component Identification via Programming Interface

The processor stepping is identified by the following register contents:

Table 2-1. Component Identification

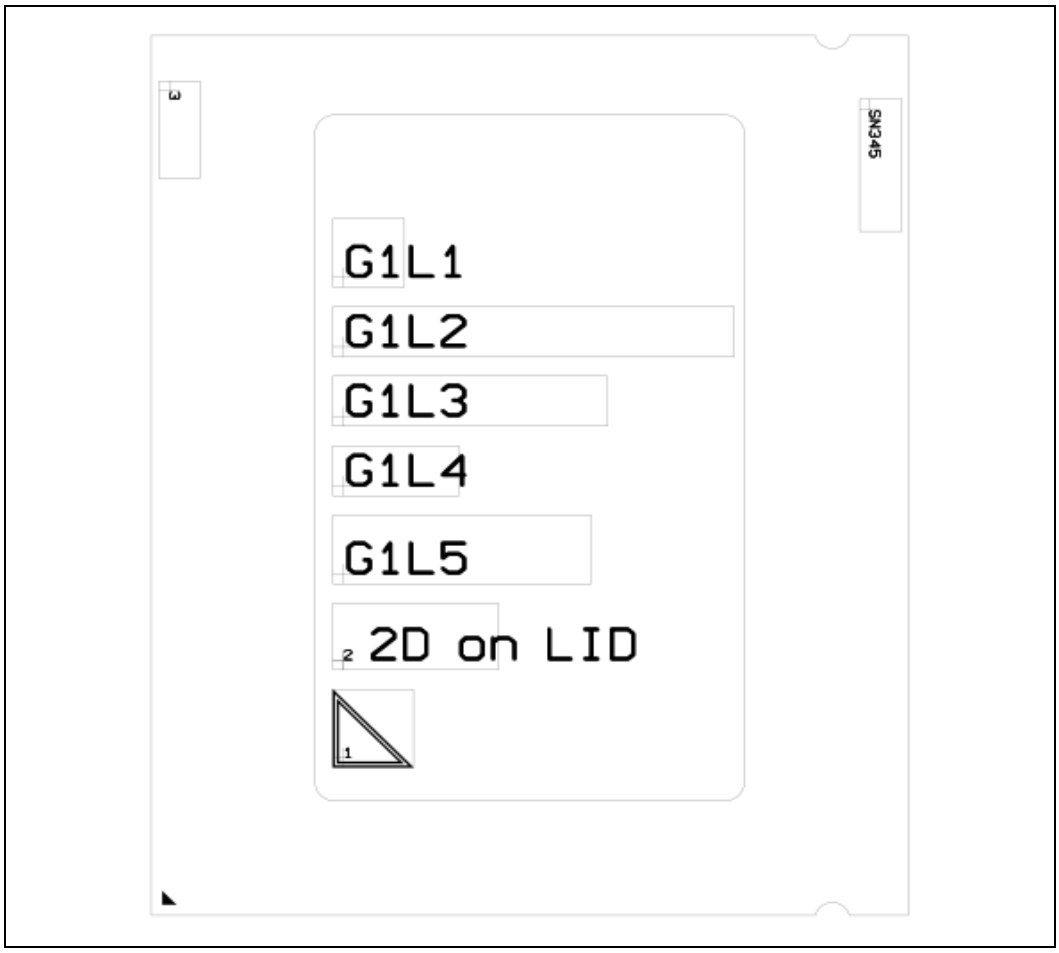
Samples	Stepping	CPUID	Reserved [31:28]	Extended Family [27:20]	Extended Model [19:16]	Reserved [15:14]	Processor Type [13:12]	Family Code [11:8]	Model Number [7:4]	Stepping ID [3:0]
ARL-S 8P+16E	B0	C0662h	Reserved	00h	Ch	Reserved	0h	6h	6h	2h
ARL-S 6P+8E	A0	C0662h	Reserved	00h	Ch	Reserved	0h	6h	6h	2h
ARL-HX 8P+16E	B0	C0662h	Reserved	00h	Ch	Reserved	0h	6h	6h	2h
ARL-H 6P+8E	A1	C0652h	Reserved	00h	Ch	Reserved	0h	6h	5h	2h
ARL-U 2P+8E	A1	B0650h	Reserved	00h	Bh	Reserved	0h	6h	5h	0h

1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits[11:8], to indicate whether the processor belongs to the Celeron®, Pentium®, or Intel® Core™ processor family.
2. The Extended Model, Bits [19:16] in conjunction with the Model Number, specified in Bits [7:4], are used to identify the model of the processor within the processor's family.
3. The Family Code corresponds to Bits [11:8] of the EDX register after RESET, Bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
4. The Model Number corresponds to Bits [7:4] of the EDX register after RESET, Bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
5. The Stepping ID in Bits [3:0] indicates the revision number of that model. Refer table above for the processor stepping ID number in the CPUID information.
6. Refer to Processor BIOS Specification for additional information. When EAX is initialized to a value of '1', the CPUID instruction returns the Extended Family, Extended Model, Processor Type, Family Code, Model Number and Stepping ID value in the EAX register. The EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.

2.2 Component Marking Information

Figure 2-1. S-Series Chip Package LGA Top-Side Markings



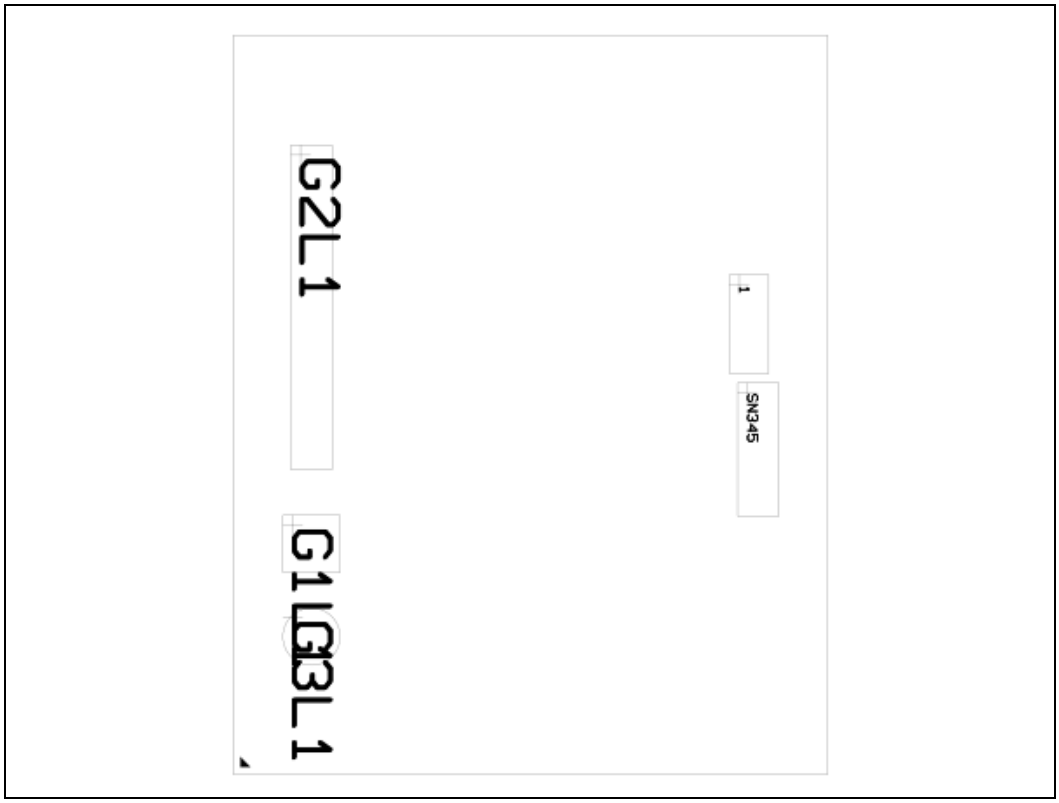
Pin Count: 1851 Package Size (width x height): 37.5mm x 45mm

Production (SSPEC):

- SN345
- G1L1: SPARK
- G1L2: TRADEMARK
- G1L3: PROC NUMBER
- G1L4: FPO_ SSPEC
- G1L5: {ex}

Note: "3" is used to extract the unit visual ID (2D ID).

Figure 2-2. HX-Series Chip Package BGA Top-Side Markings



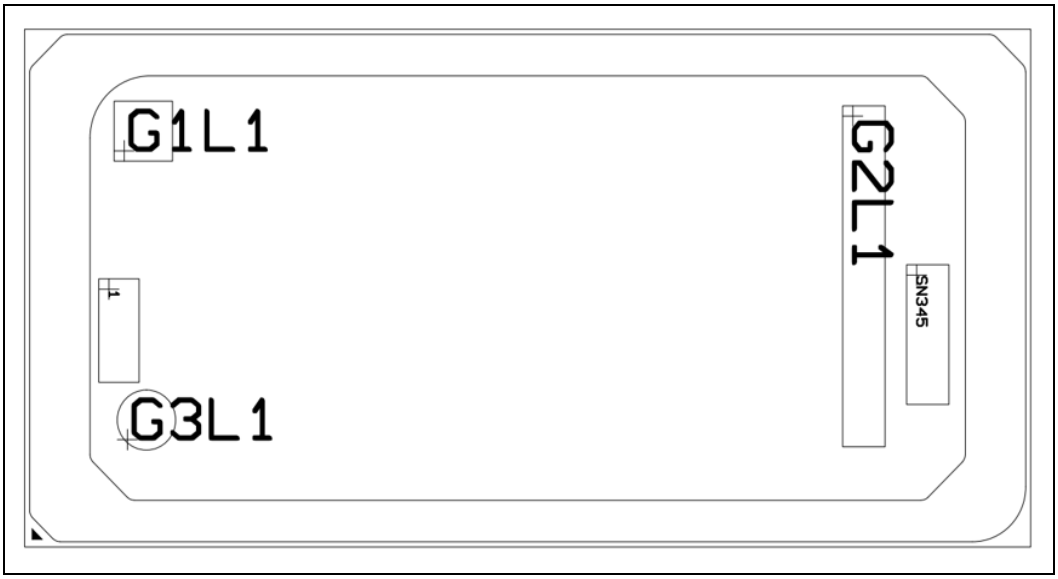
Pin Count: 2114 Package Size (width x height): 30.2 mm x 37.5 mm

Production (SSPEC):

- SN345
- G1L1: SPARK
- G2L1: FPO_SSPEC
- G3L1: {ex}

Note: "1" is used to extract the unit visual ID (2D ID).

Figure 2-3. H/U-Series Chip Package BGA Top-Side Markings



Pin Count: 2049 Package Size (width x height): 50mm x 25mm

Production (SSPEC):

- SN345
- G1L1: SPARK
- G2L1: FPO_SSPEC
- G3L1: {ex}

Note: "1" is used to extract the unit visual ID (2D ID).

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3 Summary Tables of Changes

The following tables indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed processor stepping. Intel may intend to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. These tables use the following notations:

3.1 Codes Used in Summary Table

Stepping	Description
(No mark) or (Blank box)	This erratum is fixed or does not apply to the listed stepping or specification change does not apply to the listed stepping.

Status	Description
Plan Fix	This erratum may be fixed in a future hardware stepping, firmware, or software update.
Fixed	This erratum has been previously fixed in Intel hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

3.2 Errata Summary Table

Erratum ID	Processor Line					Title
	S 8+16	S 6+8	HX	U	H	
ARL001	N/A	N/A	N/A	No Fix	N/A	Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit
ARL002	No Fix	No Fix	No Fix	No Fix	No Fix	Intel® VT-d Remapping Hardware Does Not Perform Reserved(0) Check on PGSNP Field of Scalable-mode PASID Table Entry
ARL003	N/A	N/A	N/A	N/A	N/A	N/A. Erratum has been removed.
ARL004	No Fix	No Fix	No Fix	No Fix	No Fix	MSI From VMD-Owned Device May Pass Memory Write
ARL005	No Fix	No Fix	No Fix	No Fix	No Fix	USB 3.2 Device May Not Function as Expected With TC10 Enabled
ARL006	No Fix	No Fix	No Fix	No Fix	No Fix	PCONFIG Error Reporting May be Incorrect
ARL007	No Fix	No Fix	No Fix	No Fix	No Fix	DP Monitor May Not Operate After S4/S5 Resume

Erratum ID	Processor Line					Title
	S 8+16	S 6+8	HX	U	H	
ARL008	No Fix	No Fix	No Fix	No Fix	No Fix	PCIe Root Port Lane Error Status Register May Not be Cleared
ARL009	No Fix	No Fix	No Fix	No Fix	No Fix	Type-C Display May be Blank Following S3/S4/S5 Resume
ARL010	No Fix	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Event Branch Instruction Retired Will Not Count CALLs to Next Sequential Instruction
ARL011	No Fix	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Event Branch Instruction Retired Will Overcount on Certain Types of Branch and Complex Instructions
ARL012	No Fix	No Fix	No Fix	No Fix	No Fix	Processor Trace May Generate PSB Packets Too Infrequently
ARL013	No Fix	No Fix	No Fix	No Fix	No Fix	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
ARL014	No Fix	No Fix	No Fix	N/A	No Fix	Architectural Performance Monitoring Events For Last Level Cache Will Overcount
ARL015	No Fix	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Events TOPDOWN.BACKEND_BOUND_SLOTS and IDQ_BUBBLES May be Inaccurate
ARL016	No Fix	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Event IDQ.MS_UOPS May Undercount
ARL017	No Fix	No Fix	No Fix	N/A	No Fix	Performance Monitoring Event INT_VEC_RETIRED.MUL_256 May Undercount
ARL018	No Fix	No Fix	No Fix	No Fix	No Fix	VM Exit Qualification May Not be Correctly Set on APIC Access While Serving a User Interrupt
ARL019	No Fix	No Fix	N/A	N/A	N/A	PCIe REFCLK Inactive Prior to PERST#
ARL020	No Fix	No Fix	No Fix	No Fix	No Fix	Locked Page Split Access May Not be Detected by UC-lock Disable if Split-lock Disable is Not Used
ARL021	No Fix	No Fix	No Fix	No Fix	No Fix	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
ARL022	No Fix	No Fix	No Fix	No Fix	No Fix	Display Artifacts With YUV420 Format
ARL023	N/A	N/A	N/A	No Fix	No Fix	Processor C-States With USB Full-Speed or Low-Speed Device Hotplug
ARL024	N/A	N/A	N/A	No Fix	No Fix	xHCI Out of Order ACK Due to LCRD1
ARL025	N/A	N/A	N/A	No Fix	No Fix	Non Canonical Fault May be Signaled on Access That Wraps Address Space When LAM is Enabled

Erratum ID	Processor Line					Title
	S 8+16	S 6+8	HX	U	H	
ARL026	No Fix	No Fix	No Fix	No Fix	No Fix	Processor May Encrypt TME Exclude Range if Mapped to Remap Range
ARL027	N/A	N/A	N/A	No Fix	No Fix	SPI0 Dual IO Mode With SPI0_IO2 And SPI0_IO3 Connected to SPI Device

3.3 Specification Changes

No.	Specification Changes
	None for this revision of this specification update.

3.4 Specification Clarifications

No.	Specification Clarifications
	None for this revision of this specification update.

3.5 Documentation Changes

No.	Documentation Changes
	None for this revision of this specification update.

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4 Errata Details

ARL001	**Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit**
Problem	Under complex micro-architectural conditions, single step on branches (IA32_DEBUGCTLMSR (Offset 1D9h, bit [1]) and also TF flag in EFLAGS register is set) in guest might be missed when VMM enables notification on VM Exit (IA32_VMX_PROCBASED_CTLS2 MSR, Offset 48Bh, bit [31]) while the dirty access bit is not set for the code page (bit [6] in paging-structure entry).
Implication	When single step is enabled under the above condition, some single step branches will be missed. Intel has only observed this erratum in a synthetic test environment.
Workaround	When enabling single step on branches for debugging, software should first set the dirty bit of the code page.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL002	**Intel® VT-d Remapping Hardware Does Not Perform Reserved(0) Check on PGSNP Field of Scalable-mode PASID Table Entry**
Problem	Intel® VT-d remapping hardware does perform Reserved(0) check on Page Snoop (PGSNP) field in scalable-mode Process Address ID (PASID) table entry when Snoop Control capability is defined as not available in the Extended Capability Register Offset 10h bit 7 (ECAP.SC=0).
Implication	There are no known functional implications due to this erratum. Intel has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL003	**N/A. Erratum has been removed.**

ARL004	**MSI From VMD-Owned Device May Pass Memory Write**
Problem	When the storage subsystem is configured to operate in RAID 0 or 1 mode, a Message Signaled Interrupt (MSI) from an Intel® Volume Management Device (Intel® VMD) owned device may interrupt a core before a previous write from the device is completed.
Implication	Due to this erratum, the platform may experience unpredictable system behavior.
Workaround	None identified. The VMD MSI interrupt-handler should initially perform a dummy register read to the MSI initiator device prior to any writes to ensure proper PCIe ordering.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL005	USB 3.2 Device May Not Function as Expected With TC10 Enabled
Problem	When TC10 is enabled, a USB 3.2 device connected to USB Type-C port directly without retimer may not function as expected.
Implication	Due to this erratum, a USB 3.2 device may not function as expected.
Workaround	None identified. It may be possible for the BIOS to contain a mitigation for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL006	PCONFIG Error Reporting May be Incorrect
Problem	If invalid parameters are provided, the PCONFIG instruction should generate a #GP exception. Due to this erratum, the processor may instead set a ZF flag, with EAX reporting failure reasons.
Implication	Due to this erratum, incorrectly configured PCONFIG usage may lead to unexpected error reporting.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL007	DP Monitor May Not Operate After S4/S5 Resume
Problem	When switching a USB Type-C Display Port (DP) monitor connection between Alt Mode and MFD in S4/S5, the monitor may not be enumerated when resuming from S4/S5.
Implication	Due to this erratum, a DP Monitor may not operate when resuming from S4/S5 and may require a hot plug to recover.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL008	PCIe Root Port Lane Error Status Register May Not be Cleared
Problem	Re-enabling a port following a link disable or hot reset the PCIe Lane Error Status register (Offset 0xA38) may not be cleared.
Implication	Due to this erratum, the Lane Error Status register may indicate lane errors on some of the Root Ports. Intel has not observed any functional issues due this erratum.
Workaround	None identified. Software should ignore the lane error status register to mitigate this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL009	Type-C Display May be Blank Following S3/S4/S5 Resume
Problem	When switching between Type-C Display Alt Mode and a Multi-Function Device (MFD) while the system is in S3/S4/S5, the Display may not enumerate.

Implication	When this erratum occurs, the Display may be blank. A device unplug and re-plug may be necessary to recover the display.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL010	**Performance Monitoring Event Branch Instruction Retired Will Not Count CALLs to Next Sequential Instruction**
Problem	A CALL instruction whose target is the next sequential instruction (the same address pushed onto the stack) will not increment the performance monitoring event BR_INST_RETIRED (Event: C4H, UMask: 00H, F9H).
Implication	Due to this erratum, software monitoring Branch Instruction Retired events may undercount. Since the CALL is to the next instruction, control flow tracing with the Last Branch Retired (LBR) records should not be affected.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL011	**Performance Monitoring Event Branch Instruction Retired Will Overcount on Certain Types of Branch and Complex Instructions**
Problem	On certain types of branch and complex instructions, the performance monitoring event BR_INST_RETIRED (Event: C4H, UMask: 00H / 7EH / BFH / C0H / DFH / EBH / FBH / F9H) will overcount by 1. Affected instructions include FAR CALL/JMP, RETF, IRET, VMENTRY/VMEXIT/VMPTRLD, and complex SGX/SMX/CSTATE instructions/flows.
Implication	Due to this erratum, software monitoring Branch Instruction Retired events may overcount.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL012	**Processor Trace May Generate PSB Packets Too Infrequently**
Problem	A Packet Stream Boundary (PSB) packet should be generated for every PSBFreq number of trace output bytes. Due to this erratum, PSB packets may be generated only after as many as four times that number of output bytes have been generated.
Implication	Due to this erratum, trace decoder software may see fewer PSB packets than expected. This may lead to the trace decoder software needing to search further to find a starting point to decode or, when used in circular mode, being unable to decode the trace due to lacking any PSB packets.
Workaround	None identified. The software can request more frequent PSB packets by programming PSBFreq (bits[27:24]) of IA32_RTIT_CTL MSR (570H) to a value 1/4 of the desired value.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL013	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
Problem	The act of one processor or system bus master writing data into a currently executing code segment of a second processor with the intent of having the second processor execute that data as code is called cross-modifying code (XMC). XMC that does not force the second processor to execute a synchronizing instruction prior to execution of the new code is called unsynchronized XMC. Software using unsynchronized XMC to modify the instruction byte stream of a processor can see unexpected or unpredictable execution behavior from the processor that is executing the modified code.
Implication	In this case, the phrase "unexpected or unpredictable execution behavior" encompasses the generation of most of the exceptions listed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide including a General Protection Fault (GPF) or other unexpected behaviors. In the event that unpredictable execution causes a GPF the application executing the unsynchronized XMC operation would be terminated by the operating system.
Workaround	In order to avoid this erratum programmers should use the XMC synchronization algorithm as detailed in the Intel Architecture Software Developer's Manual Volume 3: System Programming Guide Section: Handling Self- and Cross-Modifying Code.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL014	Architectural Performance Monitoring Events For Last Level Cache Will Overcount
Problem	The Performance Monitoring Event LONGEST_LAT_CACHE.REFERENCES (Event: 2EH, UMask: 4FH) and LONGEST_LAT_CACHE.MISS (Event: 2EH, UMask: 41H) will double count.
Implication	Due to this erratum, software monitoring these two events for last level cache will observe counts that are two times the actual value.
Workaround	None identified. Software may mitigate this issue by dividing the counter value by two.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL015	Performance Monitoring Events TOPDOWN.BACKEND_BOUND_SLOTS and IDQ_BUBBLES May be Inaccurate
Problem	The performance monitoring events TOPDOWN.BACKEND_BOUND_SLOTS (Event A4h, UMask 02h) and IDQ_BUBBLES.* (Event 9Ch, UMask 01h) may not count when the processor is in the C0.2 power sub-state, which is entered via the TPAUSE or UWAIT instructions. This erratum also impacts the accuracy of MSR_PERF_METRICS fields Frontend Bound, Backend Bound, and Fetch Latency (MSR 329h, Bits [23:16], [31:24] and [55:48]).
Implication	Due to this erratum, these performance monitoring events and the fields in MSR_PERF_METRICS may be inaccurate.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL016	Performance Monitoring Event IDQ.MS_UOPS May Undercount
Problem	The performance monitoring events IDQ.MS_UOPS, IDQ.MS_SWITCHES, and IDQ.MS_CYCLES_ANY (Event 79h, UMask 30h) may undercount MS_UOPS that come from the Decode Stream Buffer (DSB).
Implication	Due to this erratum, performance monitoring counters may report counts lower than expected.
Workaround	None identified. Performance monitoring event UOPS_RETIRED.MS may be used instead.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL017	Performance Monitoring Event INT_VEC_RETIRED.MUL_256 May Undercount
Problem	The performance monitoring event INT_VEC_RETIRED.MUL_256 (Event E7h, Umask 80h) may not count VPMULLQ instructions.
Implication	Due to this erratum, the performance monitoring event may report lower counts than expected.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL018	VM Exit Qualification May Not be Correctly Set on APIC Access While Serving a User Interrupt
Problem	A VM Exit that occurs while the processor is serving a user interrupt in non-root mode should set the "asynchronous to instruction execution" bit in the Exit Qualification field in the Virtual Machine Control Structure (bit 16). However, if a VM Exit occurs during processing a user interrupt due to an APIC access, the bit will not be set.
Implication	Due to this erratum, the "asynchronous to instruction execution" bit will not be set if an APIC Access VM Exit occurs while the processor is serving a user interrupt. Intel has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL019	PCIe REFCLK Inactive Prior to PERST#
Problem	PCIe differential reference clocks may go inactive prior to the assertion of PERST#.
Implication	Due to this erratum, the PCI Express® Card Electromechanical Specification, Revision 5.0, Version 1.0 Power Section 2.2.2 "Management States (S0 to S3/S4 to S0)" requirement is not followed. Intel has not observed any functional implications due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL020	Locked Page Split Access May Not be Detected by UC-lock Disable if Split-lock Disable is Not Used
Problem	The UC-lock disable feature (MSR_MEMORY_CTRL bit [28] (MSR 33h)) may not cause a fault (#AC(4)) for a page split lock that accesses a page with non-WB memory type if the split lock disable (MSR_MEMORY_CTRL bit [29]) is not set.
Implication	Due to this erratum, system software may not be able to fully prevent bus locks due to locks to non-WB memory unless they use the split-lock disable feature to prevent bus locks due to splits. Intel has not observed this erratum with any commercially available software.
Workaround	None identified. Software using the UC-lock disable feature should also enable the split lock disable feature.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL021	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
Problem	The PTM Propagation Delay Adaptation Interpretation B (PTMPDAIB) Bit is implemented at Configuration Space (CFG) Offset 158h instead of at 50h as documented in the PCI-SIG PTM Byte Ordering Adaptation Engineering Change Notice (ECN).
Implication	End Point Device (EPD) software that implements the PTM Byte Ordering Adaptation ECN will not be able to program their PTMPDAIB Bit correctly since it is located at a different register offset.
Workaround	None identified. To mitigate this issue, EPD software that implements the PTM Byte Ordering Adaptation ECN must access PTMPDAIB at CFG Offset 158h.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL022	Display Artifacts With YUV420 Format
Problem	While in DP2.1 UHBR mode and using the YUV420 format with scaling, displays with a resolution higher than 5K @ 60Hz may show display artifacts.
Implication	Due to this erratum, display artifacts may be seen.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL023	Processor C-States With USB Full-Speed or Low-Speed Device Hotplug
Problem	When doing a hotplug on a USB hub with two or more USB Full-speed or Low-speed devices each with a 1 ms service interval interrupt endpoint, a race condition may occur between the PMC and the xHCI controller.
Implication	The processor may fail to enter C3 or deeper package C-States. Note: This erratum has only been observed in a synthetic environment.
Workaround	None identified. This condition is recovered after the xHCI controller has successfully entered D3.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL024	xHCI Out of Order ACK Due to LCRD1
Problem	A delay in the availability of LCRD1 (Link Credit 1) from a USB 3.2 hub, with two or more downstream USB 3.2 bulk endpoint devices engaged in SuperSpeedPlus concurrent transfers, may lead to the connected xHCI controller sending the ACK and Status of a transfer packet out of order.
Implication	Due to this erratum, a USB 3.2 bulk endpoint device may not respond to subsequent transfers. It may be possible for a device driver to recover the USB 3.2 device.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL025	Non Canonical Fault May be Signaled on Access That Wraps Address Space When LAM is Enabled
Problem	When Linear Address Masking (LAM) is enabled, a non-canonical fault may be signaled if there is an access which splits the 64-bit linear address space (and thus touches both linear address FFFF_FFFF_FFFF_FFFFh and 0h).
Implication	Due to this erratum, software may receive an unexpected exception on such accesses. Intel has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL026	Processor May Encrypt TME Exclude Range if Mapped to Remap Range
Problem	The processor accesses to TME exclude range may be encrypted but not decrypted if mapped to remap range.
Implication	Due to this erratum, the processor exclude range it will be encrypted but will but not decrypted if mapped to remap range.
Workaround	It may be possible for BIOS to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ARL027	SPI0 Dual IO Mode With SPI0_IO2 And SPI0_IO3 Connected to SPI Device
Problem	On systems with dual IO mode enabled, SPI0_IO2 and SPI0_IO3 may momentarily drive low before these signals are pulled high by internal resistors during boot from the G3 state.
Implication	Due to this erratum, unexpected system behavior may occur on systems when SPI0_IO2 and SPI0_IO3 signals are connected to an SPI device.
Workaround	None identified. To mitigate this erratum, do not connect SPI0_IO2 and SPI0_IO3 to an SPI device in SPI0 dual IO mode enabled systems.
Status	For the steppings affected, refer to the Summary Table of Changes.

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5 Specification Changes

None.

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6 Specification Clarification

None.

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7 Document Change

None.

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