

AGILEX™ 5 FPGA E-SERIES 065B MODULAR DEVELOPMENT KIT - SOM

PB : N19944-002

PBA : N19360-002

TA : N19359-002

BOM : 99CA38
MMID

Project Drawing Number	
Raw PCB	100-0330723-B1
Gerber Files	110-0330723-B1
PCB Design Files	120-0330723-B1
Assembly Drawing	130-0330723-B1
Fab Drawing	140-0330723-B1
Schematic Drawing	150-0330723-B1
PCB Film	160-0330723-B1
Bill of Materials	170-0330723-B1
Schematic Design Files	180-0330723-B1
Functional Specification	210-0330723-B1
PCB Layout Guidelines	220-0330723-B1
Assembly Rework	320-0330723-B1

Mon Sep 30 16:21:57 2024

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DEPARTMENT

altera
An Intel Company

SIZE
C+

CODE
34649

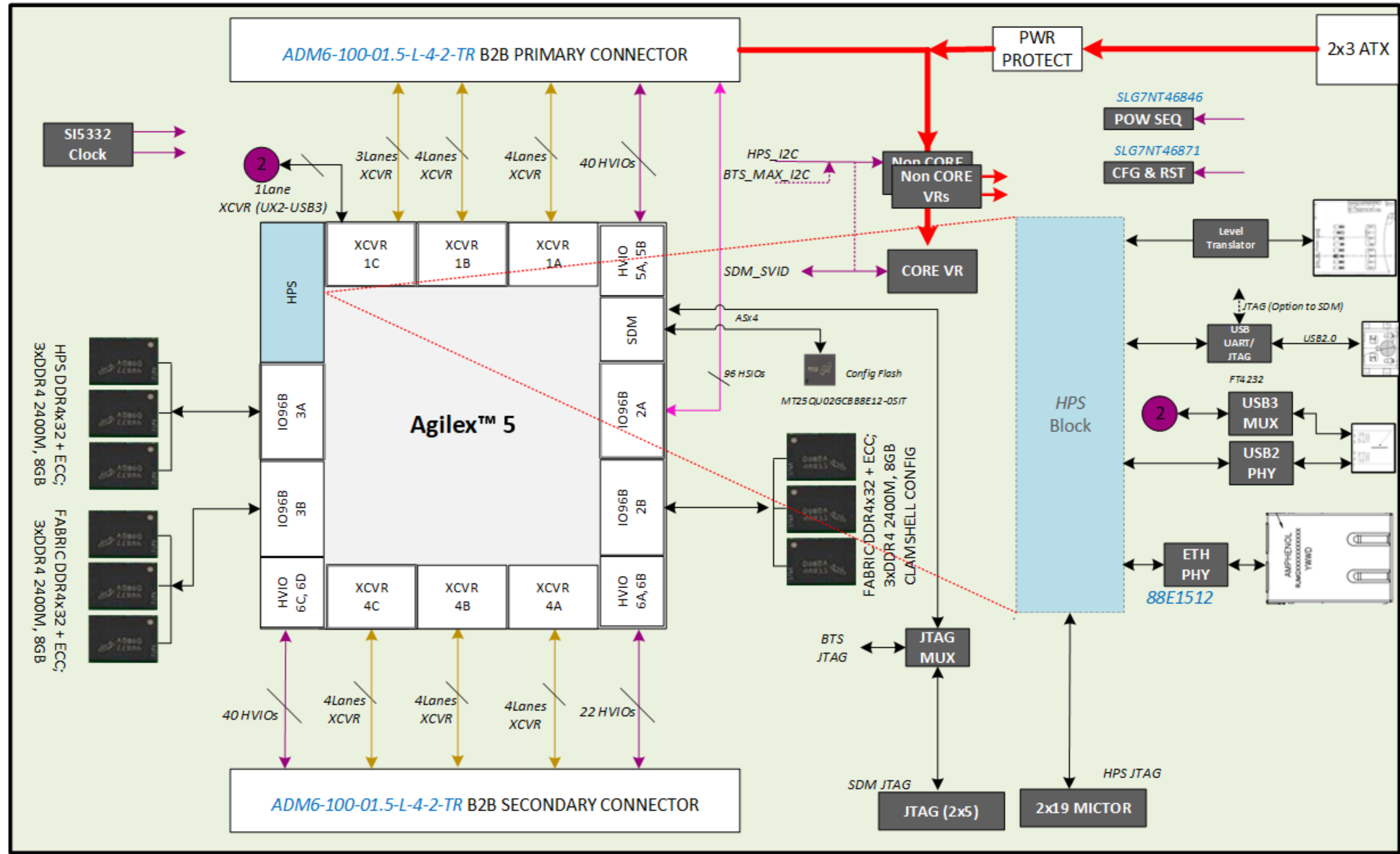
DOCUMENT NUMBER
150-0330723-B1

REV
2.1

SCALE:


DO NOT SCALE DRAWING

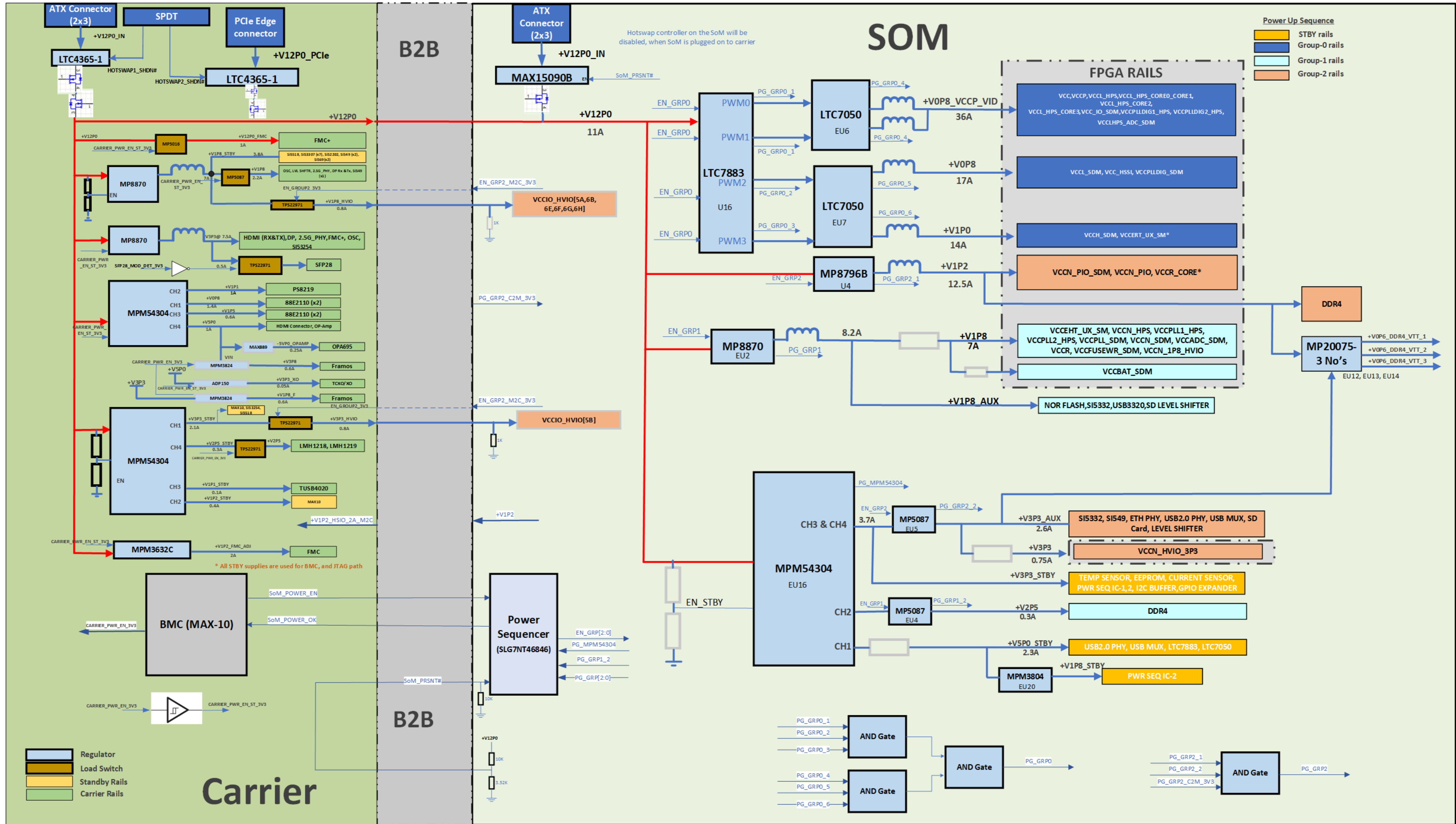
SHEET 1 OF 62



BLOCK DIAGRAM

Mon Sep 30 16:21:03 2024

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING		SHEET	3 OF 62

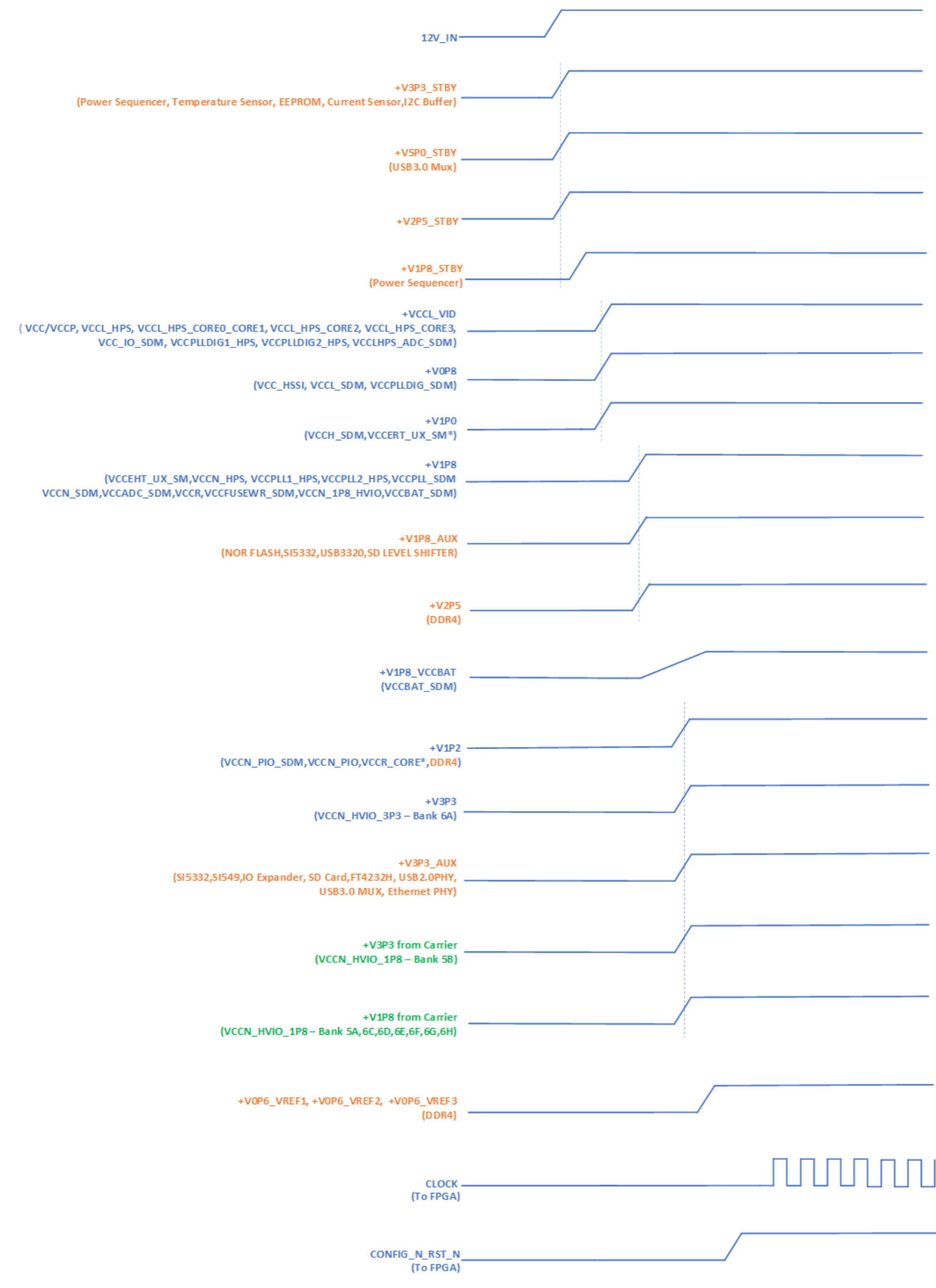


POWER TREE

Mon Sep 30 16:21:04 2024

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:	DO NOT SCALE DRAWING			SHEET	4 OF 62

Agilex™ 5 SOM Board Power Sequence



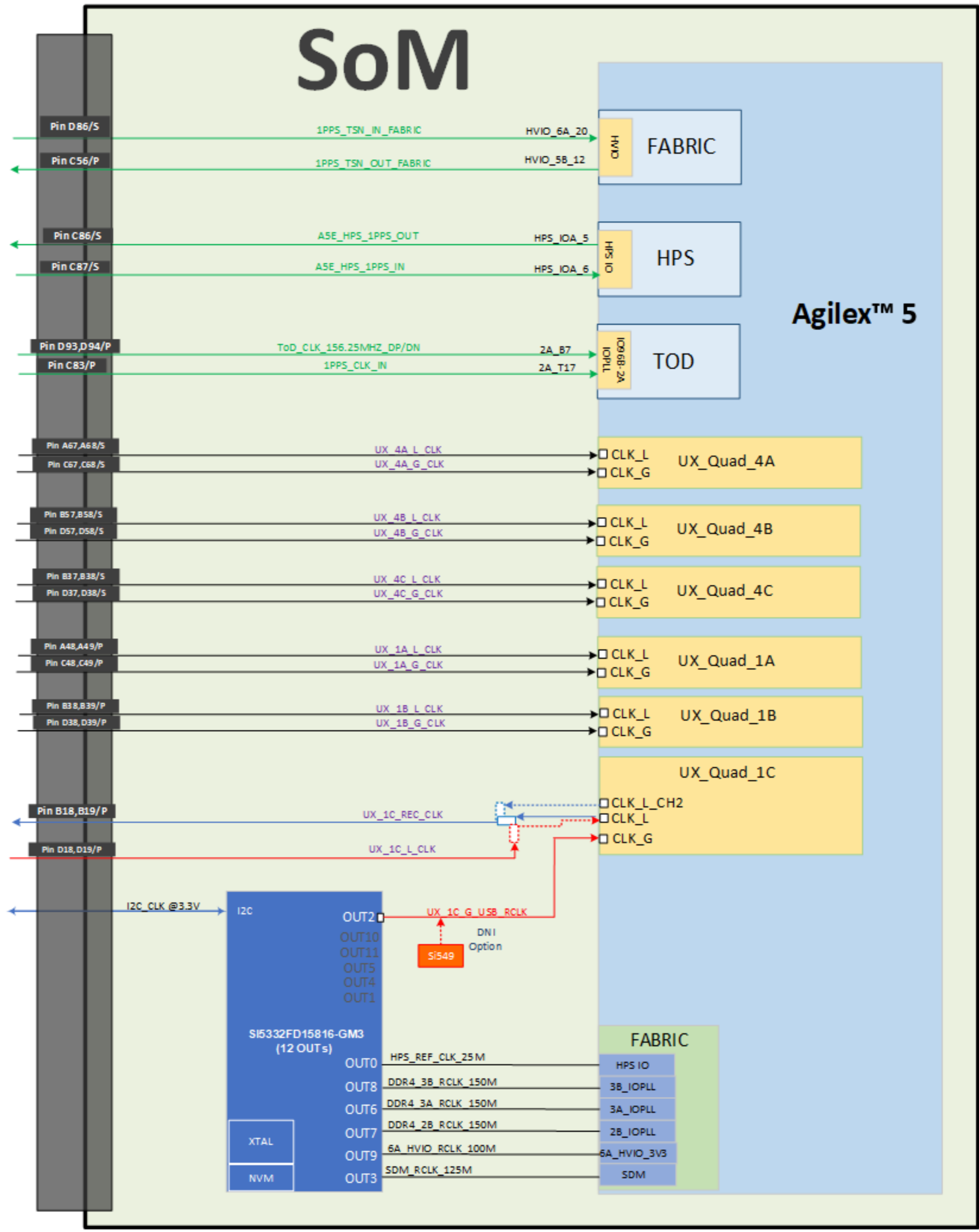
Mon Sep 30 16:21:05 2024

POWER SEQUENCE

DEPARTMENT




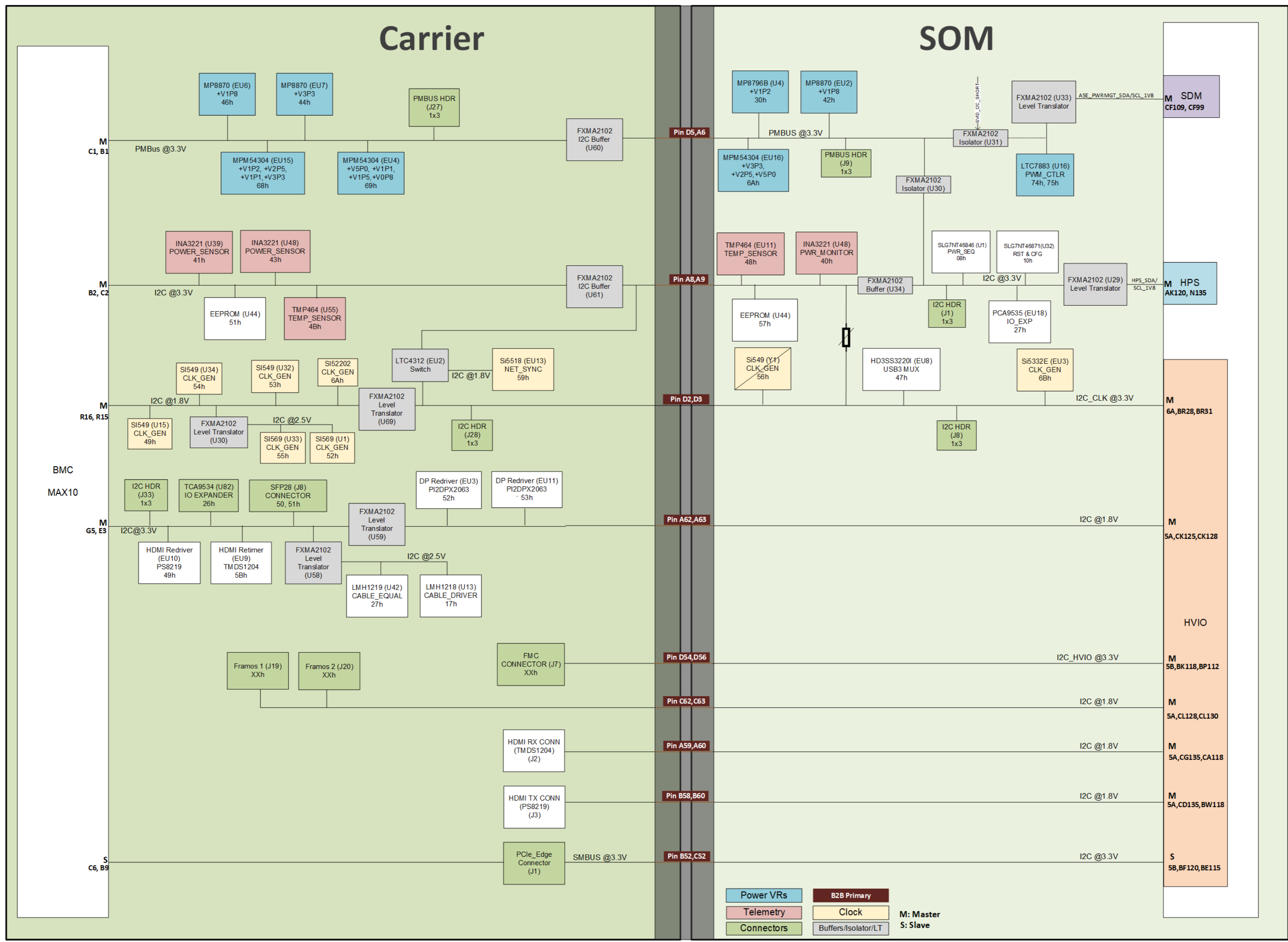
SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330723-B1	REV 2.1
SCALE:		DO NOT SCALE DRAWING	SHEET 5 OF 62



Mon Sep 30 16:21:06 2024

CLOCK TREE

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING		SHEET 6 OF 62	



B

B

A

A

4

3

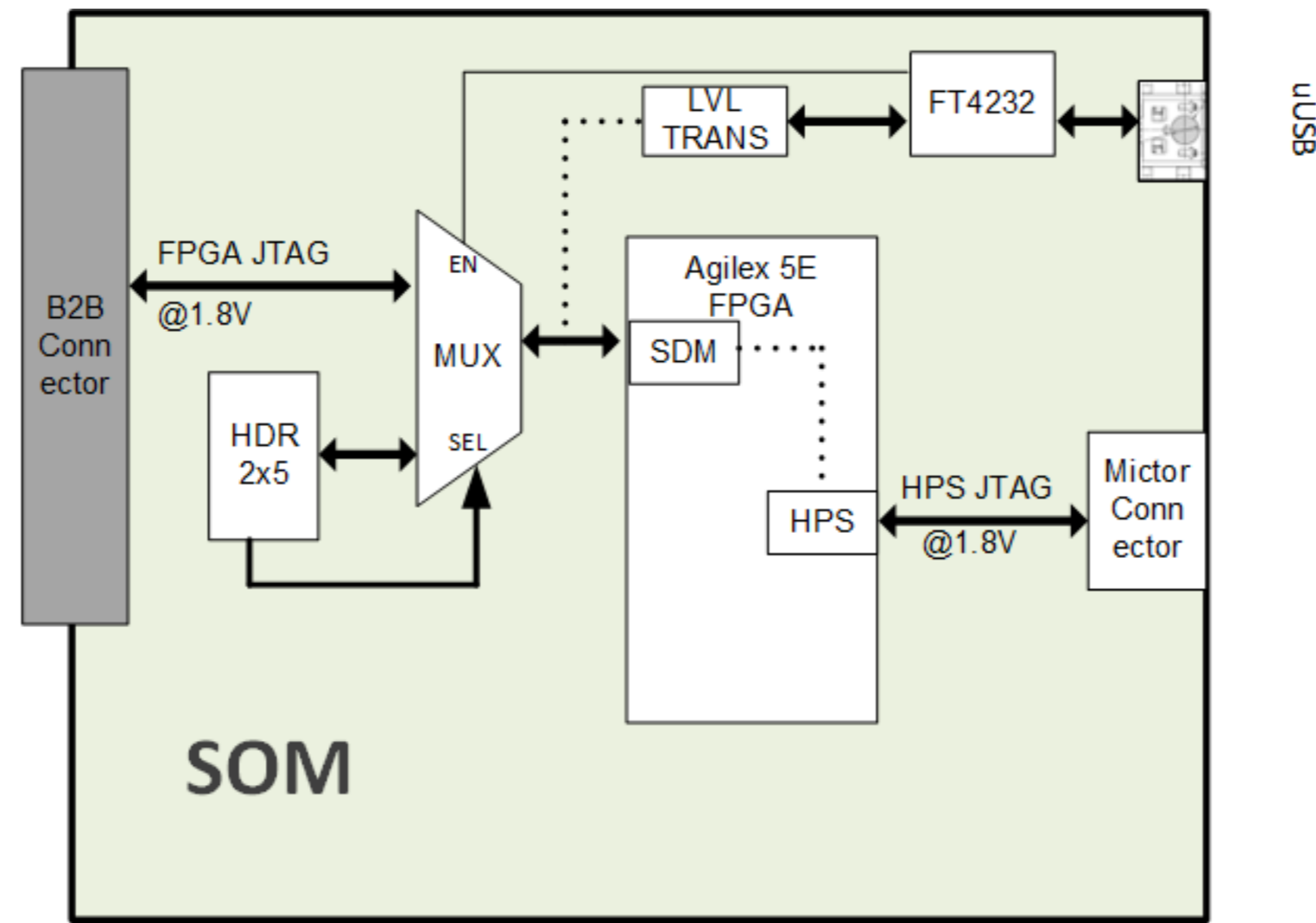
2


1

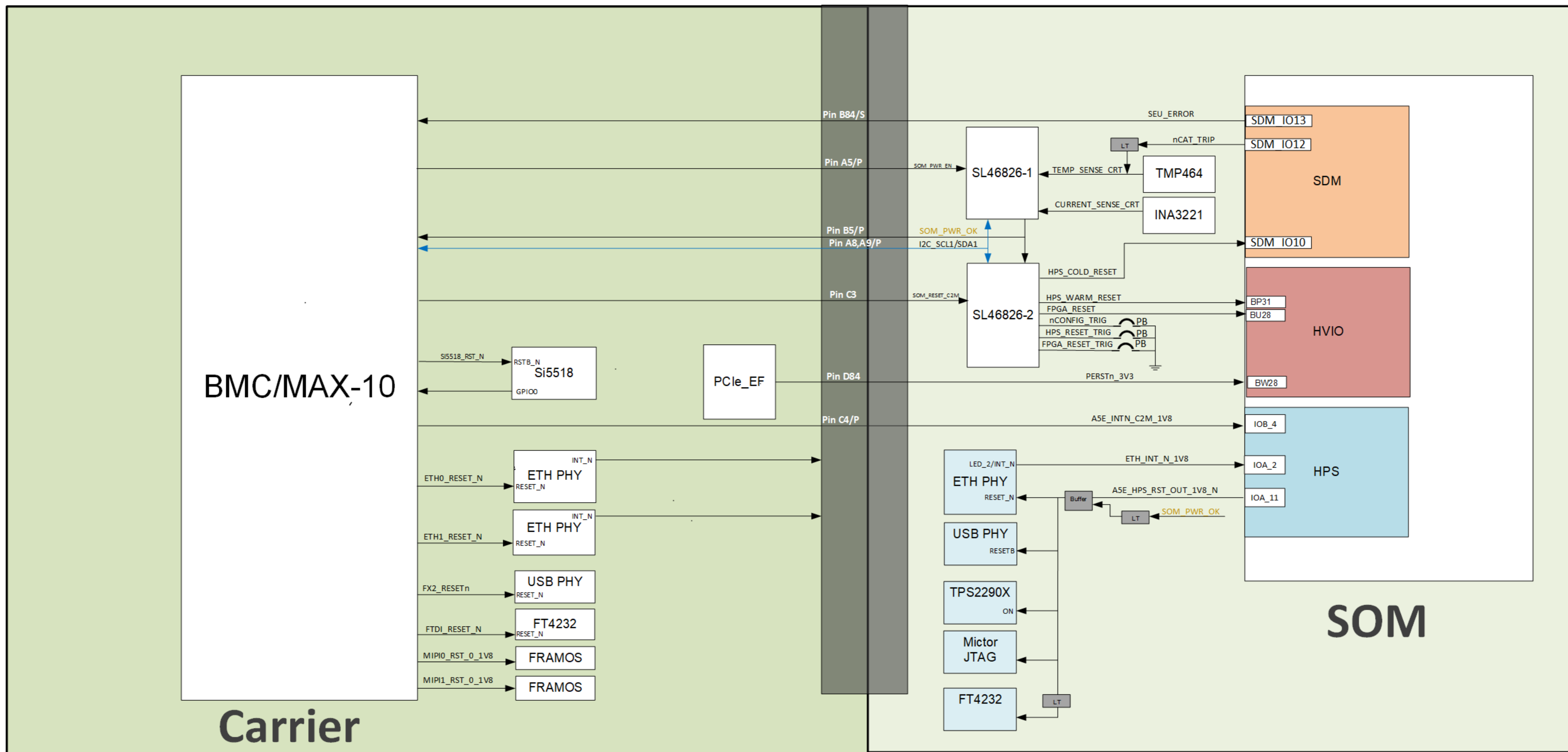
I2C TREE

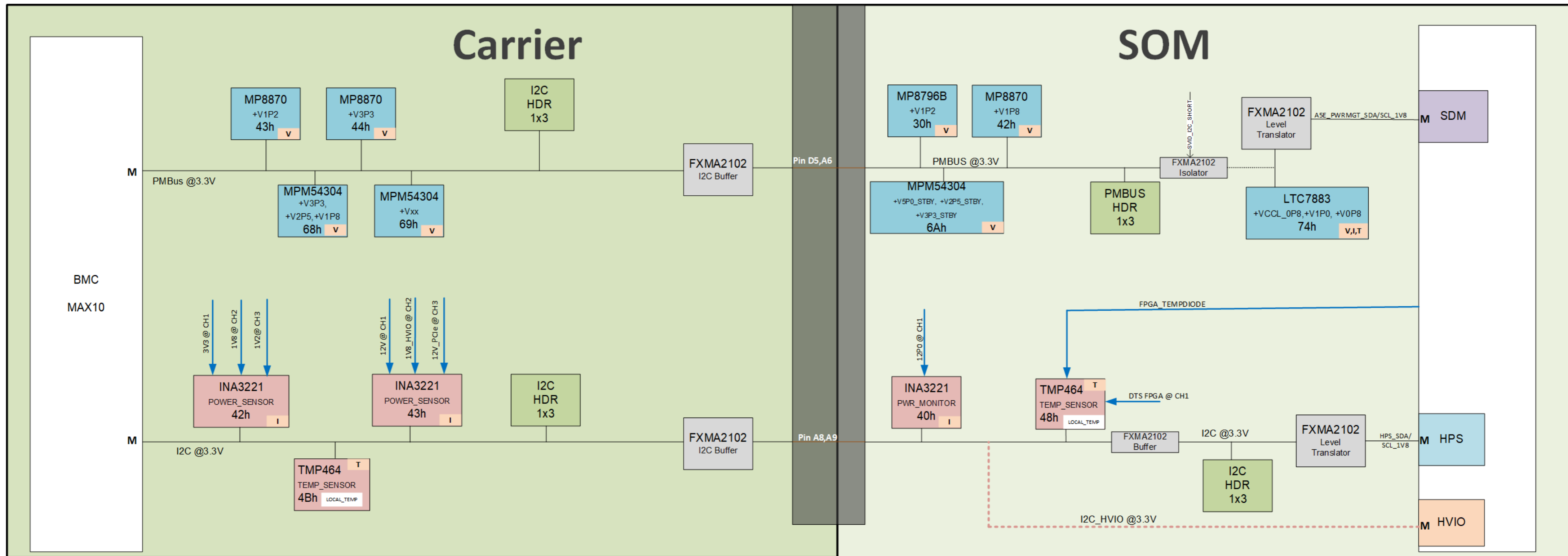
DEPARTMENT	<p>An Intel Company</p>	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
		SCALE:	DO NOT SCALE DRAWING		SHEET 7 OF 62

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DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING		SHEET	8 OF 62





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TELEMETRY TREE

DEPARTMENT



SIZE
C+

CODE
34649

DOCUMENT NUMBER
150-0330723-B1

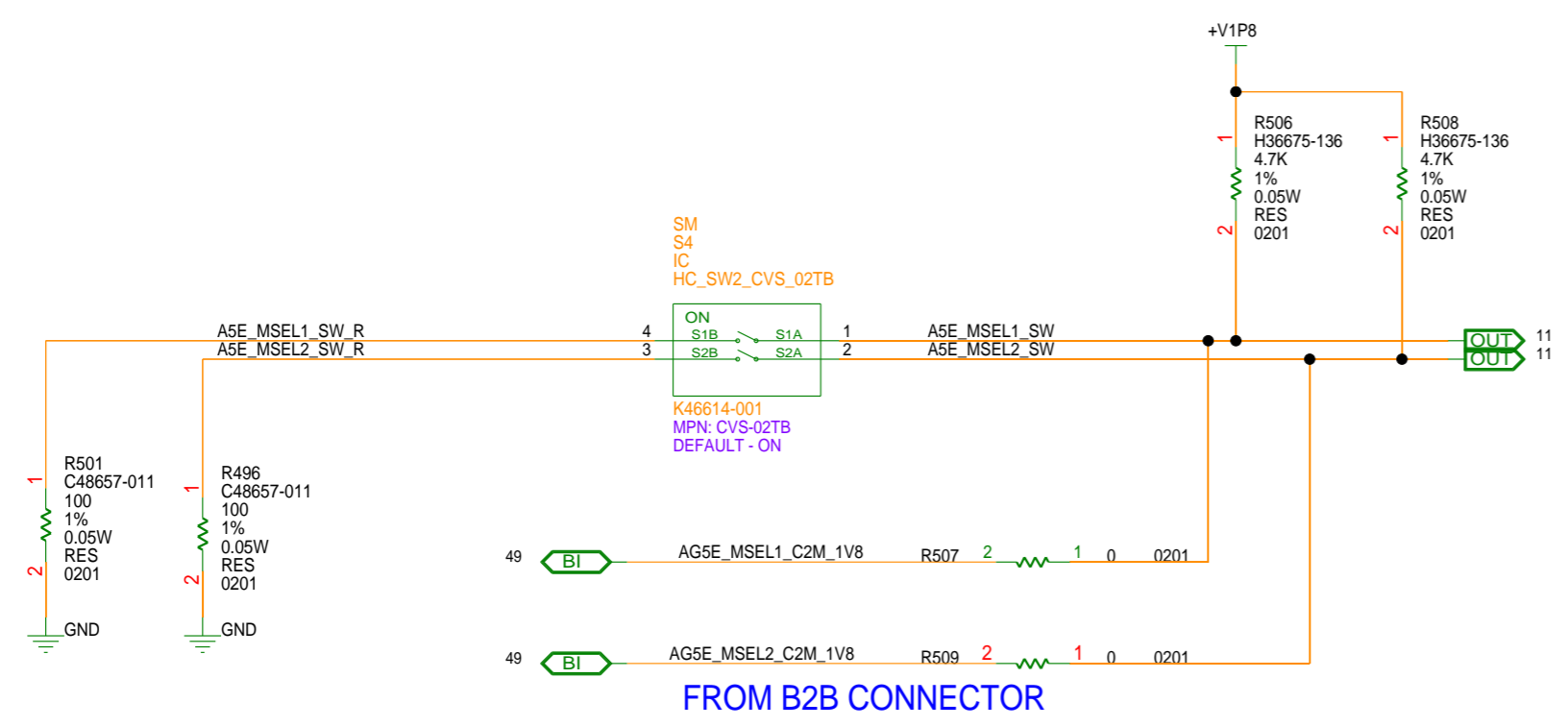
REV
2.1

SCALE:

DO NOT SCALE DRAWING

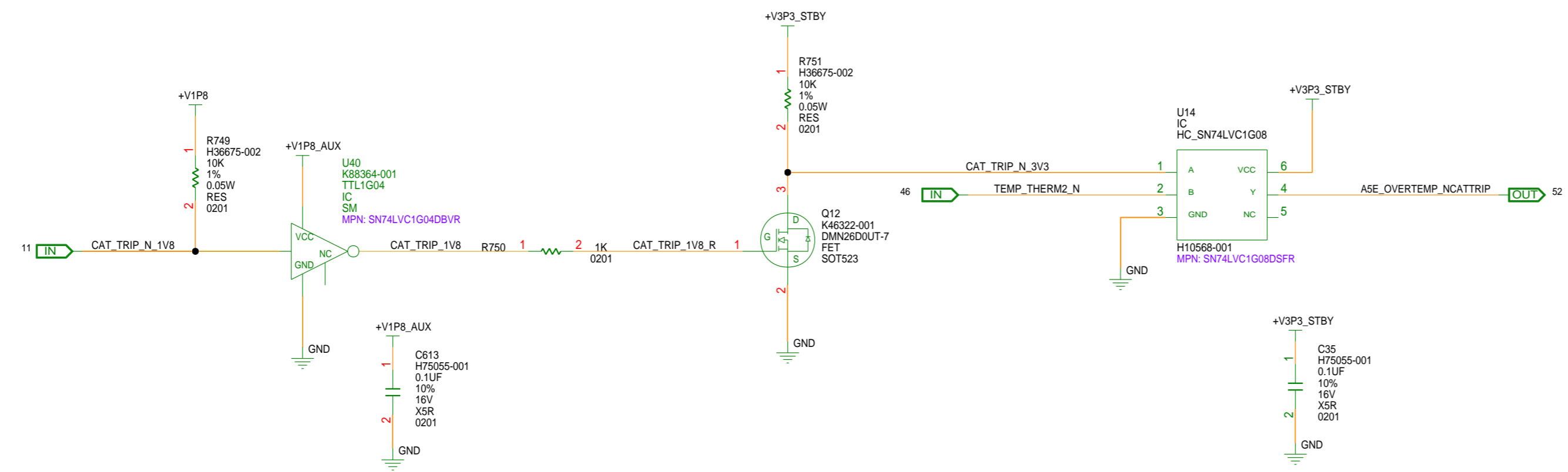
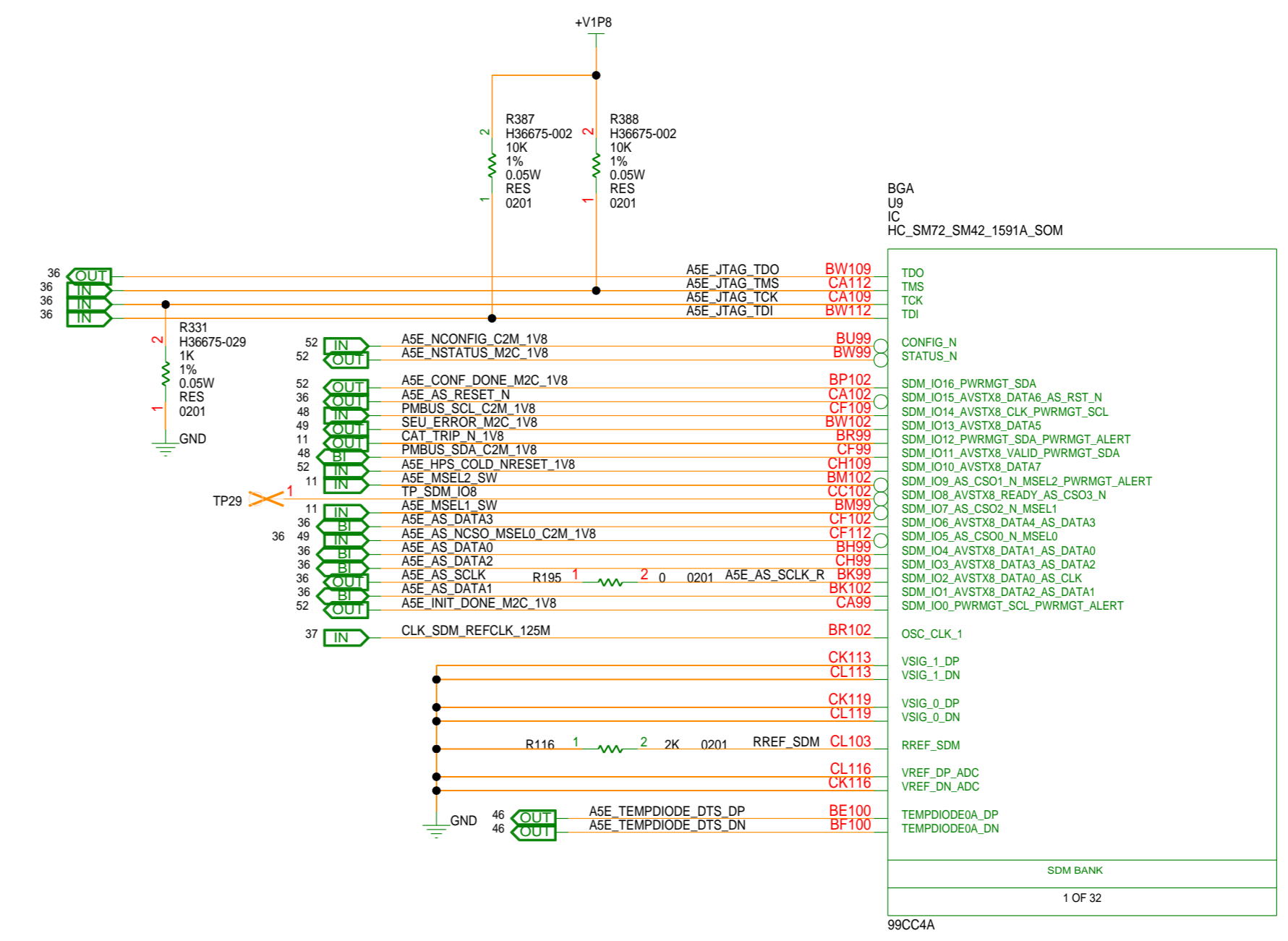
SHEET 10 OF 62

BOOT DEVICE SELECTION



MSEL[2:0]	CONFIG MODE
111	JTAG
001	AS (FAST MODE)
011	AS (NORMAL MODE)

SWITCH STATUS	SIGNAL LOGIC LEVEL
OFF	HIGH
ON	LOW



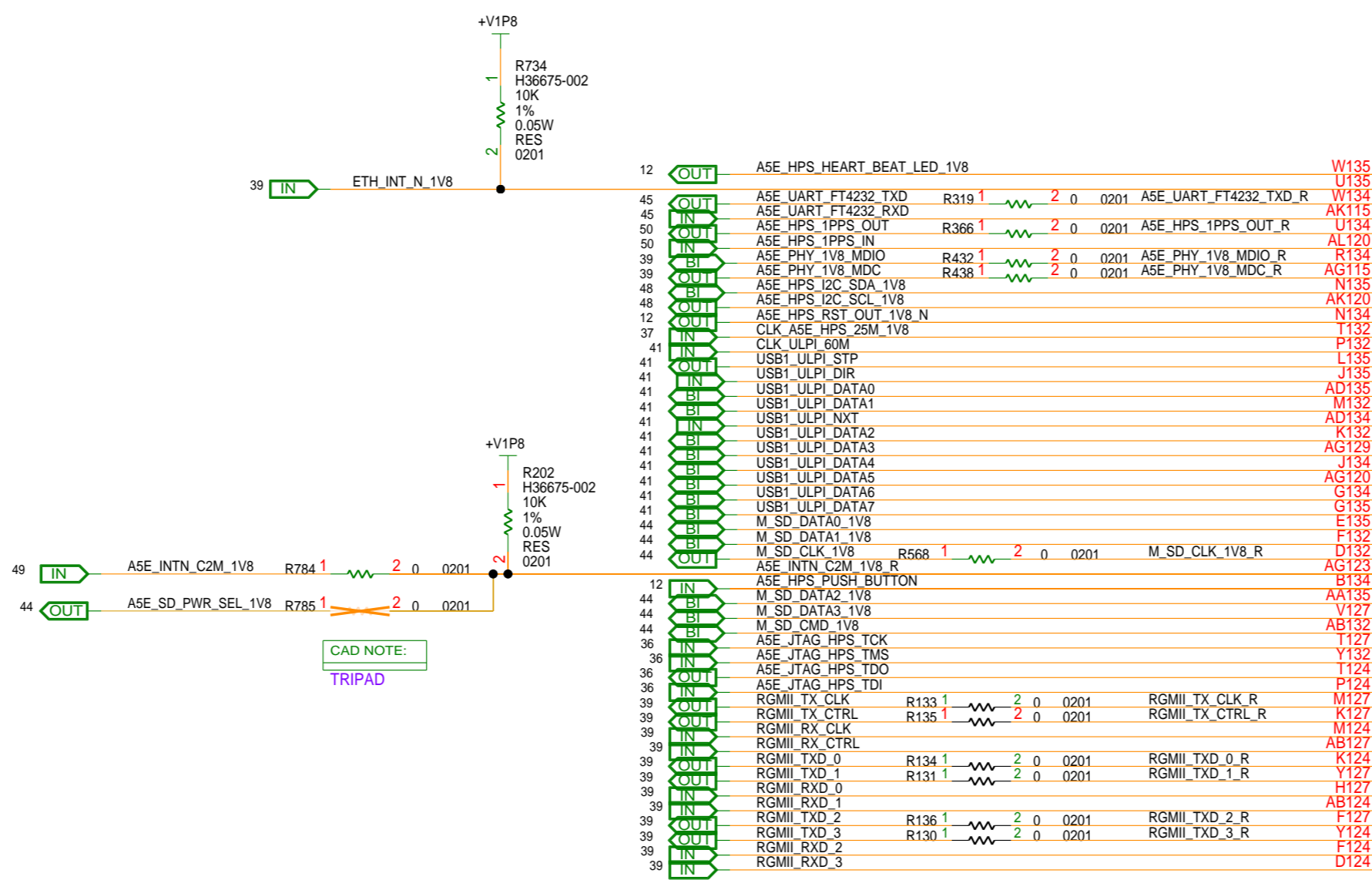
AG5E BANK - SDM

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 11 OF 62

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HPS IO MAP

PIN NUMBER	PIN NAME	SIGNAL NAME
W135	HPS_IOA_1	A5E_HPS_HEART_BEAT_LED_1V8
U135	HPS_IOA_2	ETH_INT_N_1V8
W134	HPS_IOA_3	A5E_UART_FT4232_TXD
AK115	HPS_IOA_4	A5E_UART_FT4232_RXD
U134	HPS_IOA_5	A5E_HPS_1PPS_OUT
AL120	HPS_IOA_6	A5E_HPS_1PPS_IN
R134	HPS_IOA_7	A5E_PHY_1V8_MDIO
AG115	HPS_IOA_8	A5E_PHY_1V8_MDC
N135	HPS_IOA_9	A5E_HPS_I2C_SDA_1V8
AK120	HPS_IOA_10	A5E_HPS_I2C_SCL_1V8
N134	HPS_IOA_11	A5E_HPS_RST_OUT_1V8_N
T132	HPS_IOA_12	CLK_A5E_HPS_25M_1V8
P132	HPS_IOA_13	CLK_ULPI_60M
L135	HPS_IOA_14	USB1_ULPI_STP
J135	HPS_IOA_15	USB1_ULPI_DIR
AD135	HPS_IOA_16	USB1_ULPI_DATA0
M132	HPS_IOA_17	USB1_ULPI_DATA1
AD134	HPS_IOA_18	USB1_ULPI_NXT
K132	HPS_IOA_19	USB1_ULPI_DATA2
AG129	HPS_IOA_20	USB1_ULPI_DATA3
J134	HPS_IOA_21	USB1_ULPI_DATA4
AG120	HPS_IOA_22	USB1_ULPI_DATA5
G134	HPS_IOA_23	USB1_ULPI_DATA6
G135	HPS_IOA_24	USB1_ULPI_DATA7
E135	HPS_IOB_1	M_SD_DATA0_1V8
F132	HPS_IOB_2	M_SD_DATA1_1V8
D132	HPS_IOB_3	M_SD_CLK_1V8
AG123	HPS_IOB_4	A5E_INTN_C2M_1V8
B134	HPS_IOB_5	A5E_HPS_PUSH_BUTTON
AA135	HPS_IOB_6	M_SD_DATA2_1V8
V127	HPS_IOB_7	M_SD_DATA3_1V8
AB132	HPS_IOB_8	M_SD_CMD_1V8
T127	HPS_IOB_9	A5E_JTAG_HPS_TCK
Y132	HPS_IOB_10	A5E_JTAG_HPS_TMS
T124	HPS_IOB_11	A5E_JTAG_HPS_TDO
P124	HPS_IOB_12	A5E_JTAG_HPS_TDI
M127	HPS_IOB_13	RGMII_TX_CLK
K127	HPS_IOB_14	RGMII_TX_CTRL
M124	HPS_IOB_15	RGMII_RX_CLK
AB127	HPS_IOB_16	RGMII_RX_CTRL
K124	HPS_IOB_17	RGMII_TXD_0
Y127	HPS_IOB_18	RGMII_TXD_1
H127	HPS_IOB_19	RGMII_RXD_0
AB124	HPS_IOB_20	RGMII_RXD_1
F127	HPS_IOB_21	RGMII_TXD_2
Y124	HPS_IOB_22	RGMII_TXD_3
F124	HPS_IOB_23	RGMII_RXD_2
D124	HPS_IOB_24	RGMII_RXD_3



BGA
U9
IC
HC_SMT2_SM42_1591A_SOM

HPS_IOA_1_GPI00_I00_SPI0_SS1_N_SPI0_CLK_UART0_CTS_N_NAND_ADO0_SDMMC_DATA0_USB0_CLK_EMAC0_PPS0_TRACE_D10
HPS_IOA_2_GPI00_I01_SPI0_SS1_N_SPI0_MOSI_UART0_RTS_N_NAND_ADO1_SDMMC_DATA1_USB0_STP_EMAC0_PPSTRIG0_TRACE_D9
HPS_IOA_3_GPI00_I02_SPI0_SS0_N_UART0_TX_I2C1_SDA_NAND_WE_N_SDMMC_CLK_USB0_DIR_EMAC1_PPS1_TRACE_D8
HPS_IOA_4_GPI00_I03_SPI0_MISO_UART0_RX_I2C1_SCL_NAND_RE_N_USB0_DATA0_EMAC1_PPSTRIG1_TRACE_D7
HPS_IOA_5_GPI00_I04_SPI0_CLK_UART1_CTS_N_I2C0_SDA_NAND_WP_N_SDMMC_WRITE_PROTECT_USB0_DATA1_EMAC2_PPS2_TRACE_D6
HPS_IOA_6_GPI00_I06_SPI0_MOSI_UART1_RTS_N_I2C0_SCL_NAND_ADO2_SDMMC_DATA2_USB0_NXT_EMAC2_PPSTRIG2_TRACE_D5
HPS_IOA_7_GPI00_I08_SPI0_MISO_MDI02_MDI0_UART1_TX_I2C_EMAC2_SDA_NAND_ADO3_SDMMC_DATA3_USB0_DATA2_TRACE_D4
HPS_IOA_8_GPI00_I07_SPI0_SS0_N_MDI02_MDC_UART1_RX_I2C_EMAC2_SCL_NAND_CLE_SDMMC_CMD_USB0_DATA3_TRACE_D15
HPS_IOA_9_GPI00_I08_SPI0_CLK_SPI1_CLK_MDI01_MDI0_I2C_EMAC1_SDA_NAND_ADO4_SDMMC_DATA4_USB0_DATA4_I3C1_SDA_TRACE_D14
HPS_IOA_10_GPI00_I09_SPI1_MOSI_SPI1_MOSI_MDI01_MDC_I2C_EMAC1_SCL_NAND_ADO5_SDMMC_DATA5_USB0_DATA5_I3C1_SCL_TRACE_D13
HPS_IOA_11_GPI00_I010_SPI1_MISO_SPI1_SS0_N_MDI00_MDI0_I2C_EMAC0_SDA_NAND_ADO6_SDMMC_DATA6_USB0_DATA6_I3C0_SDA_TRACE_D12
HPS_IOA_12_GPI00_I011_SPI1_SS1_N_SPI1_MISO_MDI00_MDC_I2C_EMAC0_SCL_NAND_ADO7_SDMMC_DATA7_USB0_DATA7_I3C0_SCL_TRACE_D11
HPS_IOA_13_GPI00_I012_NAND_ALE_SDMMC_PU_PD_DATA2_USB1_CLK_EMAC0_TX_CLK_TRACE_D10
HPS_IOA_14_GPI00_I013_NAND_RB_N_SDMMC_PWR_ENA_USB1_STP_EMAC0_TX_CTL_TRACE_D9
HPS_IOA_15_GPI00_I014_NAND_CE_N_USB1_DIR_EMAC0_RX_CLK_TRACE_D8
HPS_IOA_16_GPI00_I015_NAND_DQS_SDMMC_DATA_STROBE_USB1_DATA0_EMAC0_RX_CTL_TRACE_D7
HPS_IOA_17_GPI00_I016_I3C1_SDA_NAND_ADO8_USB1_DATA1_EMAC0_TXD0_TRACE_D6
HPS_IOA_18_GPI00_I017_I3C1_SCL_NAND_ADO9_USB1_NXT_EMAC0_TXD1_TRACE_D5
HPS_IOA_19_GPI00_I018_I3C0_SDA_NAND_ADO10_USB1_DATA2_EMAC0_RXD0_TRACE_D4
HPS_IOA_20_GPI00_I019_SPI1_SS1_N_I3C0_SCL_NAND_ADO11_USB1_DATA3_EMAC0_RXD1_TRACE_CLK
HPS_IOA_21_GPI00_I020_SPI1_CLK_SPI0_CLK_UART0_CTS_N_I2C1_SDA_NAND_ADO12_USB1_DATA4_EMAC0_TXD2_TRACE_D0
HPS_IOA_22_GPI00_I021_SPI1_MOSI_SPI0_MOSI_UART0_RTS_N_I2C1_SCL_NAND_ADO13_USB1_DATA5_EMAC0_TXD3_TRACE_D1
HPS_IOA_23_GPI00_I022_SPI1_MISO_SPI0_SS0_N_UART0_TX_I2C0_SDA_NAND_ADO14_USB1_DATA6_EMAC0_RXD2_TRACE_D2
HPS_IOA_24_GPI00_I023_SPI1_SS1_N_SPI0_MISO_UART0_RX_I2C0_SCL_NAND_ADO15_USB1_DATA7_EMAC0_RXD3_TRACE_D3
HPS_IOB_1_GPI01_I00_SPI1_CLK_UART0_CTS_N_EMAC0_PPS0_NAND_ADO0_SDMMC_DATA0_EMAC1_TX_CLK_TRACE_D10
HPS_IOB_2_GPI01_I01_SPI1_MOSI_UART0_RTS_N_EMAC0_PPSTRIG0_NAND_ADO1_SDMMC_DATA1_EMAC1_TX_CTL_TRACE_D9
HPS_IOB_3_GPI01_I02_SPI1_MISO_UART0_TX_I2C0_SDA_NAND_WE_N_SDMMC_CLK_EMAC1_RX_CLK_TRACE_D8
HPS_IOB_4_GPI01_I03_SPI1_SS0_N_UART0_RX_I2C0_SCL_NAND_RE_N_EMAC1_RX_CTL_TRACE_D7
HPS_IOB_5_GPI01_I04_SPI1_SS1_N_SPI1_MISO_UART1_CTS_N_EMAC2_PPS2_NAND_WP_N_SDMMC_WRITE_PROTECT_I3C1_SDA_TRACE_D6
HPS_IOB_6_GPI01_I06_SPI1_MOSI_UART1_RTS_N_EMAC2_PPSTRIG2_NAND_ADO2_SDMMC_DATA2_I3C1_SCL_EMAC1_TXD1_TRACE_D5
HPS_IOB_7_GPI01_I08_SPI1_SS0_N_UART1_TX_I2C1_SDA_NAND_ADO3_SDMMC_DATA3_I3C0_SDA_EMAC1_RXD0_TRACE_D4
HPS_IOB_8_GPI01_I07_SPI1_MISO_UART1_RX_I2C1_SCL_NAND_CLE_SDMMC_CMD_I3C0_SCL_EMAC1_RXD1_TRACE_D15
HPS_IOB_9_GPI01_I08_SPI1_CLK_SPI0_CLK_MDI02_MDI0_I2C_EMAC2_SDA_NAND_ADO4_SDMMC_DATA4_EMAC1_TXD2_TRACE_D14
HPS_IOB_10_GPI01_I09_JTAG_TMS_SPI0_MOSI_MDI02_MDC_I2C_EMAC2_SCL_NAND_ADO5_SDMMC_DATA5_EMAC1_TXD3_TRACE_D13
HPS_IOB_11_GPI01_I10_JTAG_TDO_SPI0_SS0_N_MDI00_MDI0_I2C_EMAC0_SDA_NAND_ADO6_SDMMC_DATA6_EMAC1_RXD2_TRACE_D12
HPS_IOB_12_GPI01_I11_JTAG_TDI_SPI0_MISO_MDI00_MDC_I2C_EMAC0_SCL_NAND_ADO7_SDMMC_DATA7_EMAC1_RXD3_TRACE_D11
HPS_IOB_13_GPI01_I012_I2C1_SDA_NAND_ALE_SDMMC_PU_PD_DATA2_EMAC2_TX_CLK_TRACE_D10
HPS_IOB_14_GPI01_I013_I2C1_SCL_NAND_RB_N_SDMMC_PWR_ENA_EMAC2_TX_CTL_TRACE_D9
HPS_IOB_15_GPI01_I014_UART1_TX_NAND_CE_N_I3C1_SDA_EMAC2_RX_CLK_TRACE_D8
HPS_IOB_16_GPI01_I015_UART1_RX_NAND_DQS_SDMMC_DATA_STROBE_I3C1_SCL_EMAC2_RX_CTL_TRACE_D7
HPS_IOB_17_GPI01_I016_UART1_CTS_N_NAND_ADO8_I3C0_SDA_EMAC2_TXD0_TRACE_D6
HPS_IOB_18_GPI01_I017_SPI0_SS1_N_UART1_RTS_N_NAND_ADO9_I3C0_SCL_EMAC2_TXD1_TRACE_D5
HPS_IOB_19_GPI01_I018_SPI0_MISO_MDI01_MDI0_I2C_EMAC1_SDA_NAND_ADO10_EMAC2_RXD0_TRACE_D4
HPS_IOB_20_GPI01_I019_SPI0_SS0_N_MDI01_MDC_I2C_EMAC1_SCL_NAND_ADO11_EMAC2_RXD1_TRACE_CLK
HPS_IOB_21_GPI01_I020_SPI0_CLK_SPI1_CLK_I2C_EMAC2_SDA_NAND_ADO12_EMAC2_TXD2_TRACE_D0
HPS_IOB_22_GPI01_I021_SPI0_MOSI_SPI1_MOSI_I2C_EMAC2_SDA_NAND_ADO13_EMAC2_TXD3_TRACE_D1
HPS_IOB_23_GPI01_I022_SPI0_MISO_SPI1_SS0_N_MDI00_MDI0_I2C_EMAC0_SDA_NAND_ADO14_EMAC2_RXD2_TRACE_D2
HPS_IOB_24_GPI01_I023_SPI0_SS0_N_SPI1_MISO_MDI00_MDC_I2C_EMAC0_SCL_NAND_ADO15_EMAC2_RXD3_TRACE_D3

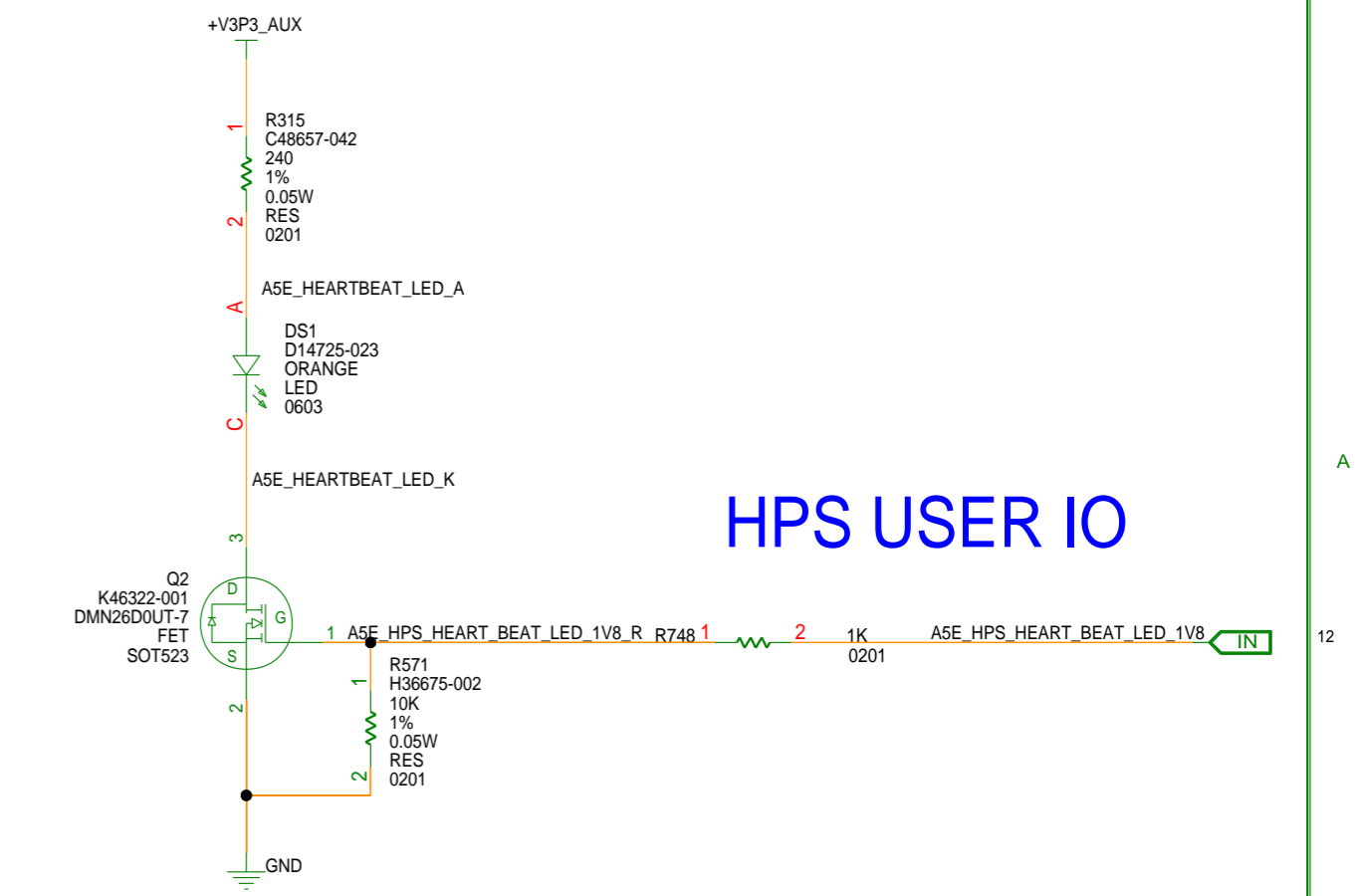
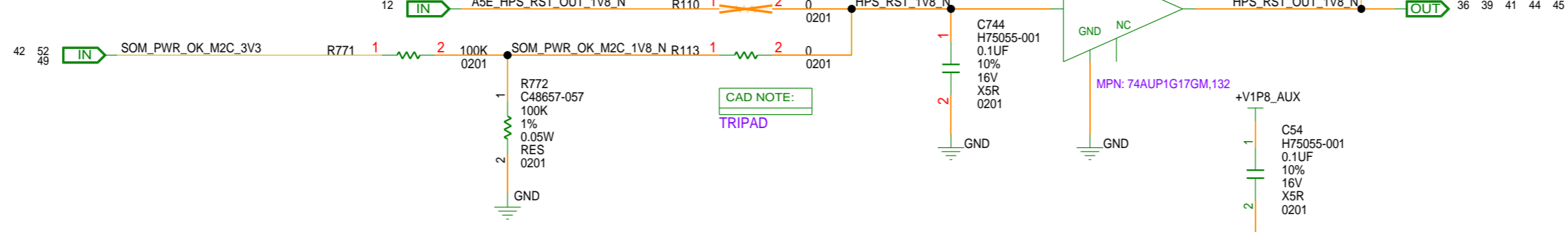
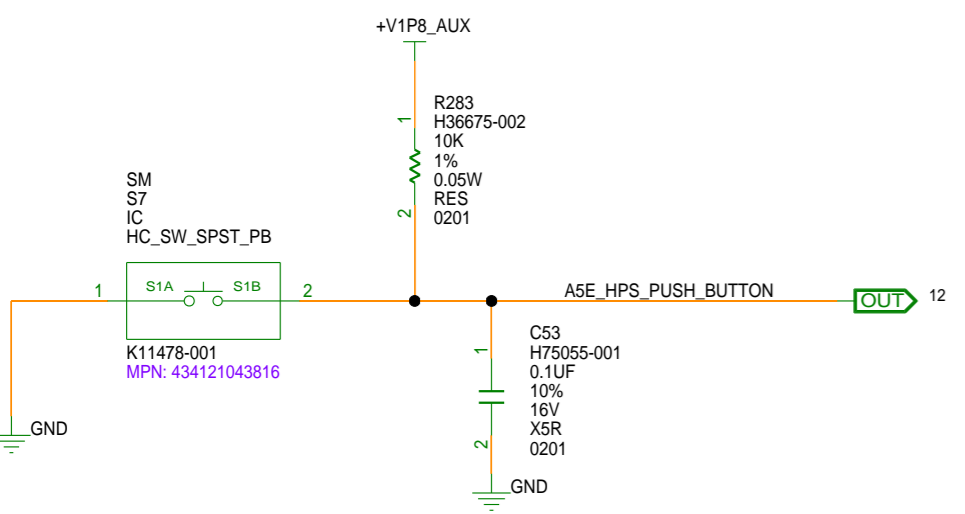
HPS BANK
2 OF 32

HPS PUSH BUTTON SWITCH

HPS RESET OUT

HEART BEAT LED

HPS USER IO



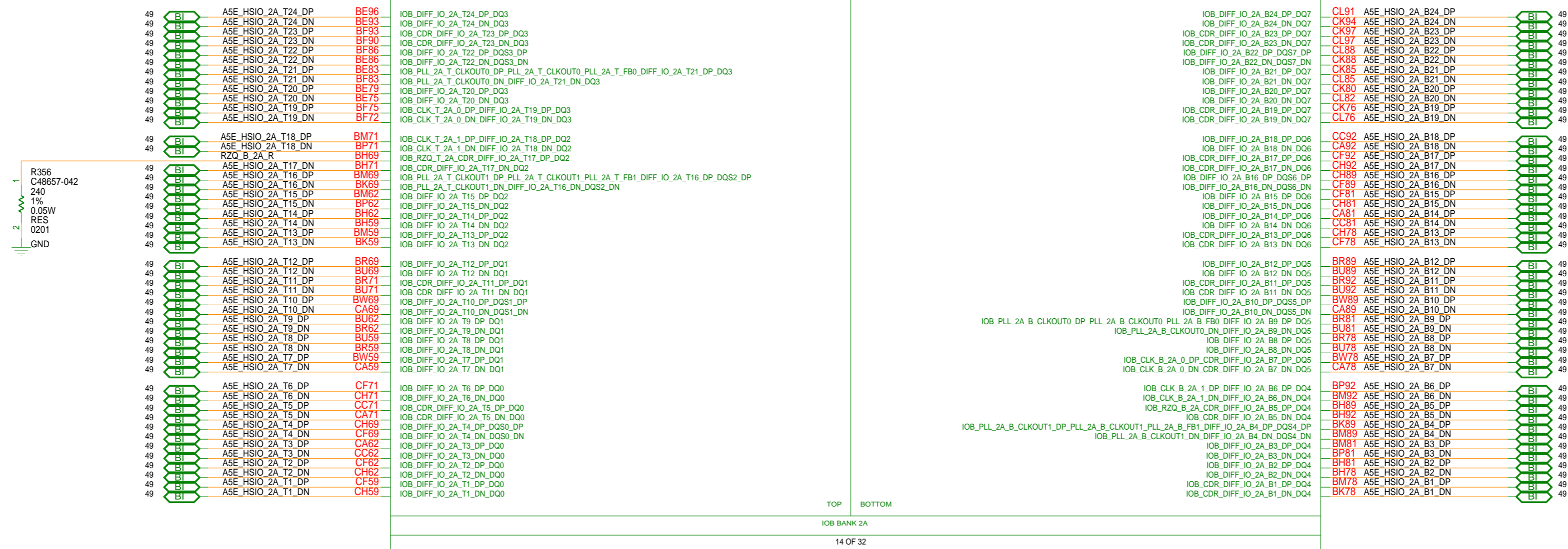
B

B

A

A

BGA
U9
IC
HC_SM72_SM42_1591A_SOM



AG5E BANK- IO96B-2A

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING		SHEET	13 OF 62

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SWIZZLING ON BANK 2B

BYTE_SWIZZLE_CH0=1,X,X,X,0,2,3,ECC;
 PIN_SWIZZLE_CH0_DQS0=7,5,1,3,4,2,0,6;
 PIN_SWIZZLE_CH0_DQS1=9,15,13,11,14,12,8,10;
 PIN_SWIZZLE_CH0_DQS2=19,23,21,17,16,18,20,22;
 PIN_SWIZZLE_CH0_DQS3=31,29,27,25,26,30,24,28;
 PIN_SWIZZLE_CH0_ECC=6,4,0,2,5,7,3,1;

BL4 - DQ0

BL5 - DQ2

BL6 - DQ3

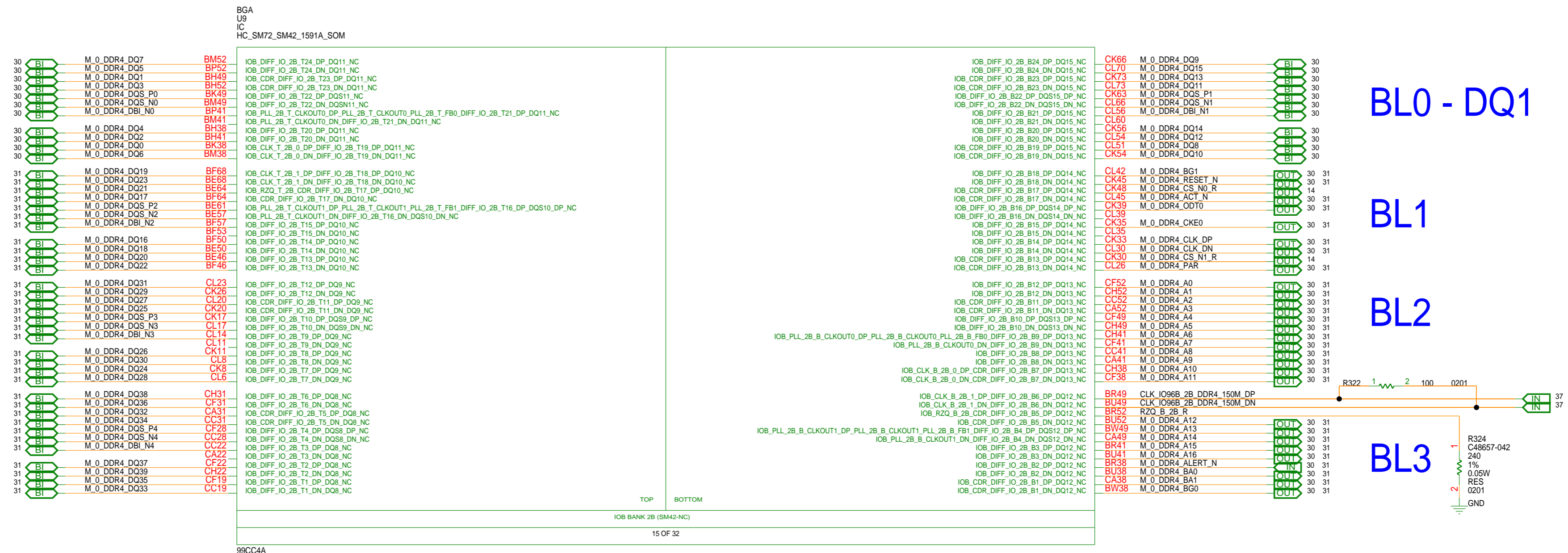
BL7 - ECC

BL0 - DQ1

BL1

BL2

BL3



AG5E BANK- IO96B-2B

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 14 OF 62

SWIZZLING ON BANK 3A

BYTE_SWIZZLE_CH0=0,X,X,X,1,2,3,ECC;
 PIN_SWIZZLE_CH0_DQS0=2,0,6,4,7,5,3,1;
 PIN_SWIZZLE_CH0_DQS1=14,11,12,8,10,9,13,15;
 PIN_SWIZZLE_CH0_DQS2=16,20,22,18,23,21,19,17;
 PIN_SWIZZLE_CH0_DQS3=26,30,28,24,25,27,29,31;
 PIN_SWIZZLE_CH0_ECC=4,6,2,0,1,7,5,3;

BL4 - DQ1

BL5 - DQ2

BL6 - DQ3

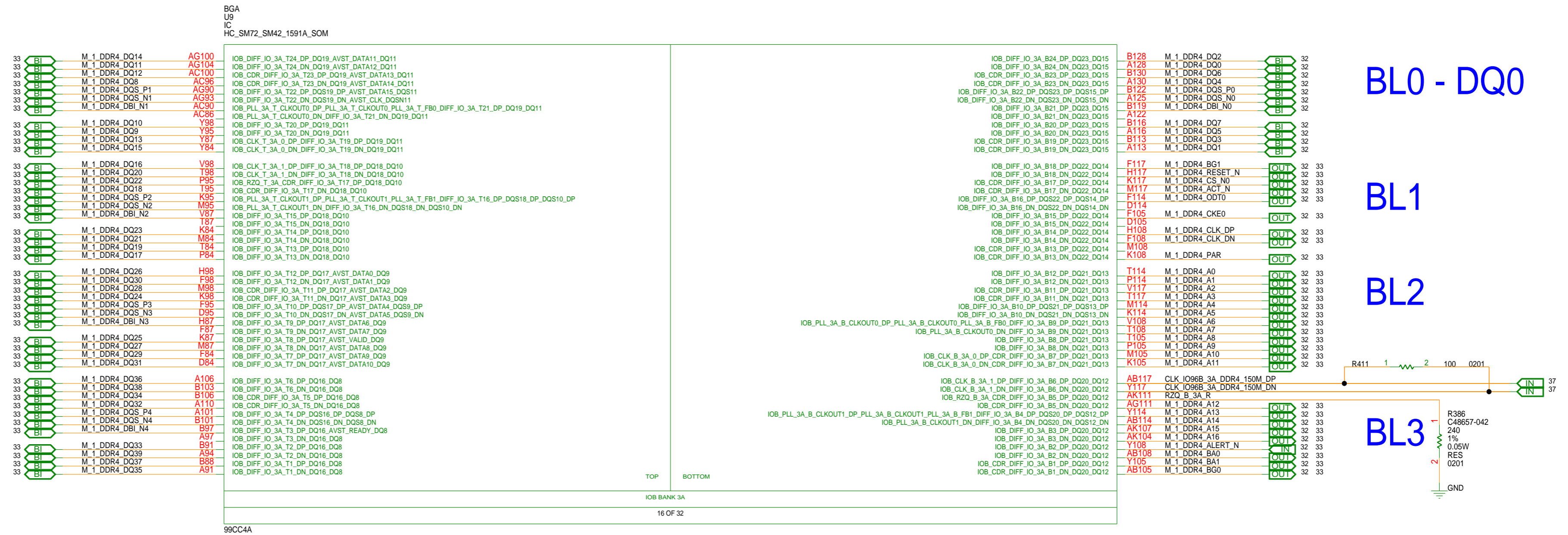
BL7 - ECC

BL0 - DQ0

BL1

BL2

BL3



AG5E BANK- IO96B-3A

DEPARTMENT	altera An Intel Company	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330723-B1	REV 2.1
		SCALE:	DO NOT SCALE DRAWING		SHEET 15 OF 62

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SWIZZLING ON BANK 3B

BYTE_SWIZZLE_CH0=0,X,X,X,1,2,3,ECC;
 PIN_SWIZZLE_CH0_DQS0=2,0,6,4,7,3,5,1;
 PIN_SWIZZLE_CH0_DQS1=12,14,13,10,8,11,15,9;
 PIN_SWIZZLE_CH0_DQS2=16,17,18,19,20,21,22,23;
 PIN_SWIZZLE_CH0_DQS3=24,25,26,27,28,29,30,31;
 PIN_SWIZZLE_CH0_ECC=0,2,6,4,1,3,7,5;

BL4 - DQ1

BL5 - DQ2

BL6 - DQ3

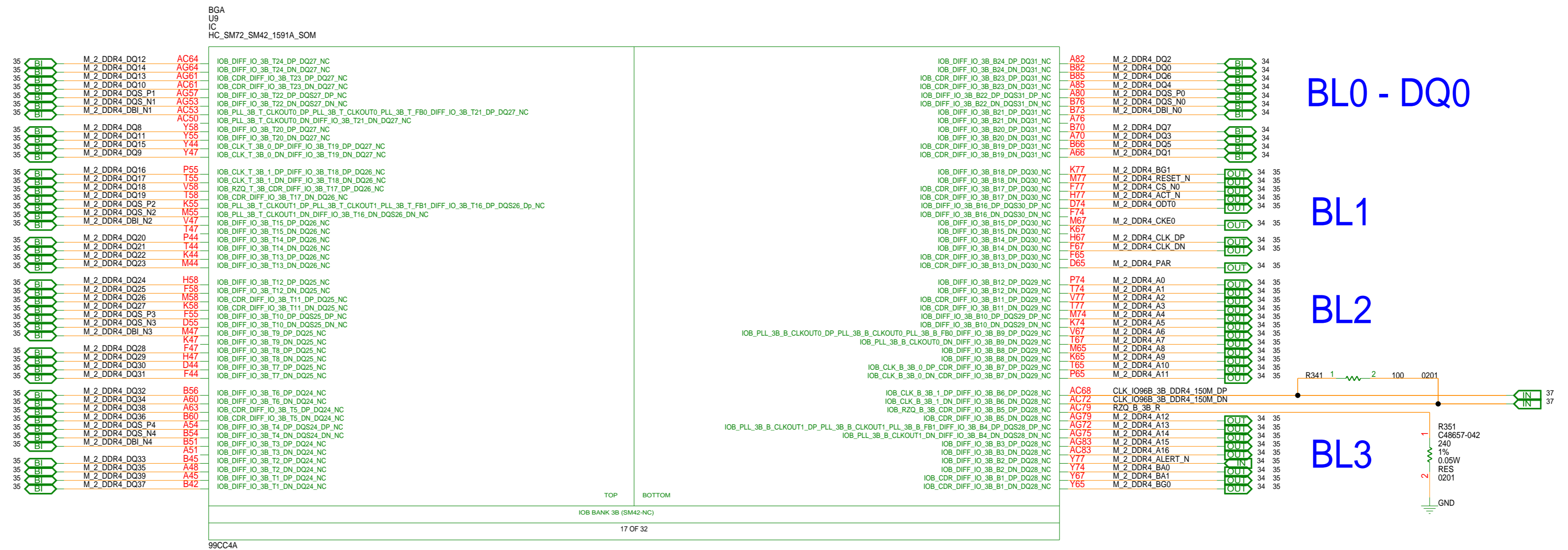
BL7 - ECC

BL0 - DQ0

BL1

BL2

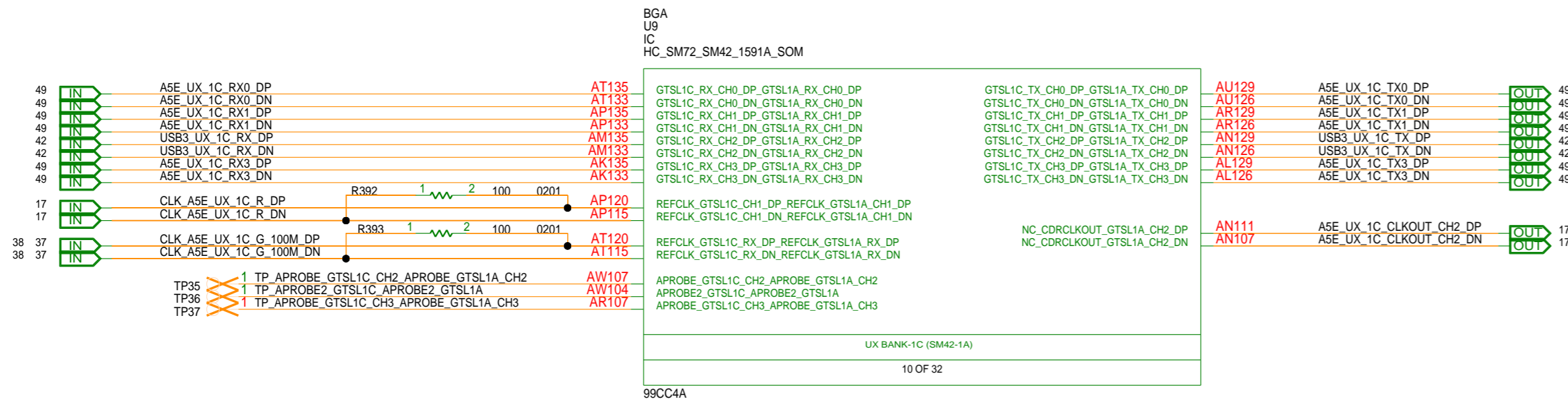
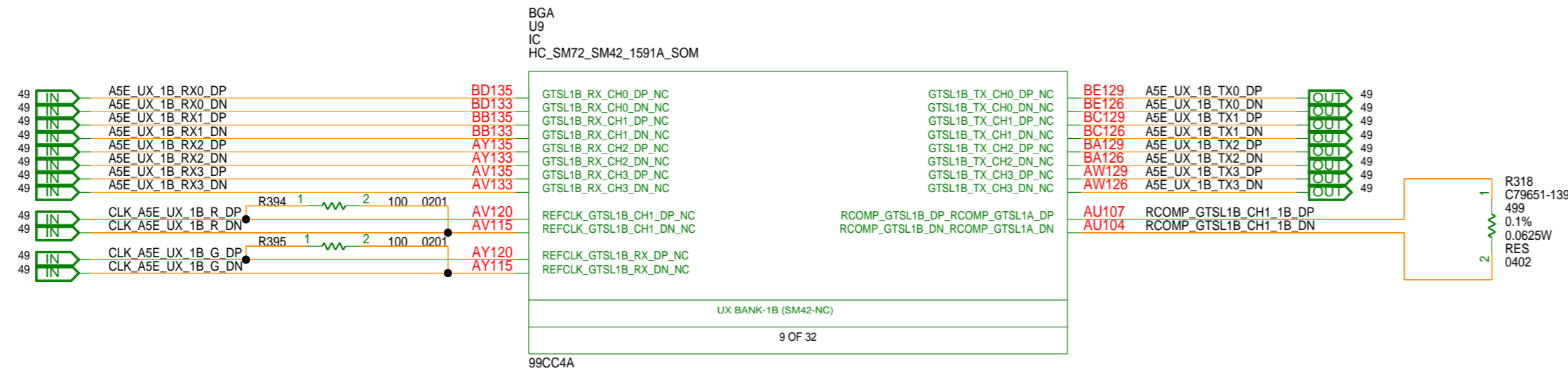
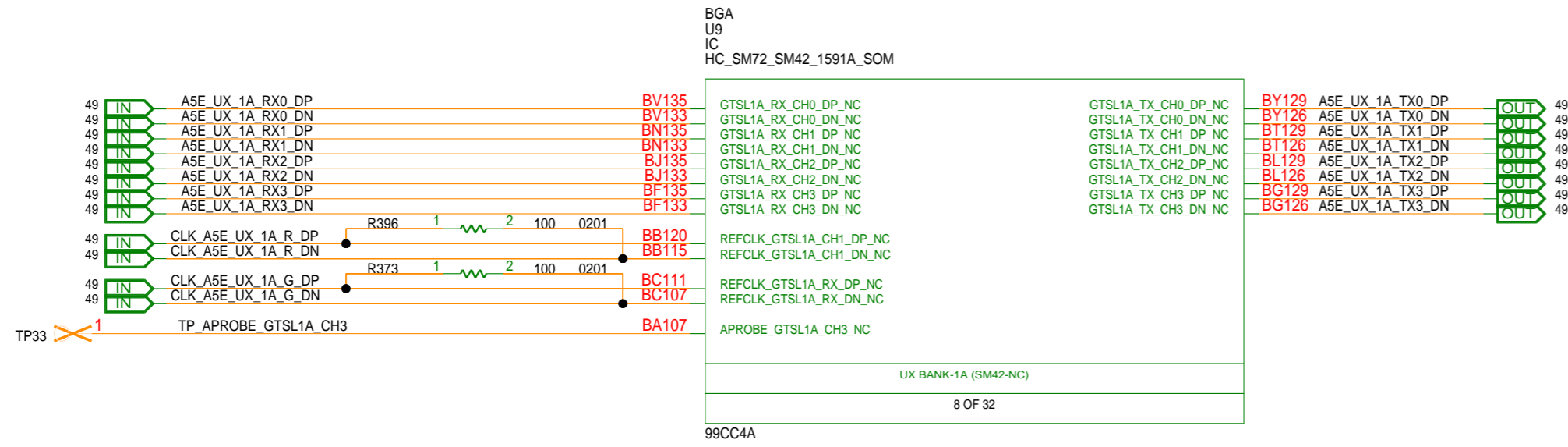
BL3



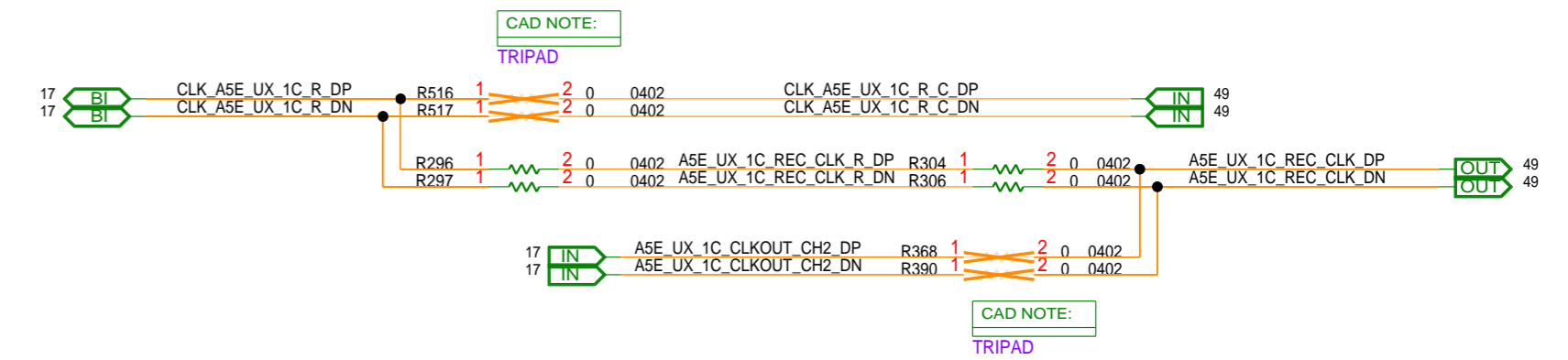
AG5E BANK- IO96B-3B

DEPARTMENT	altera An Intel Company	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330723-B1	REV 2.1
SCALE:		DO NOT SCALE DRAWING		SHEET 16 OF 62	

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1C REC CLOCK



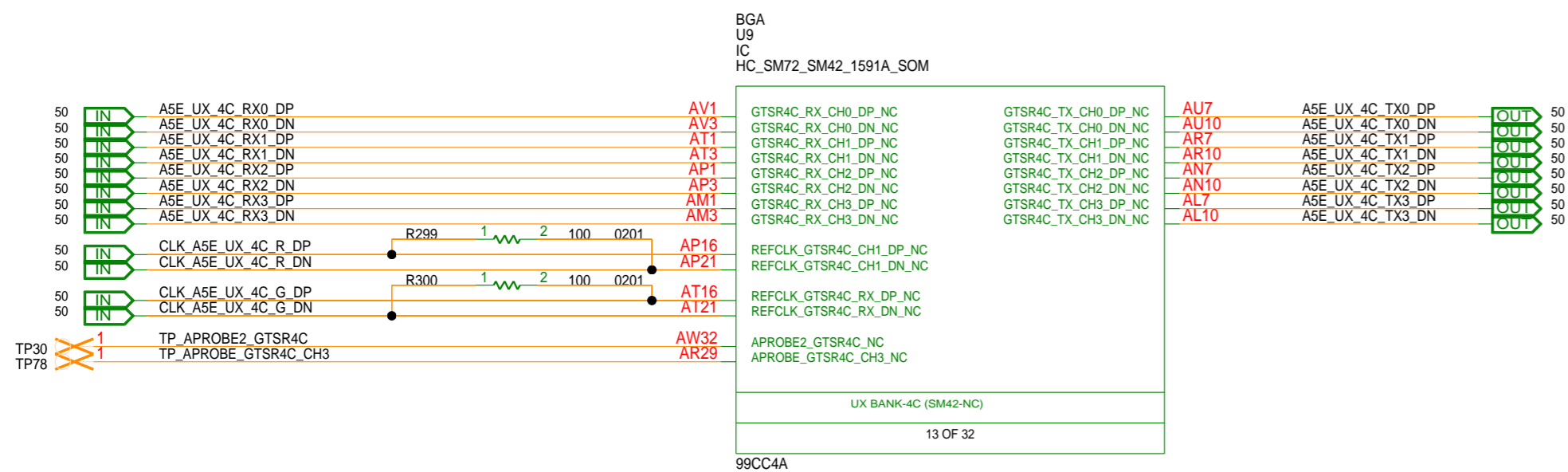
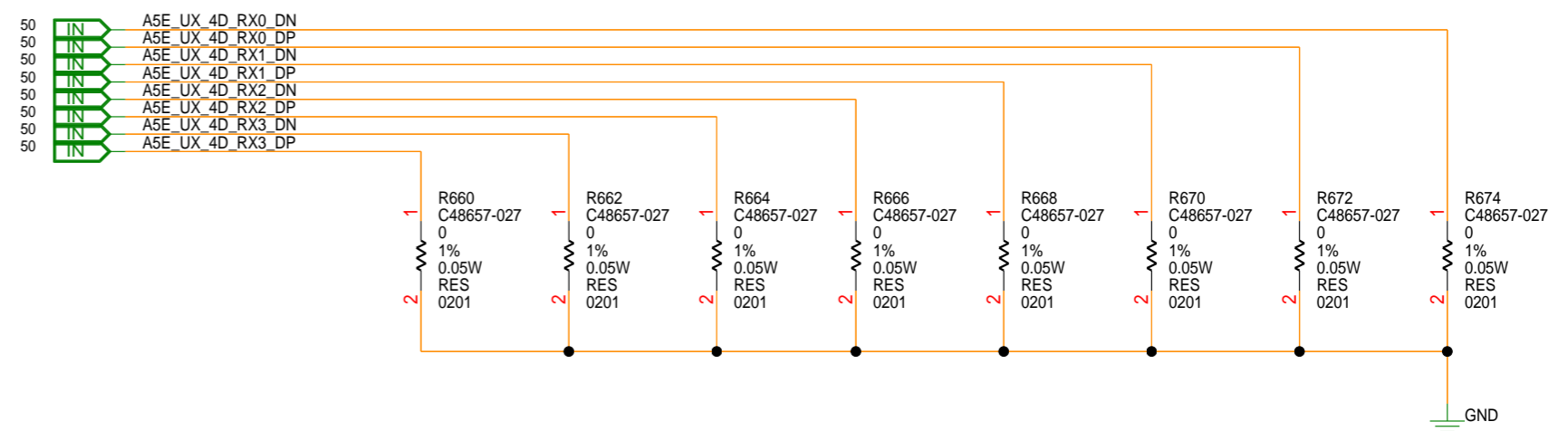
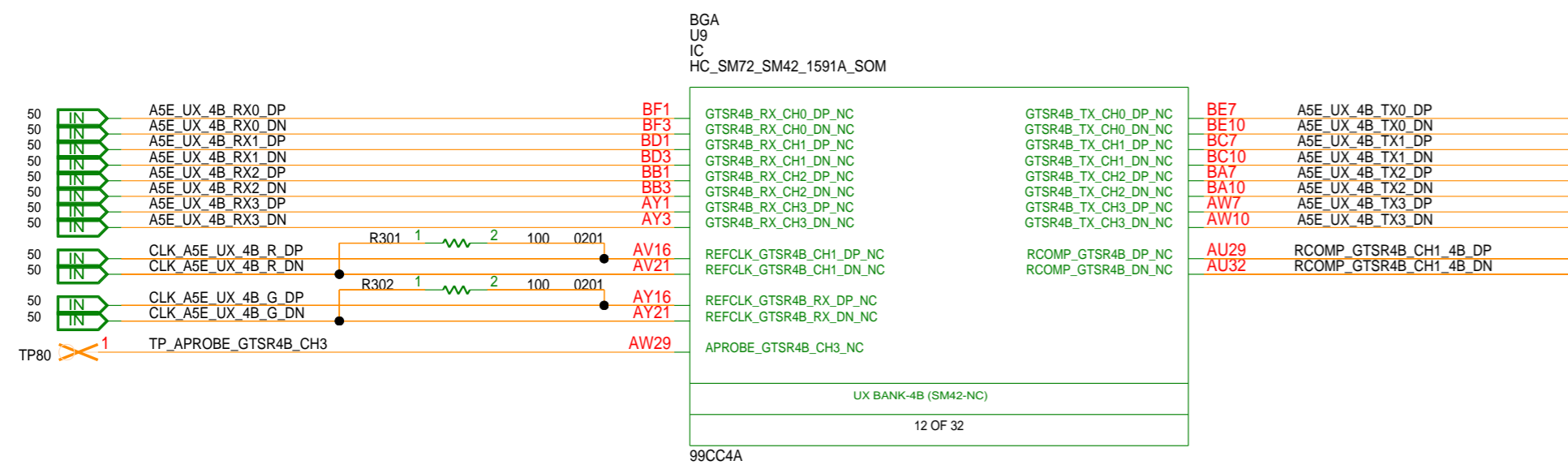
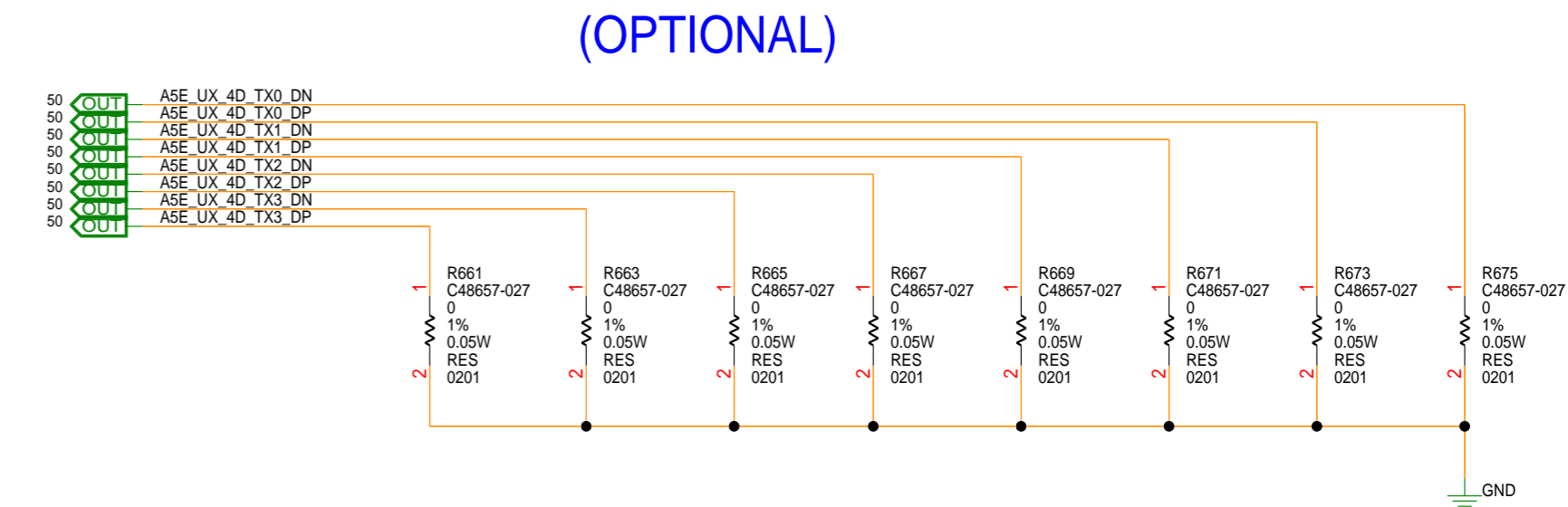
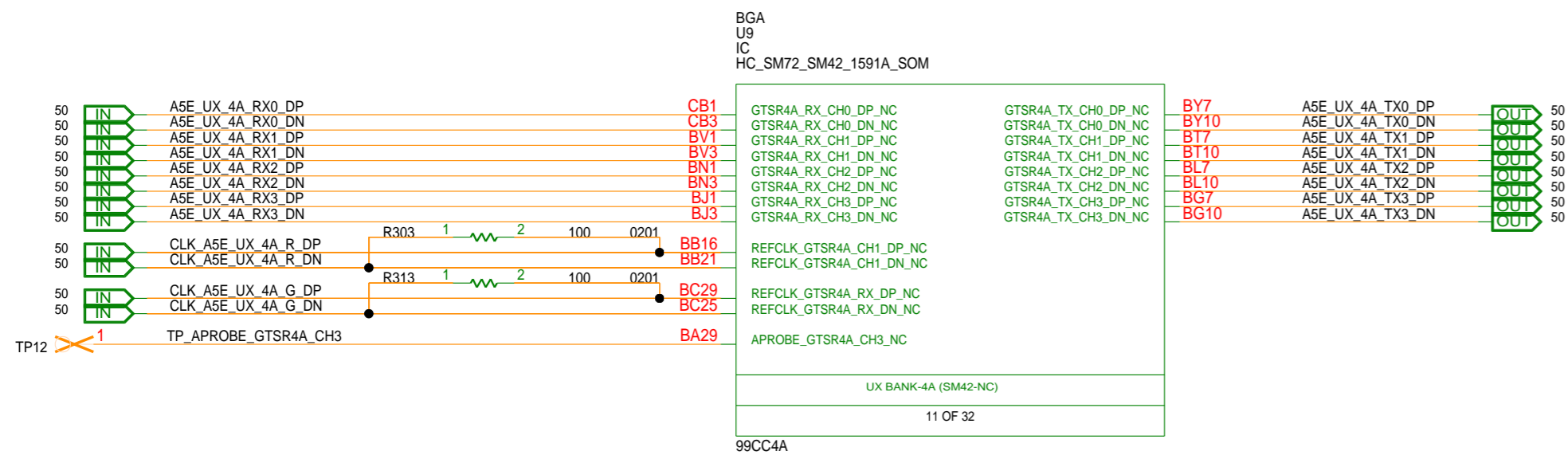
Mon Oct 14 15:08:55 2024

AG5E BANK- UX -1A ,1B,1C

DEPARTMENT



SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330723-B1	REV 2.1
SCALE:	DO NOT SCALE DRAWING		SHEET 17 OF 62

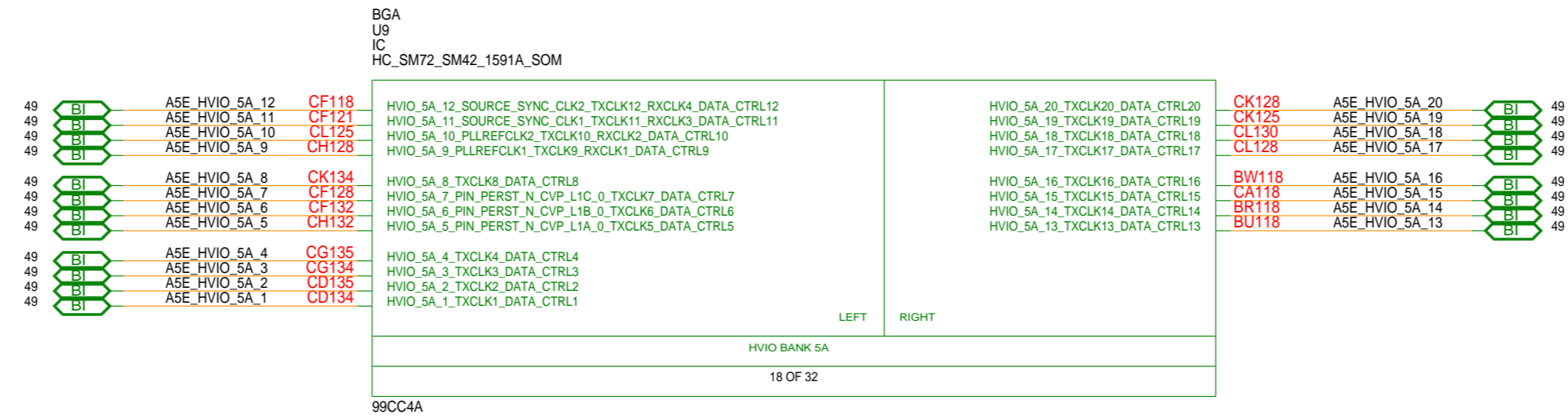


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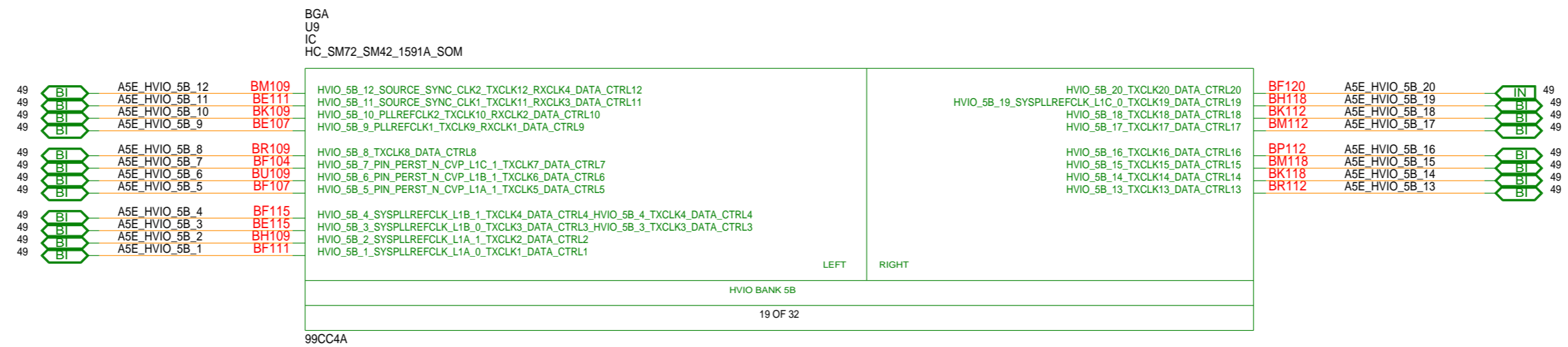
AG5E BANK- UX - 4A,4B.4C

DEPARTMENT	<p>An Intel Company</p>	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 18 OF 62

BANK 5A



BANK 5B



AG5E BANK - HVIO - 5A,5B

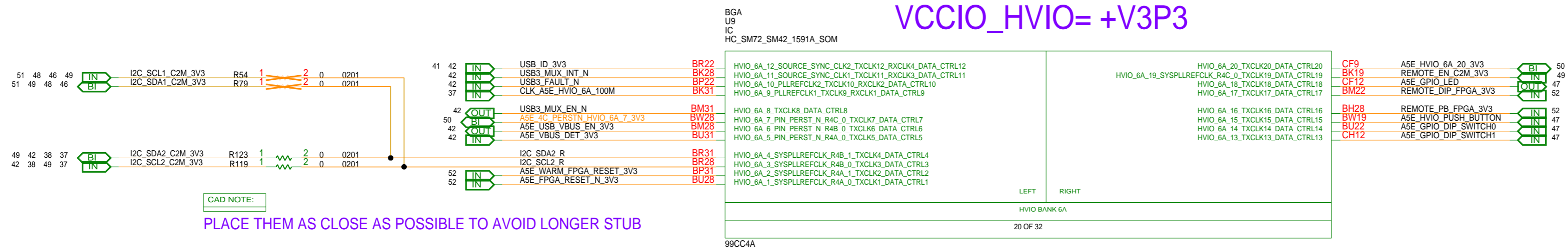
DEPARTMENT



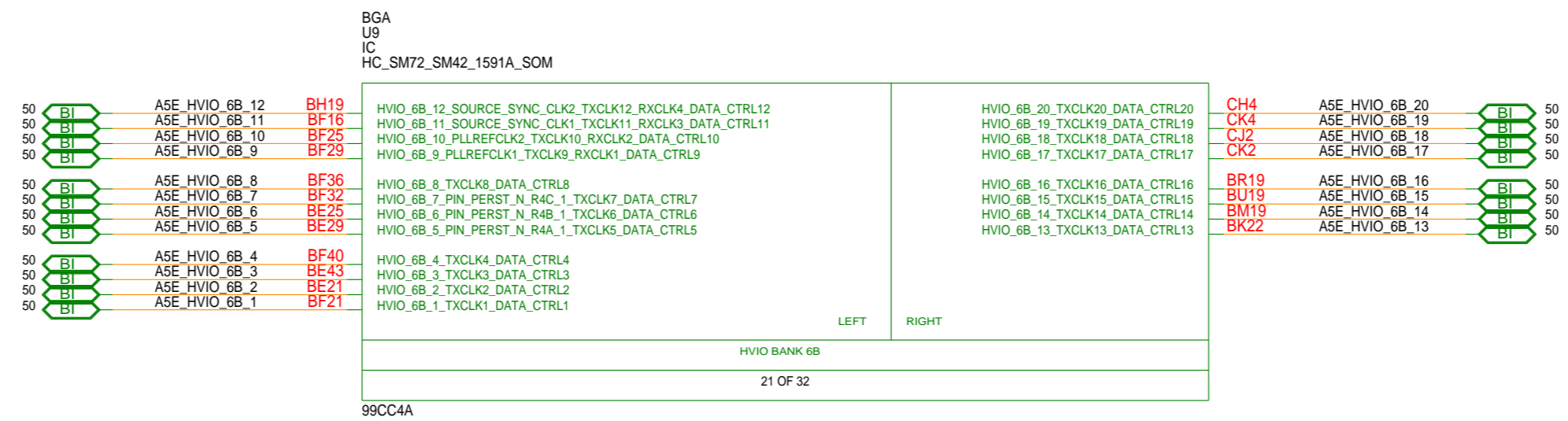
SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330723-B1	REV 2.1
SCALE:		DO NOT SCALE DRAWING	SHEET 19 OF 62

Mon Sep 30 16:21:28 2024

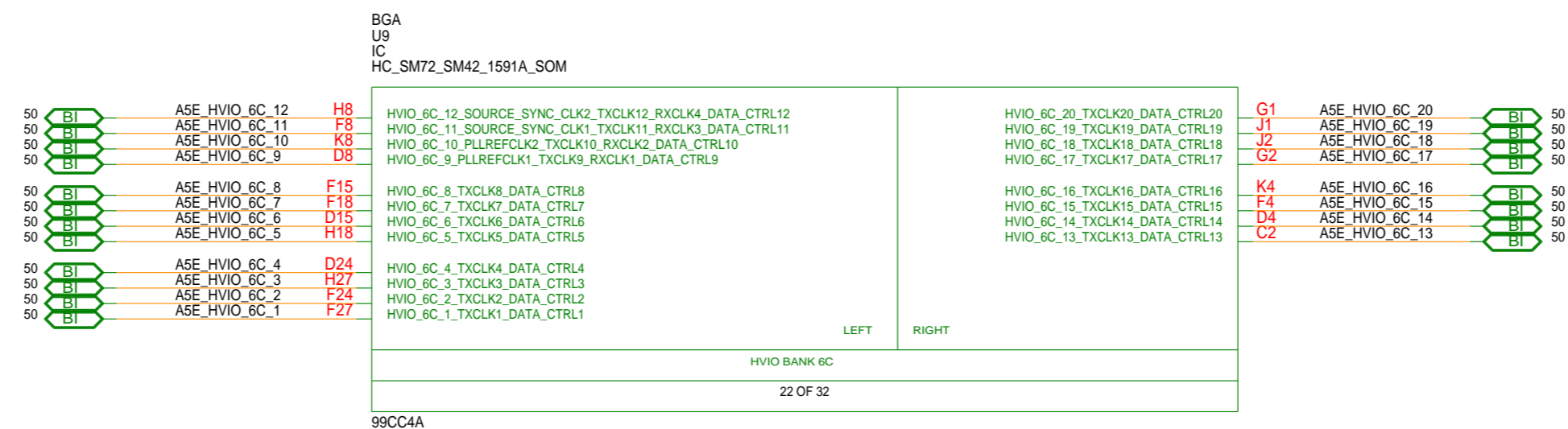
BANK 6A



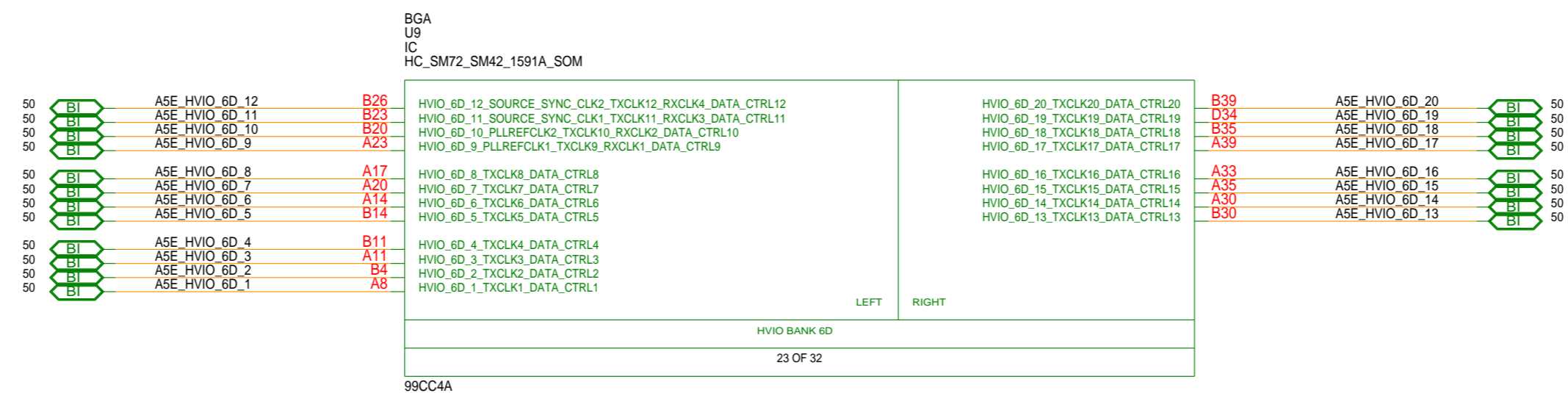
BANK 6B



BANK 6C



BANK 6D



Mon Sep 30 16:21:30 2024

AG5E BANK - HVIO - 6C,6D

DEPARTMENT



SIZE

C+

CODE

34649

DOCUMENT NUMBER

150-0330723-B1

REV

2.1

SCALE:

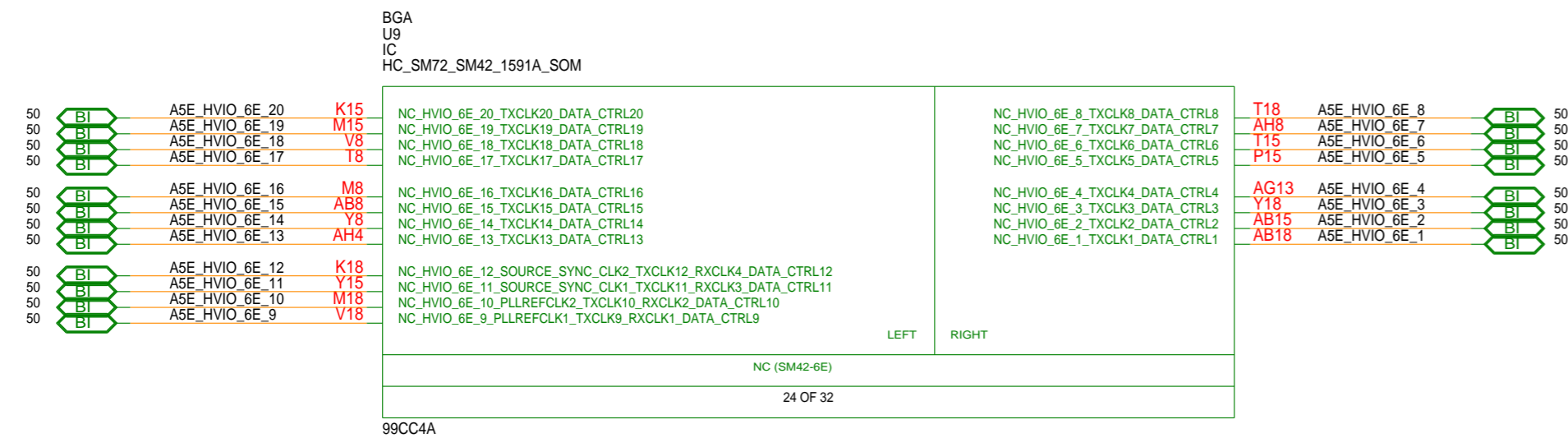
DO NOT SCALE DRAWING

SHEET

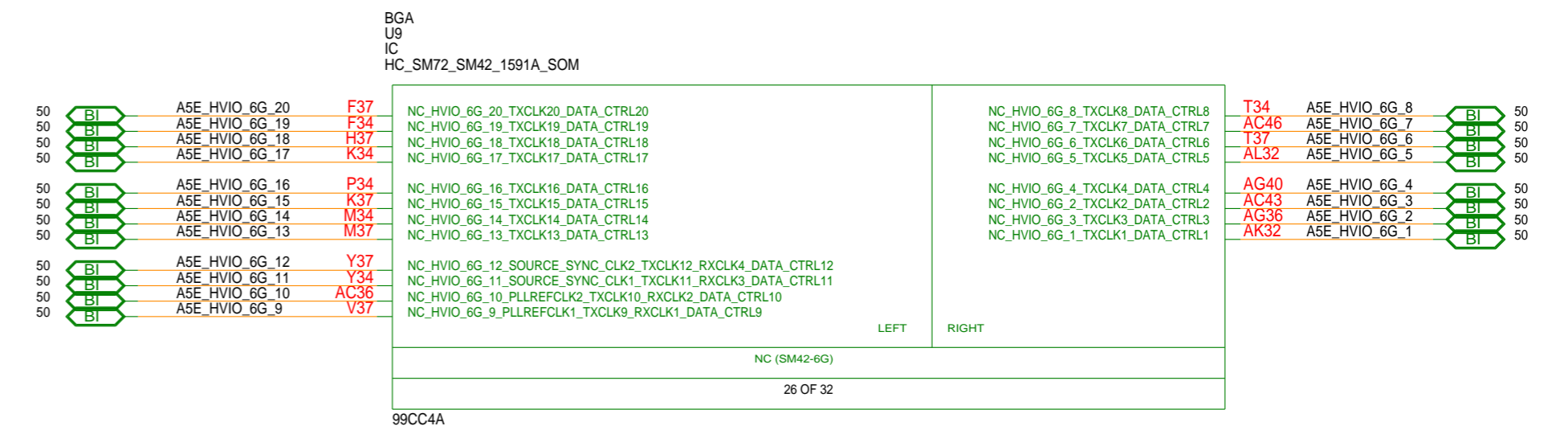
21 OF 62

(OPTIONAL)

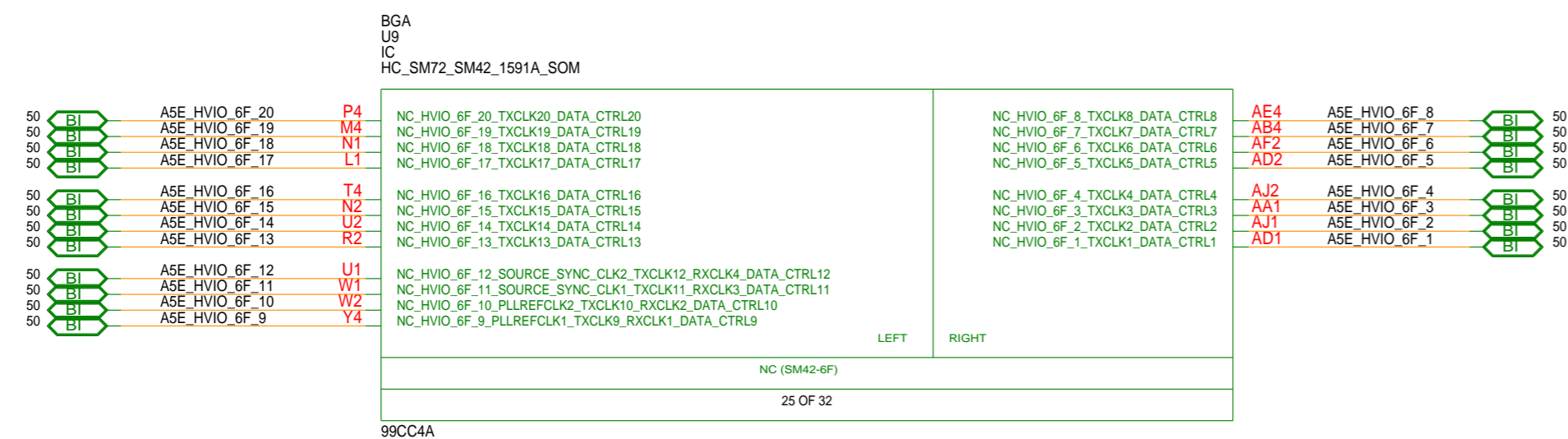
BANK 6E



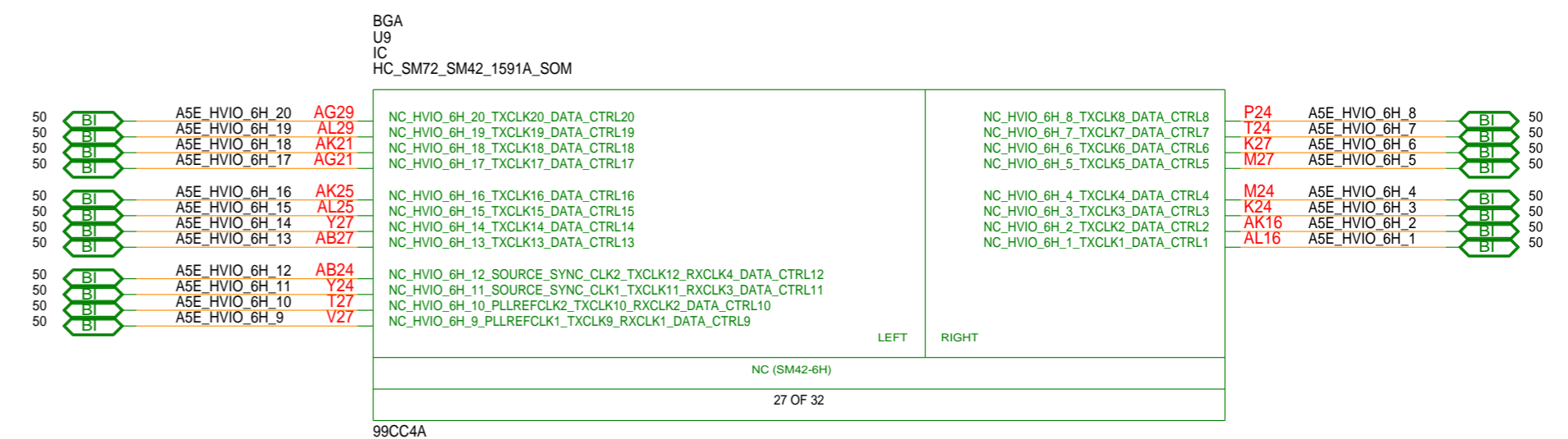
BANK 6G

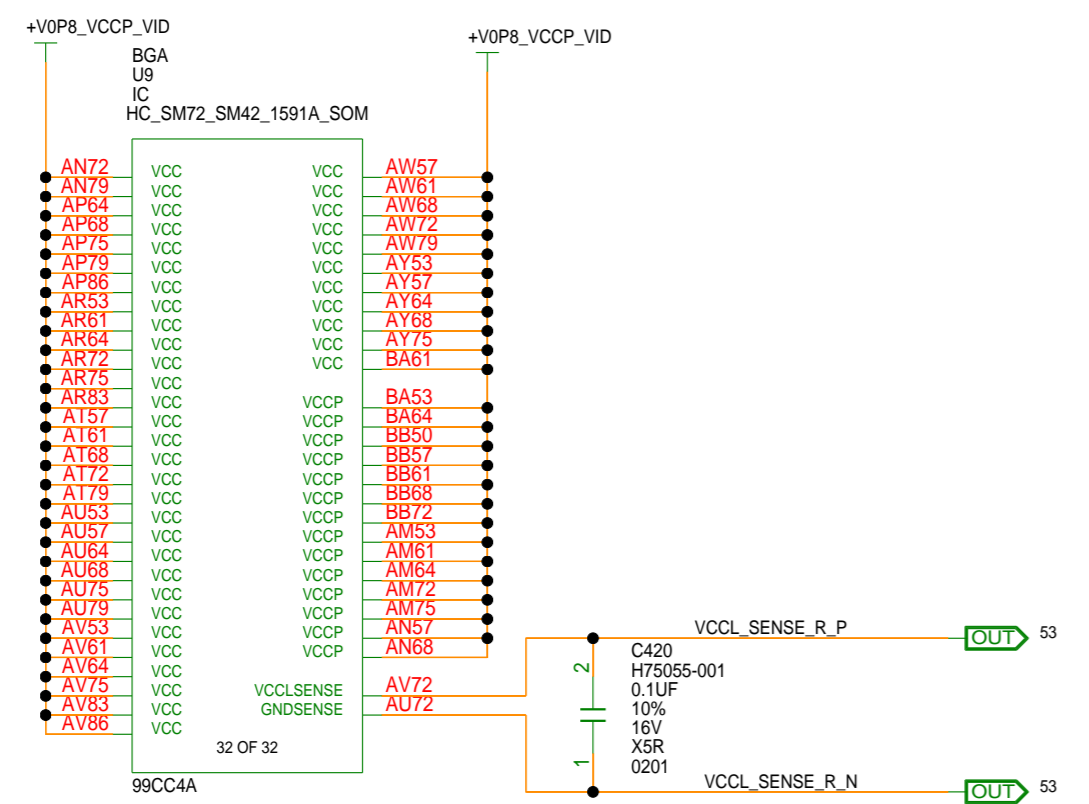


BANK 6F

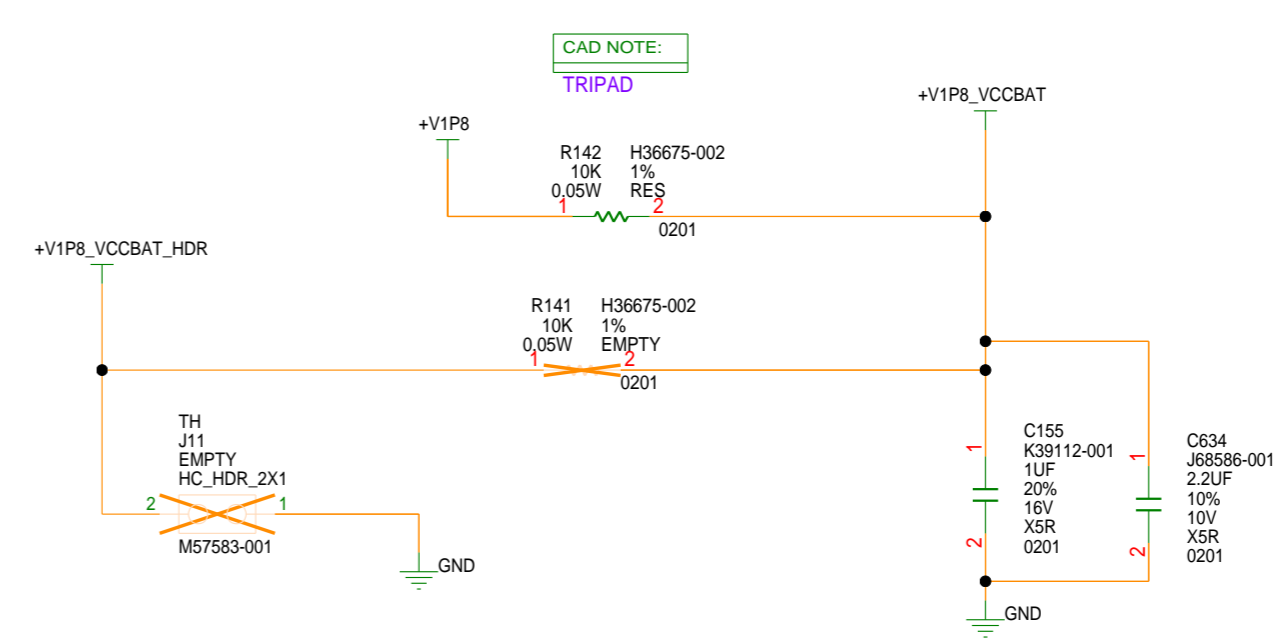
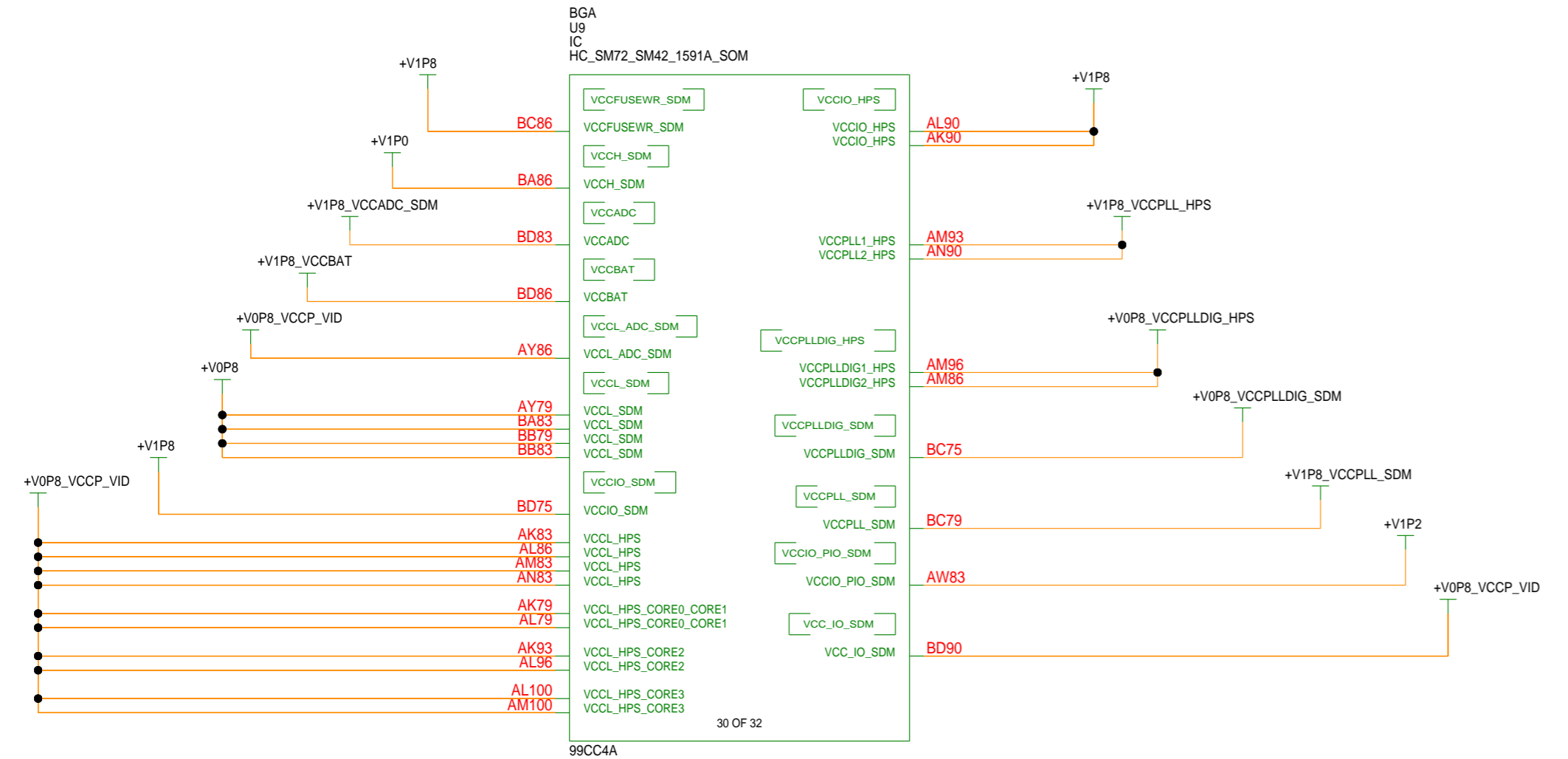
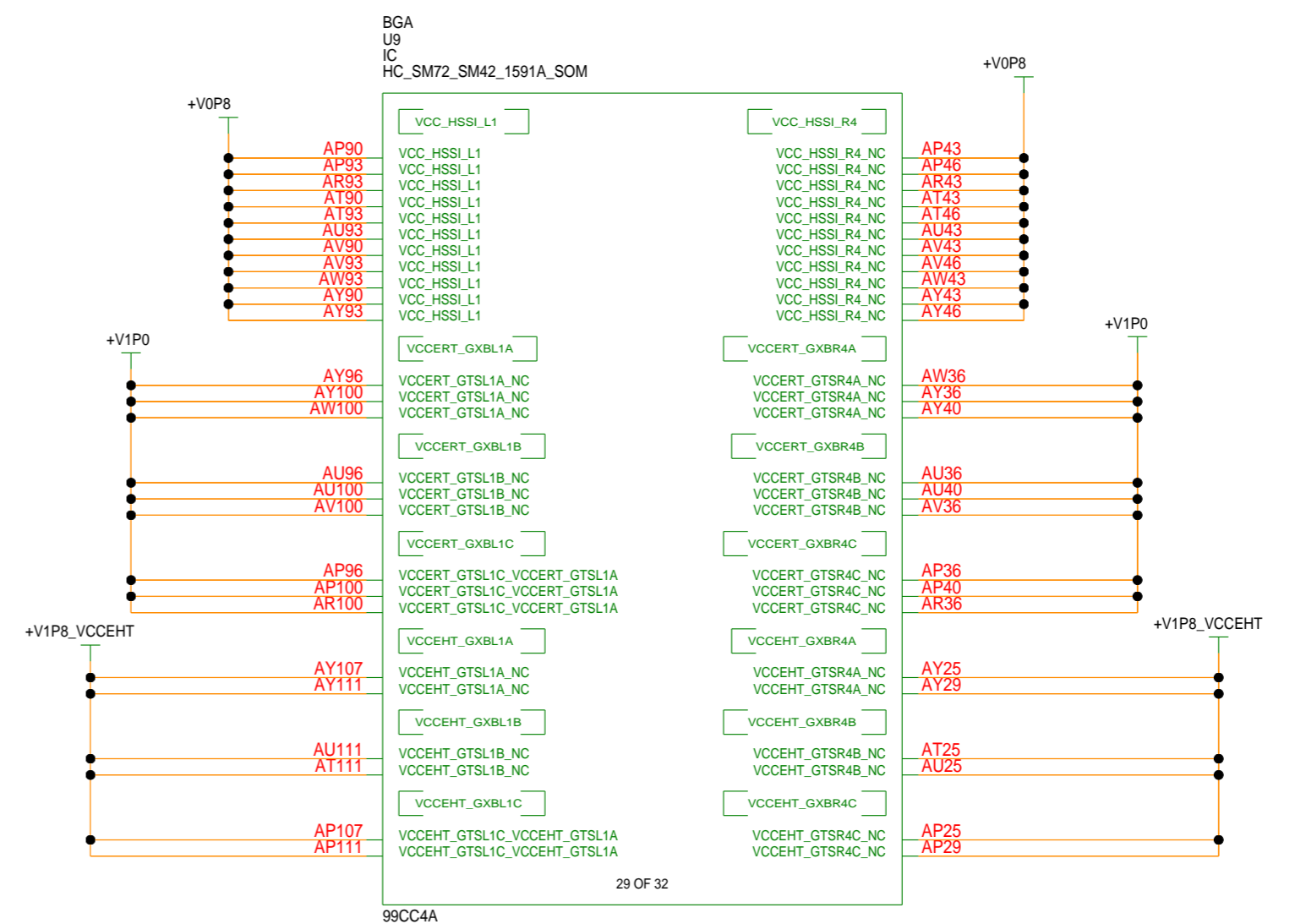


BANK 6H





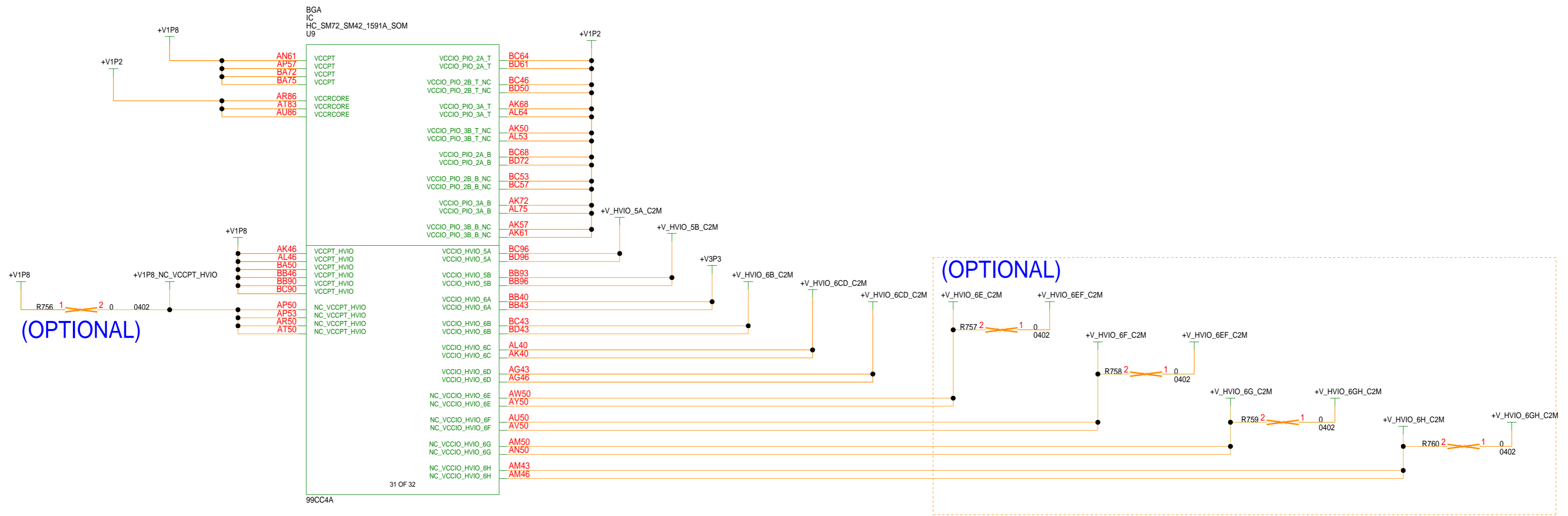
CAD NOTE:
PLACE CAP RIGHT BELOW FPGA BALLS
ON THE BREAKOUT VIAS.



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AG5E - POWER

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 23 OF 62

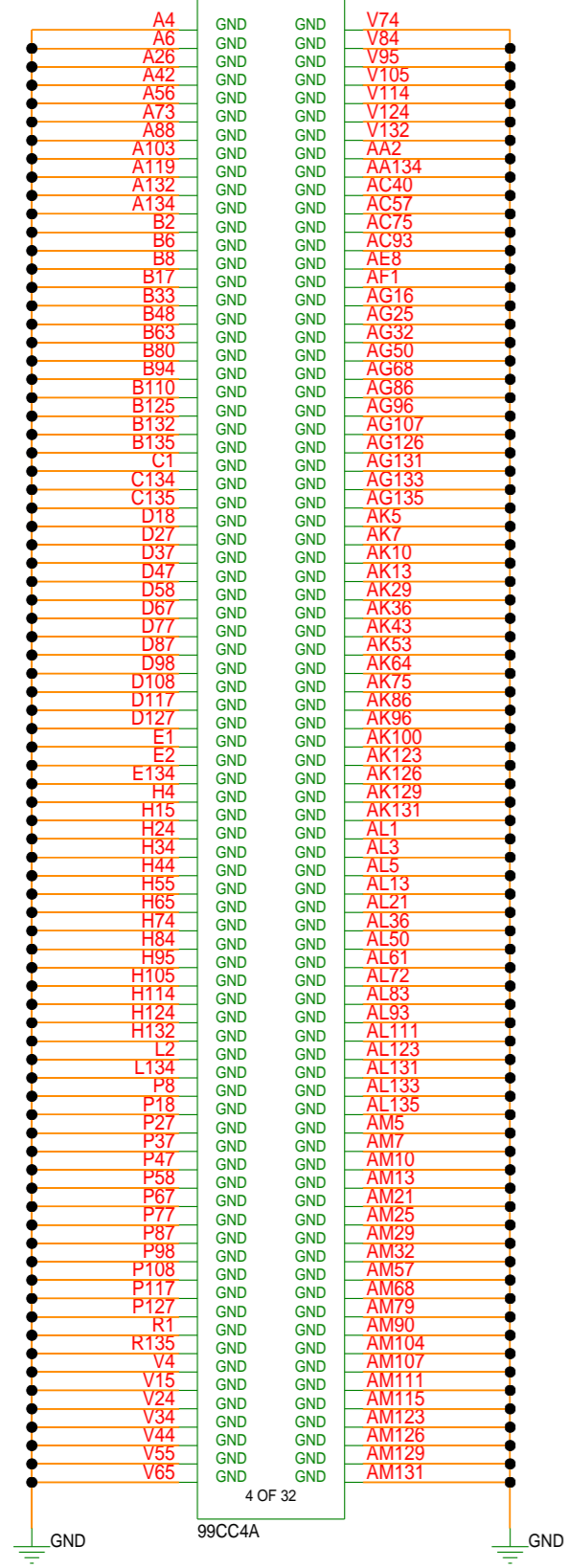


AG5E - POWER

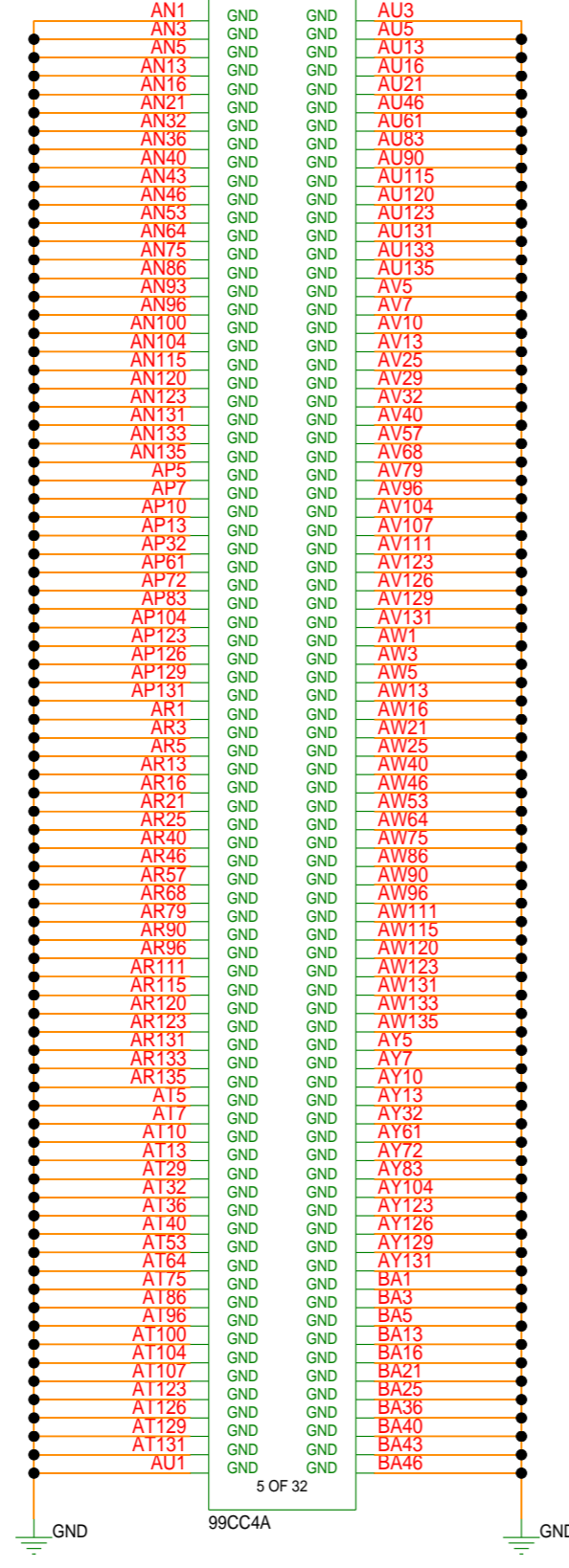
Mon Oct 14 15:09:11 2024

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 24 OF 62

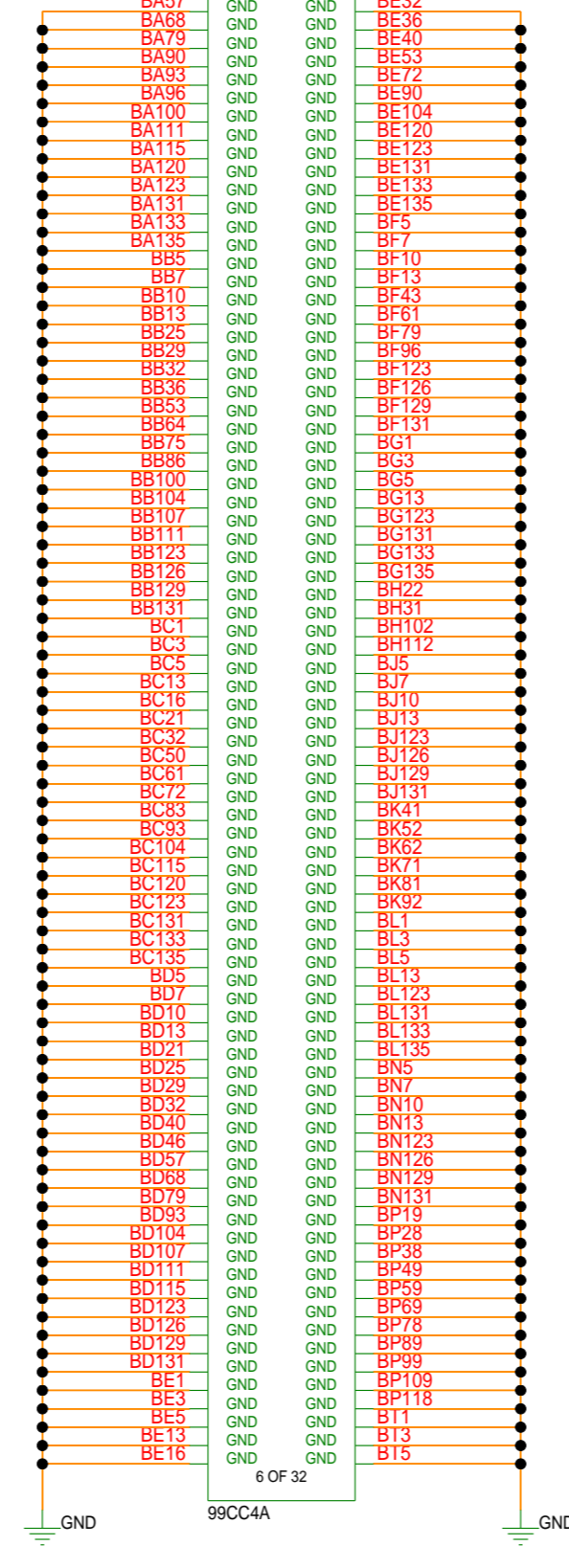
BGA
U9
IC
HC_SM72_SM42_1591A_SOM



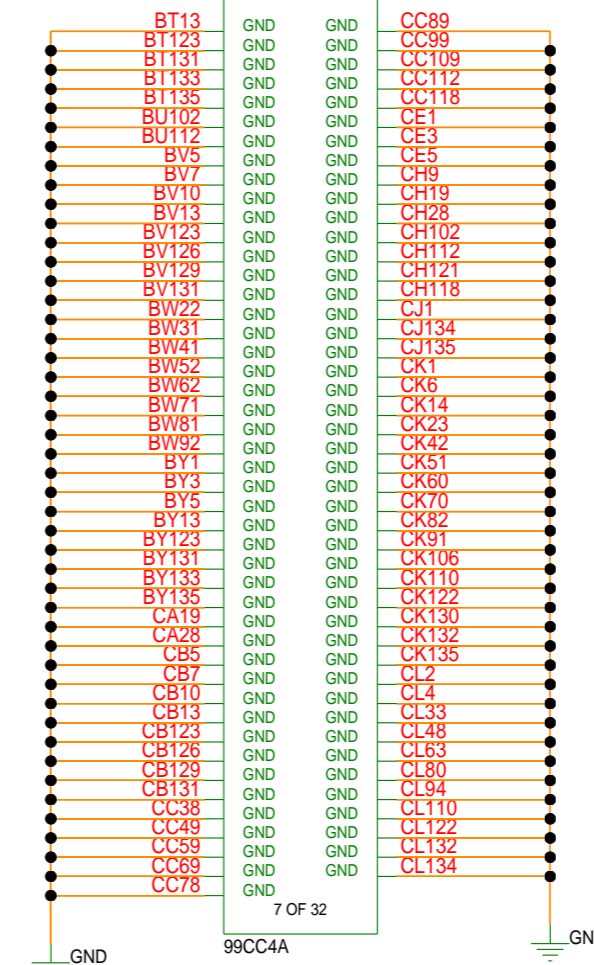
BGA
U9
IC
HC_SM72_SM42_1591A_SOM



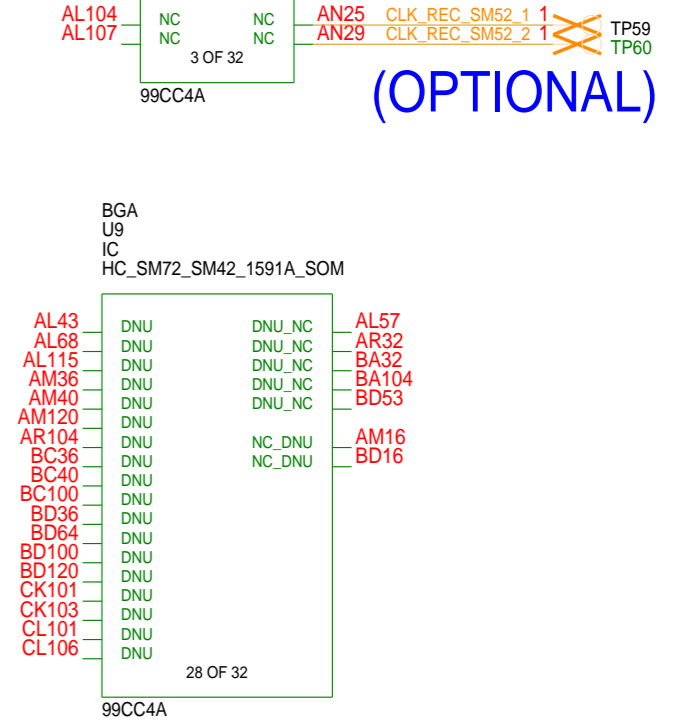
BGA
U9
IC
HC_SM72_SM42_1591A_SOM



BGA
U9
IC
HC_SM72_SM42_1591A_SOM



BGA
U9
IC
HC_SM72_SM42_1591A_SOM

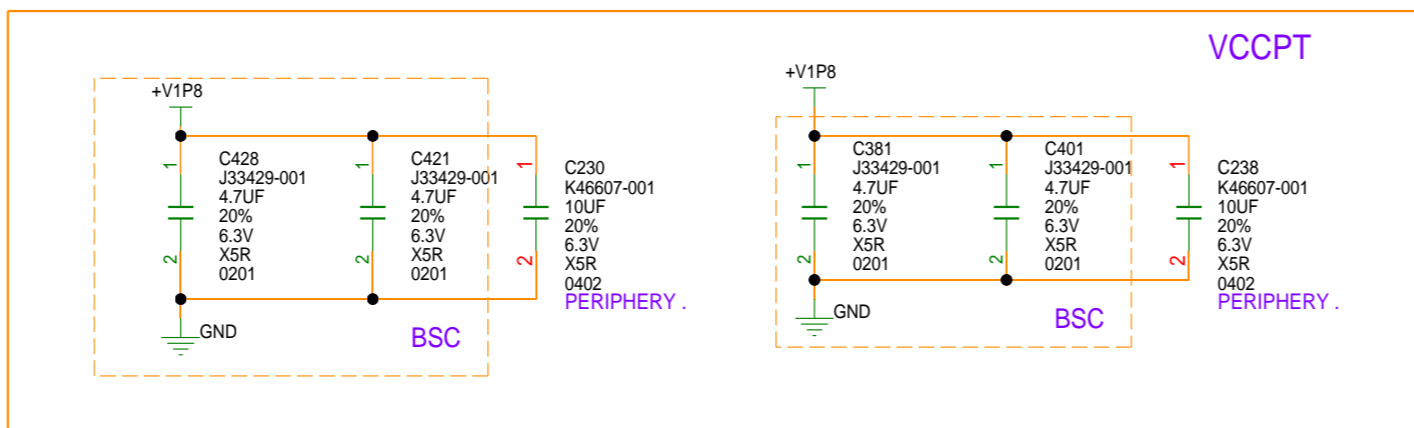
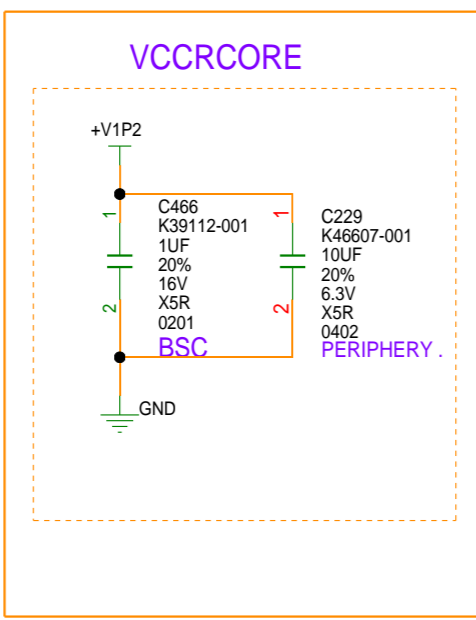
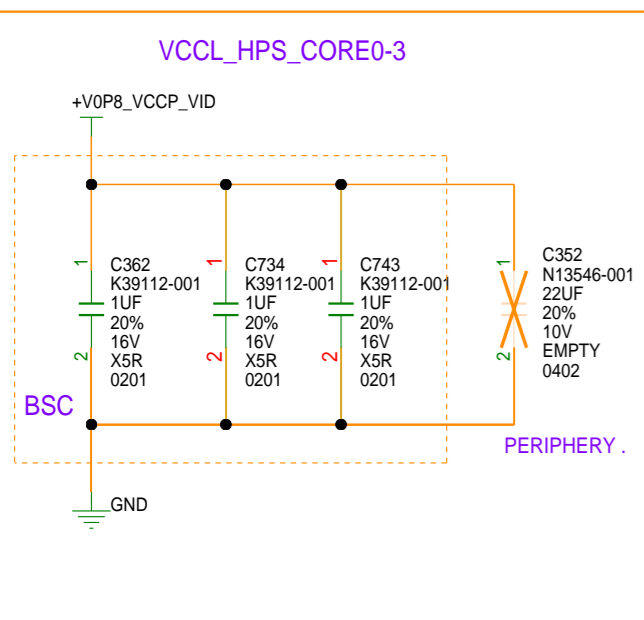
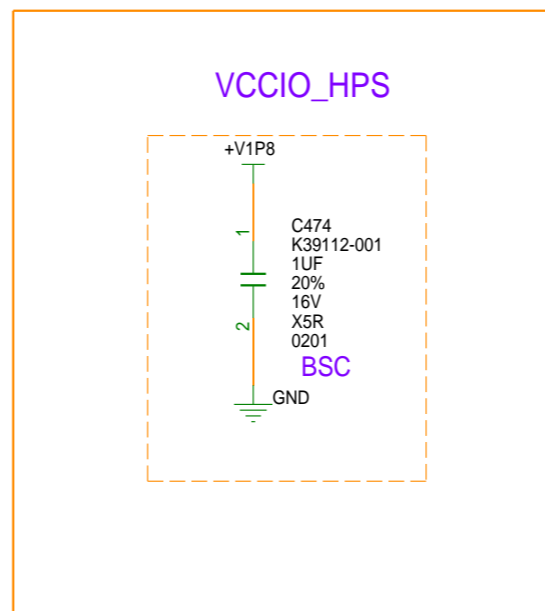
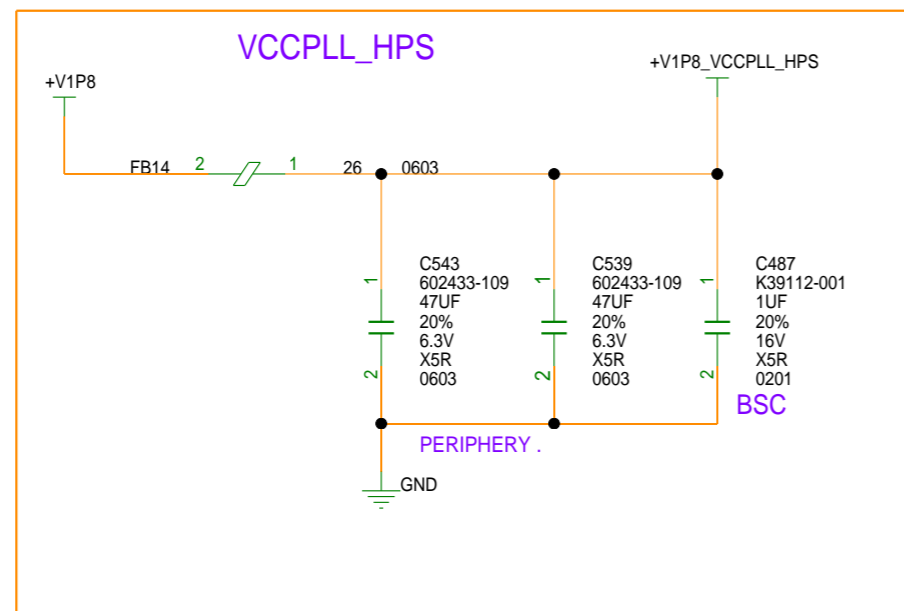
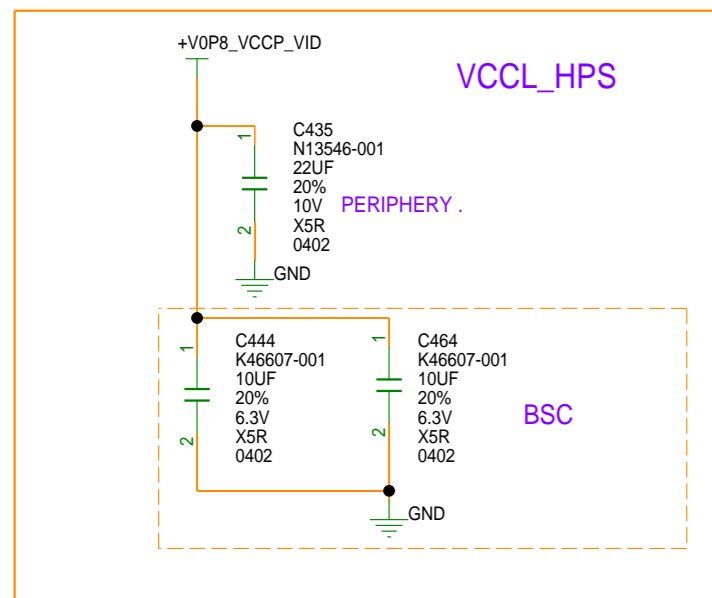
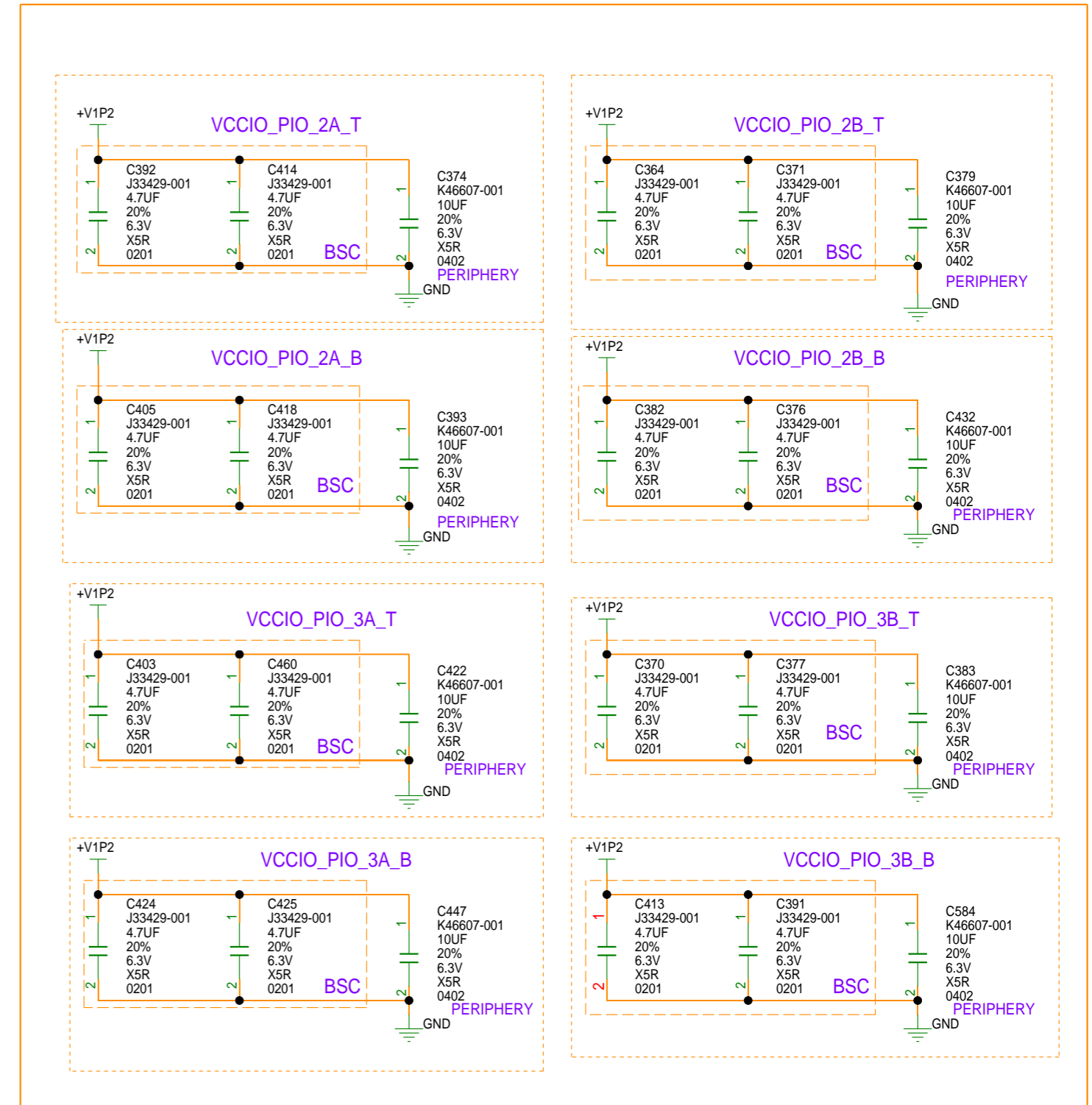
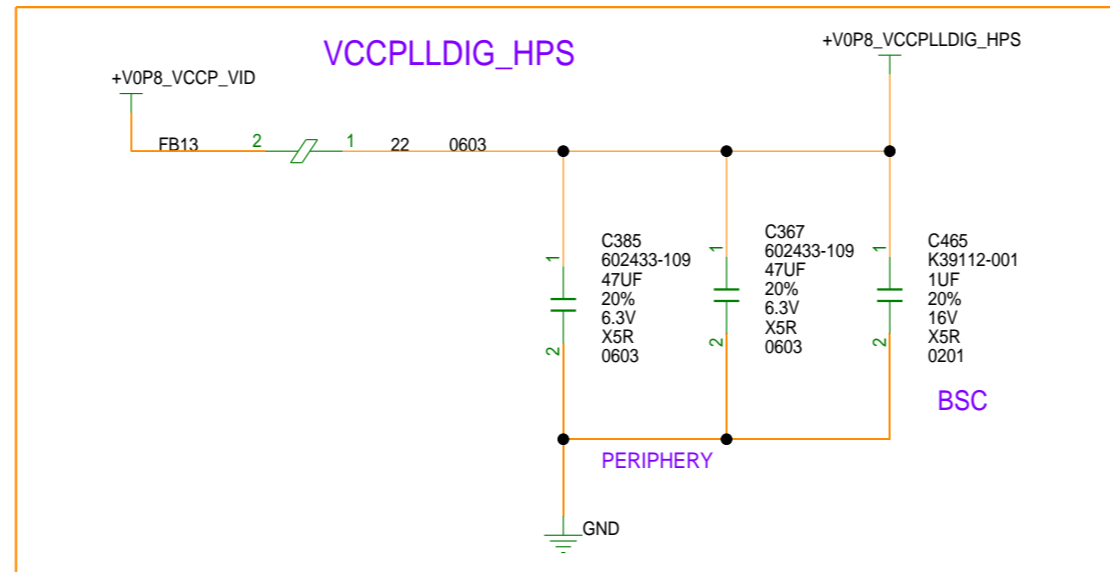
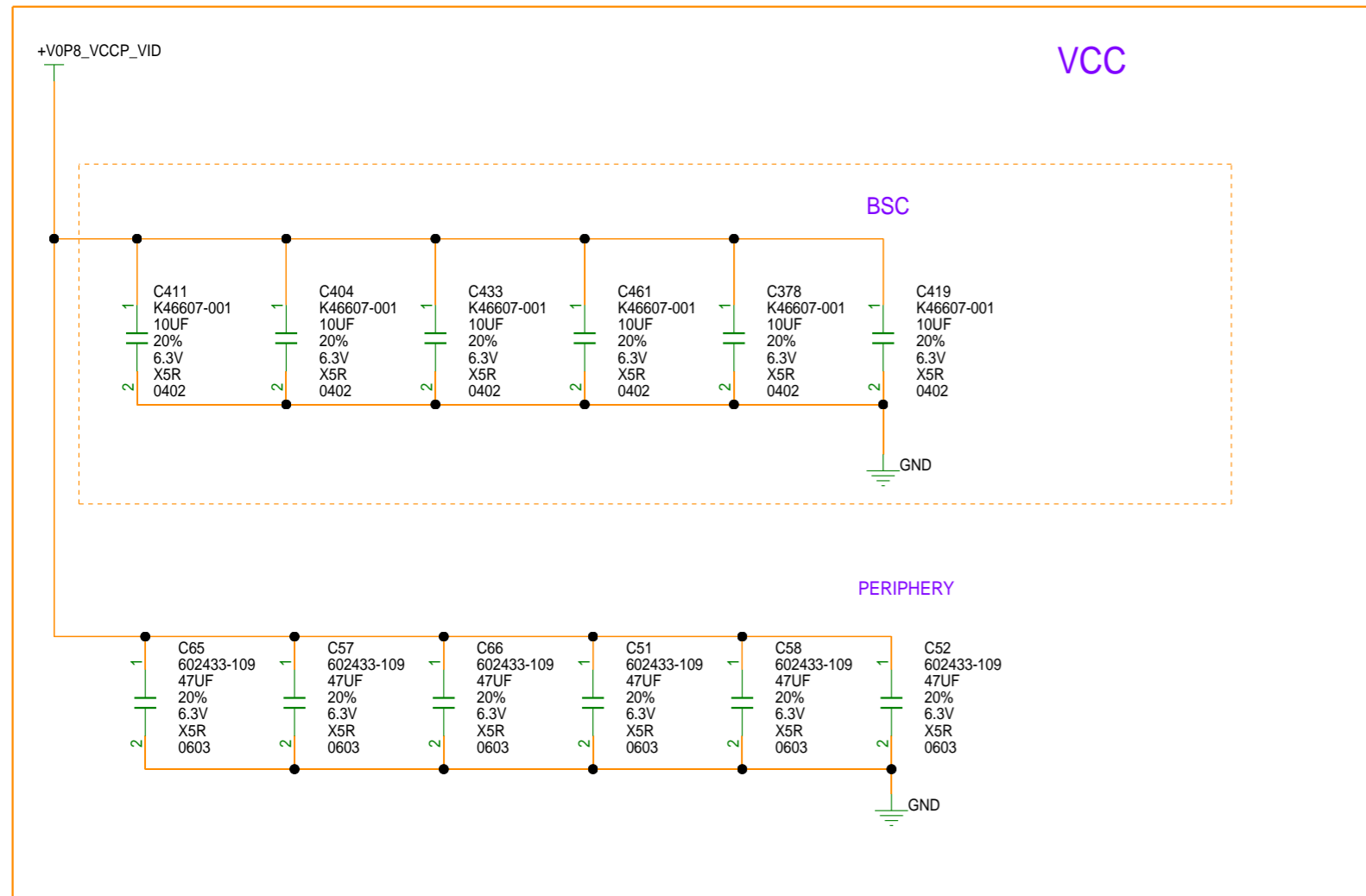


(OPTIONAL)

Mon Oct 14 15:09:16 2024

AG5E - GND

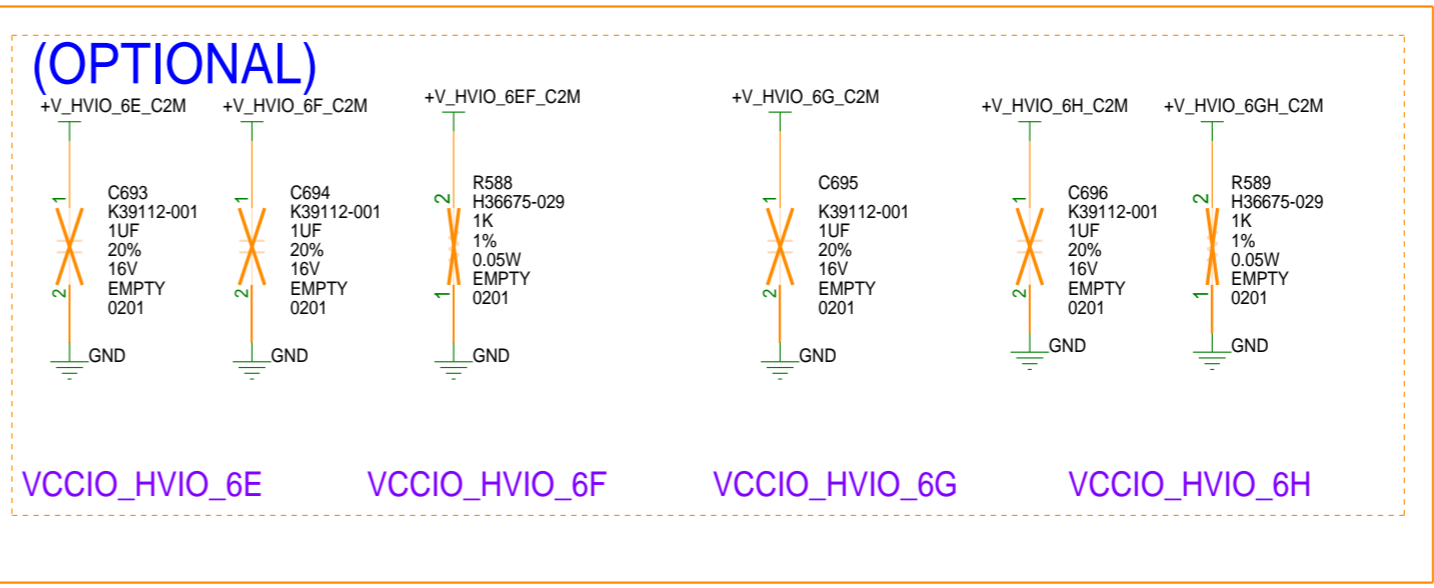
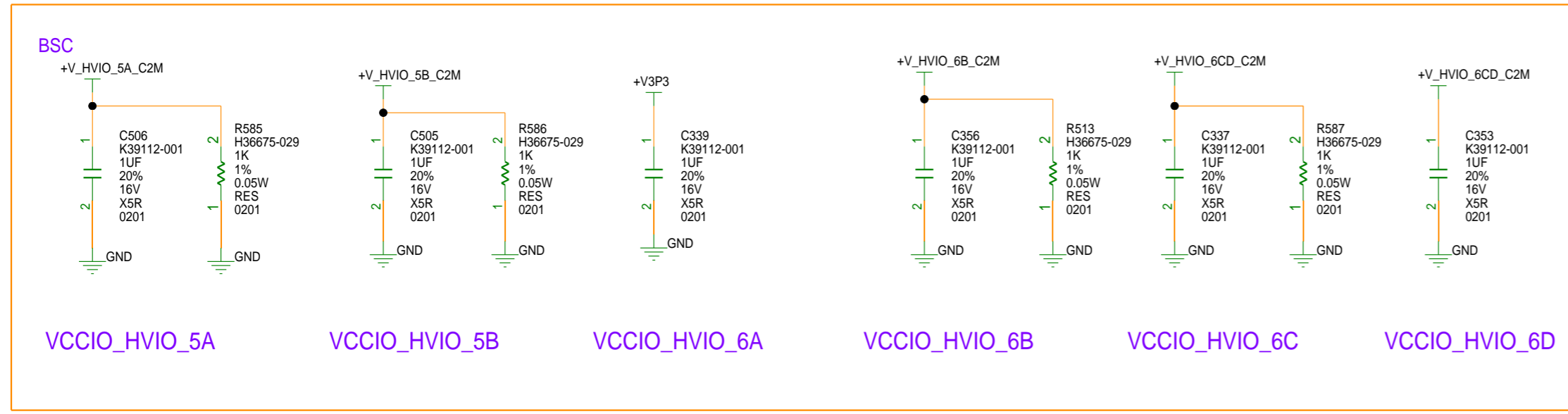
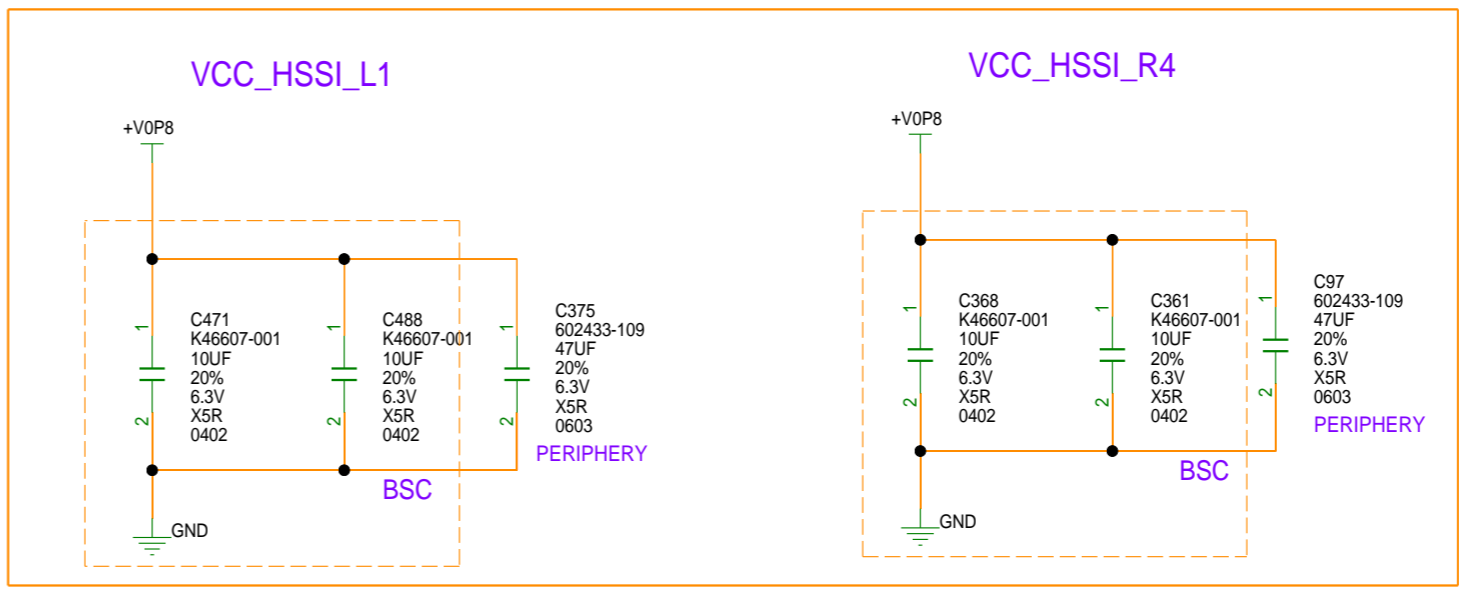
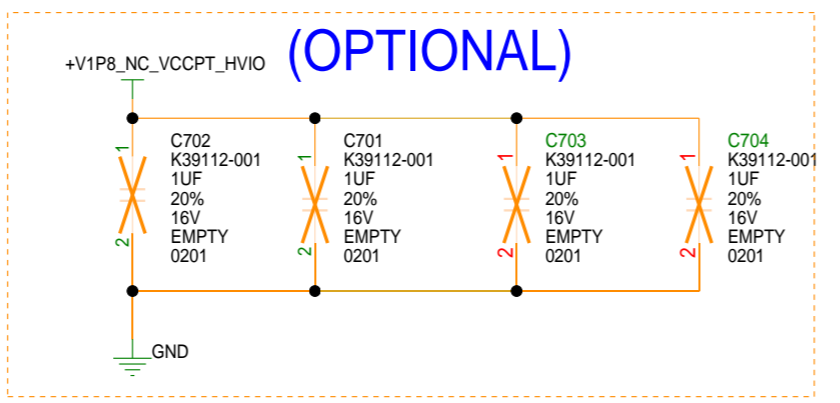
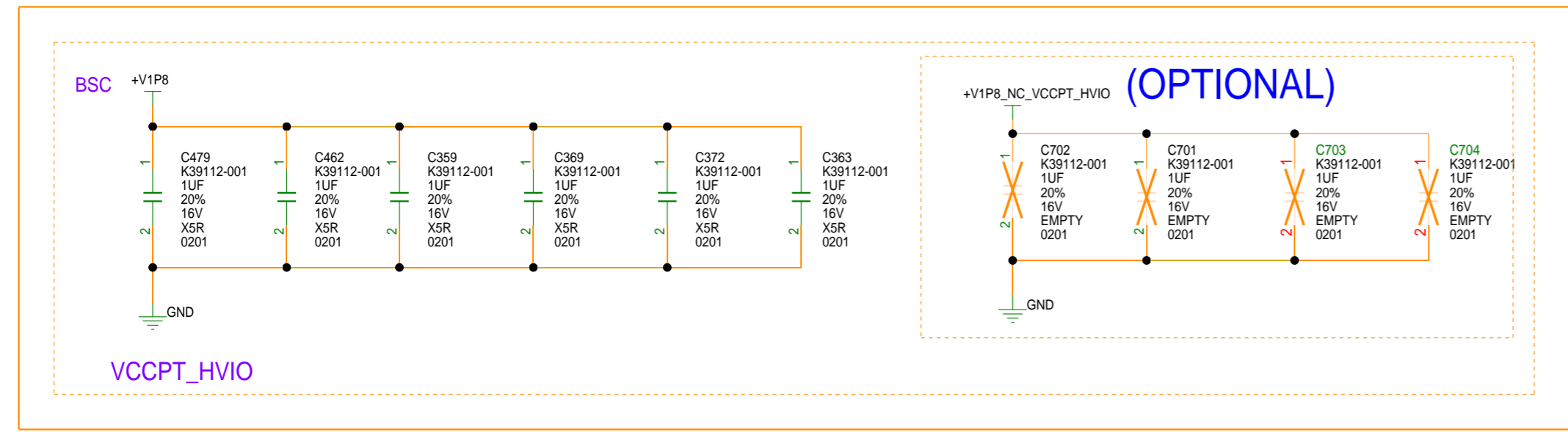
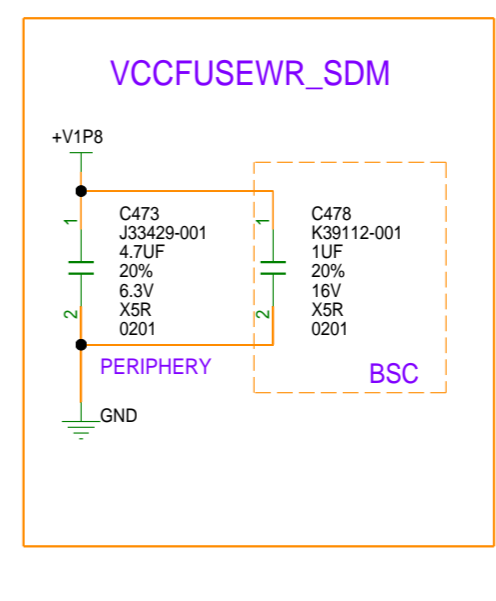
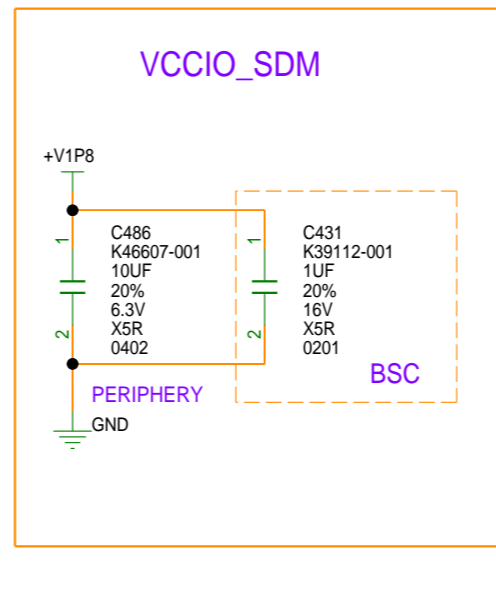
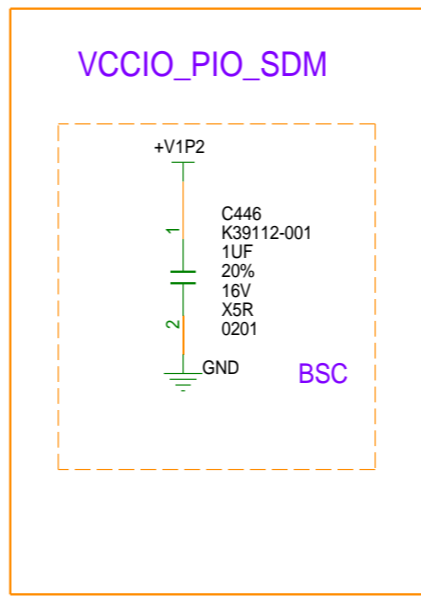
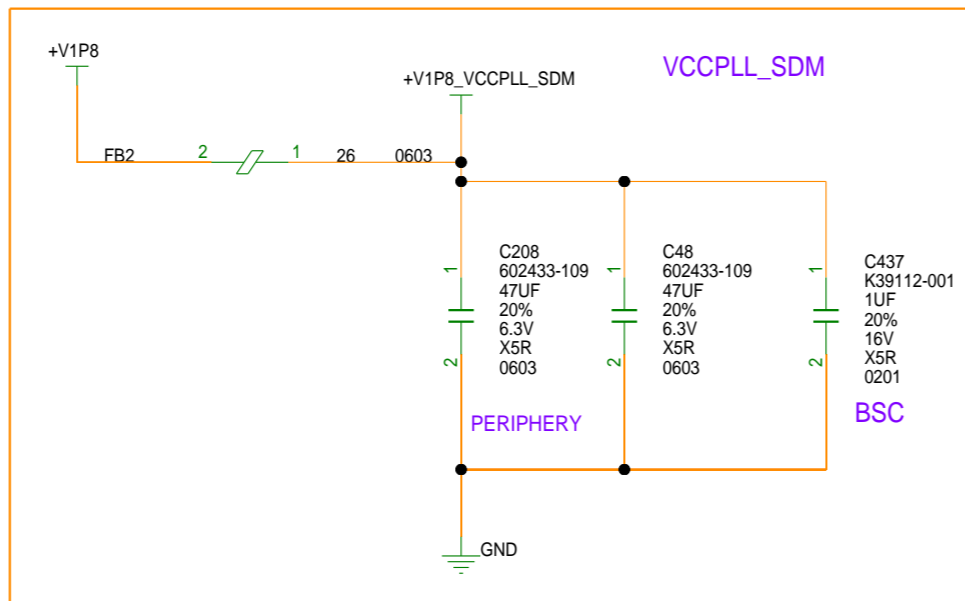
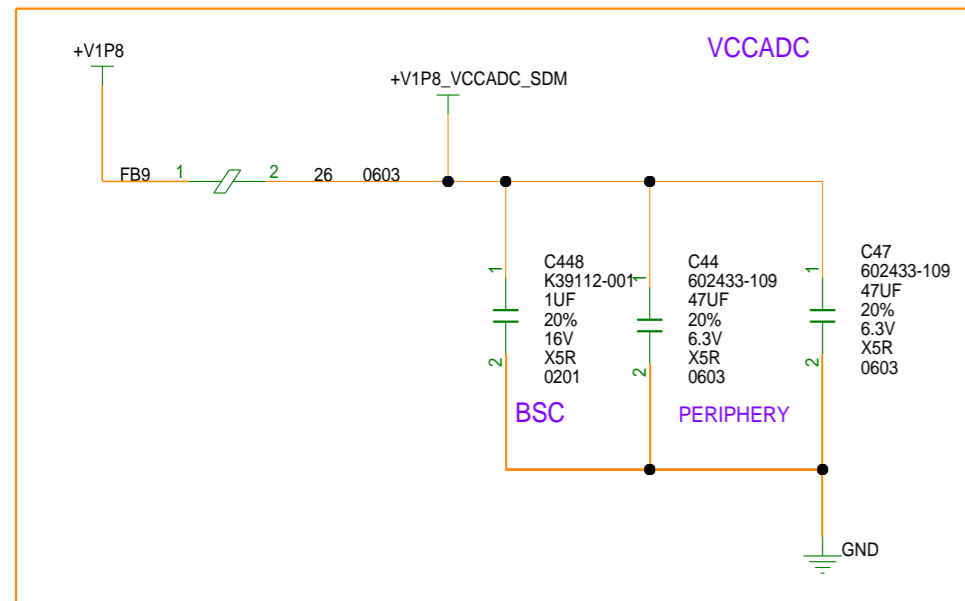
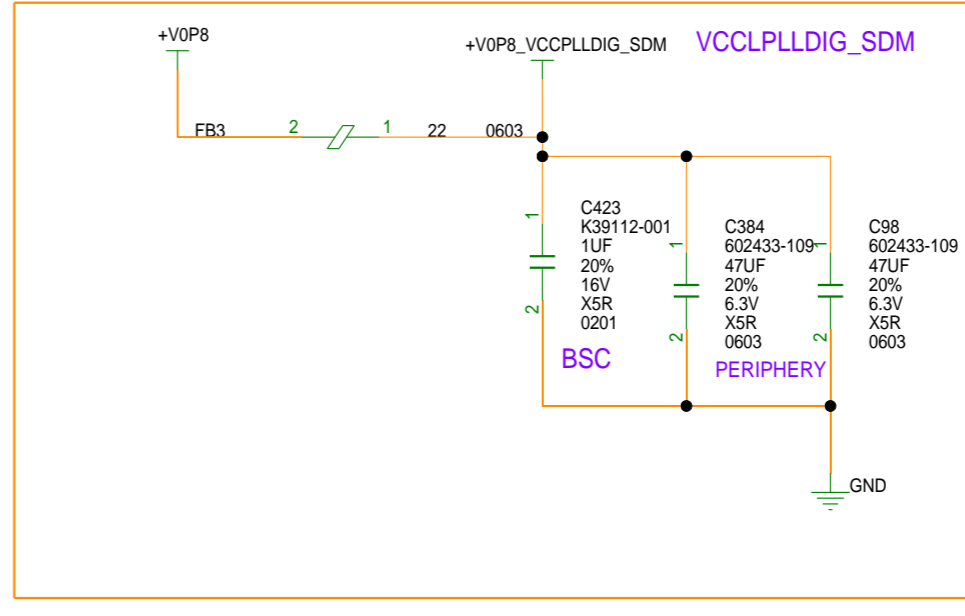
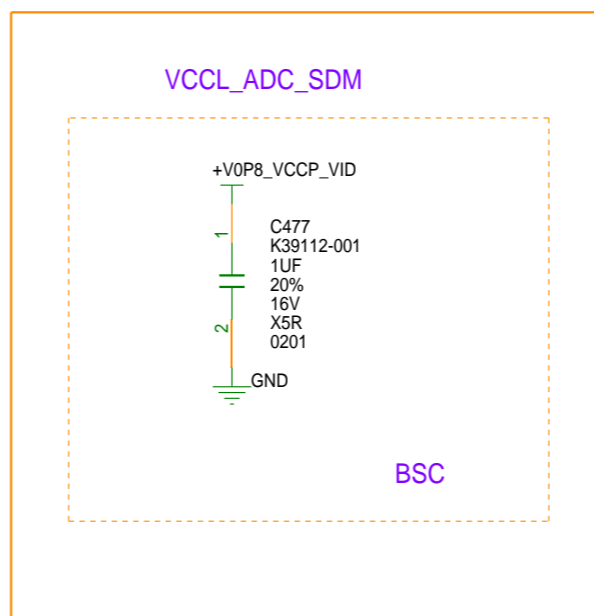
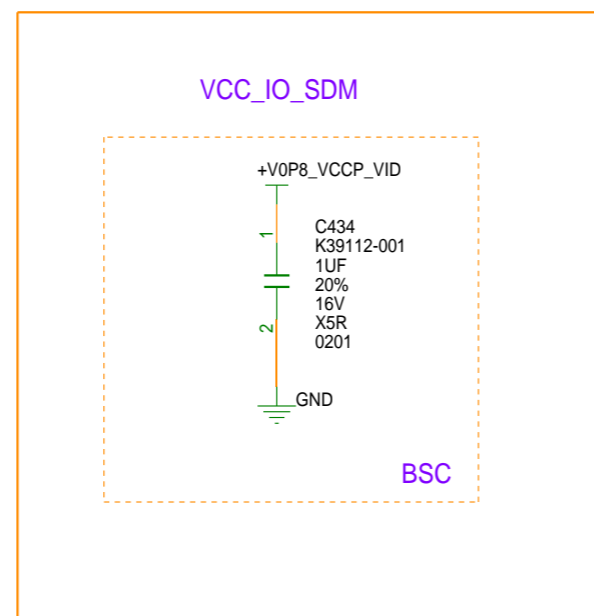
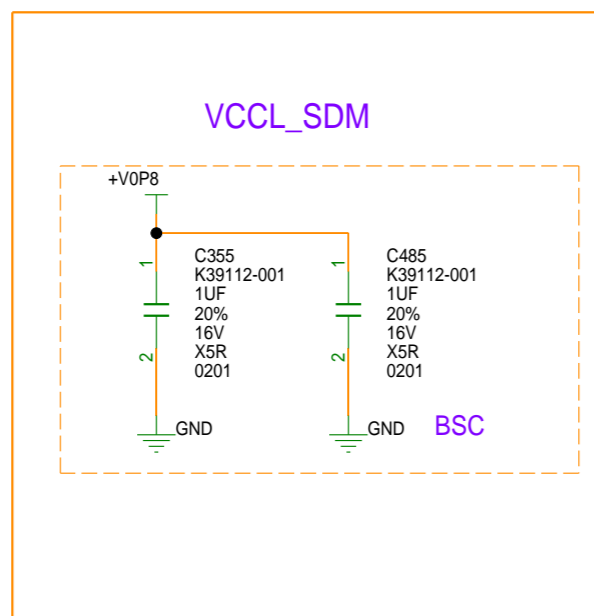
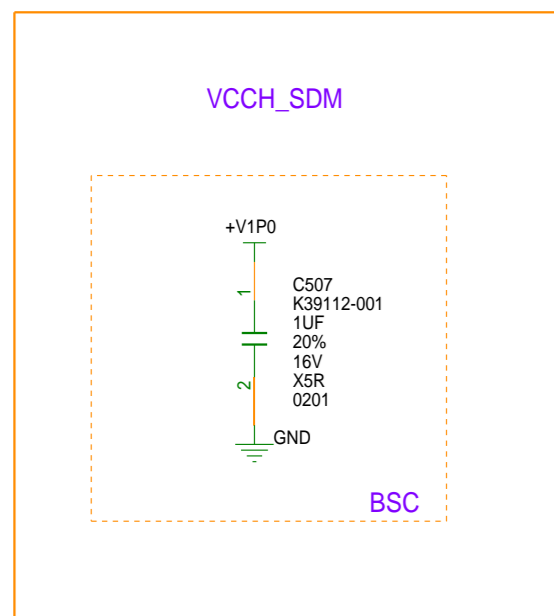
DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 25 OF 62



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AG5E - DECAP

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 26 OF 62



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AG5E - DECAP

DEPARTMENT



SIZE
C+

CODE
34649

DOCUMENT NUMBER
150-0330723-B1

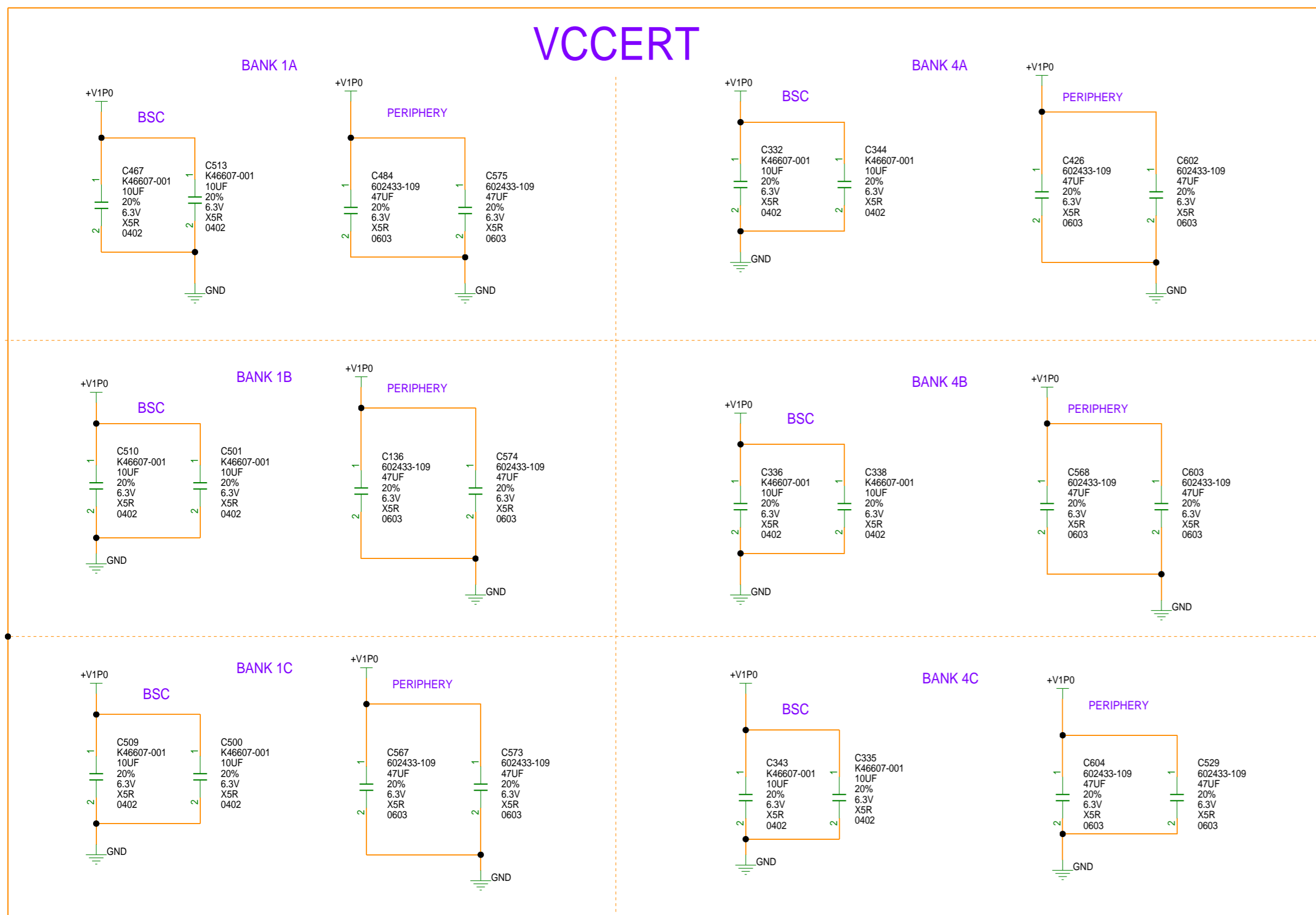
REV
2.1

SCALE:

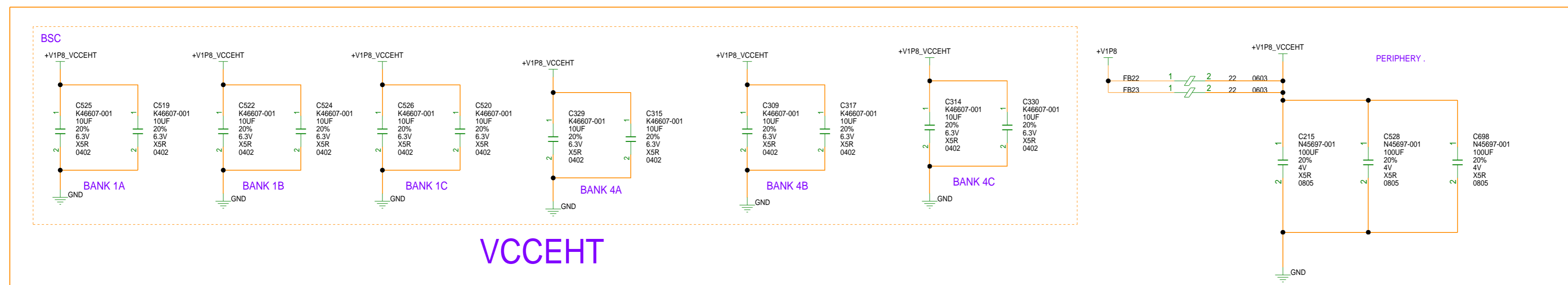
DO NOT SCALE DRAWING

SHEET 27 OF 62

VCCERT




VCCEHT



Mon Oct 14 15:09:19 2024

AG5E - DECAP

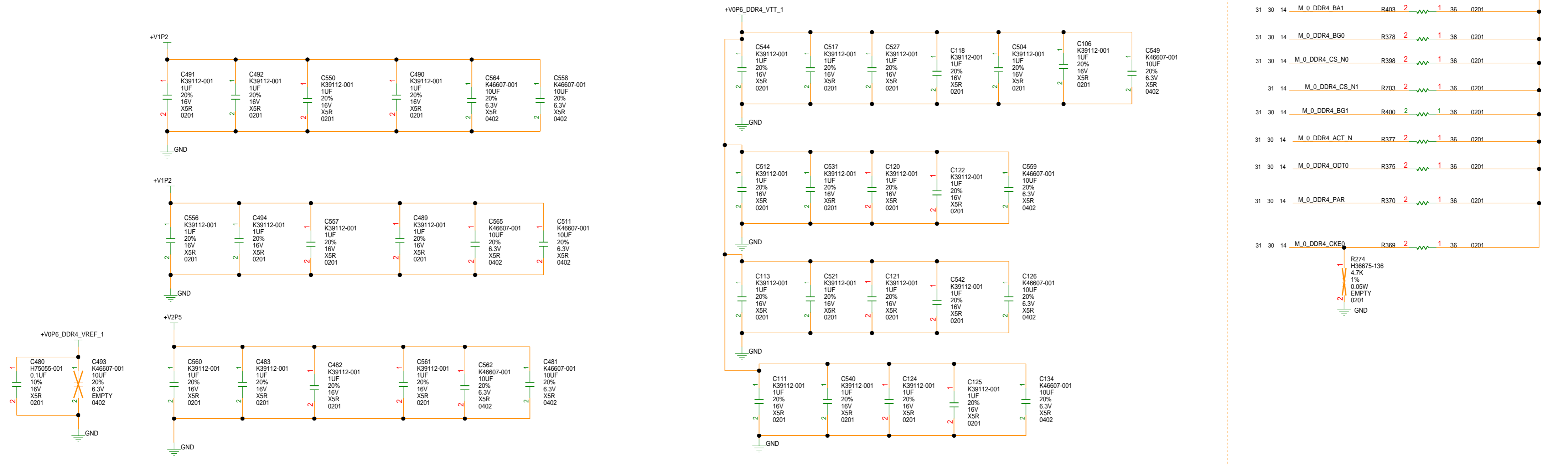
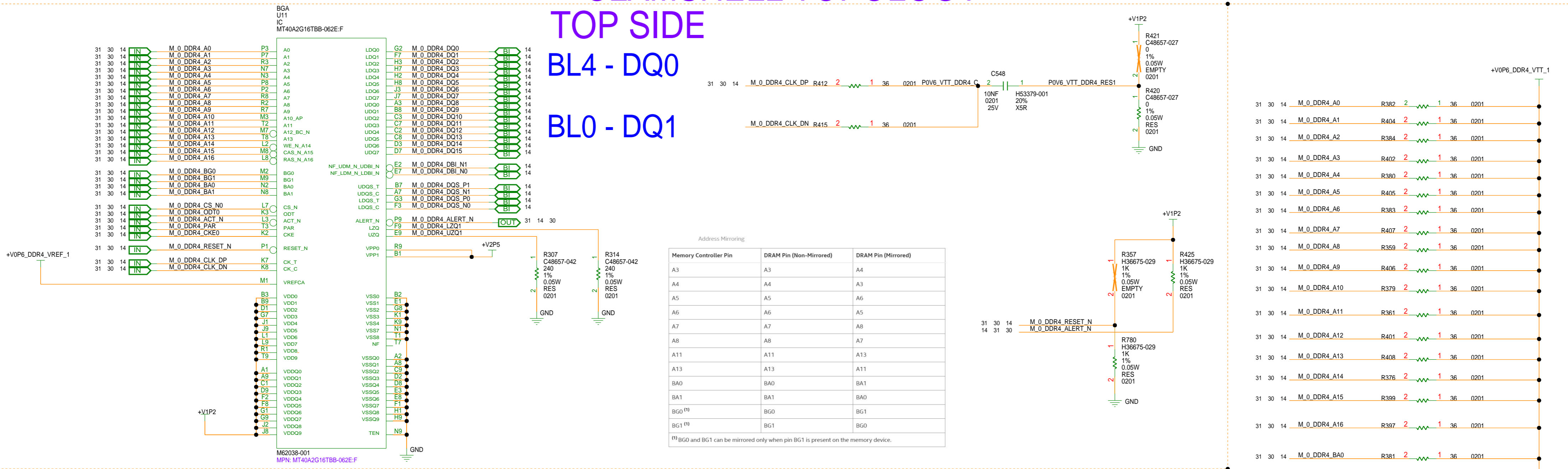
DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 28 OF 62

CLAMSHELL TOPOLOGY

TOP SIDE

BL4 - DQ0

BL0 - DQ1



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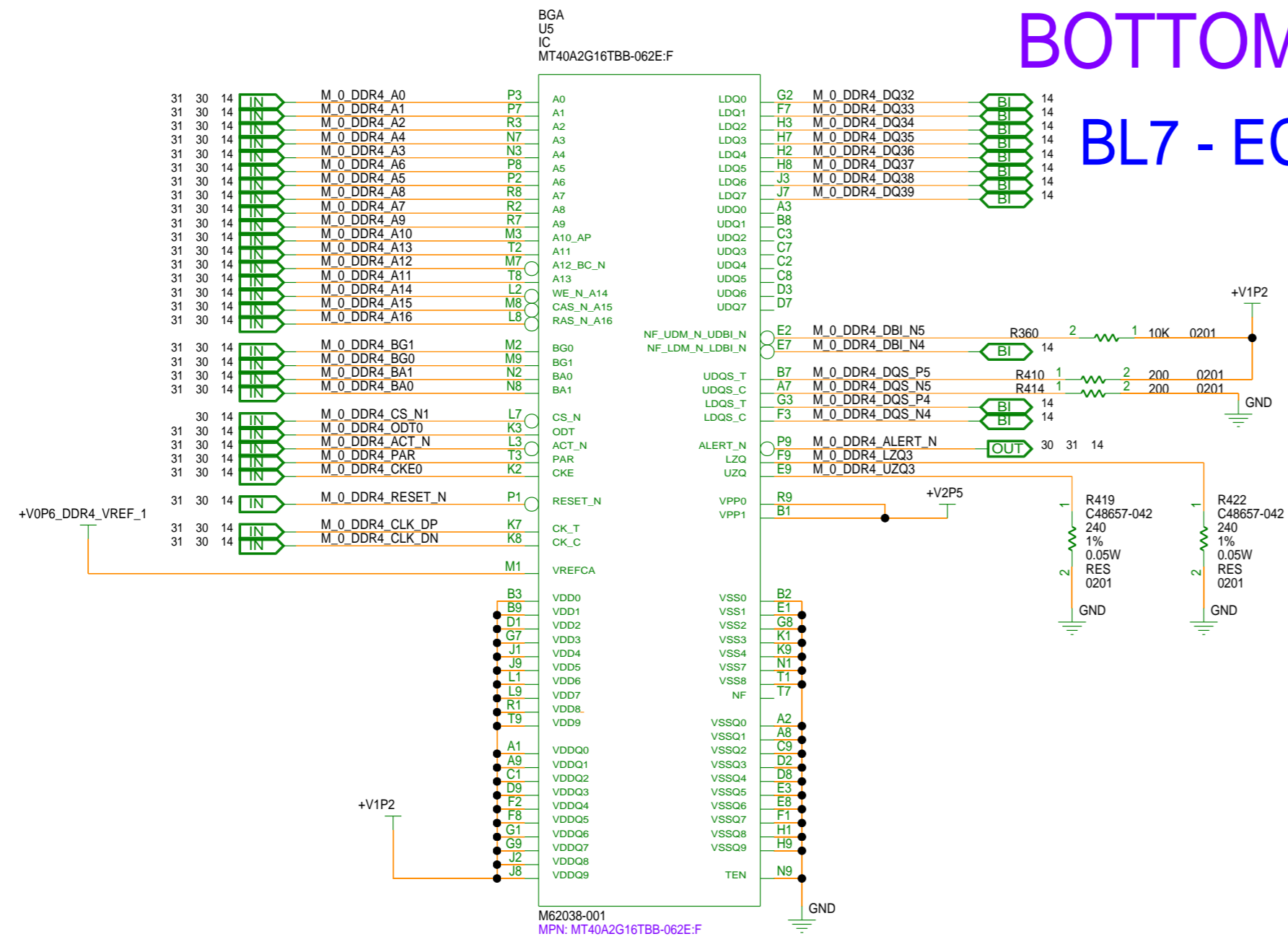
DDR4_X40_BANK2B

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING		SHEET	29 OF 62

CLAMSHELL TOPOLOGY

BOTTOM SIDE

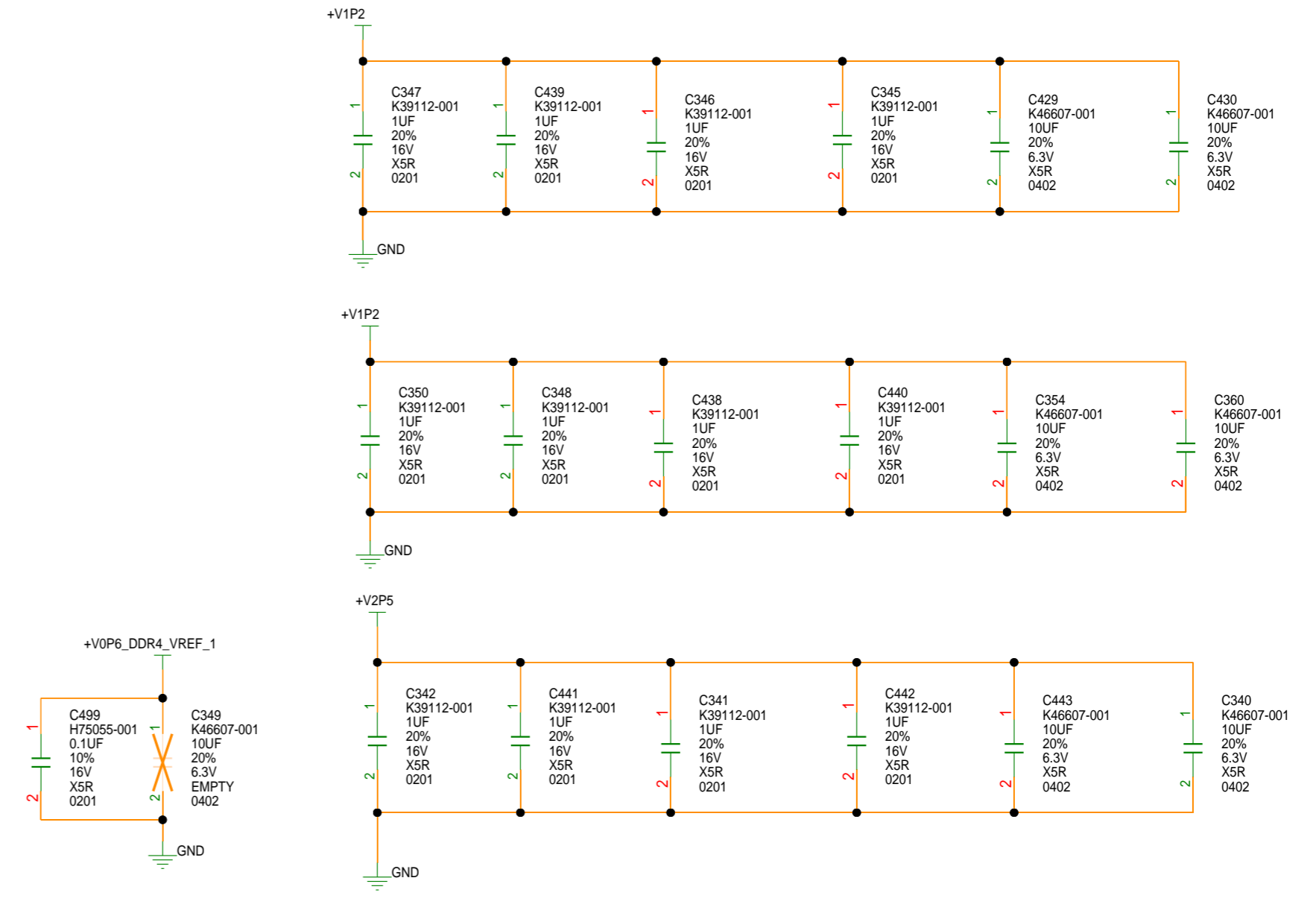
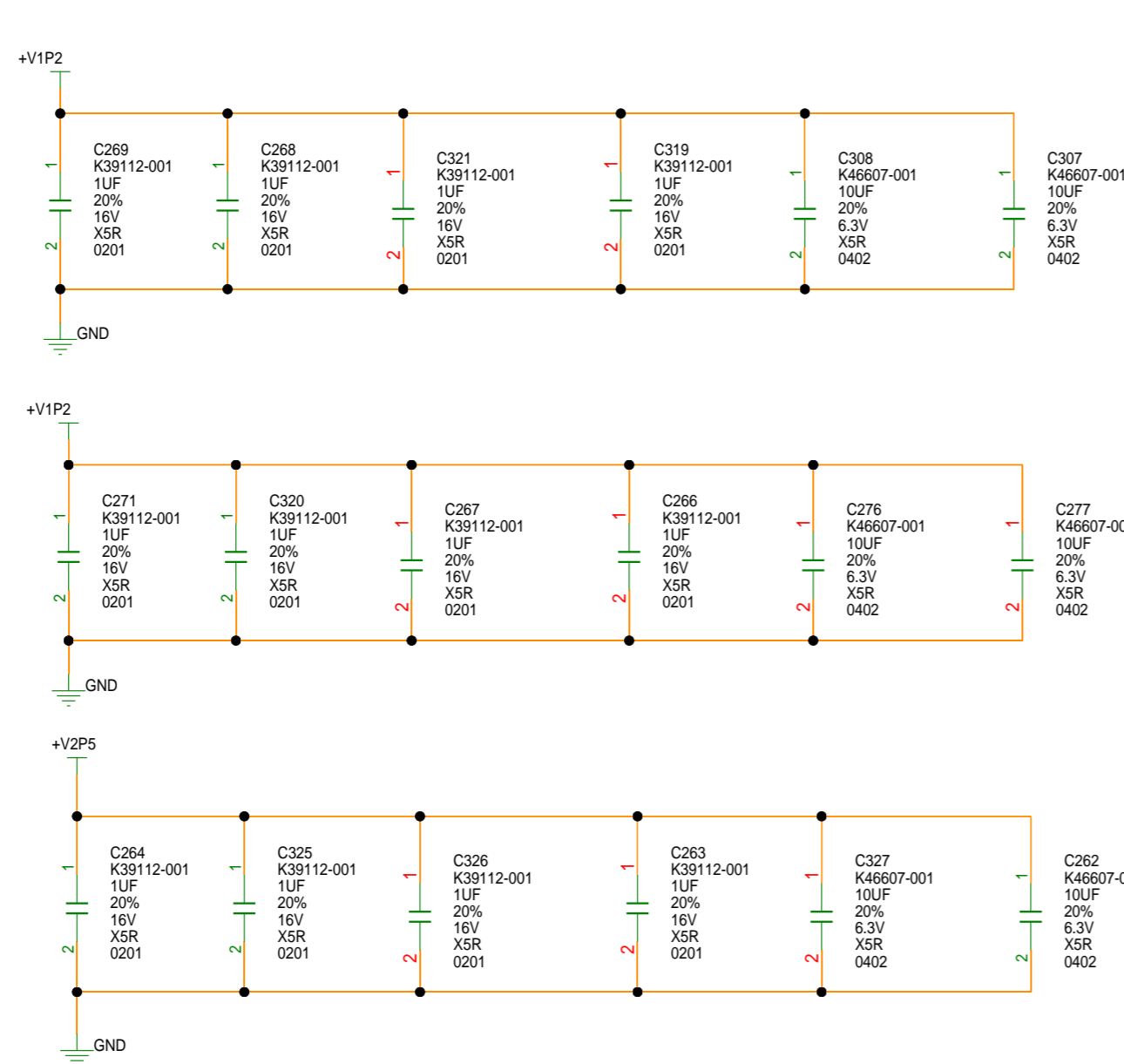
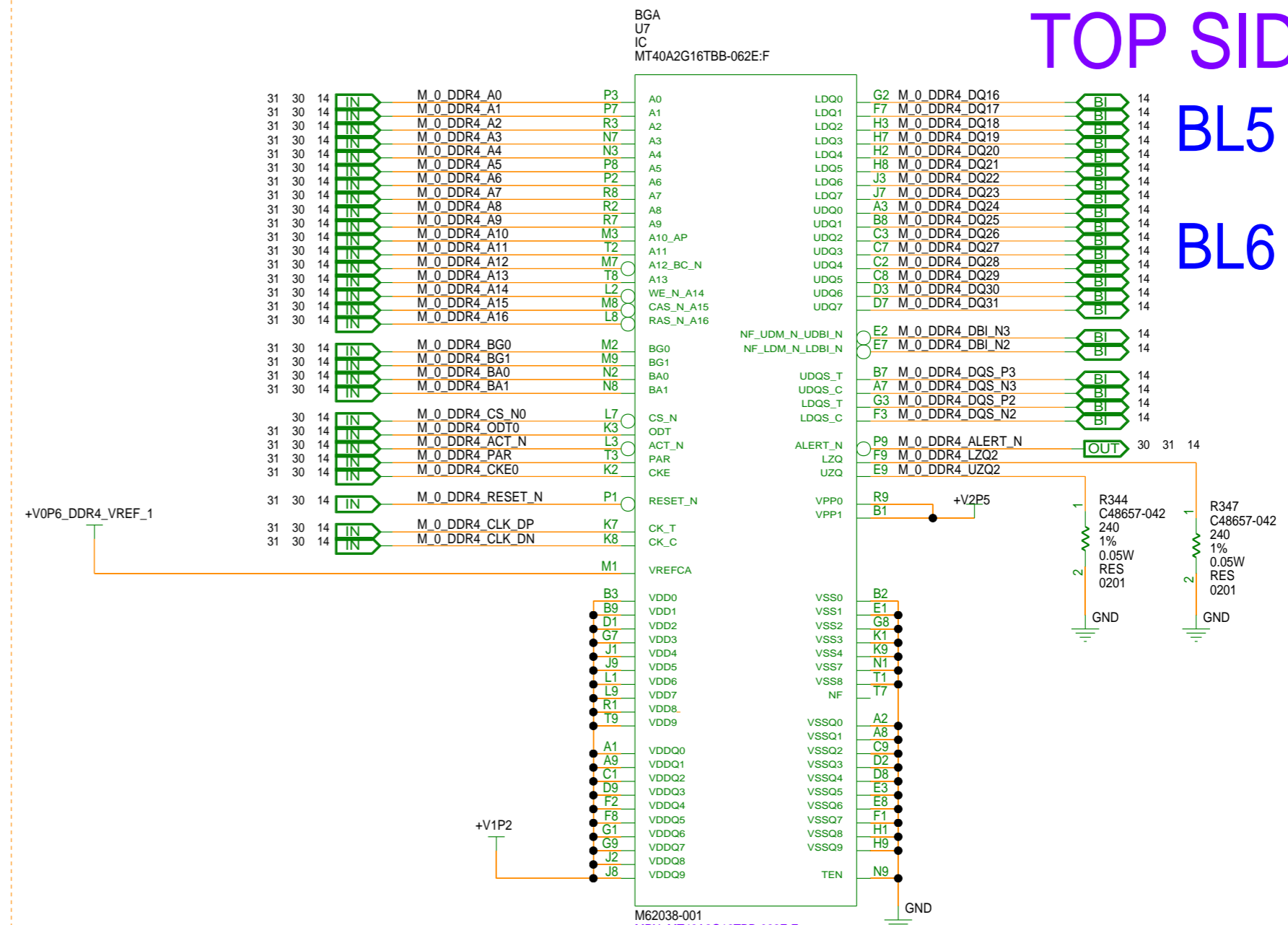
BL7 - ECC



TOP SIDE

BL5 - DQ2

BL6 - DQ3



Mon Oct 14 15:09:23 2024

DDR4_X40_BANK2B

DEPARTMENT



SIZE	CODE	DOCUMENT NUMBER	REV
C+	34649	150-0330723-B1	2.1
SCALE:	DO NOT SCALE DRAWING		SHEET 30 OF 62

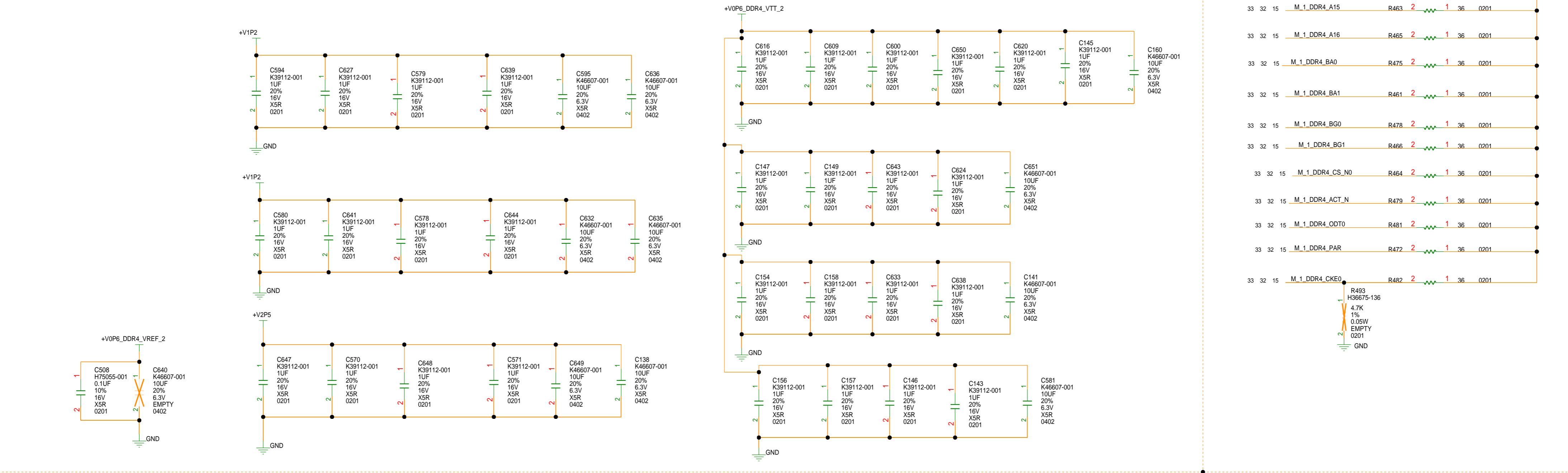
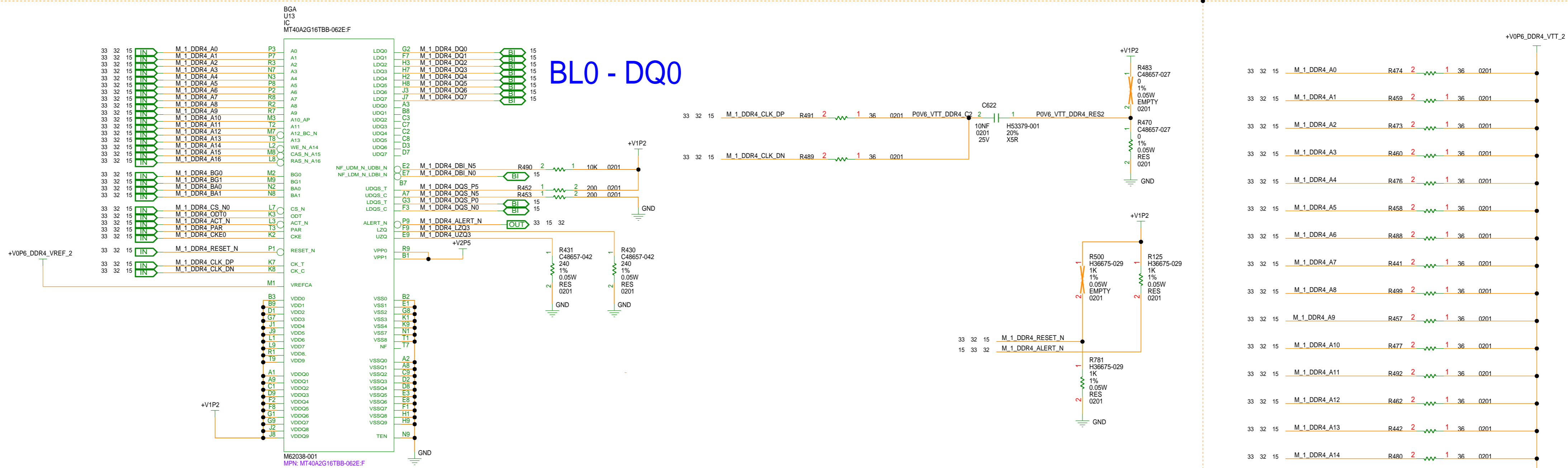
B

B

A

A

BLO - DQ0



Mon Oct 14 15:09:24 2024

DDR4_X40_BANK3A

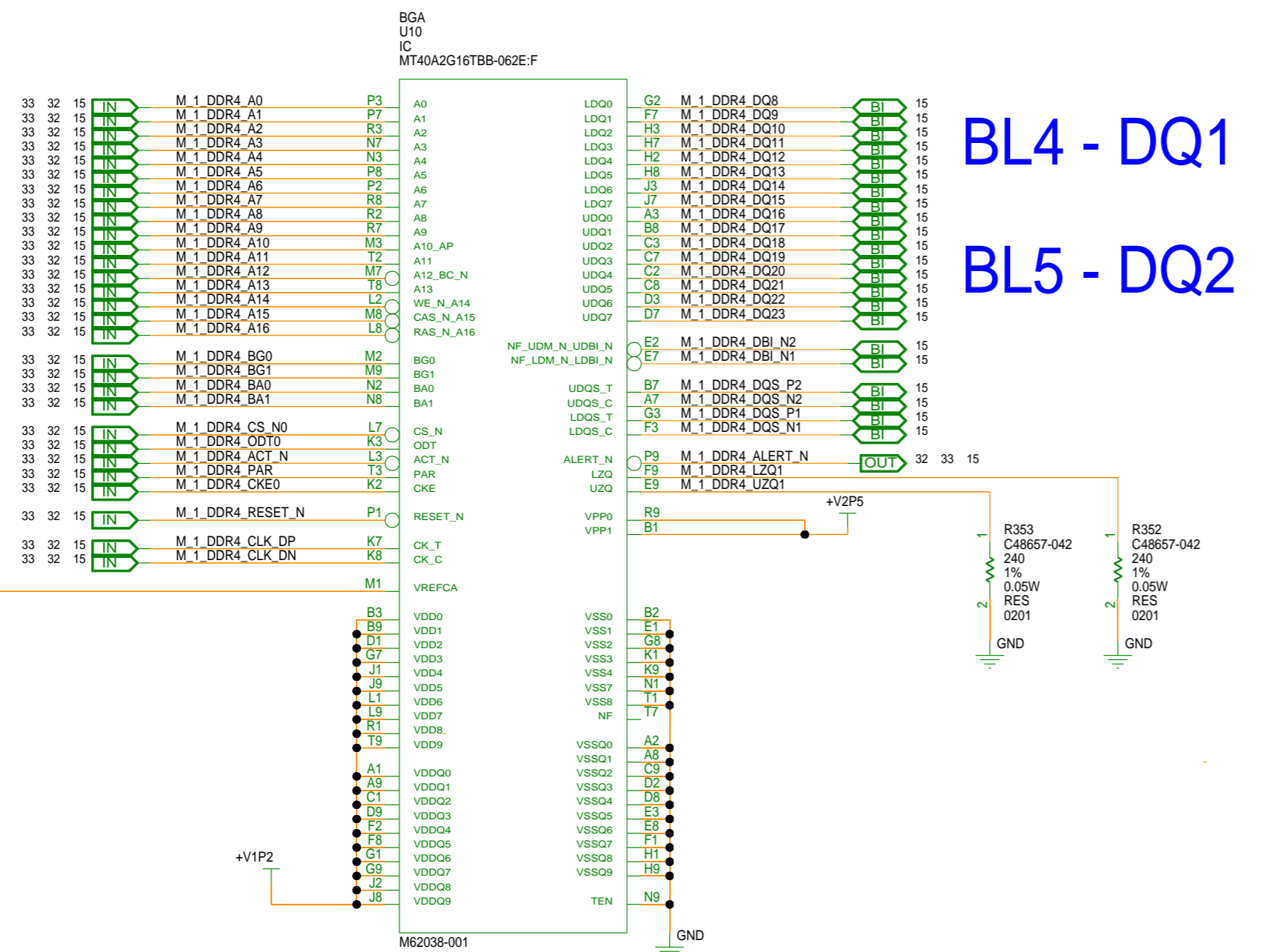
DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING		SHEET	31 OF 62

4

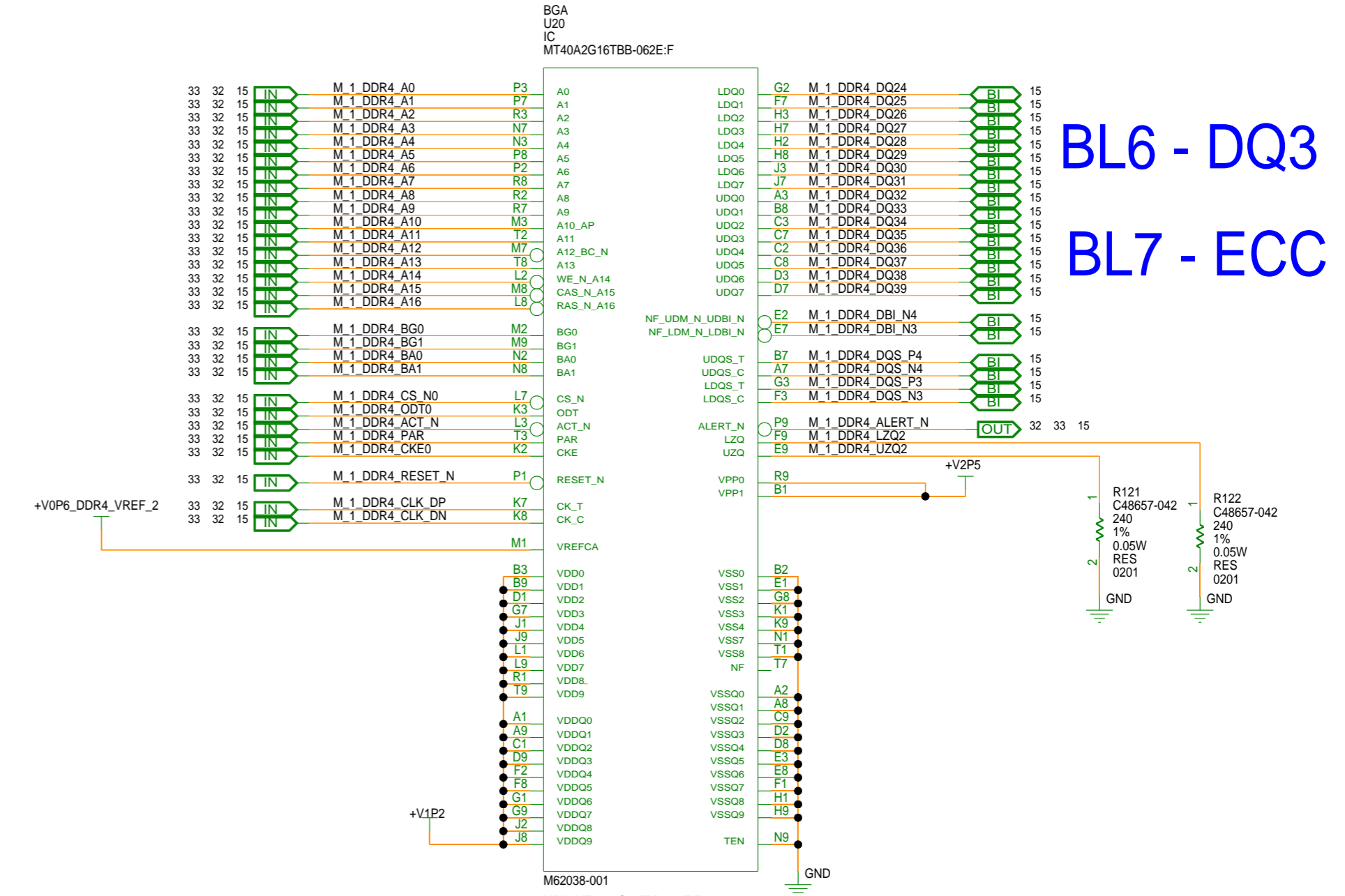
3

2

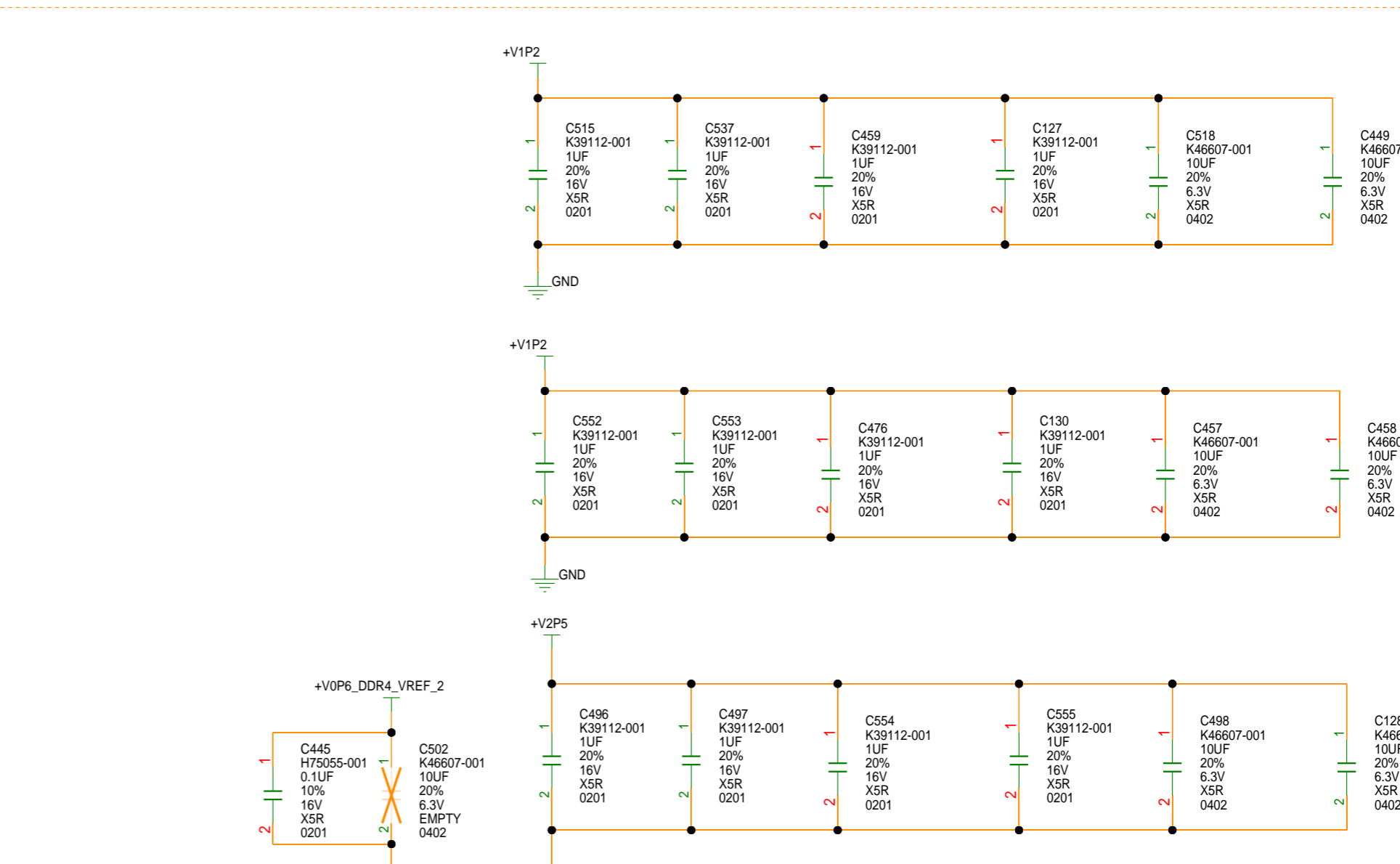
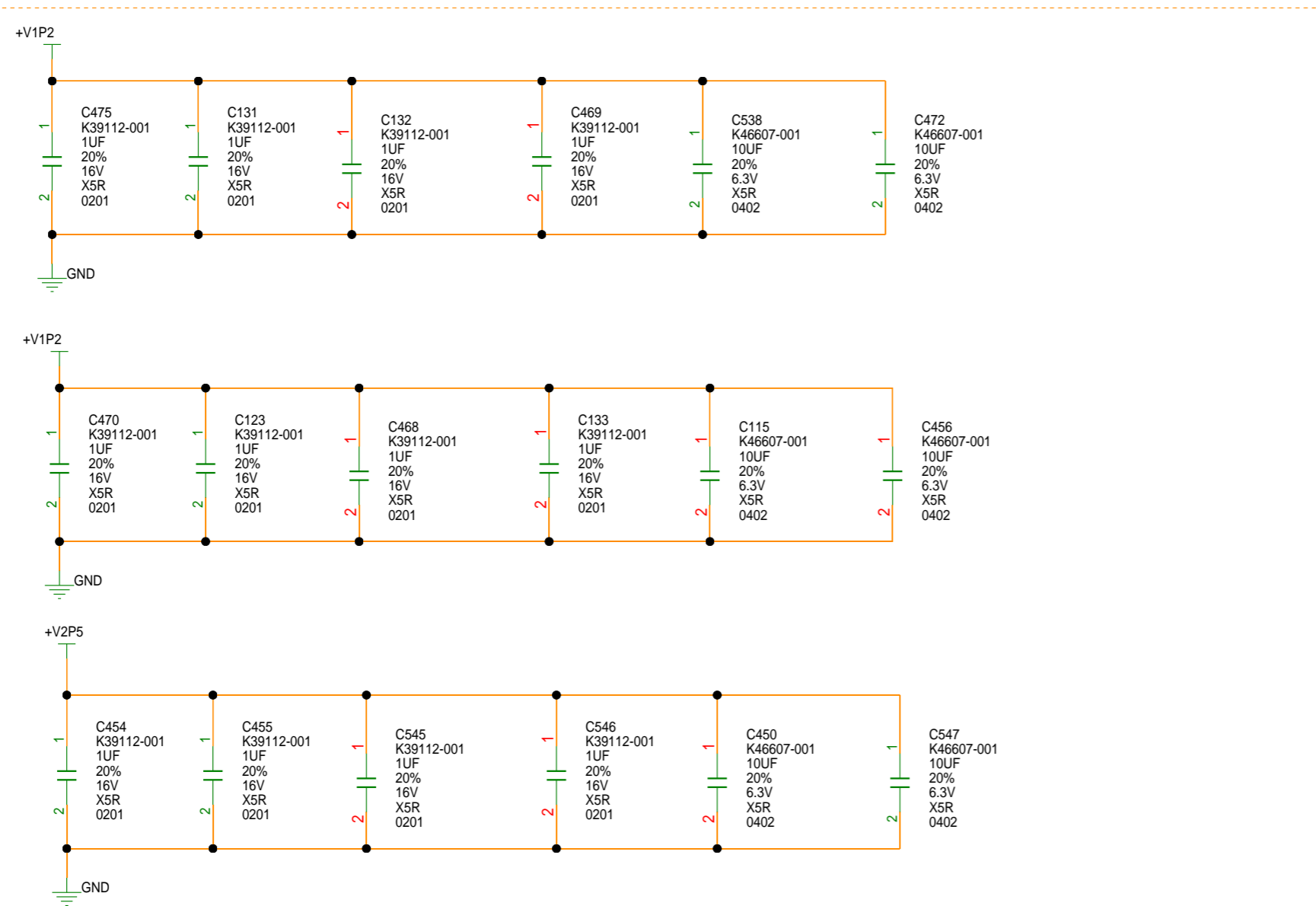
1



BL4 - DQ1
BL5 - DQ2



BL6 - DQ3
BL7 - ECC



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DDR4_X40_BANK3A

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 32 OF 62

4

3

2

1

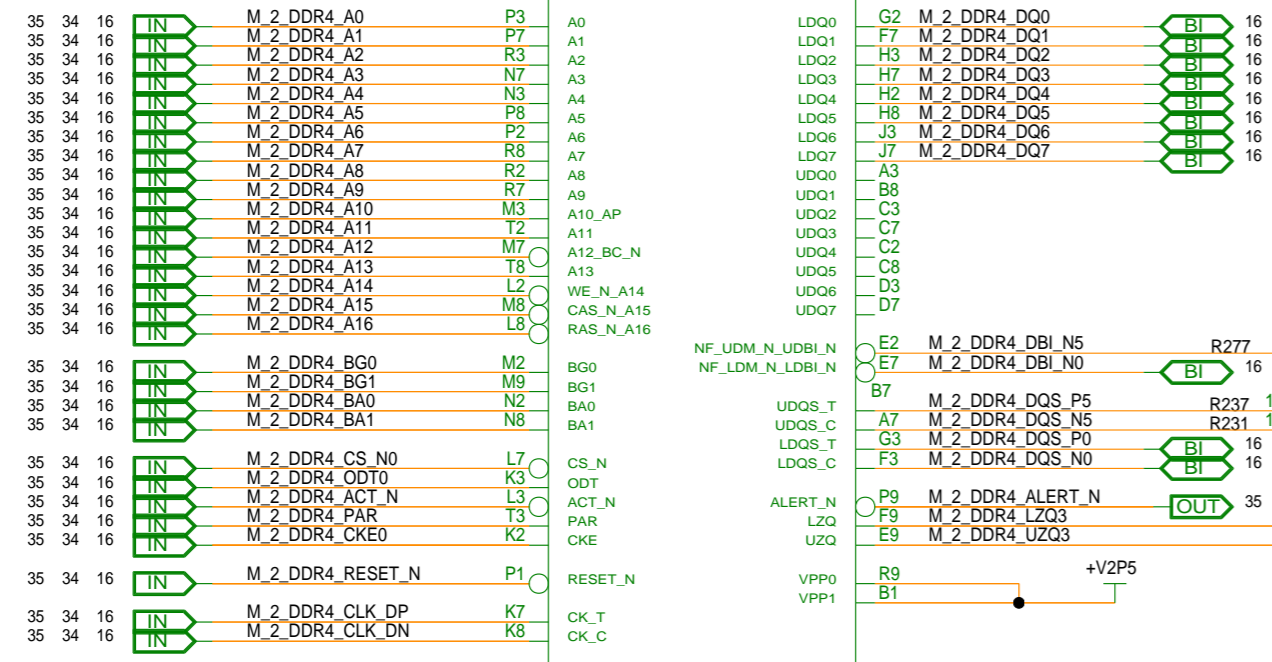
4

3

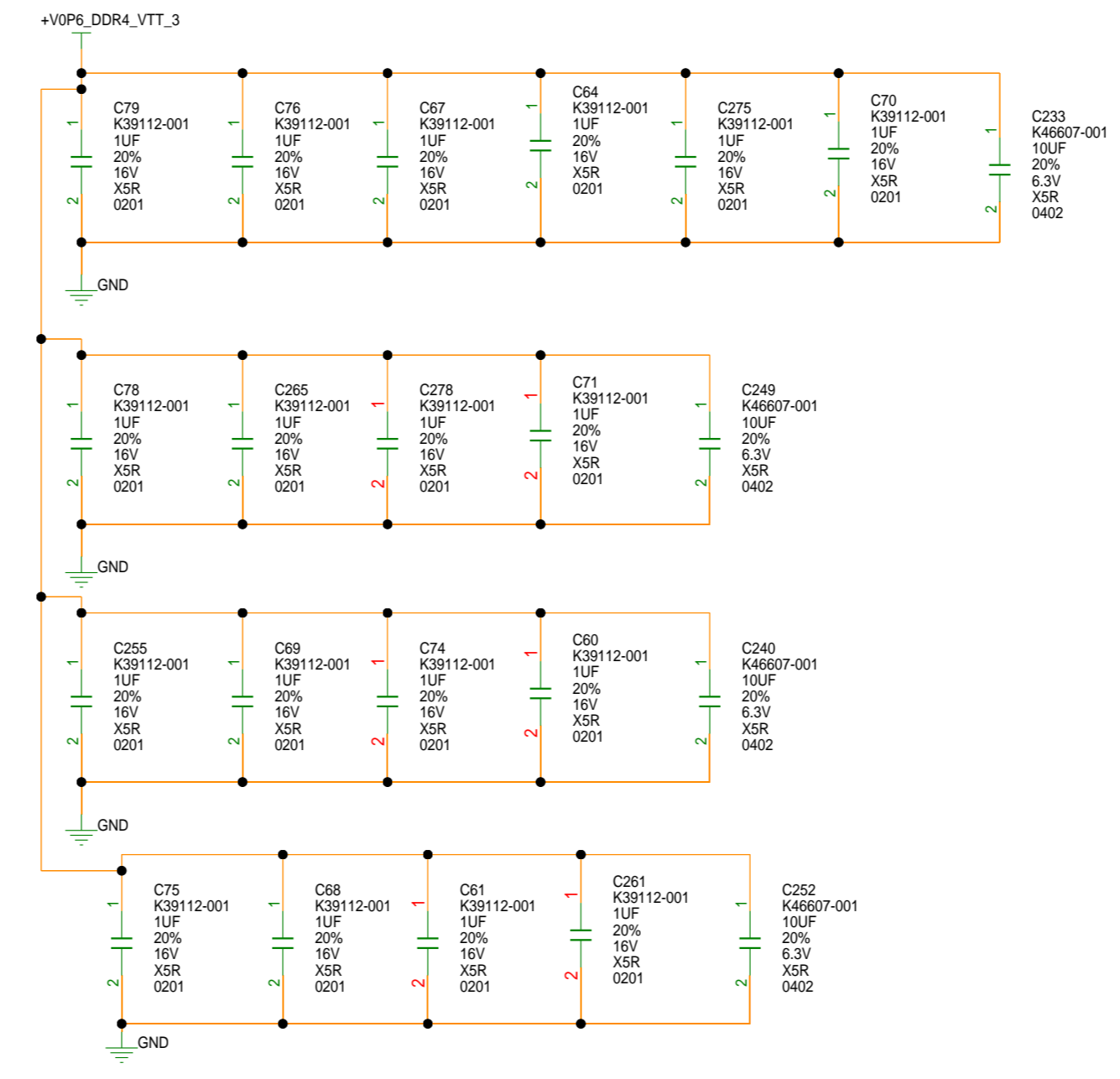
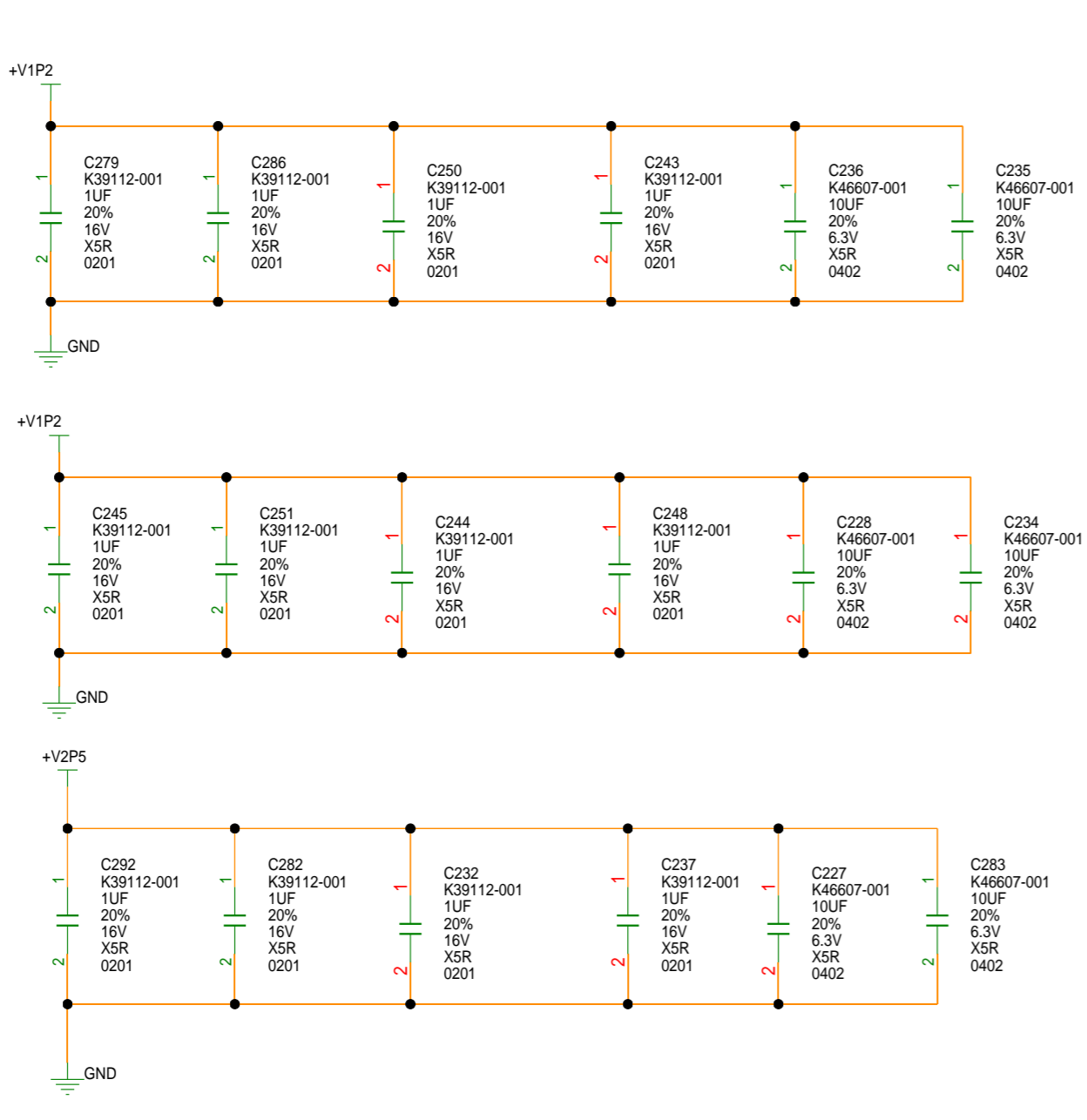
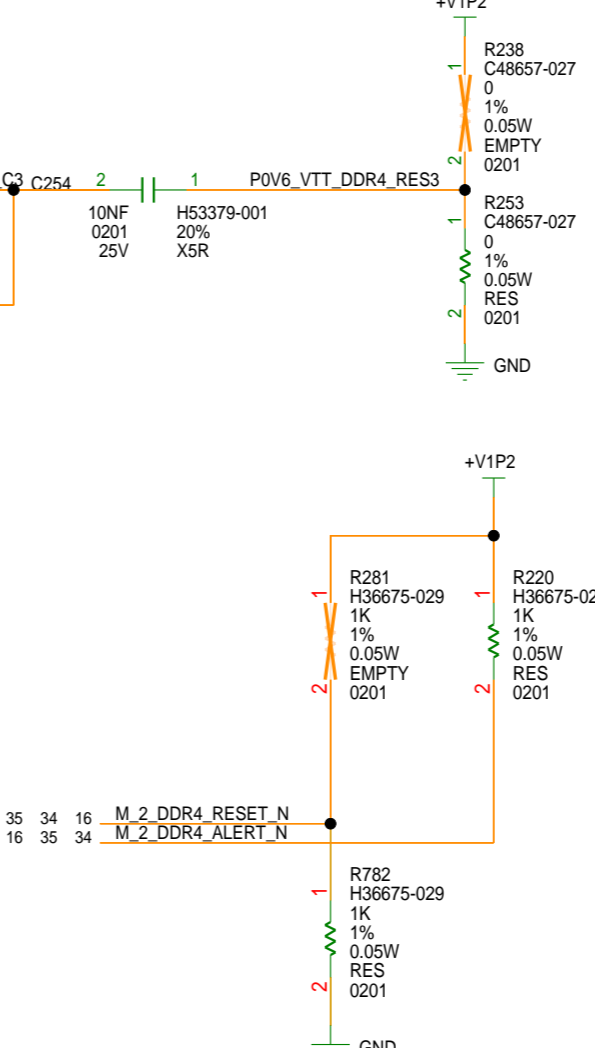
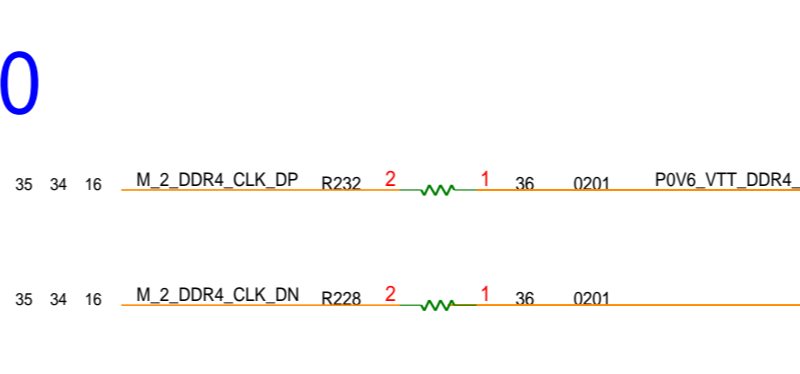
2

1

BGA U3 IC MT40A2G16TBB-062E.F



BLO - DQ0



Mon Oct 14 15:09:25 2024

DDR4_X40_BANK3B

DEPARTMENT altera
An Intel Company

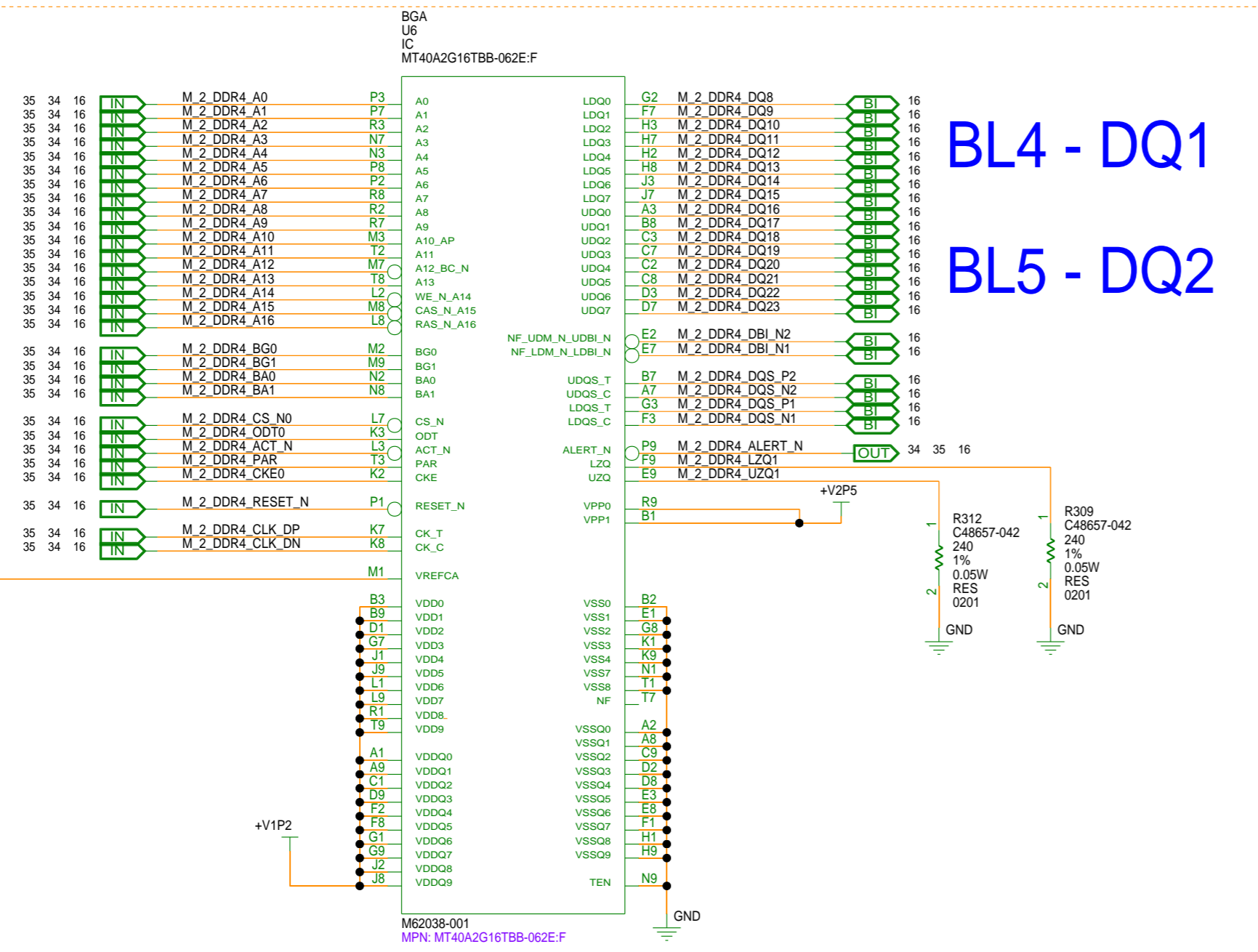
SIZE	CODE	DOCUMENT NUMBER	REV
C+	34649	150-0330723-B1	2.1
SCALE:	DO NOT SCALE DRAWING		SHEET 33 OF 62

4

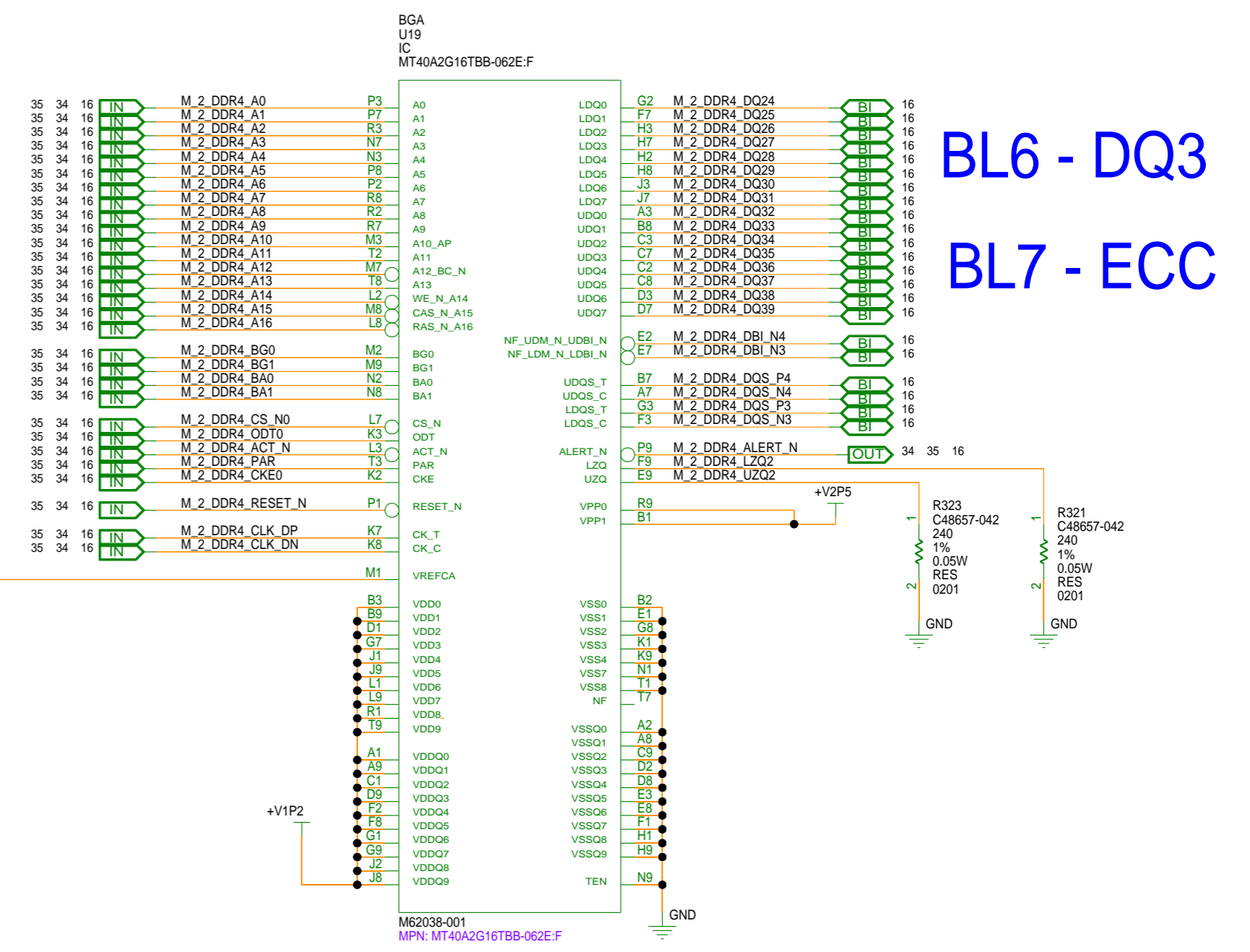
3

2

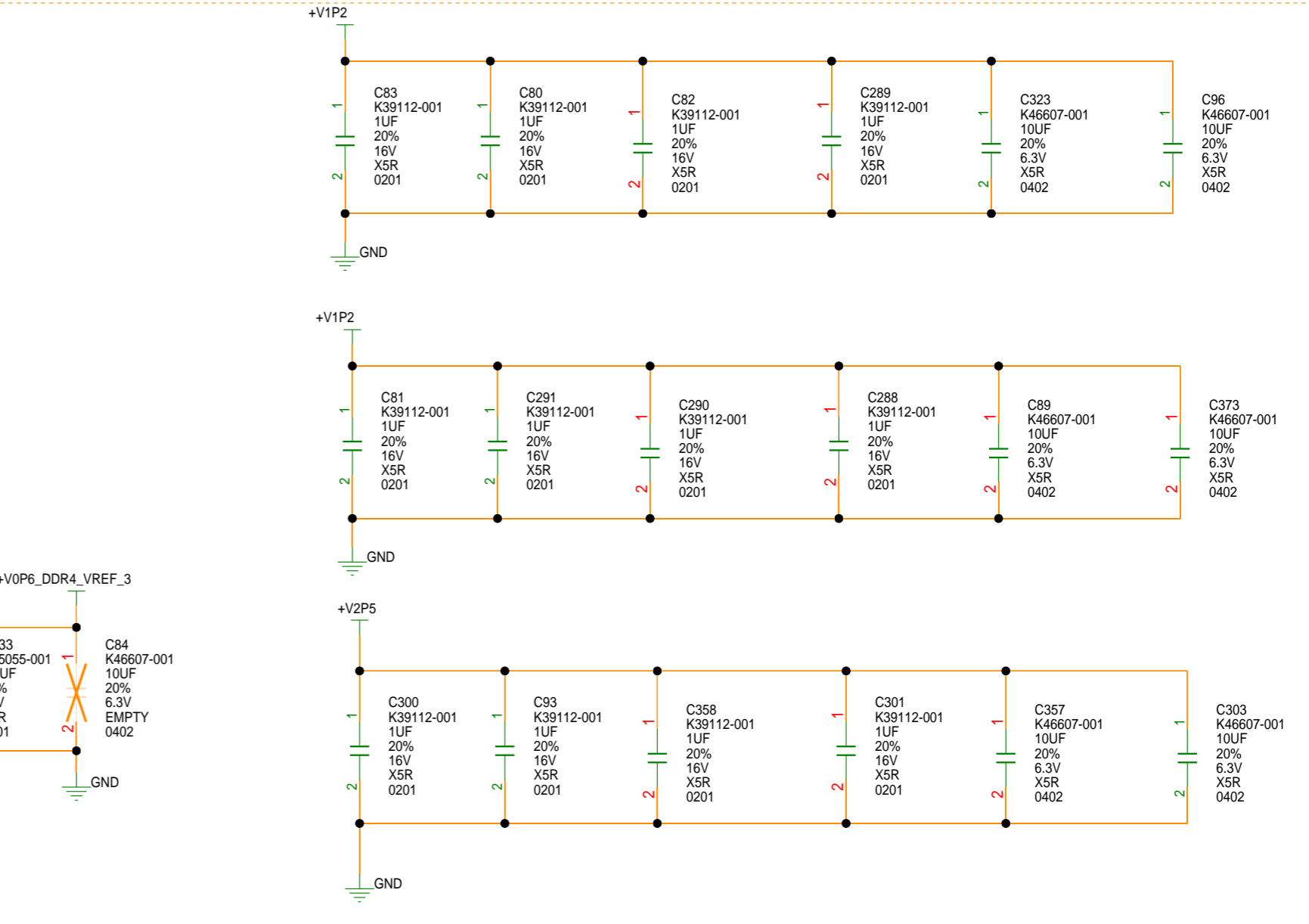
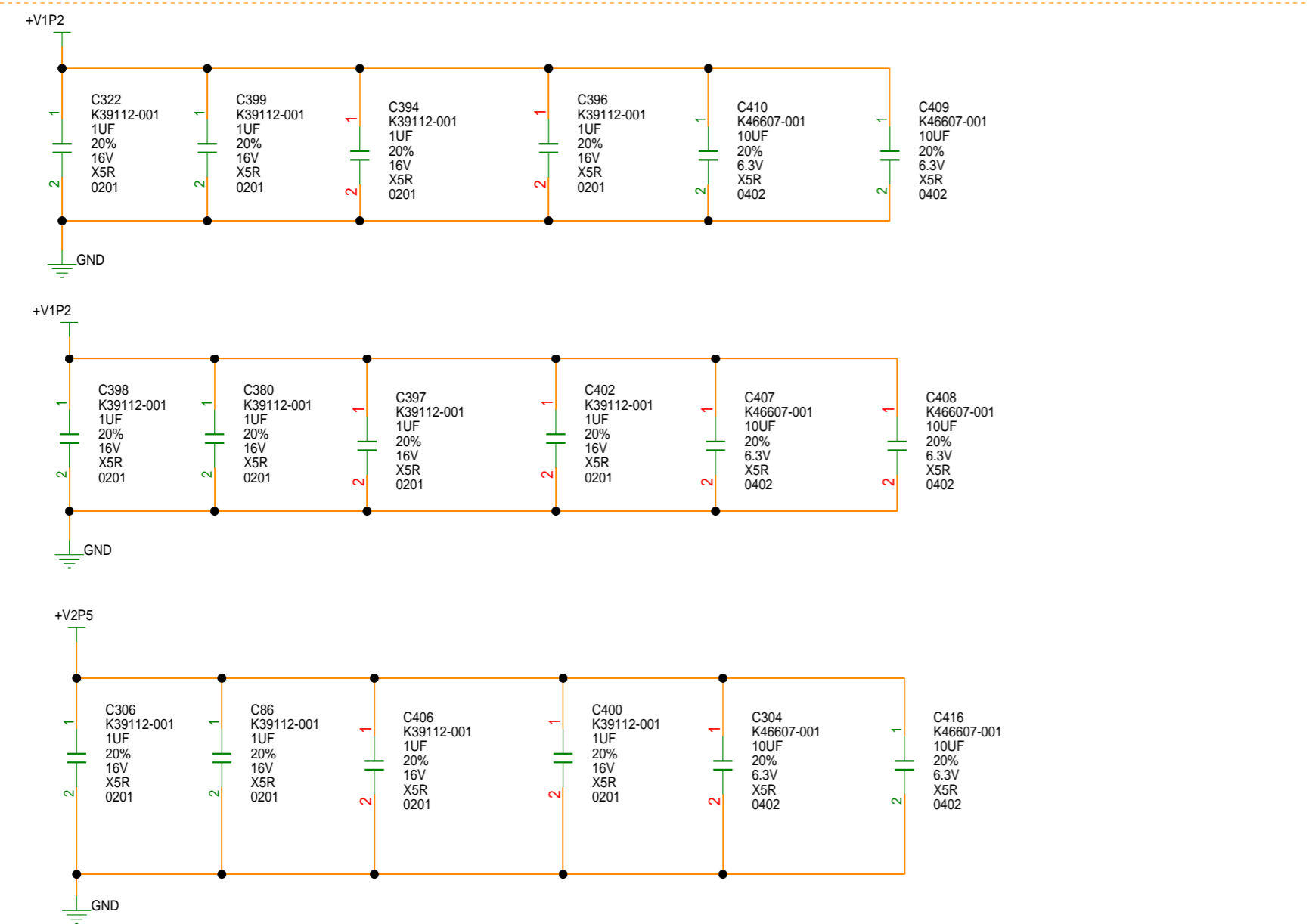
1



BL4 - DQ1
BL5 - DQ2



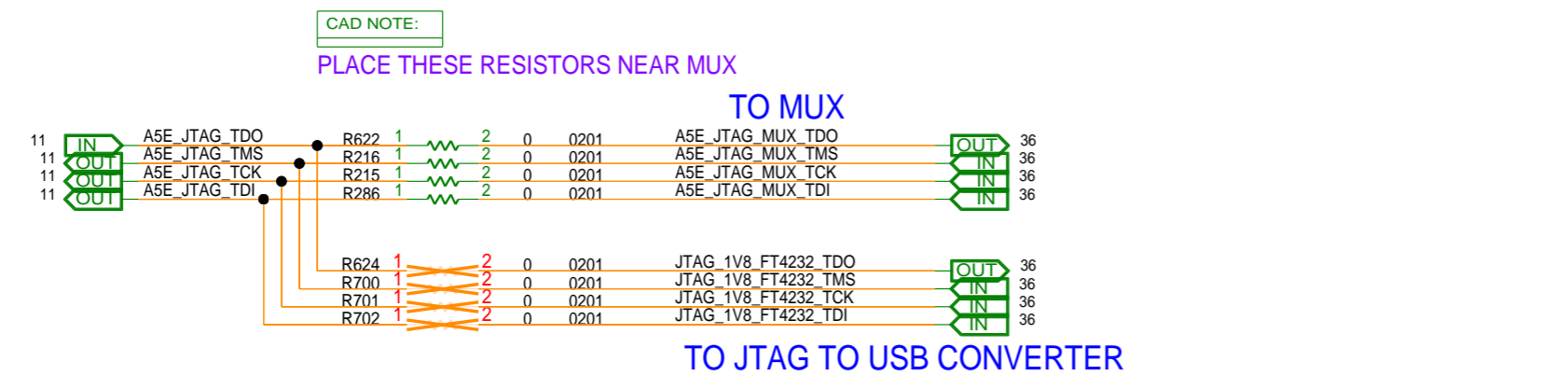
BL6 - DQ3
BL7 - ECC



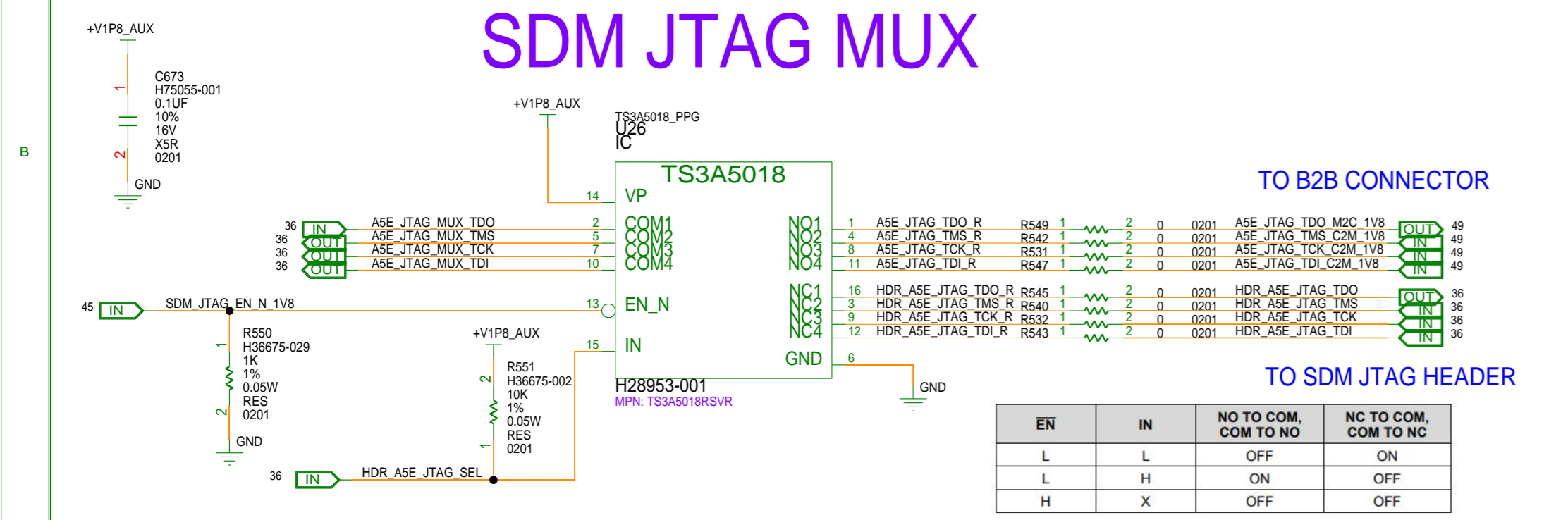
DDR4_X40_BANK3B

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 34 OF 62

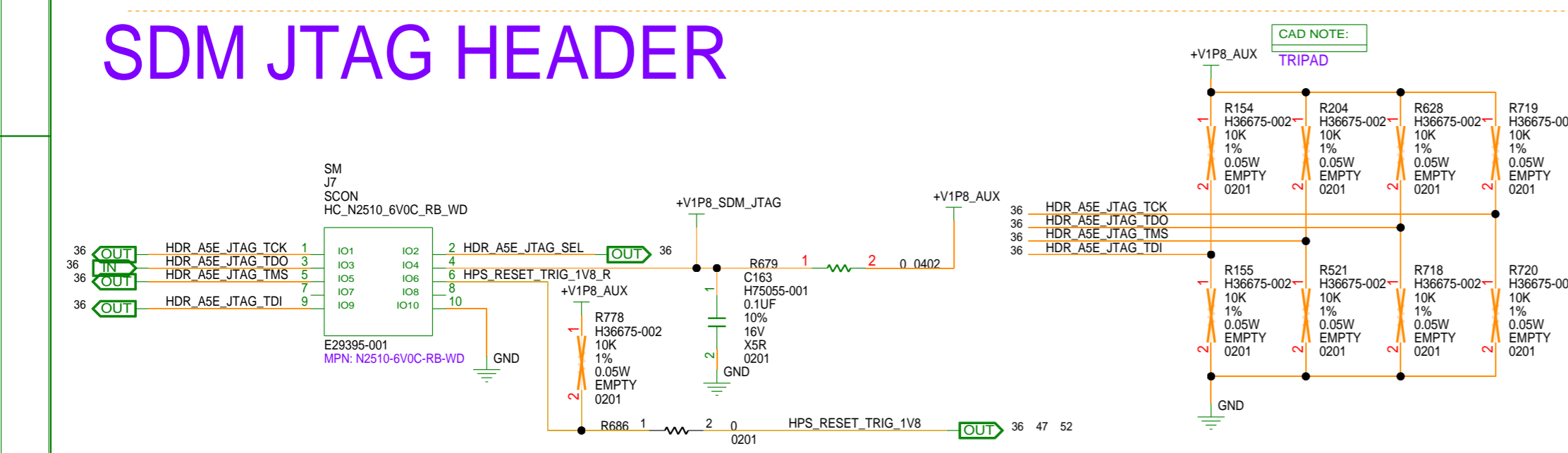
Mon Oct 14 15:09:26 2024



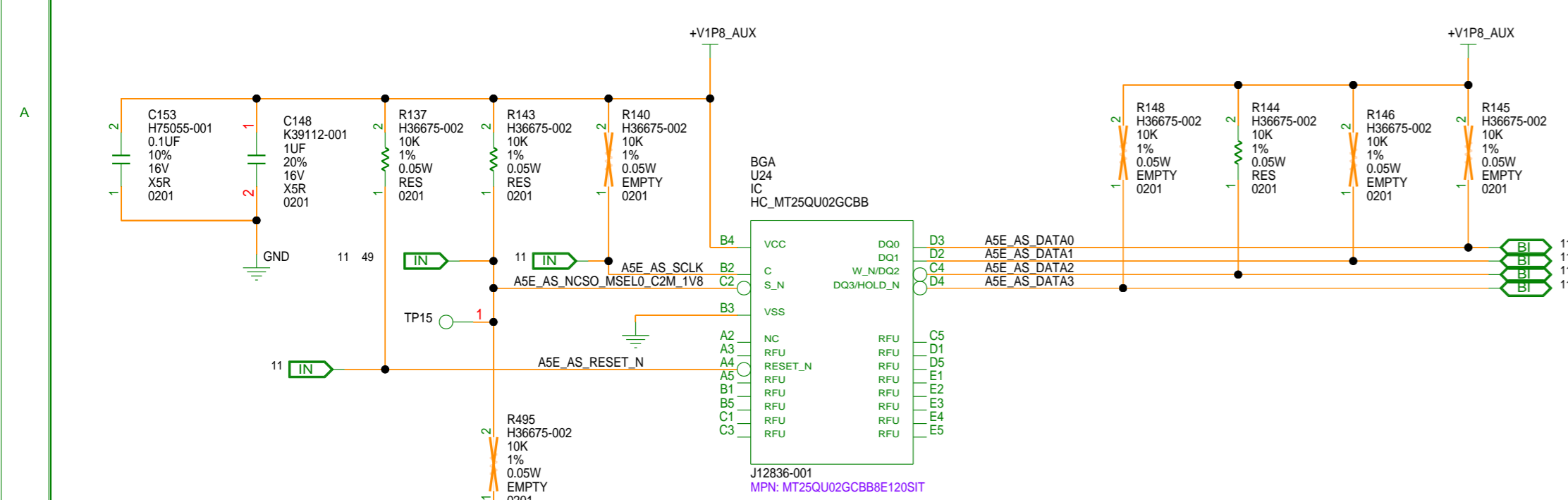
SDM JTAG MUX



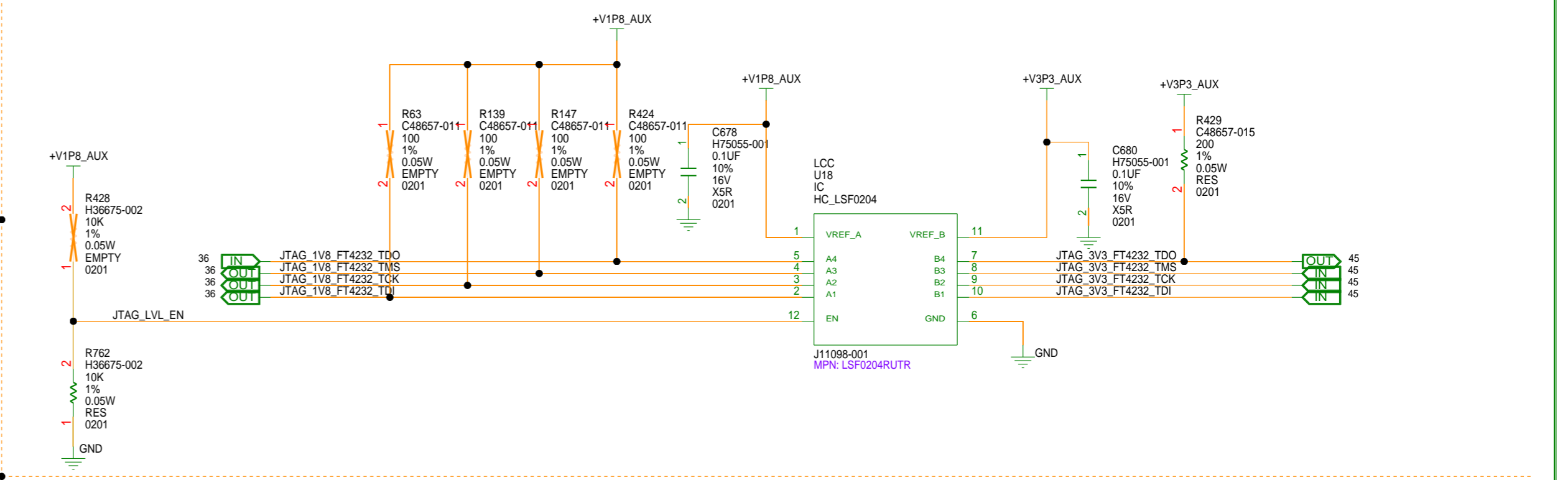
SDM JTAG HEADER



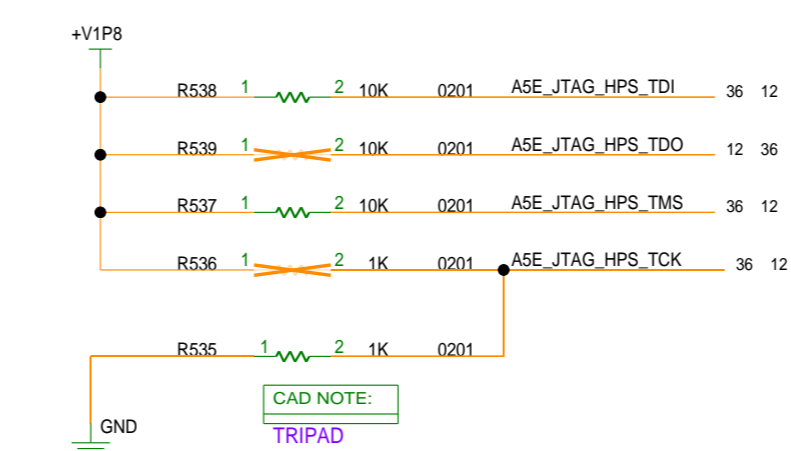
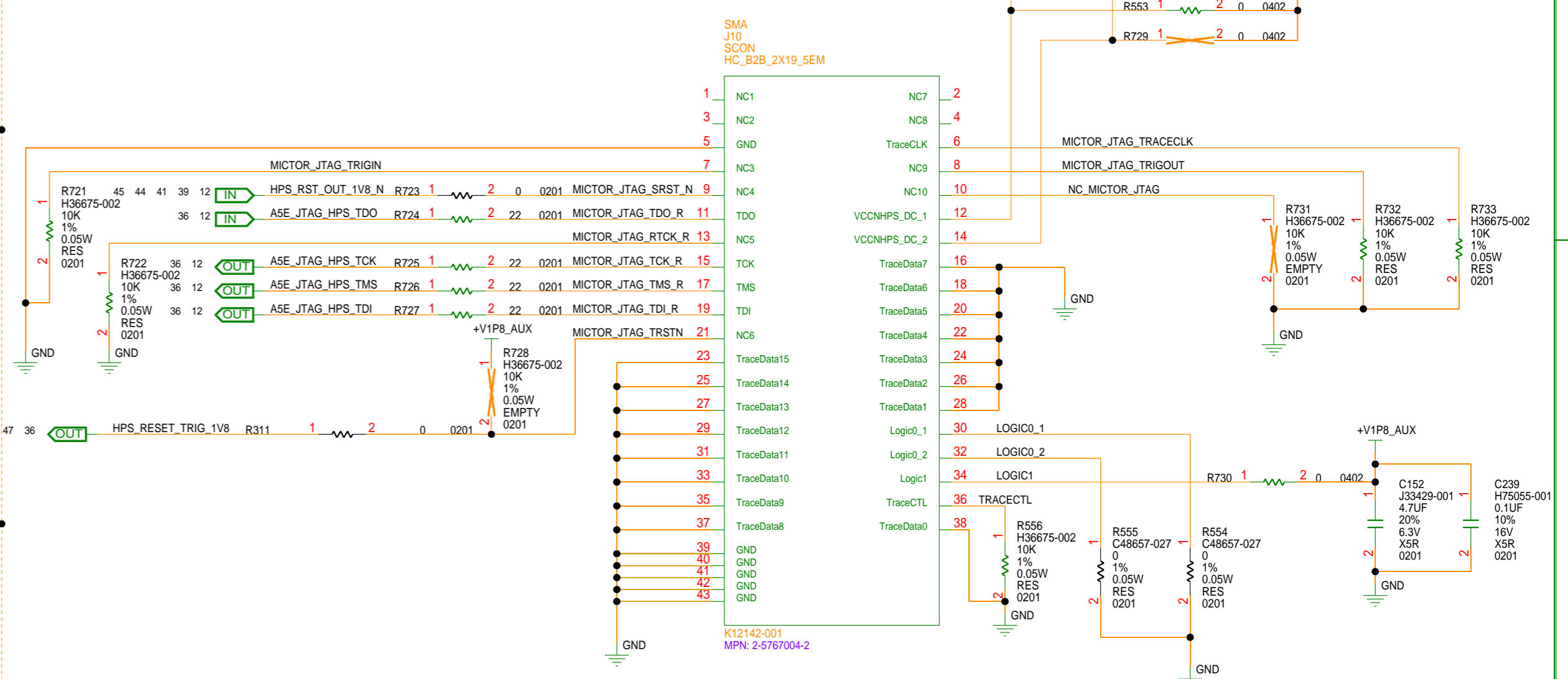
NOR FLASH



SDM JTAG LEVEL SHIFTER

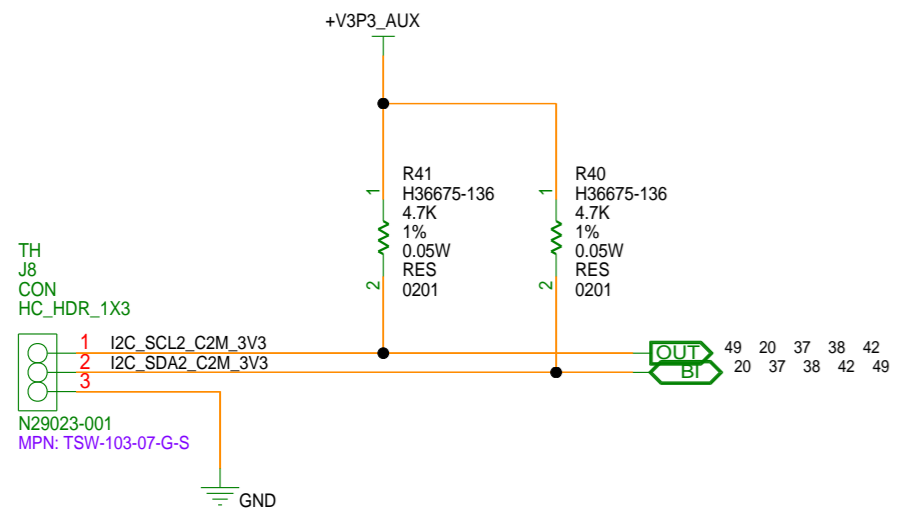
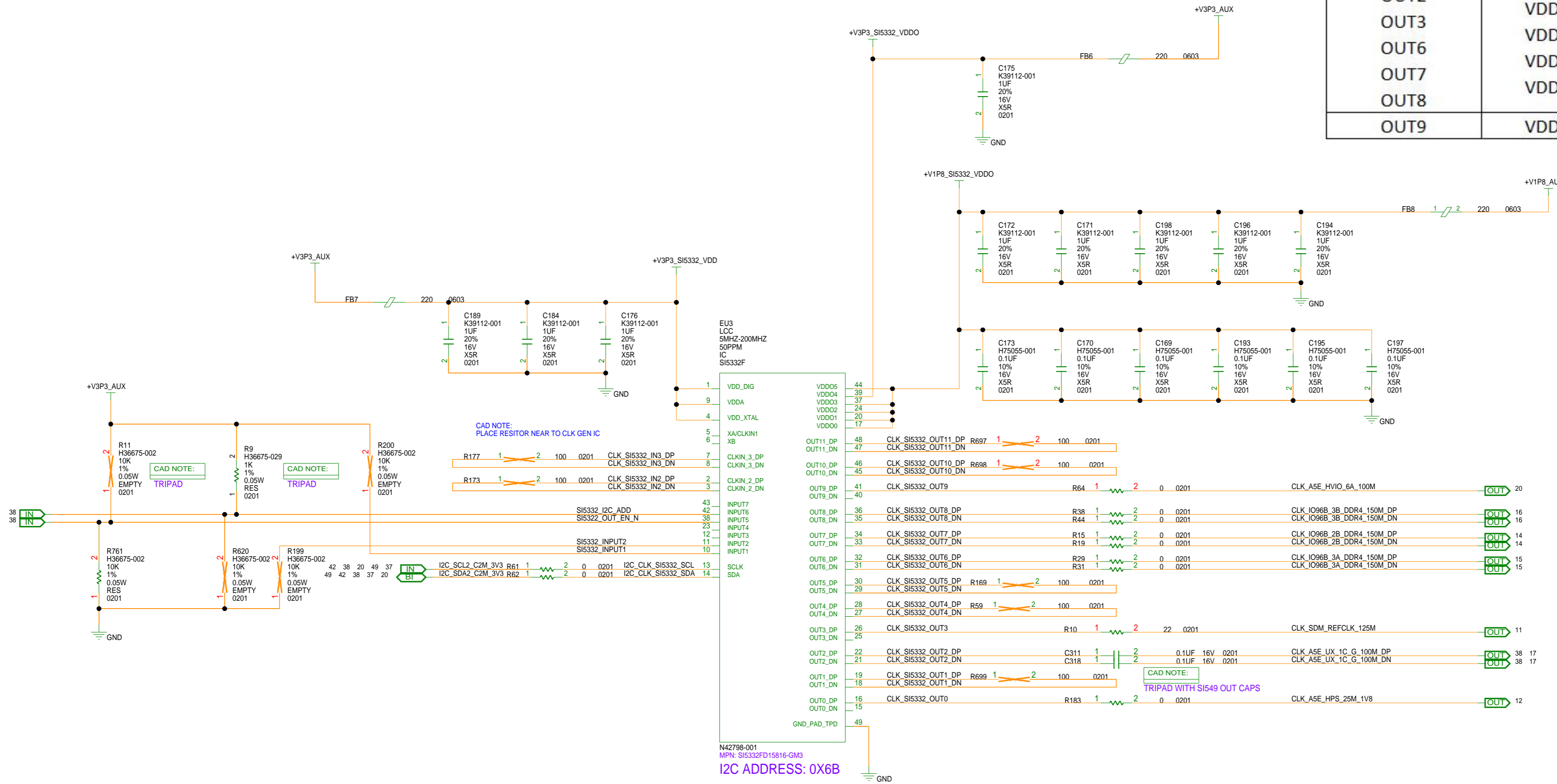


HPS JTAG MICTOR CONN



AG5E - JTAG & NOR FLASH

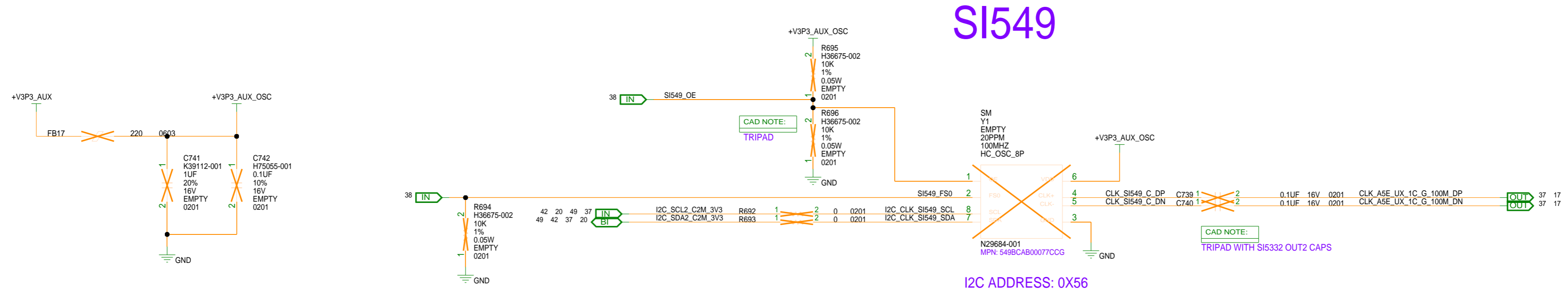
SI5332 Output Channel	SI5332 Output Supply Pin	Rail Name
OUT0	VDDO0	+V1P8_AUX
OUT2	VDDO1	
OUT3	VDDO2	
OUT6	VDDO3	
OUT8	VDDO5	
OUT9	VDDO4	+V3P3_AUX



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CLOCK_SI5332

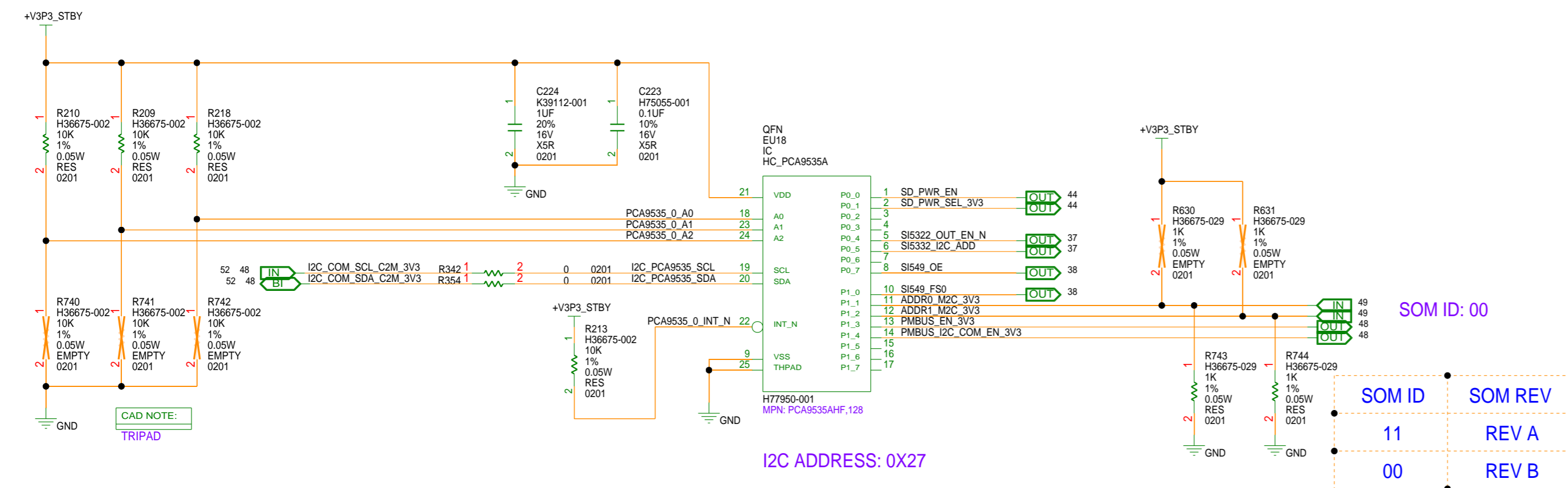
DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING		SHEET	36 OF 62



SI549

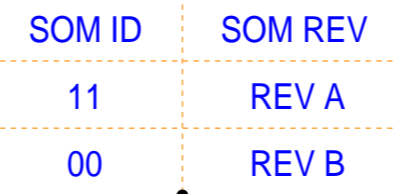
I2C ADDRESS: 0X56

IO EXPANDER



I2C ADDRESS: 0X27

SOM ID: 00



IO_Pad	IO Connected	Direction	Value to be set	Remarks
PO_0	SD_PWR_EN	OUT	High	Enable power for SD card connector
PO_1	SD_PWR_SEL_3V3	OUT	Low	SEL 1: VOUT= VIN2 (+V1P8_AUX) 0: VOUT= VIN1 (+V3P3_AUX) (Default)
PO_2	NC			
PO_3	NC			
PO_4	SI5322_OUT_EN_N	OUT	Low	High: Disable SI5332E Outputs Low: Enable SI5332E Outputs
PO_5	SI5332_I2C_ADD	OUT		
PO_6	NC			
PO_7	SI549_OE	OUT	Low	
P1_0	SI549_FSO	OUT	Low	
P1_1	ADDR0_M2C_3V3	IN		Address input to SoM to determine the location of the SoM in multi SoM carrier card.
P1_2	ADDR0_M2C_3V3	IN		Address input to SoM to determine the location of the SoM in multi SoM carrier card.
P1_3	PMBUS_EN_3V3	OUT	High	Enable the I2C buffer/isolator U31
P1_4	PMBUS_I2C_COM_EN_3V3	OUT	Low	Disable the I2C buffer/isolator U30
P1_5	NC			
P1_6	NC			
P1_7	NC			

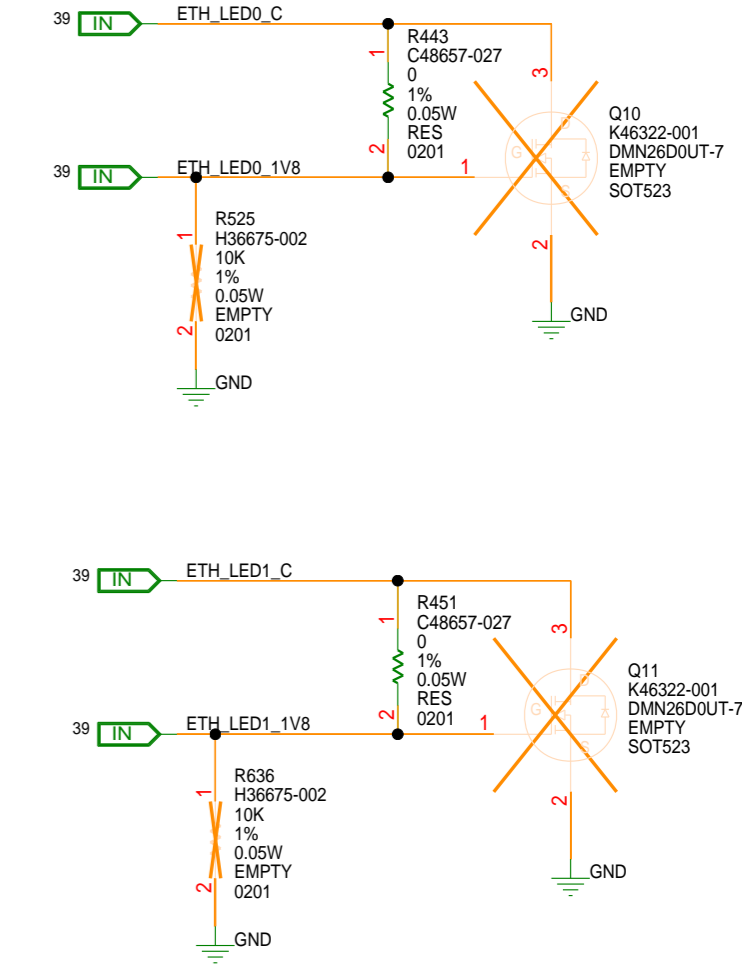
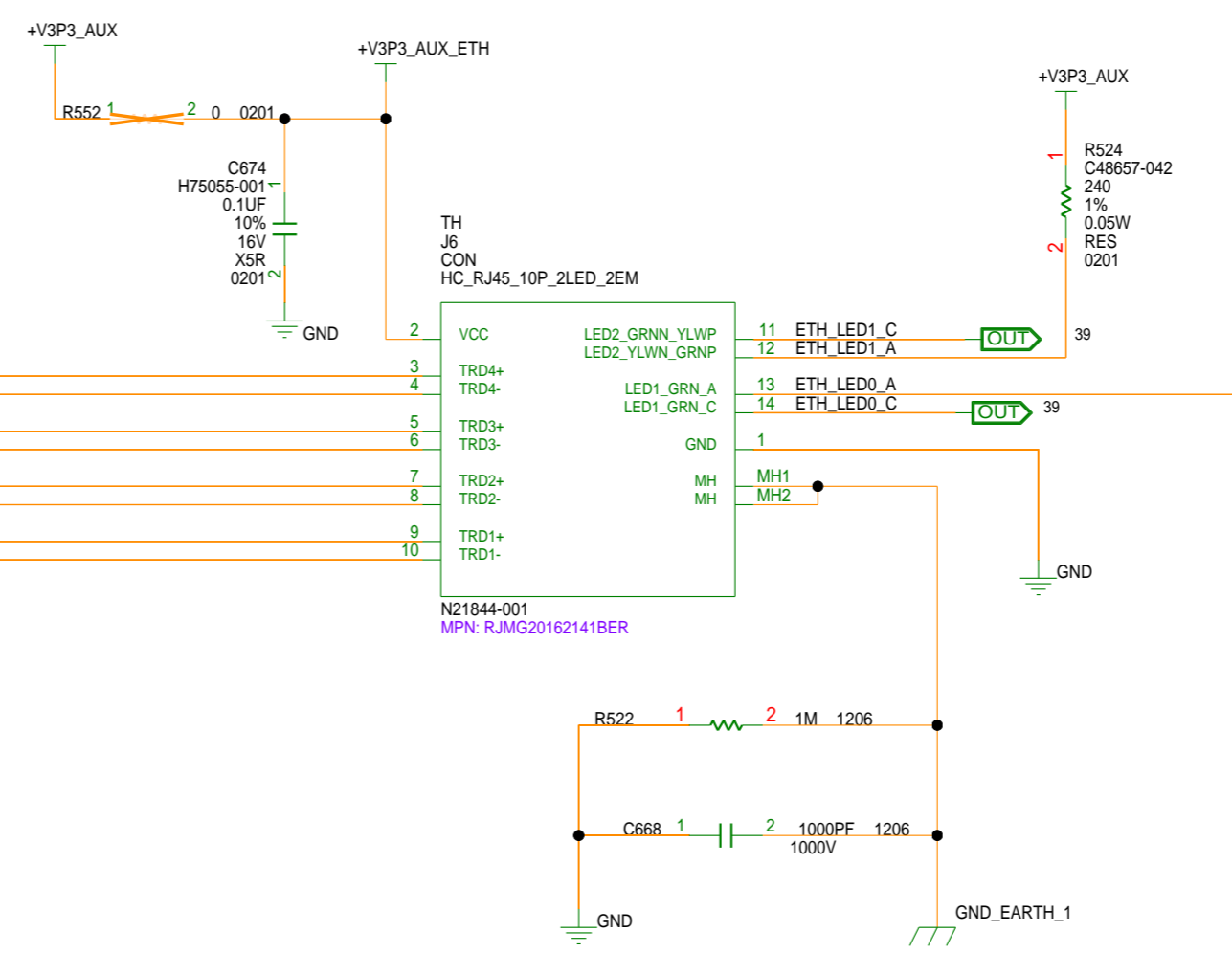
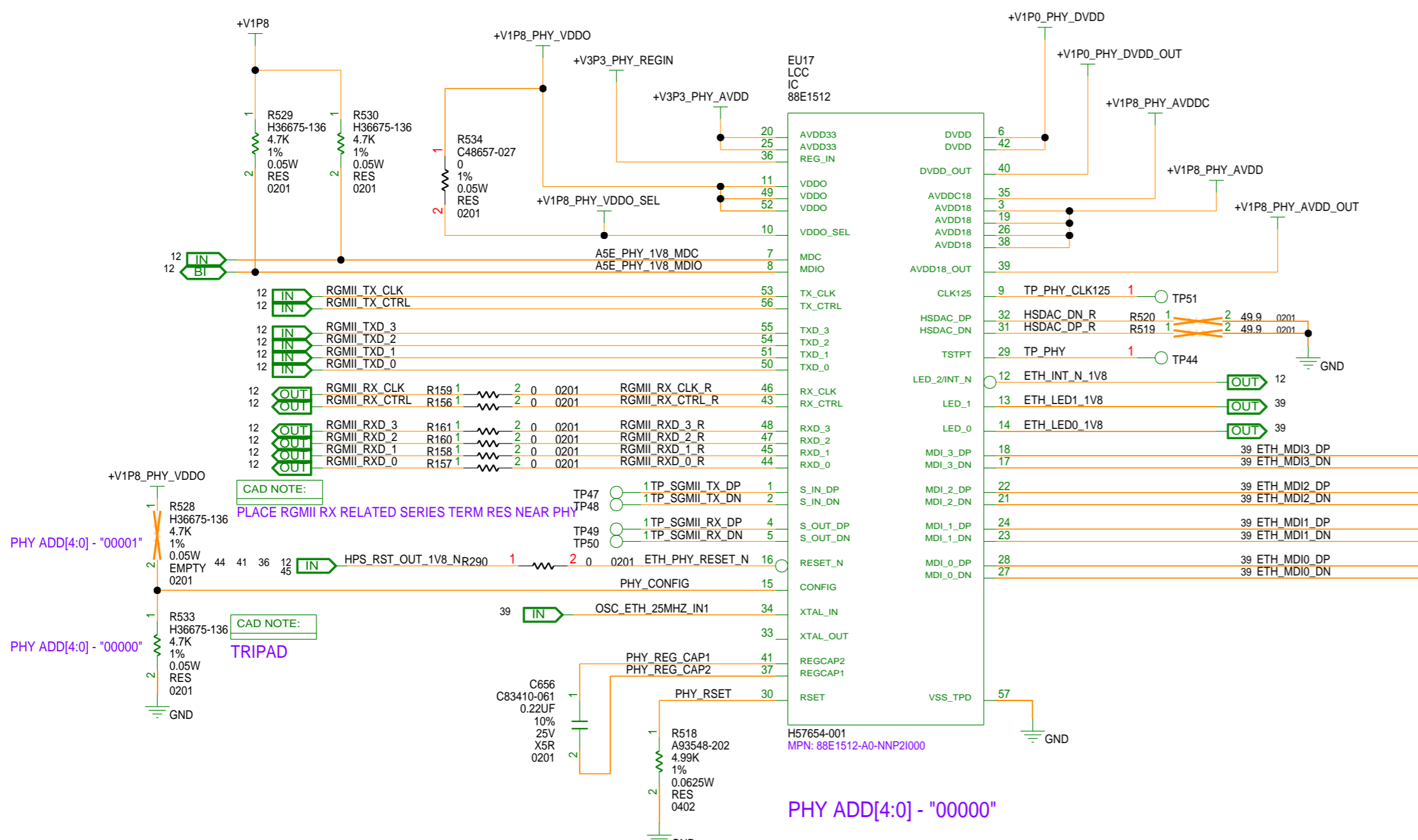
Mon Oct 14 15:09:35 2024

CLOCK_SI549 & GPIO_EXPANDER

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING		SHEET	37 OF 62

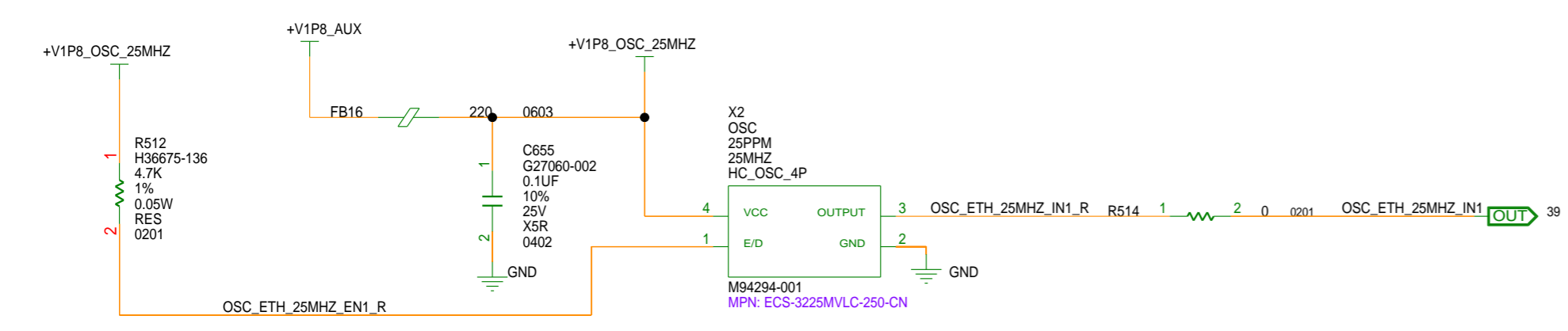
ETHERNET PHY

LED	FUNCTION
LED0 - GREEN	3 BLINKS - 1000MBPS 2 BLINKS - 100MBPS 1 BLINK - 10MBPS OFF - NO LINK
LED1 - YELLOW	ON - LINK BLINK - ACTIVITY OFF - NO LINK

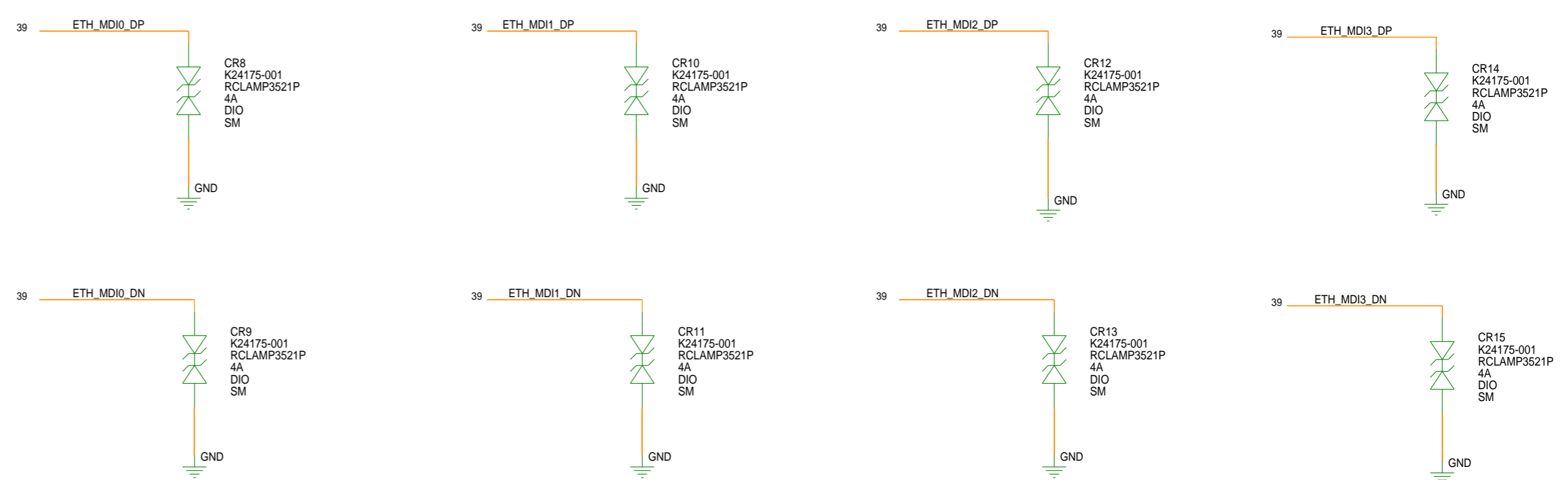


LED POLARITY:
 LED0 (REGISTER 17_3[10]: 00
 00 = ON - DRIVE LED[0] LOW, OFF - DRIVE LED[0] HIGH
 LED1 (REGISTER 17_3[3:2]: 00
 00 = ON - DRIVE LED[1] LOW, OFF - DRIVE LED[1] HIGH

25MHZ CLOCK



ESD DIODE



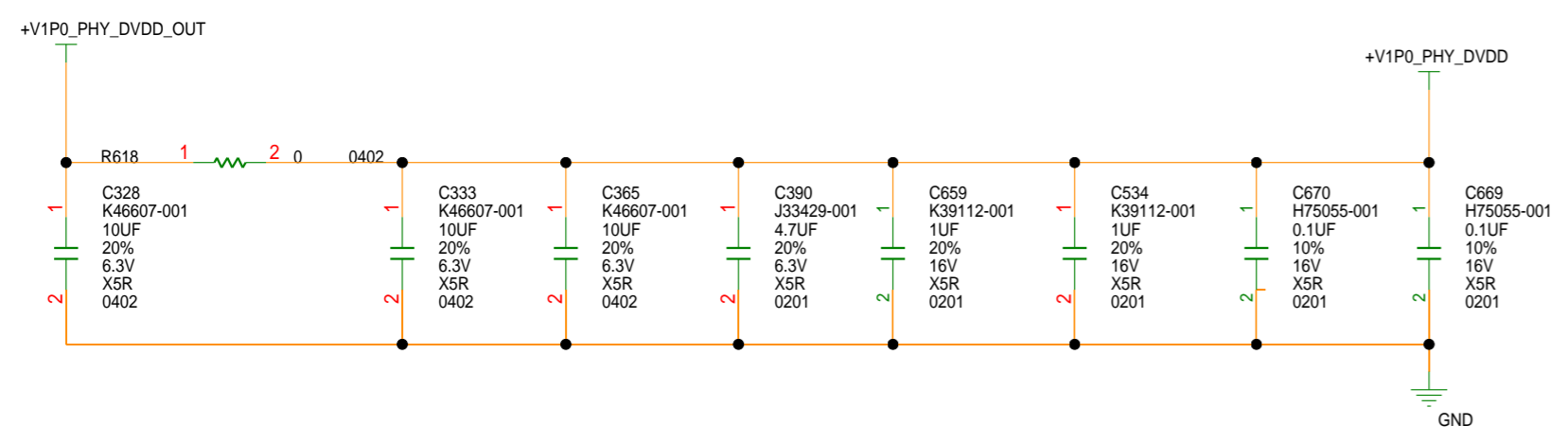
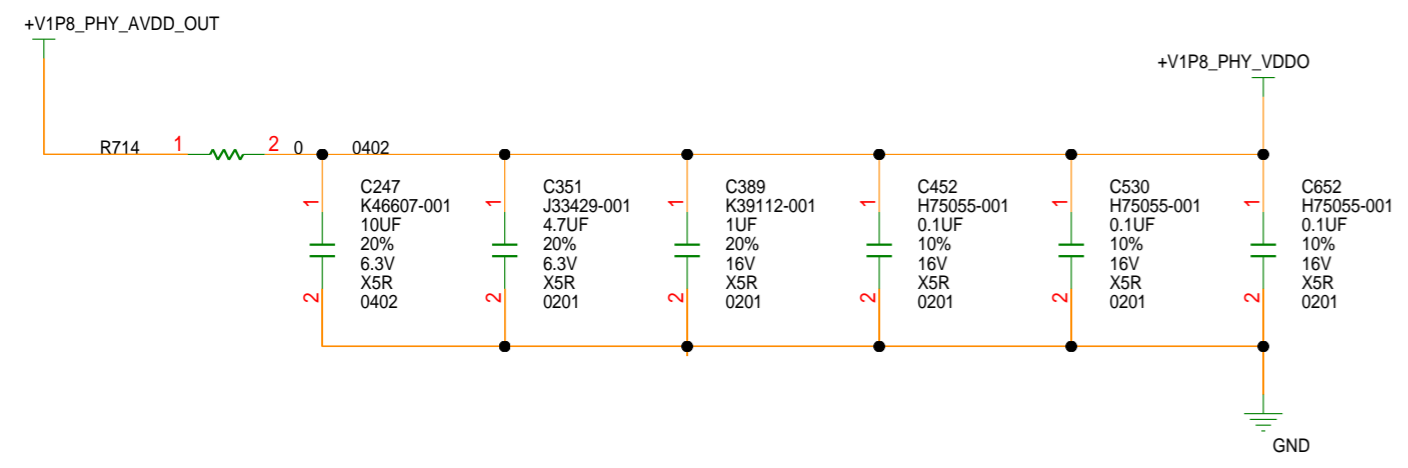
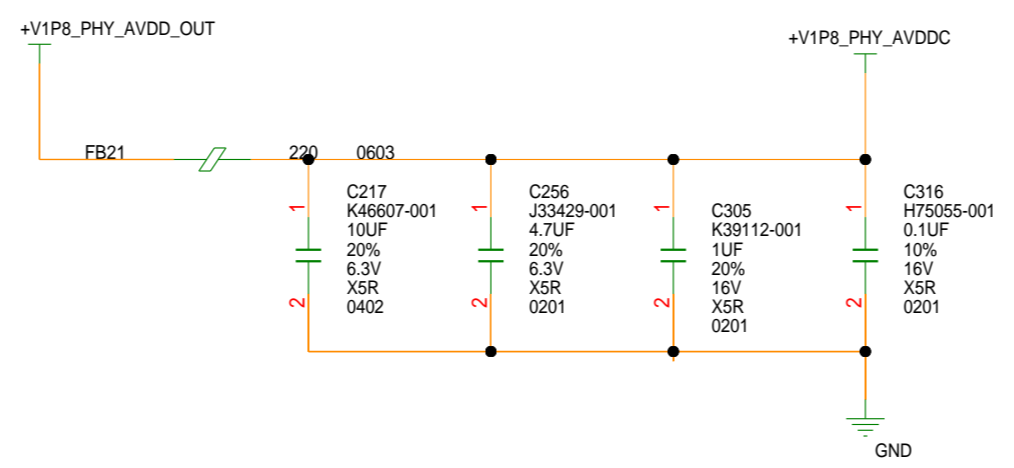
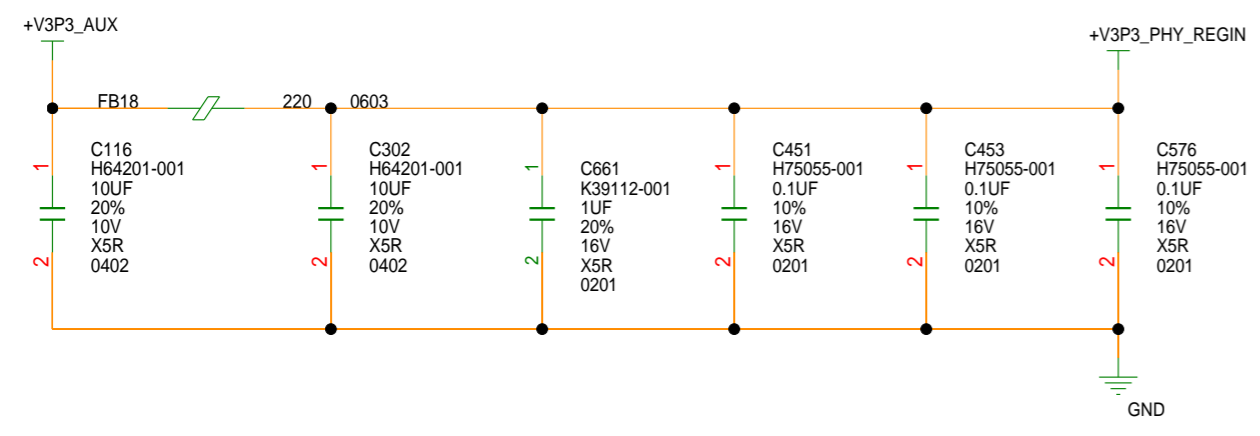
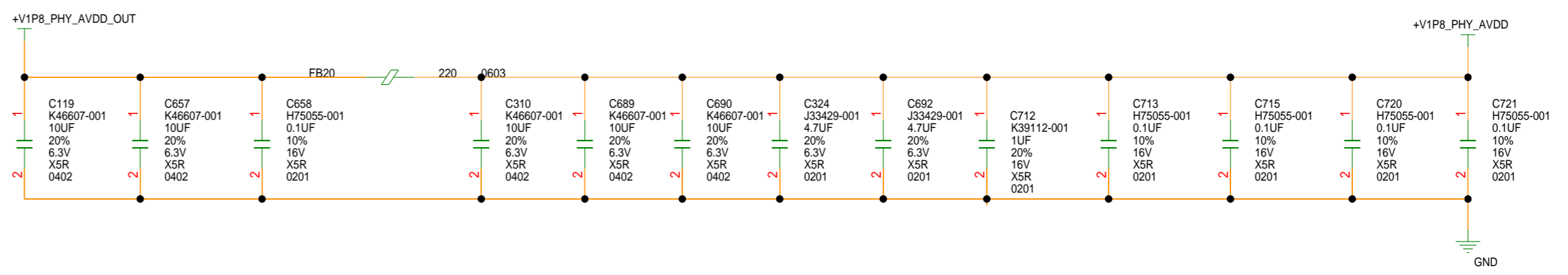
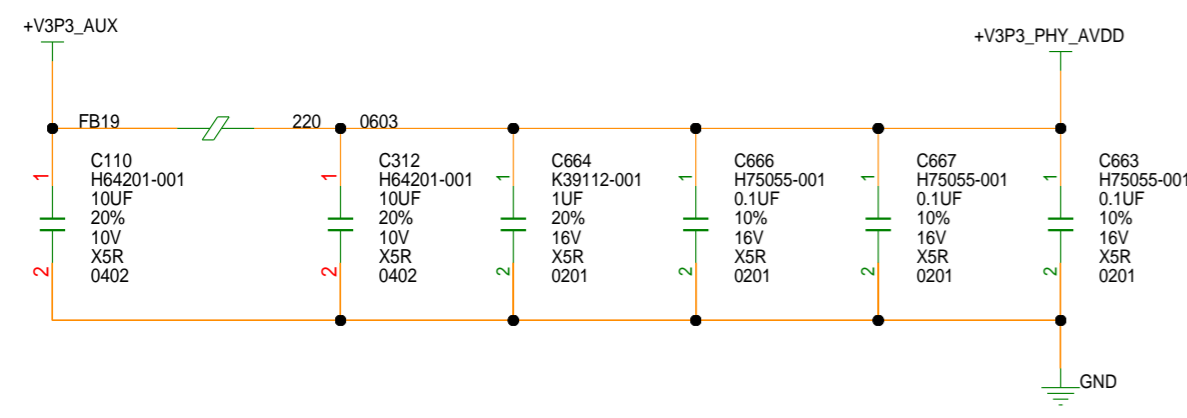
ETHERNET

DEPARTMENT	altera An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 38 OF 62

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B

B



Mon Oct 14 15:09:39 2024

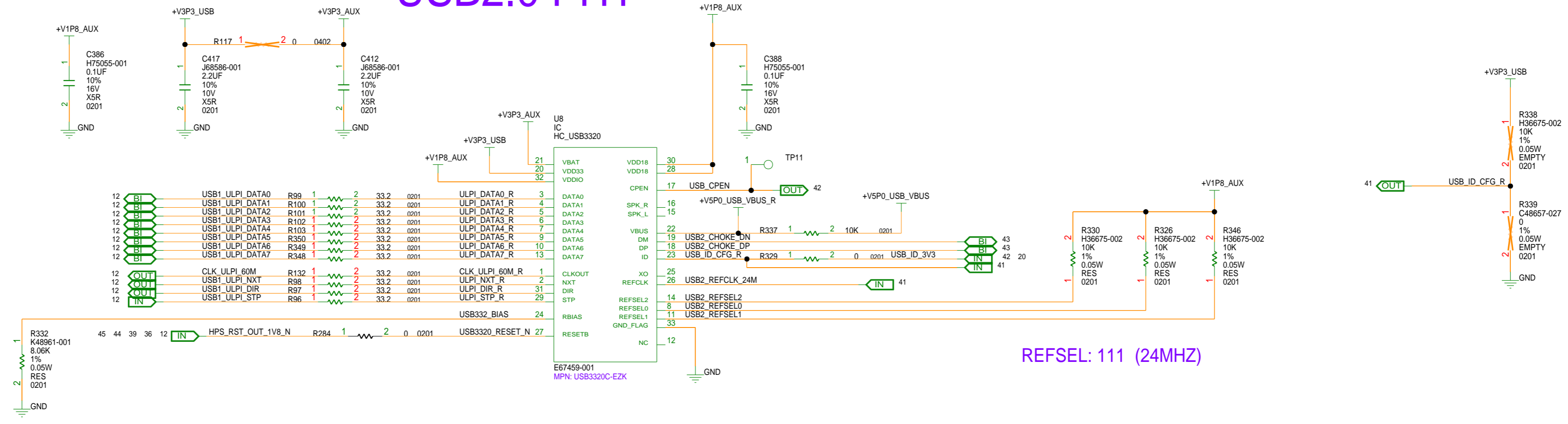
ETHERNET_PHY_DECAP

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 39 OF 62

A

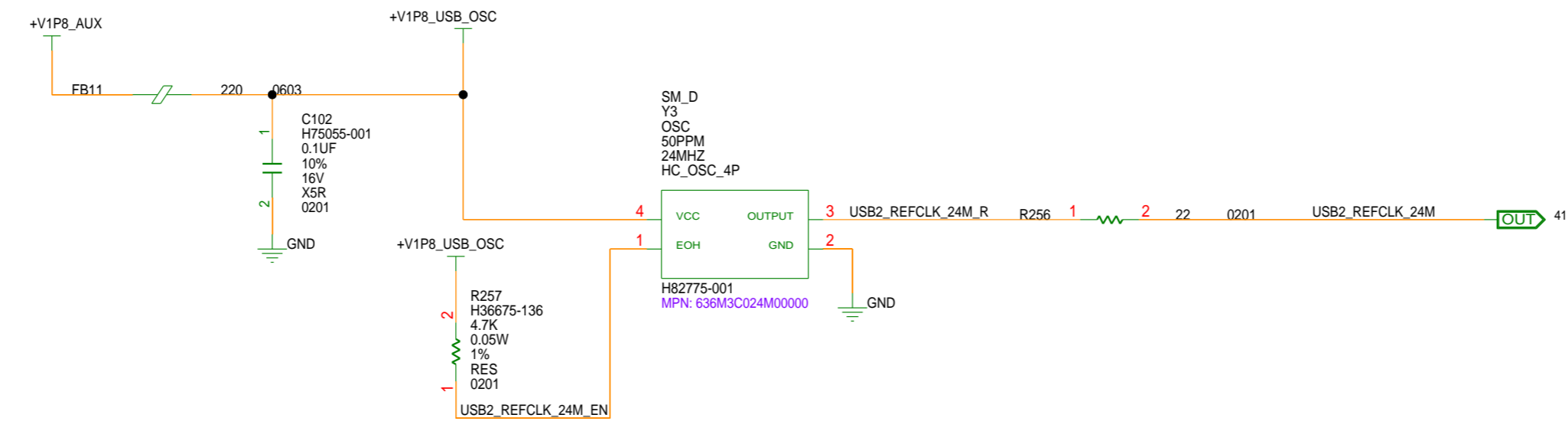
A

USB2.0 PHY




REFSEL: 111 (24MHZ)

24MHZ CLOCK

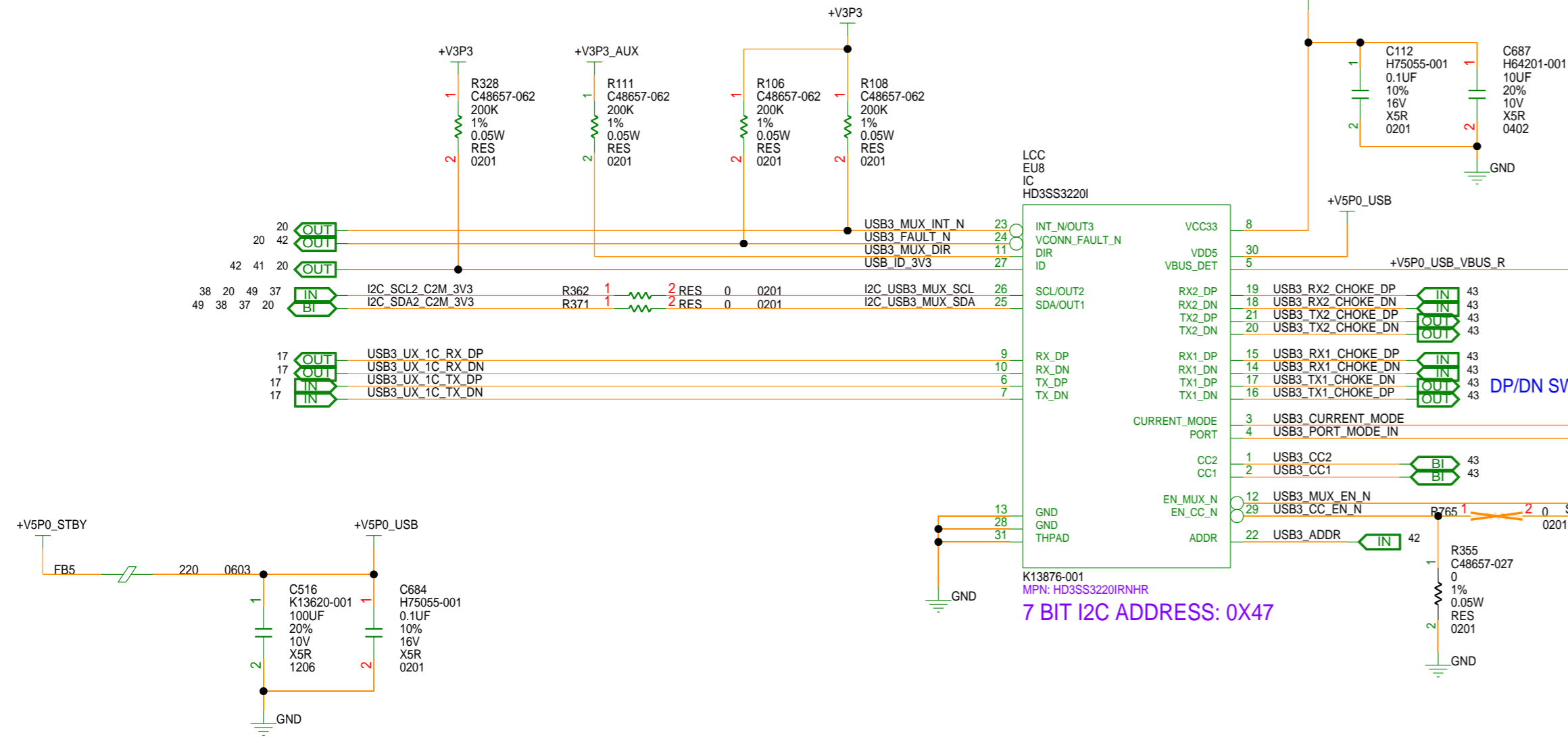


USB2.0PHY

Mon Oct 14 15:09:41 2024

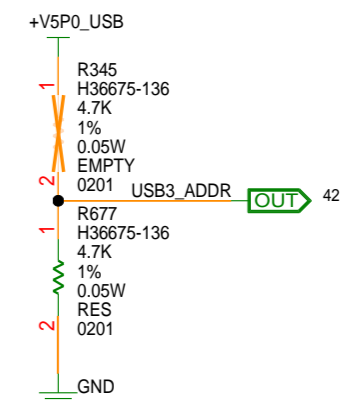
DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 40 OF 62

USB3.0 MUX

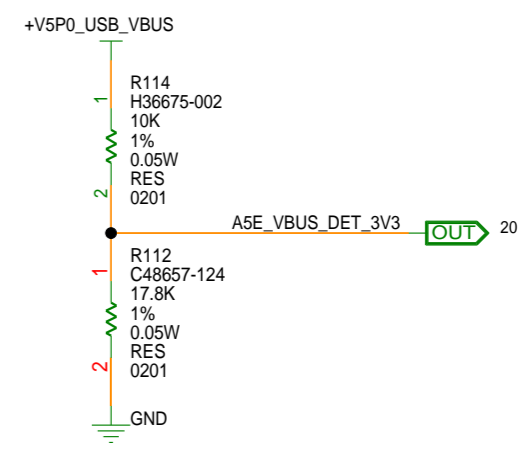


PORT	USB MODE
HIGH	DFP
LOW	UFP
NC	DRP

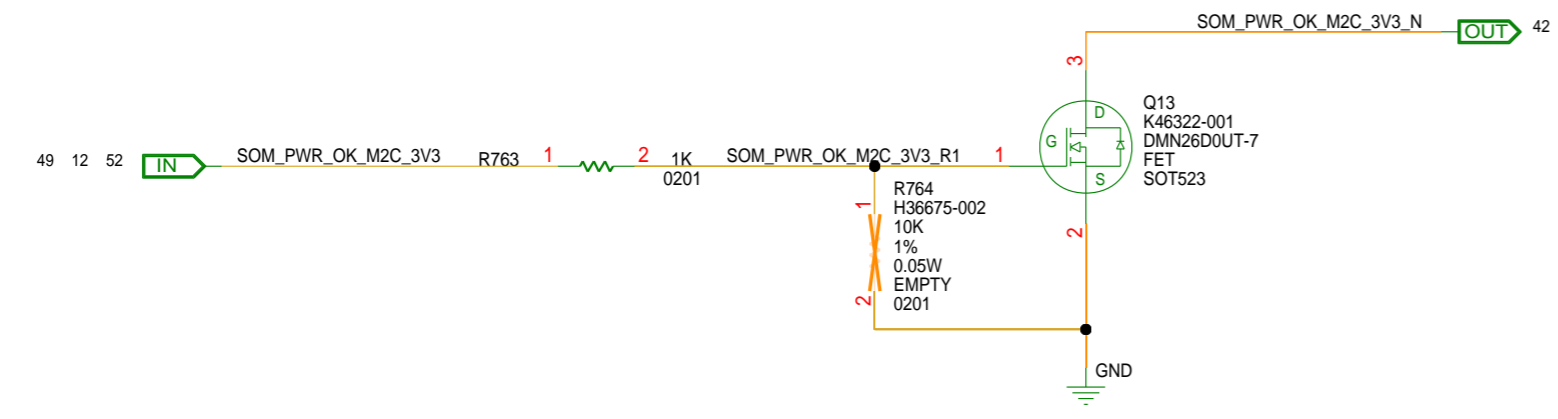
ADDR



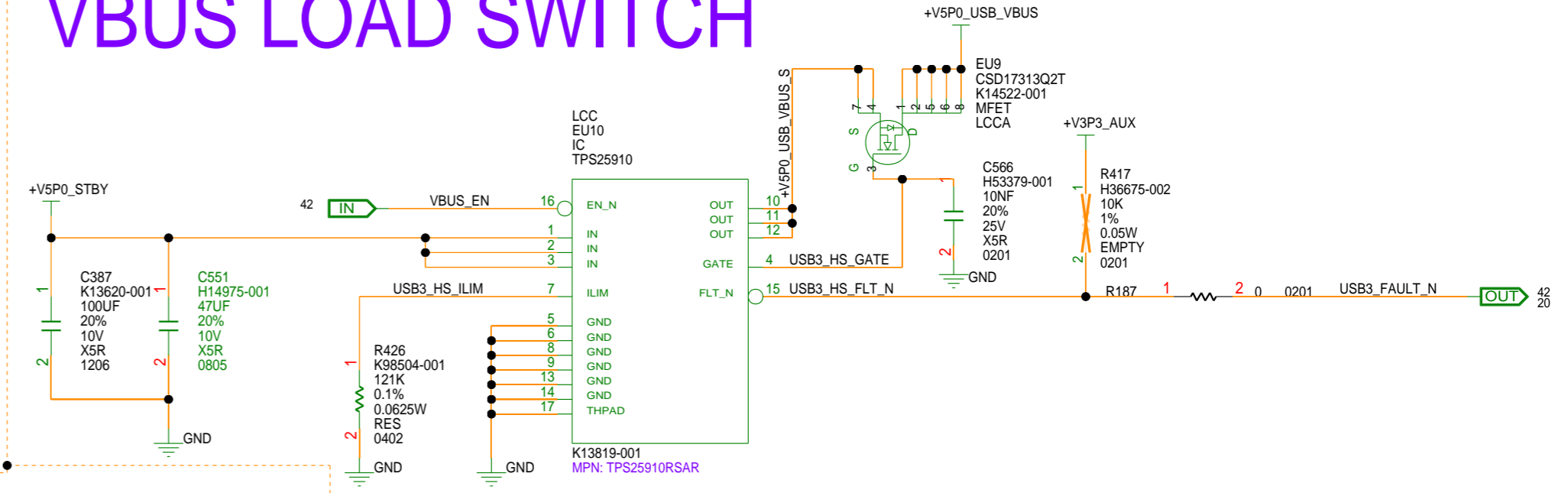
VBUS DETECT



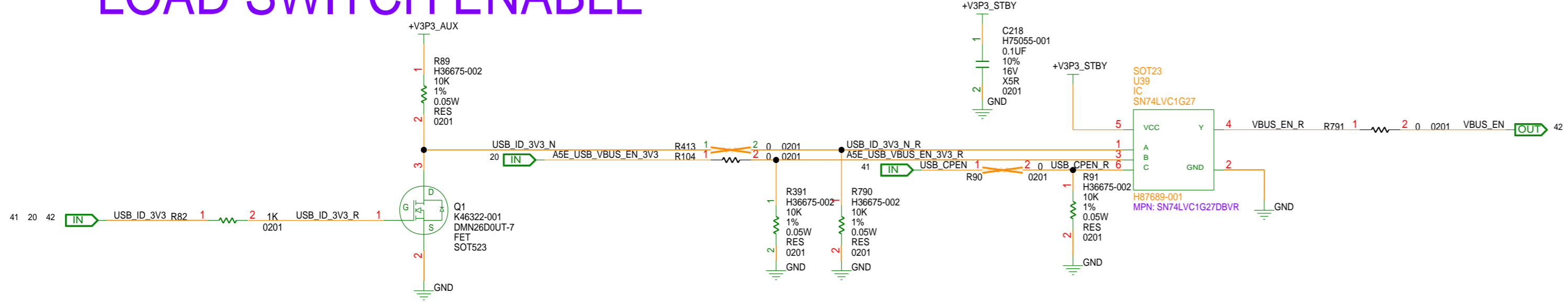
MUX CC ENABLE



VBUS LOAD SWITCH



LOAD SWITCH ENABLE

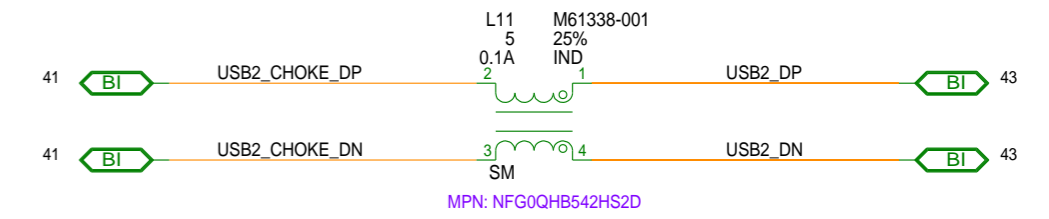
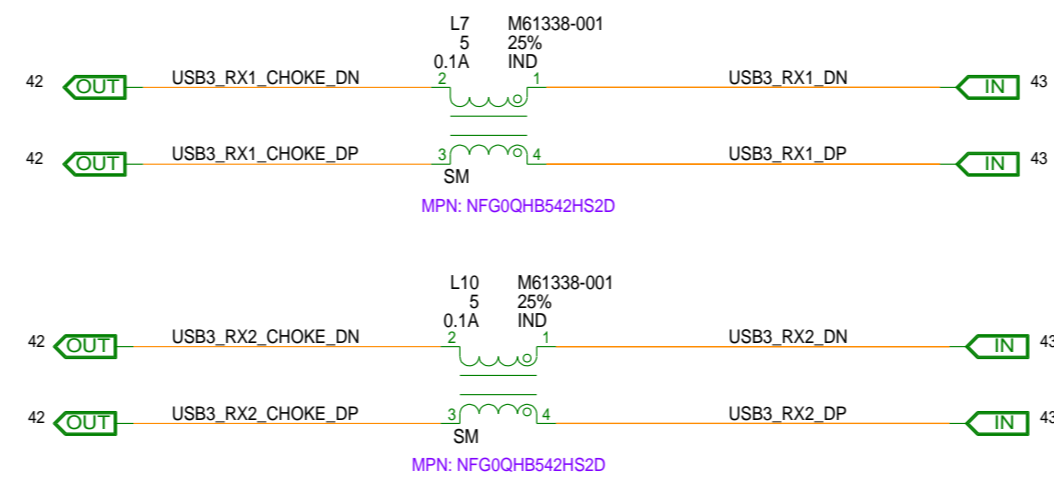
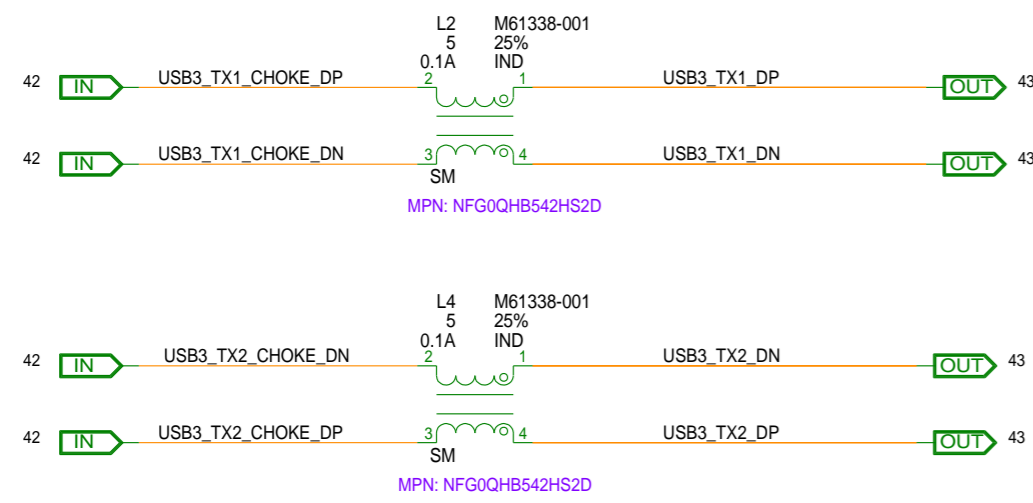


TYPE-C CURRENT (AMPS)	CURRENT_MODE	ILIM RESISTOR
0.9	DEFAULT (250K INTERNAL PULL DOWN)	200K
1.5	500K TO VDD5	120K

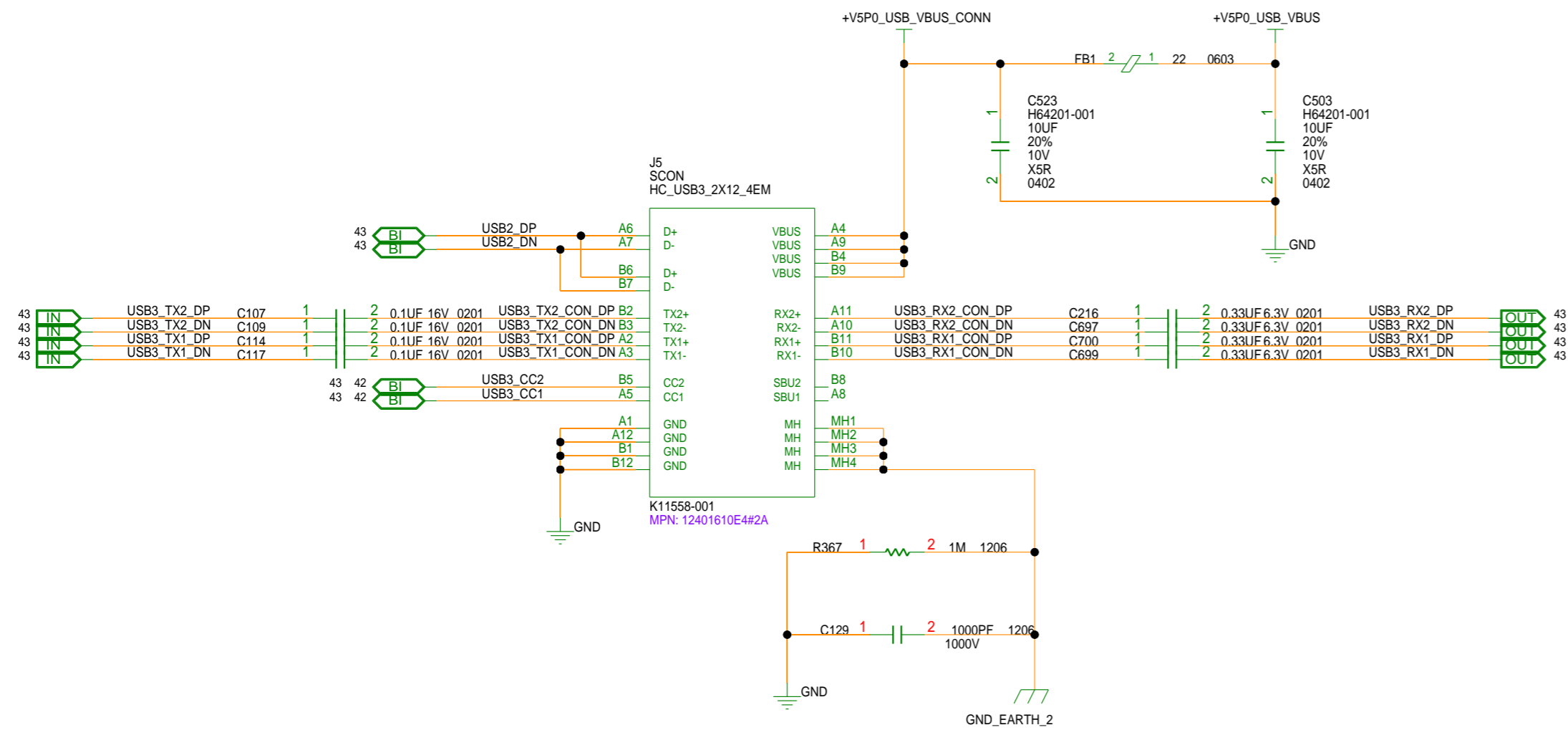
USB3.0 MUX

Mon Oct 14 15:09:44 2024

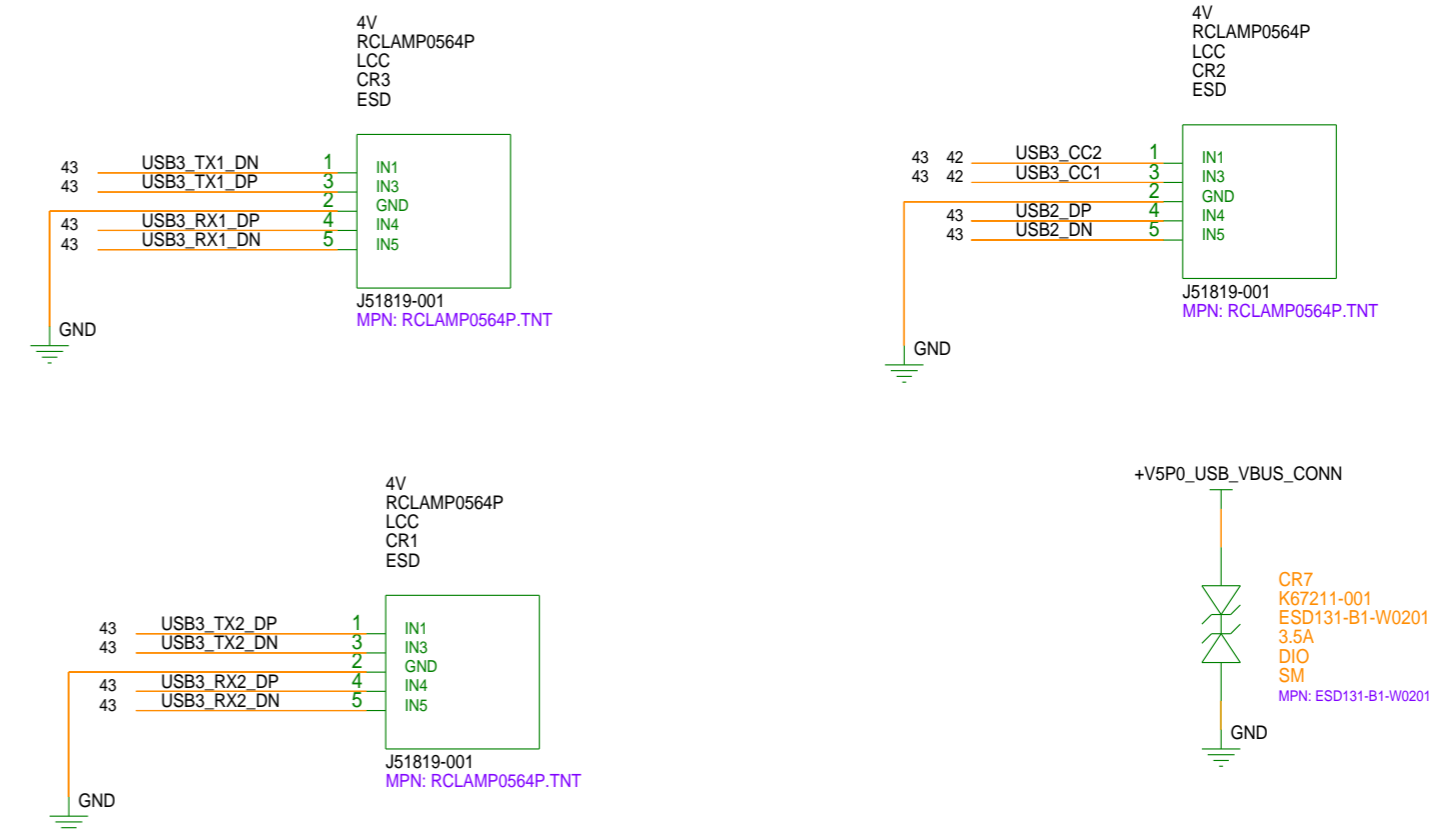
COMMON MODE CHOKE



TYPE C CONN



ESD DIODE

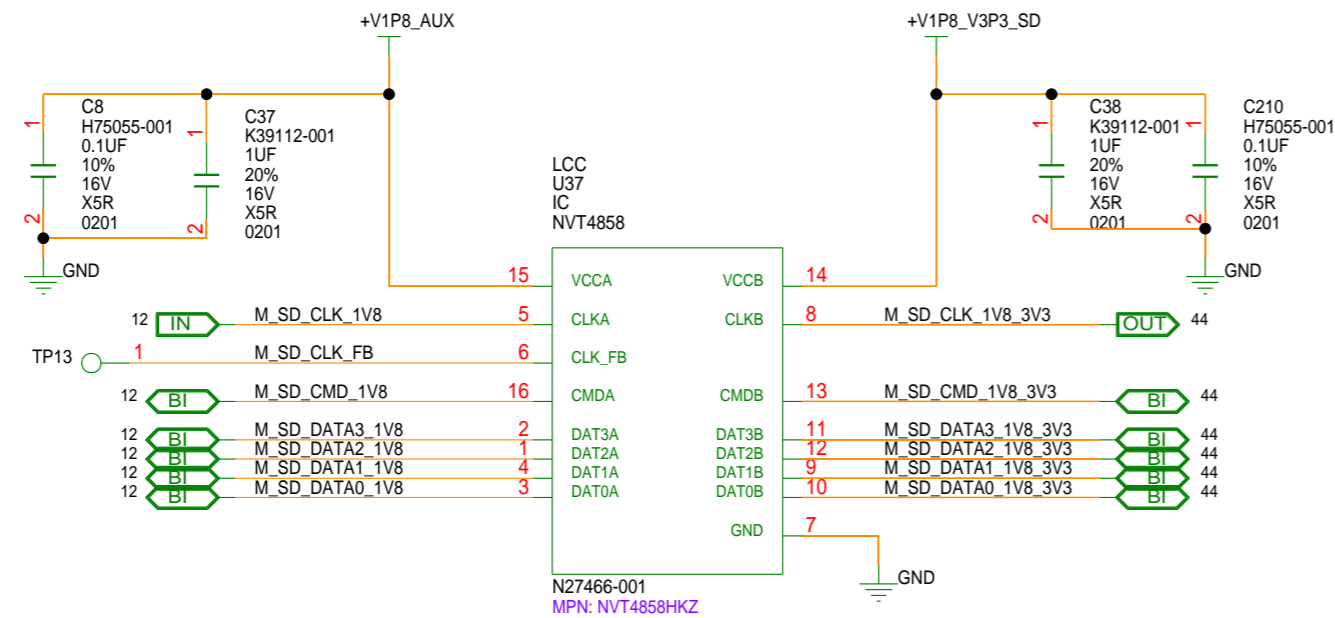


USB3.0 CONN

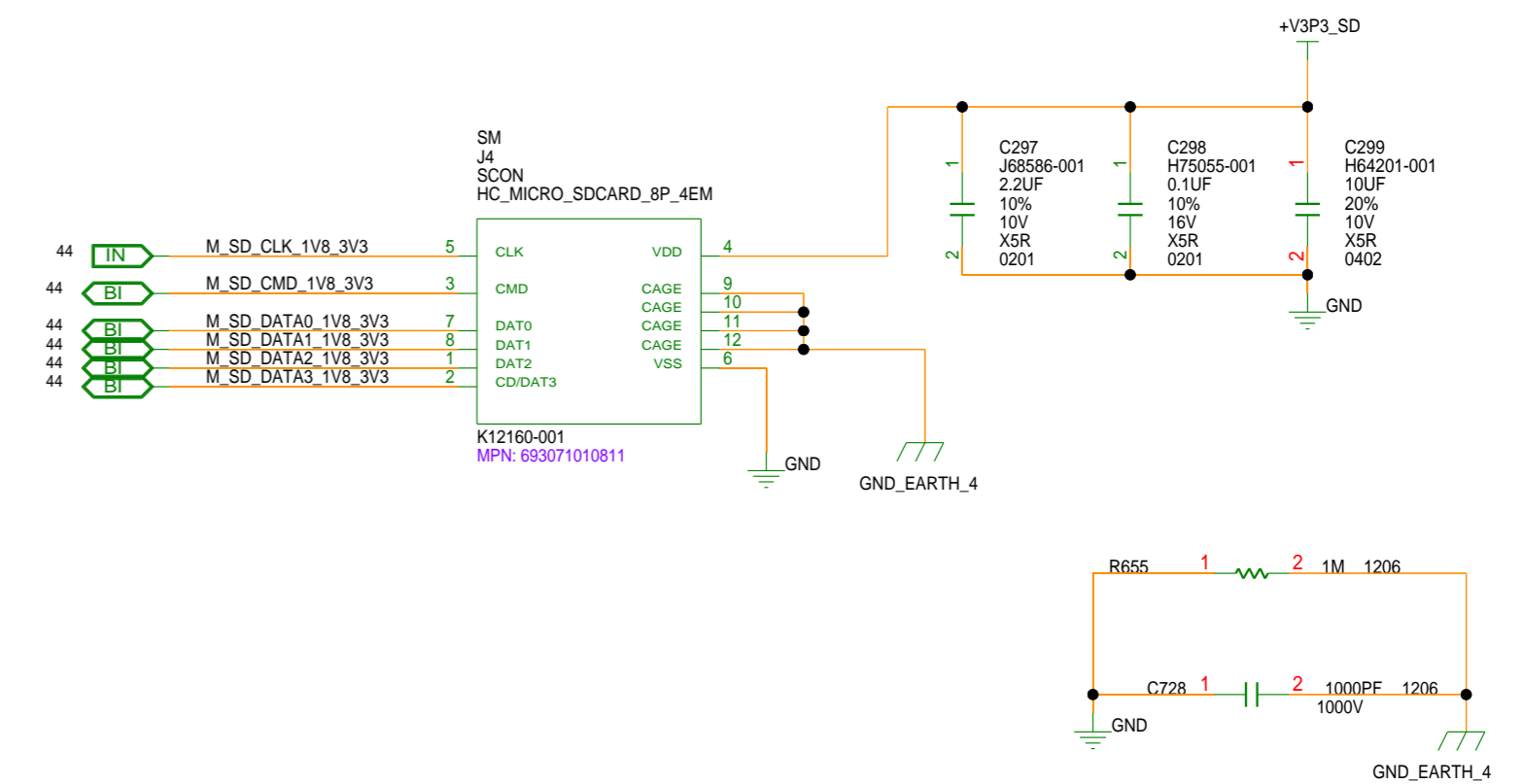
Mon Oct 14 15:09:47 2024

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 42 OF 62

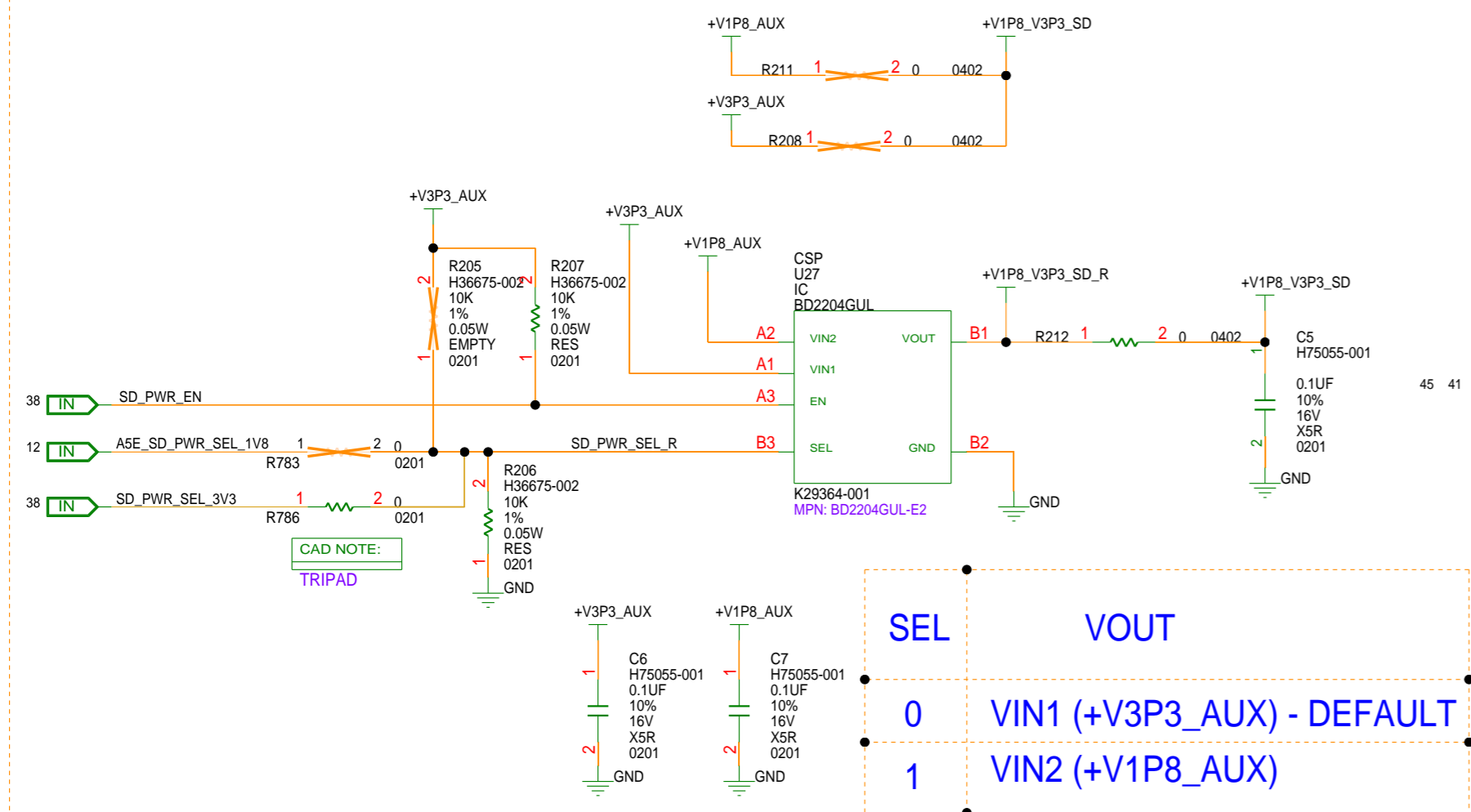
LEVEL SHIFTER



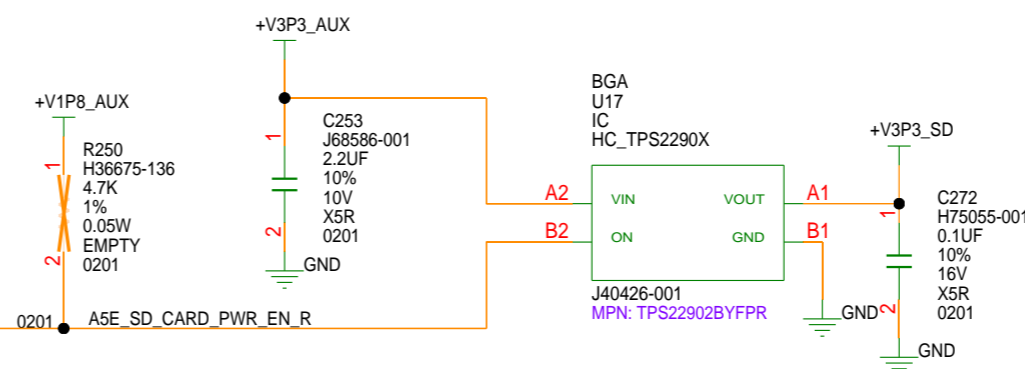
MICRO SD CARD CONNECTOR



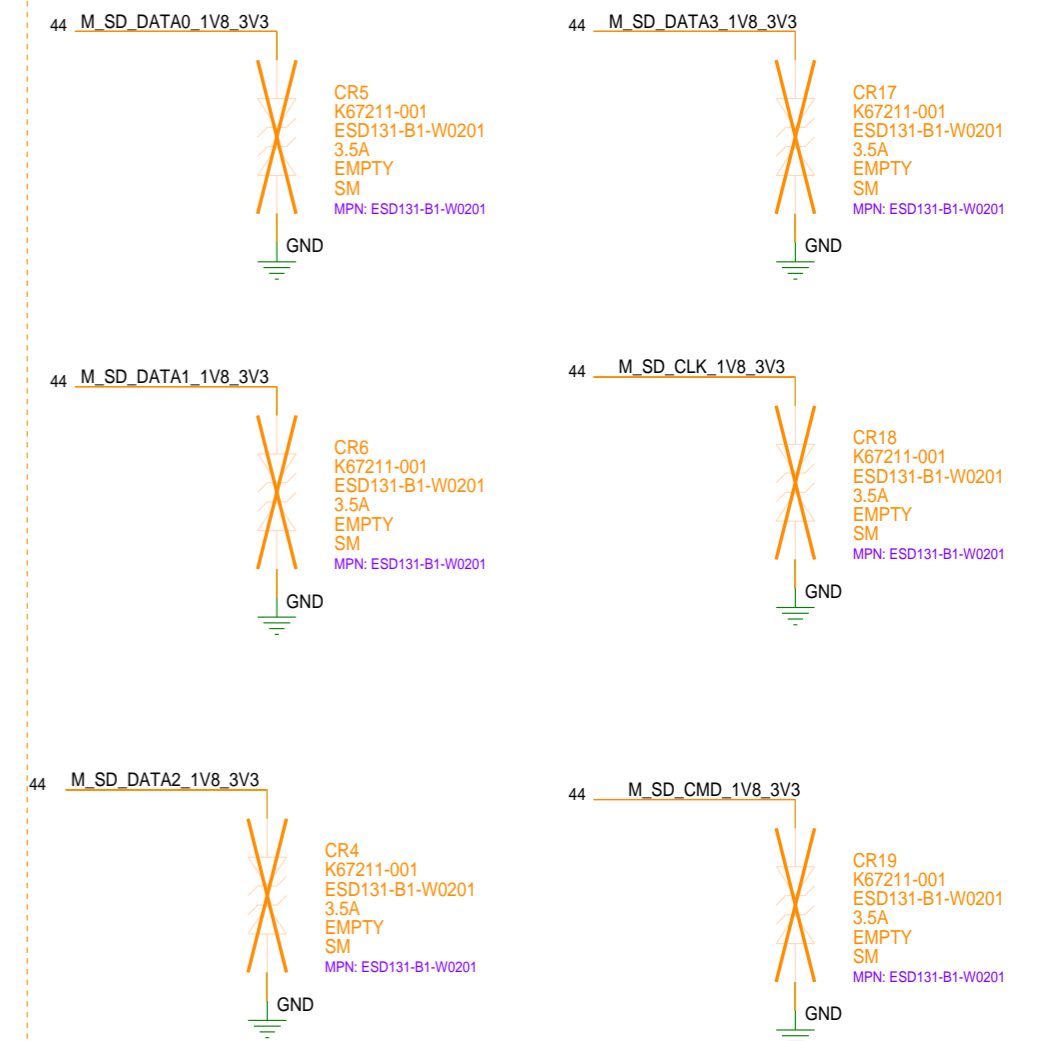
POWER SELECTION



LOAD SWITCH



ESD DIODE



SD CARD

DEPARTMENT



SIZE
C+

CODE
34649

DOCUMENT NUMBER
150-0330723-B1

REV
2.1

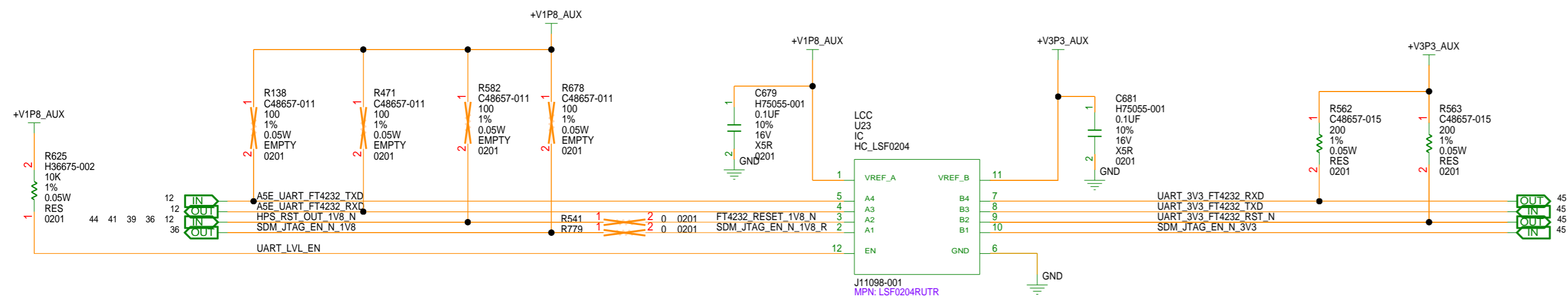
SCALE:

DO NOT SCALE DRAWING

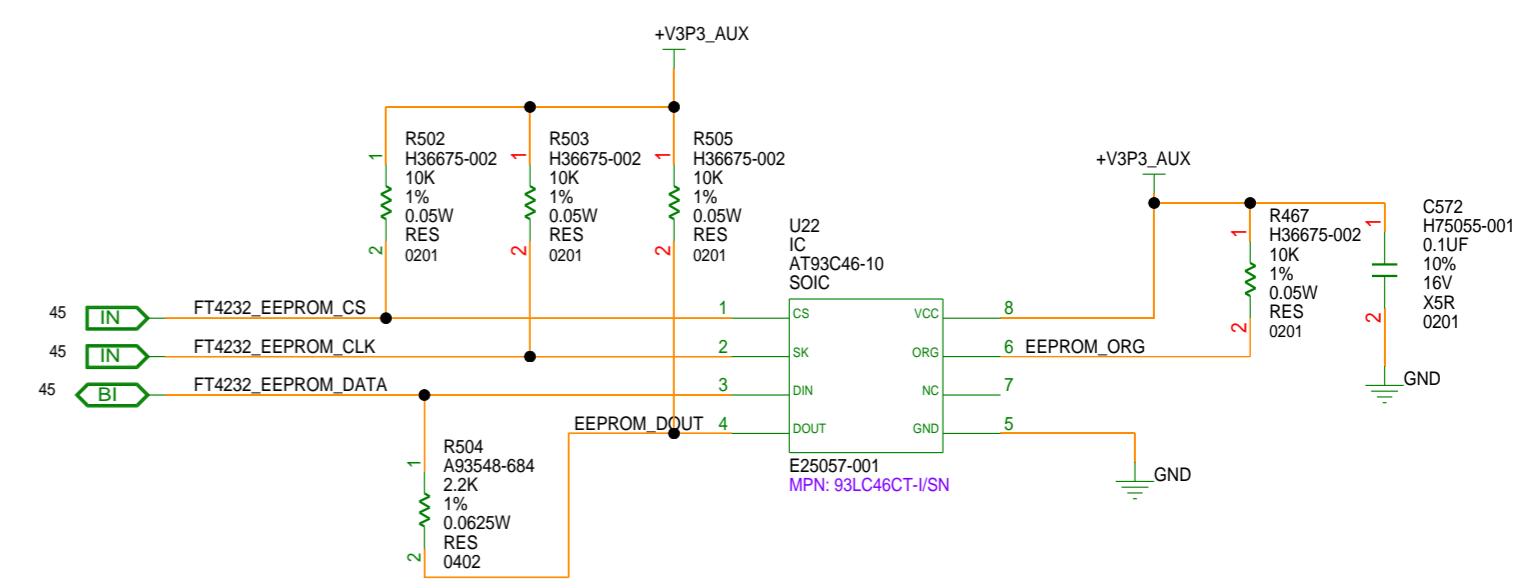
SHEET 43 OF 62

Mon Oct 14 15:09:50 2024

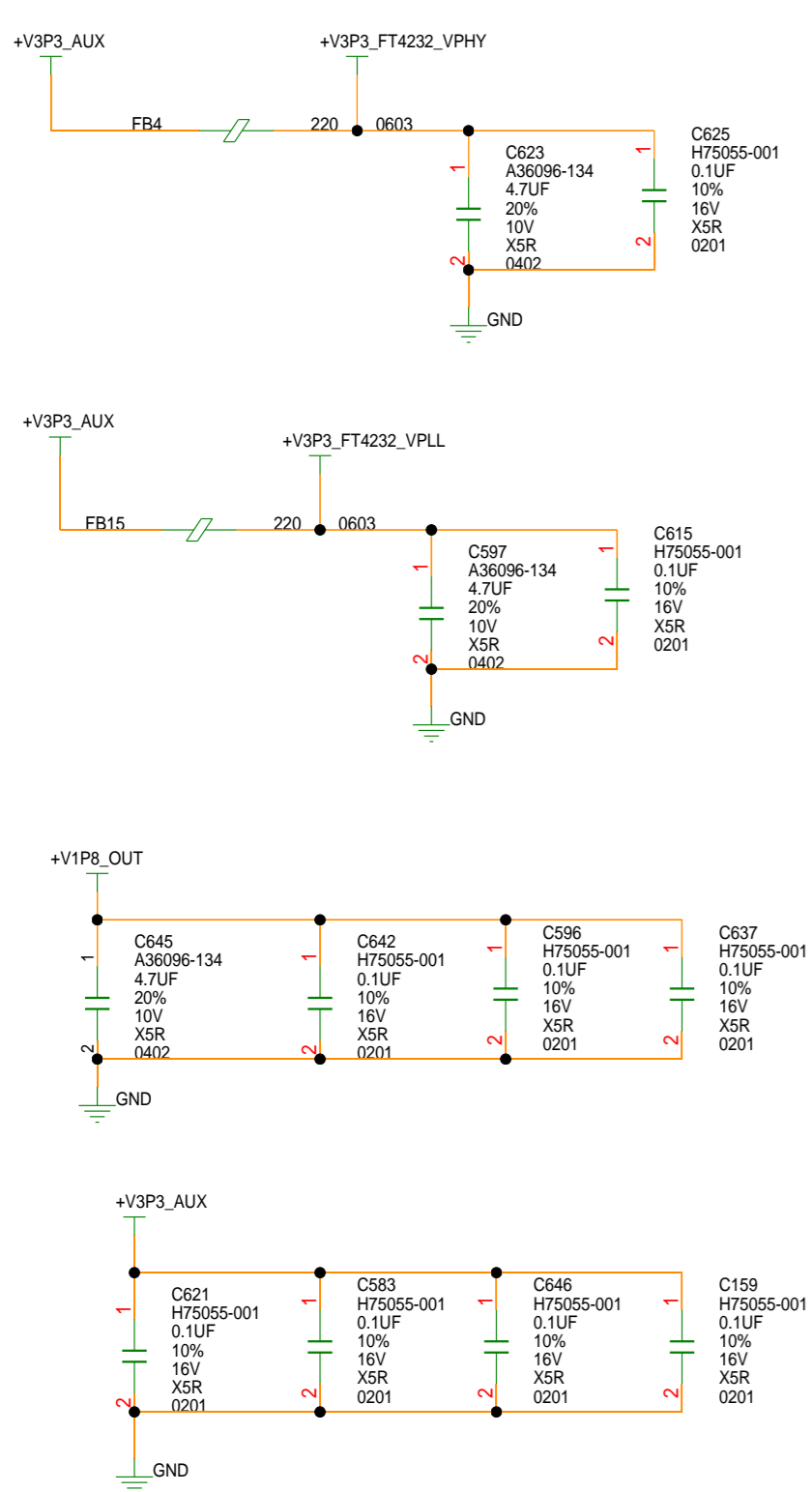
LEVEL SHIFTER



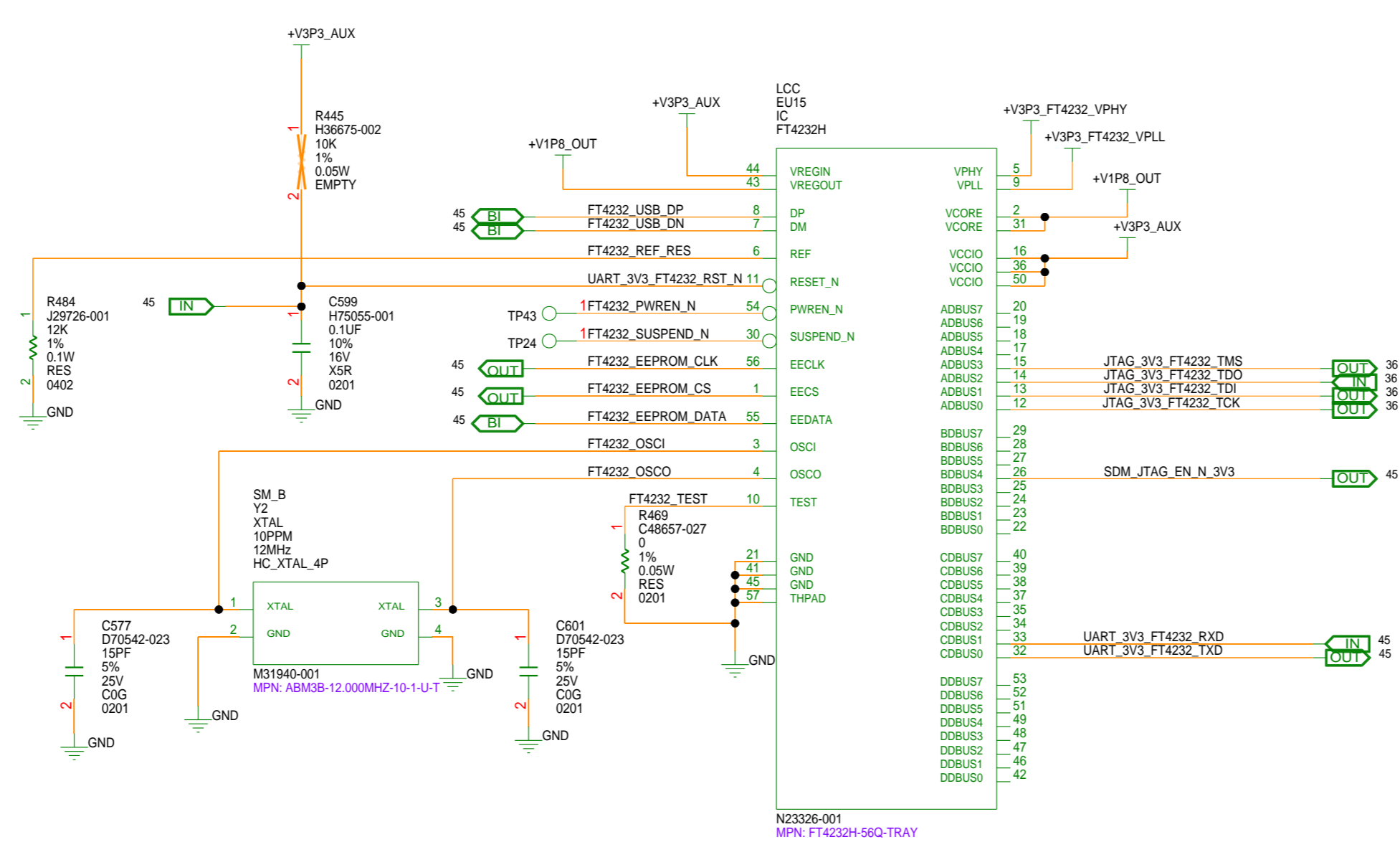
1Kbit EEPROM



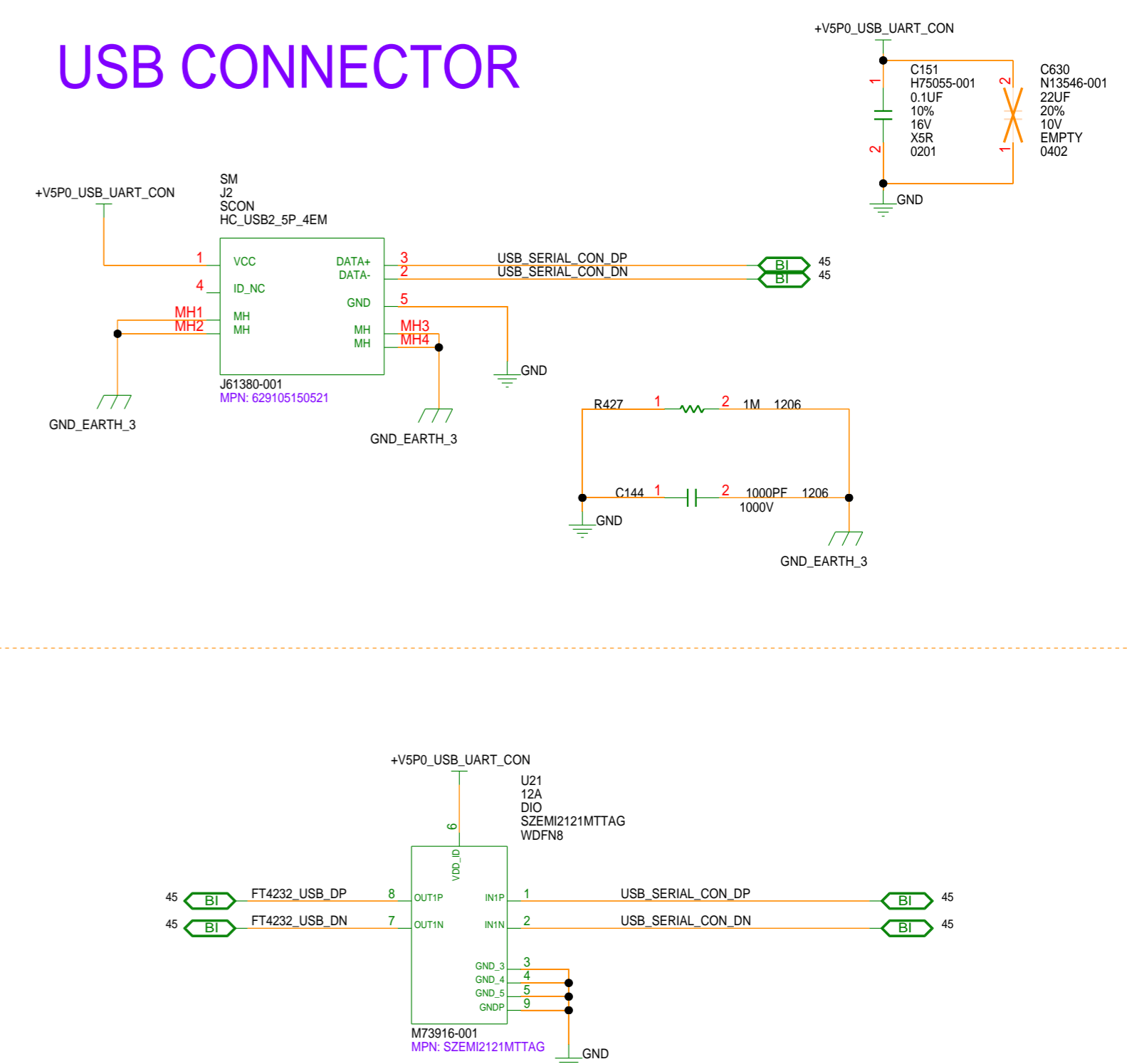
DECAPS



FT4232H



USB CONNECTOR

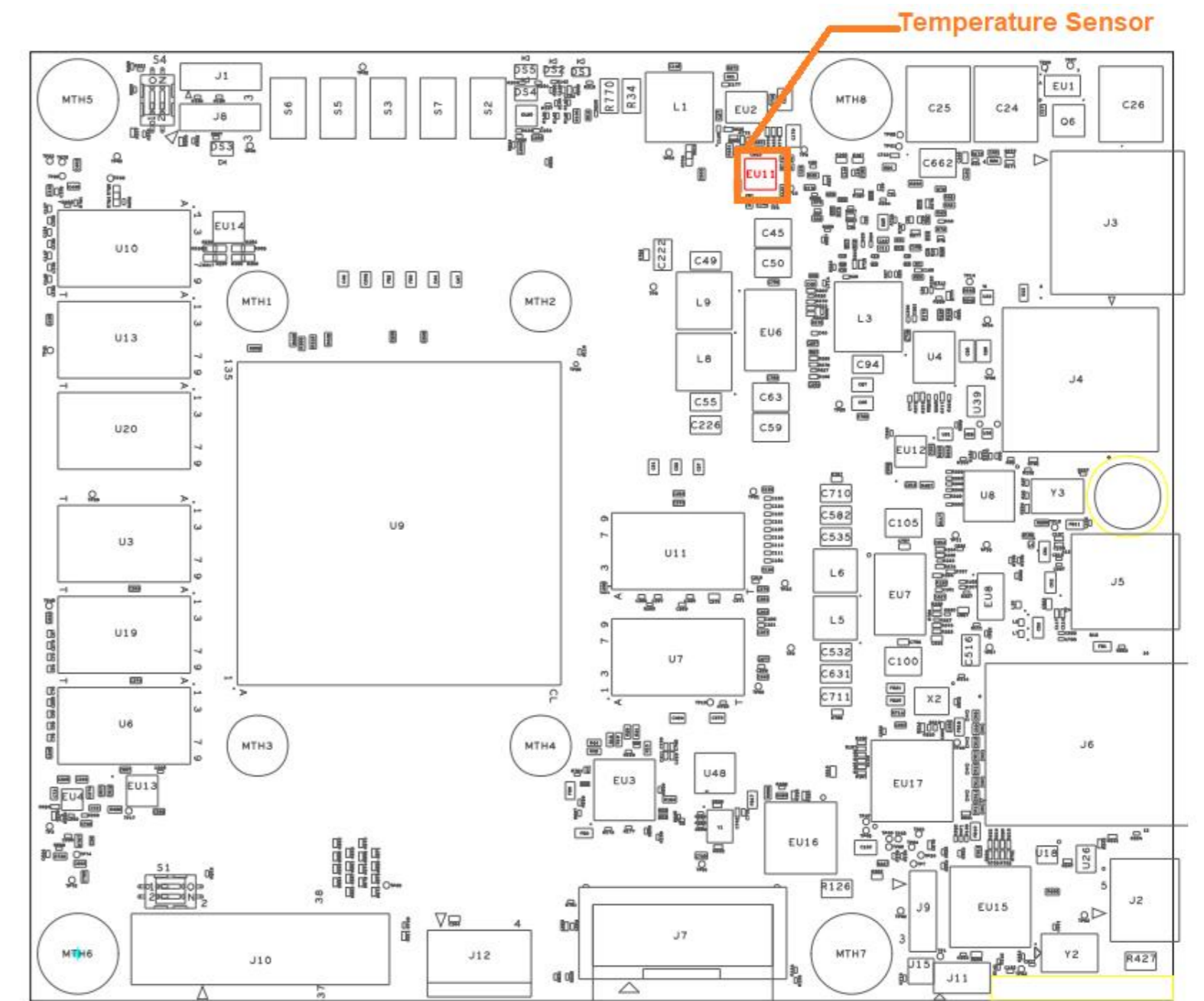
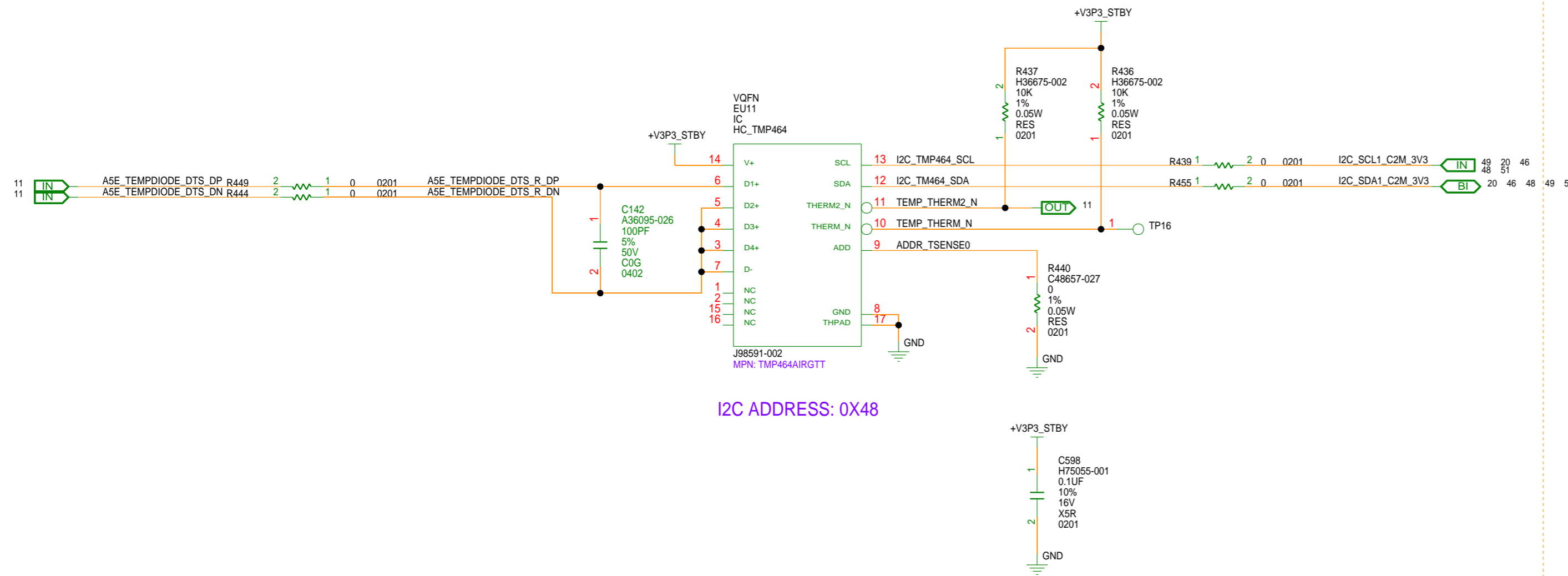


USB - JTAG/UART CONVERTER

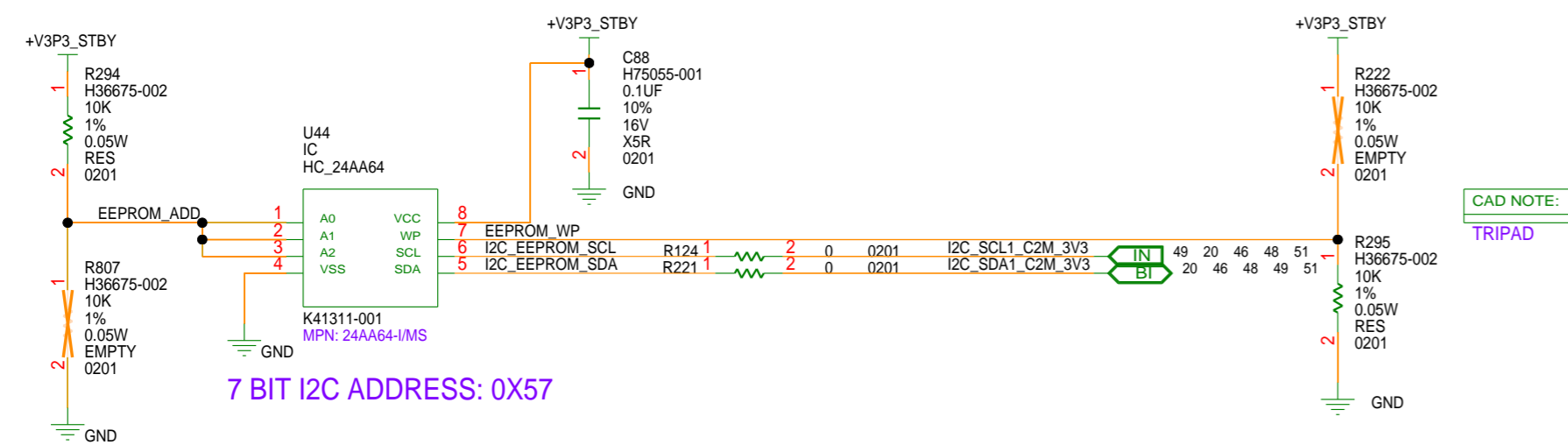
DEPARTMENT	altera An Intel Company	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330723-B1	REV 2.1
SCALE:		DO NOT SCALE DRAWING		SHEET 44 OF 62	

Mon Oct 14 15:09:54 2024

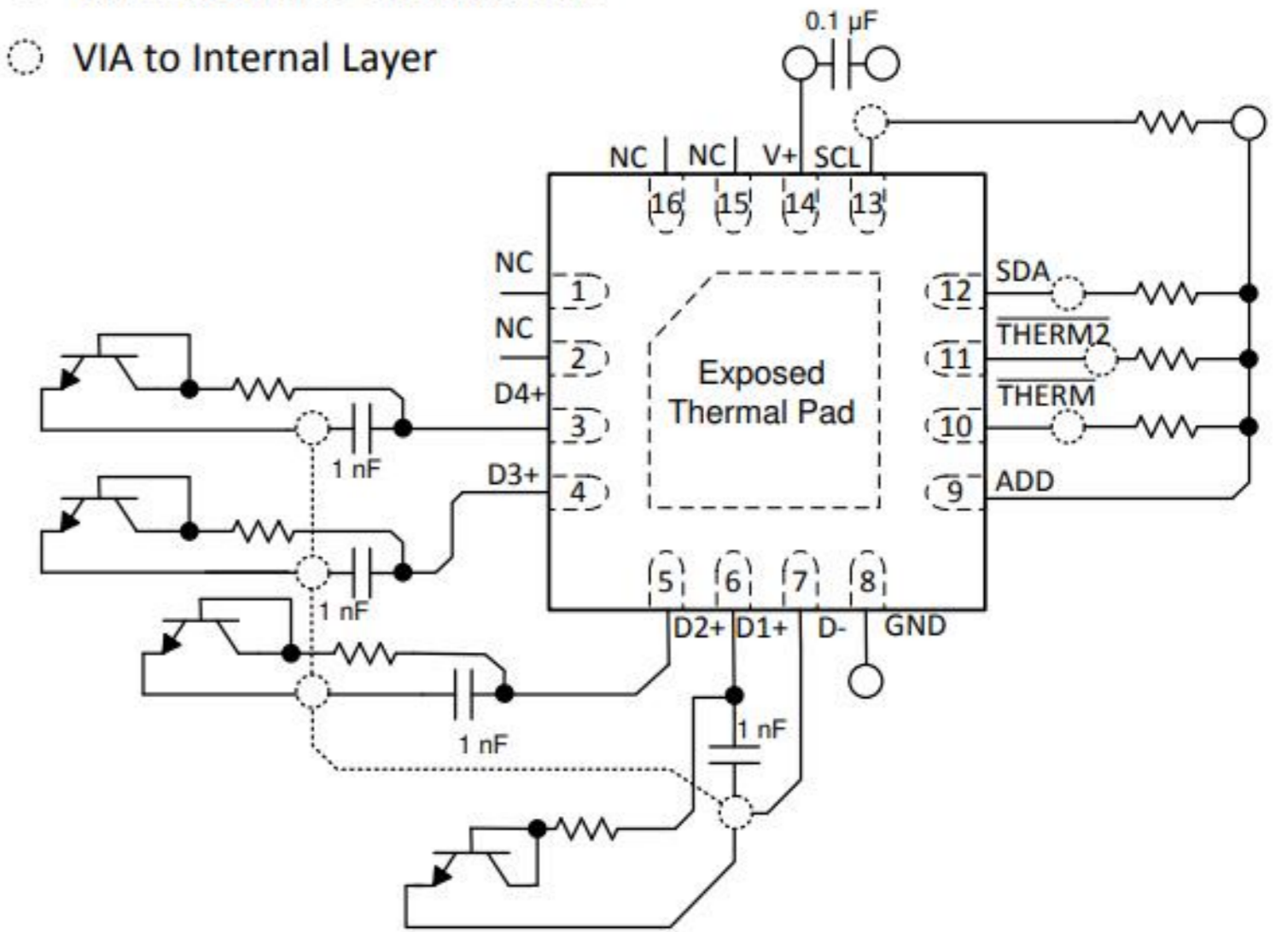
TEMPERATURE SENSOR



EEPROM



- VIA to Power or Ground Plane
- ⊙ VIA to Internal Layer



TMP464 Layout Example

Mon Oct 14 15:09:56 2024

TEMP_SENSOR & EEPROM

DEPARTMENT



SIZE
C+

CODE
34649

DOCUMENT NUMBER
150-0330723-B1

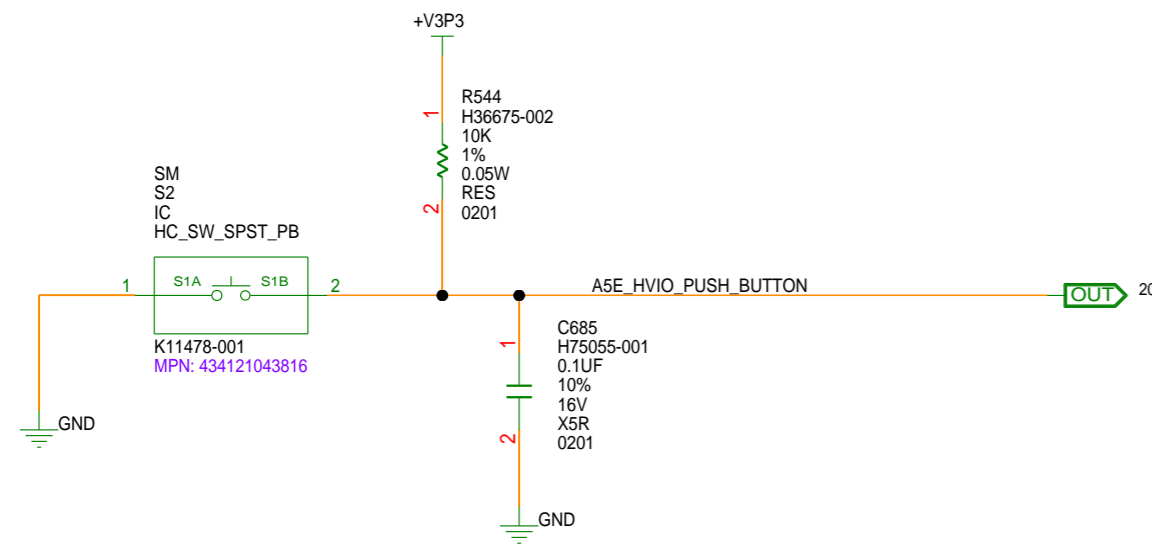
REV
2.1

SCALE:

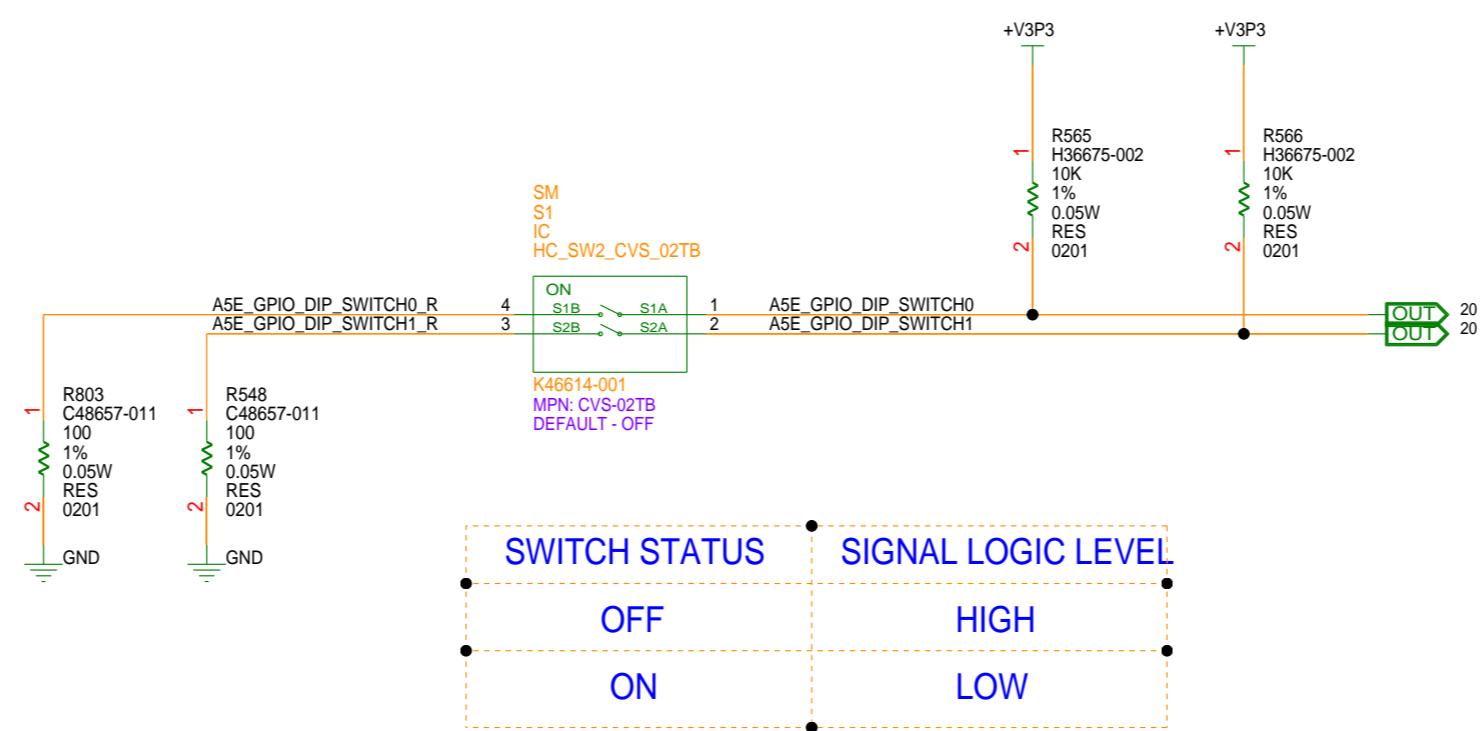
DO NOT SCALE DRAWING

SHEET 45 OF 62

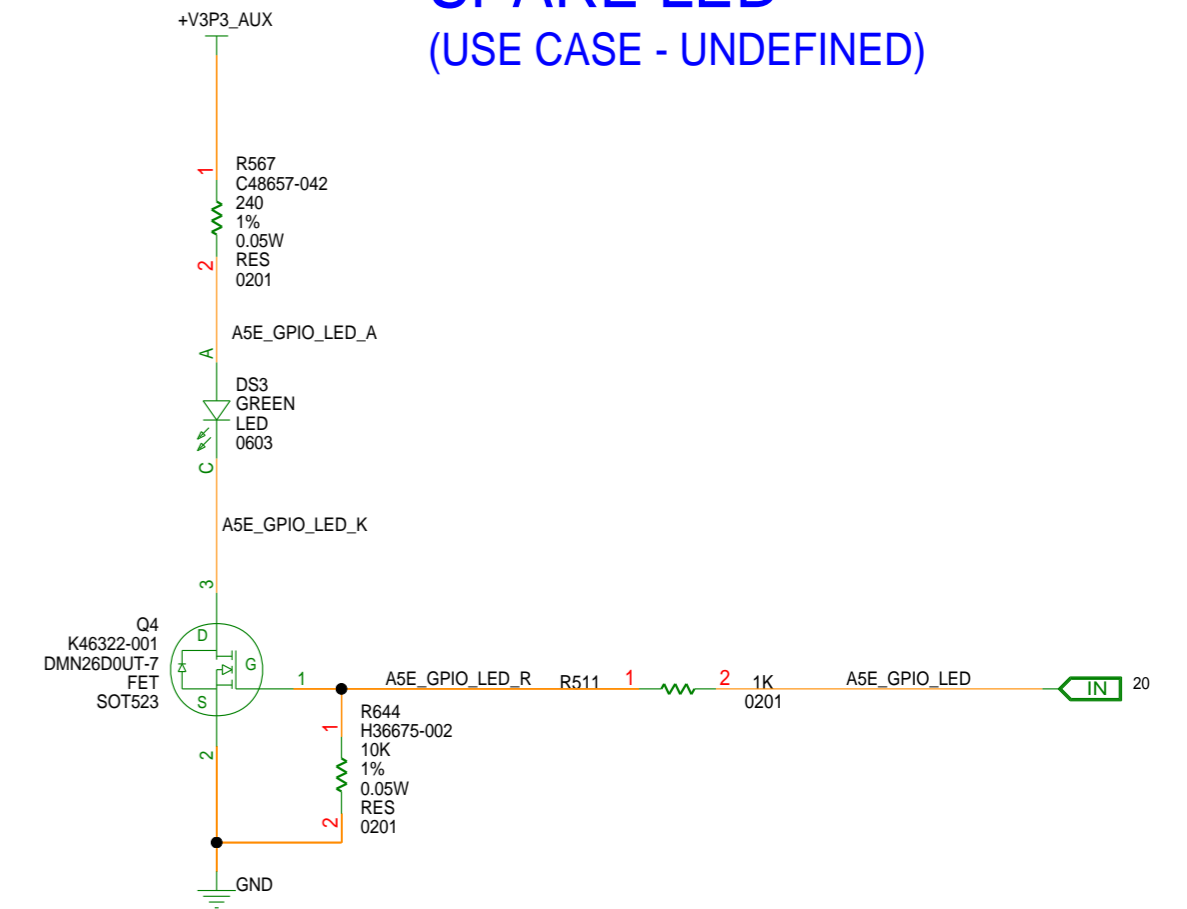
HVIO PUSH BUTTON SWITCH



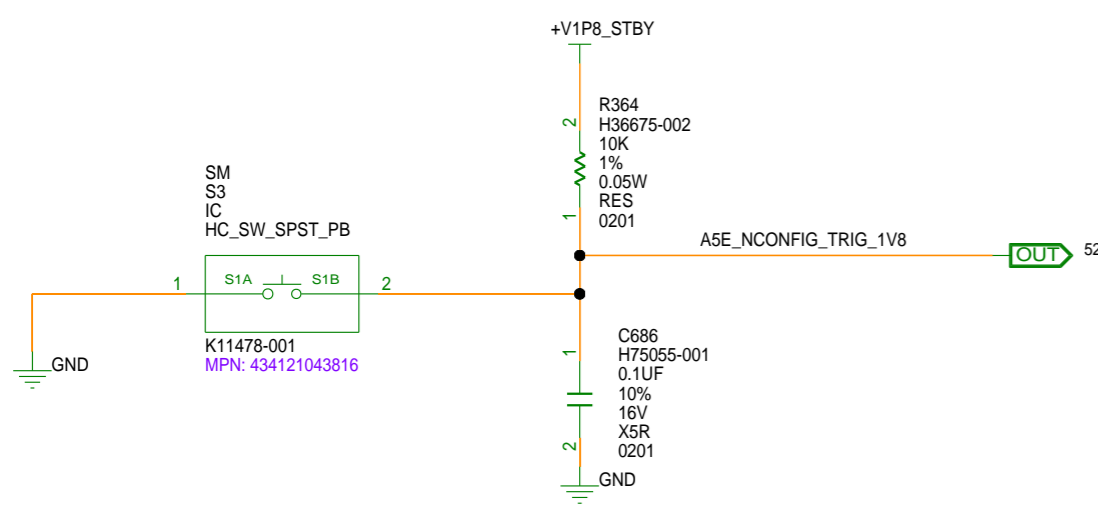
SPARE DIP SWITCH



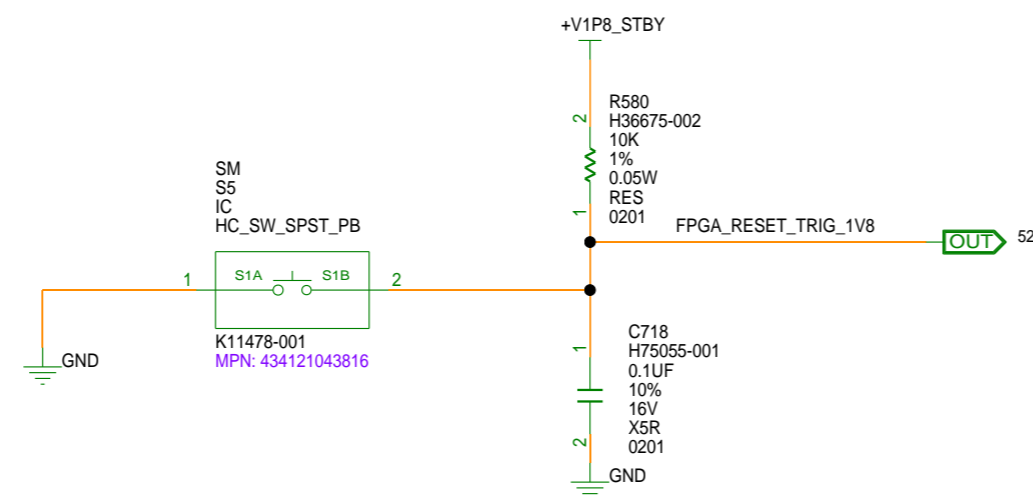
SPARE LED (USE CASE - UNDEFINED)



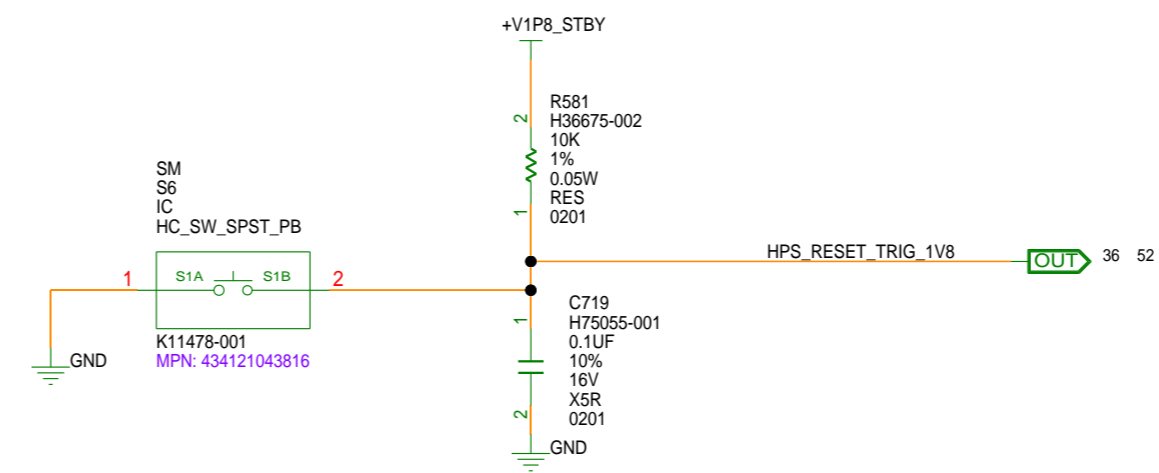
FPGA RESET SWITCH



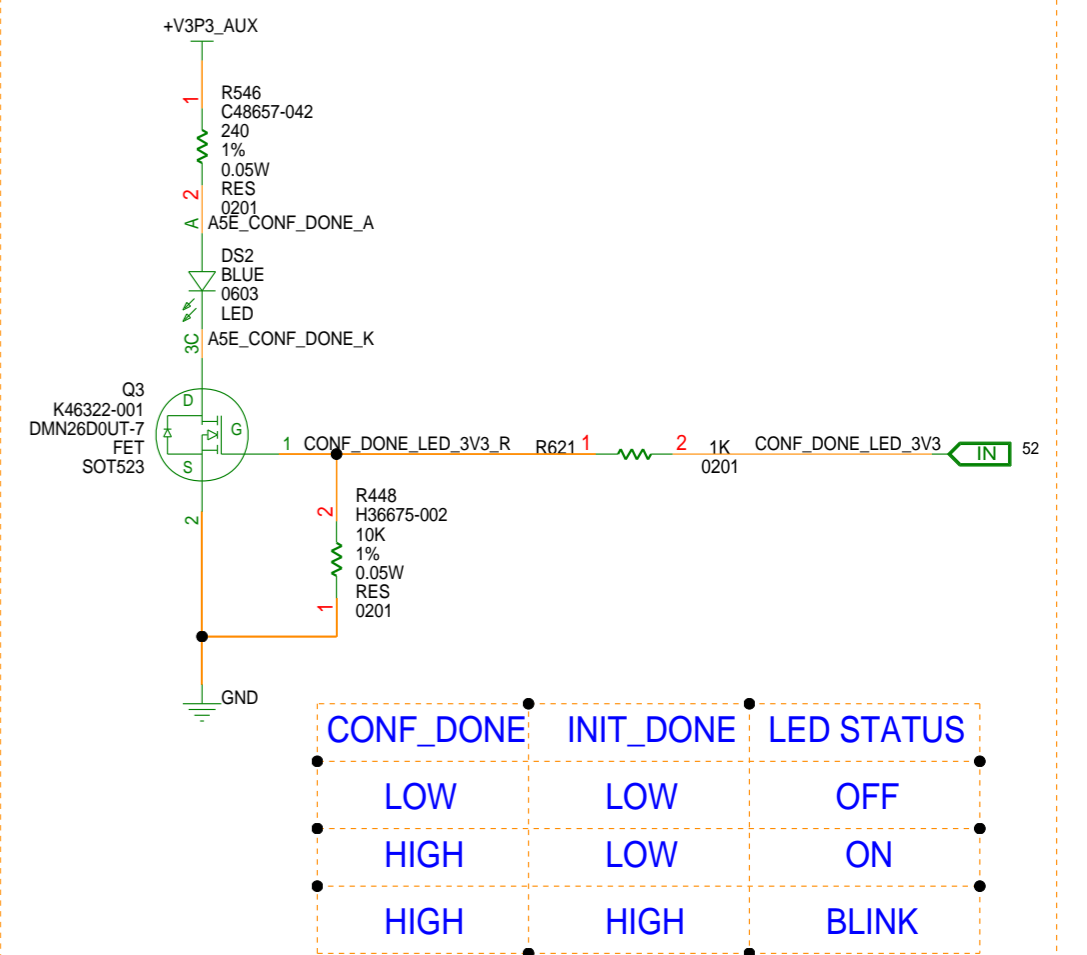
WARM RESET SWITCH



COLD RESET SWITCH



CONFIG DONE LED



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LED AND SWITCH

DEPARTMENT



SIZE

CODE

DOCUMENT NUMBER

REV

C+

34649

150-0330723-B1

2.1

SCALE:

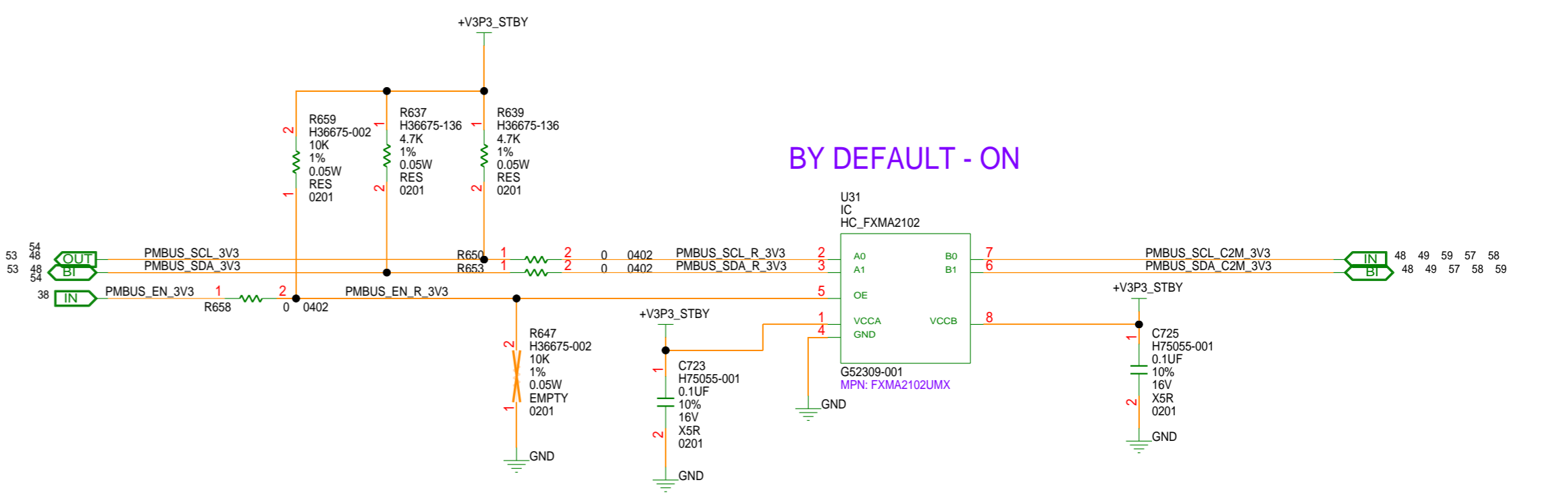
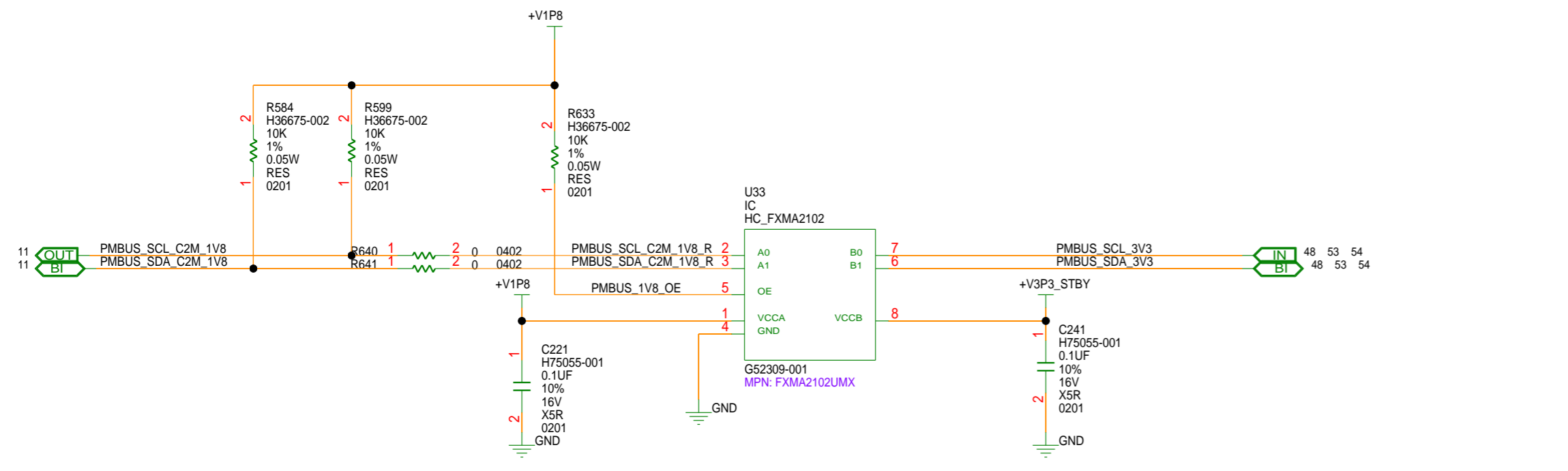
DO NOT SCALE DRAWING

SHEET 46 OF 62

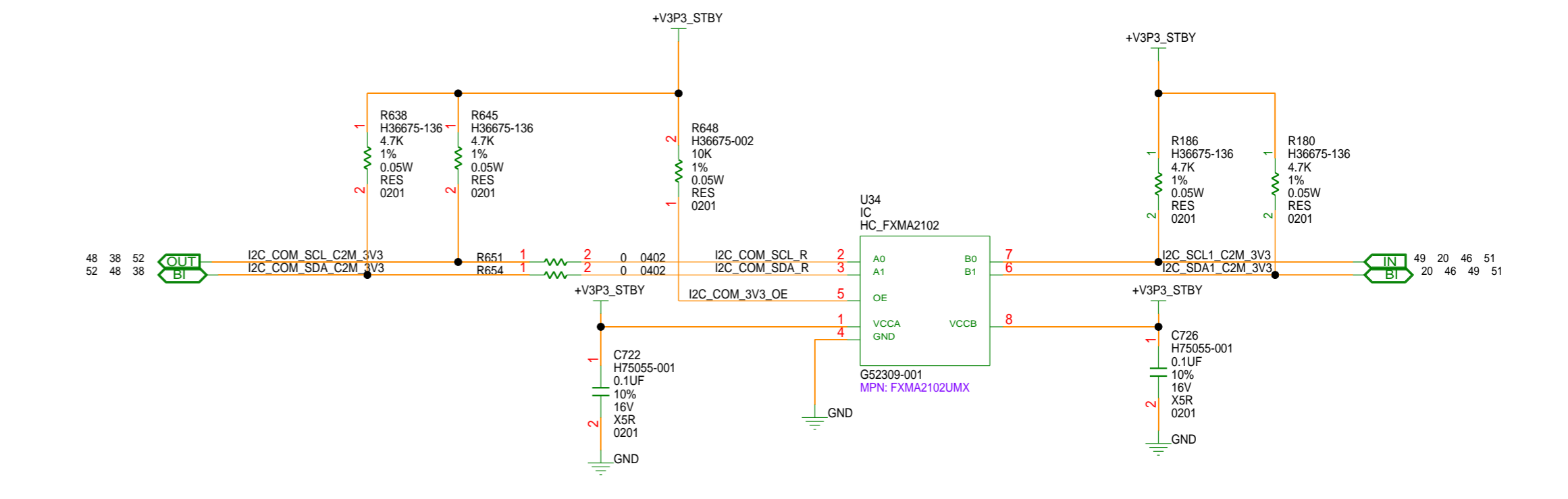
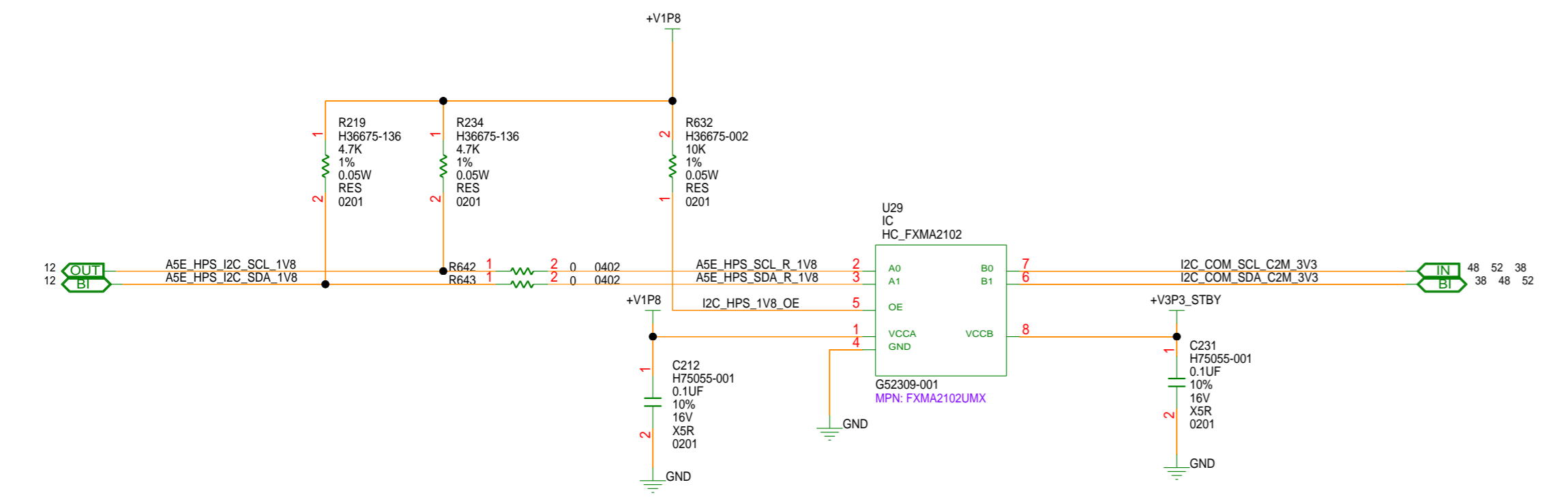
TRUTH TABLE

Control	Outputs
OE	
LOW Logic Level	3-State
HIGH Logic Level	Normal Operation

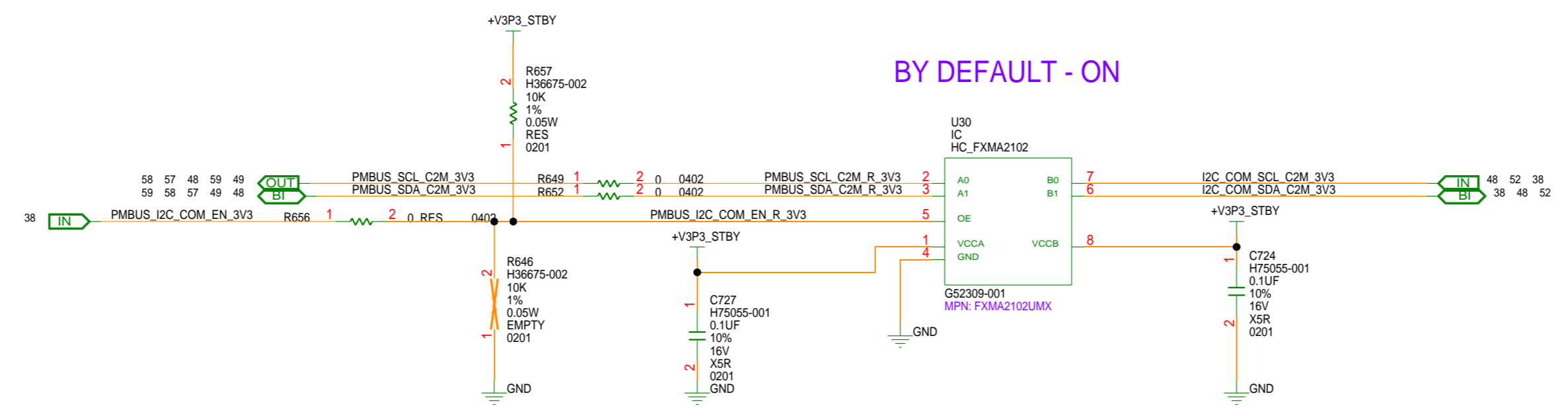
1. If the OE pin is driven LOW, the FXMA2102 is disabled and the A₀, A₁, B₀, and B₁ pins (including dynamic drivers) are forced into 3-state.



BY DEFAULT - ON



BY DEFAULT - ON



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I2C ISOLATOR

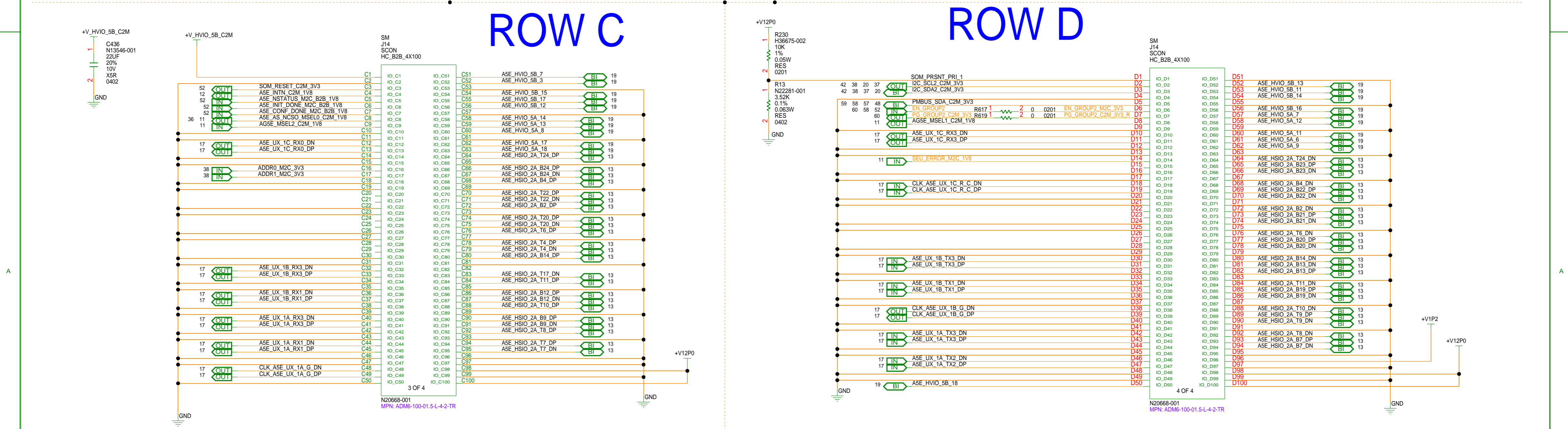
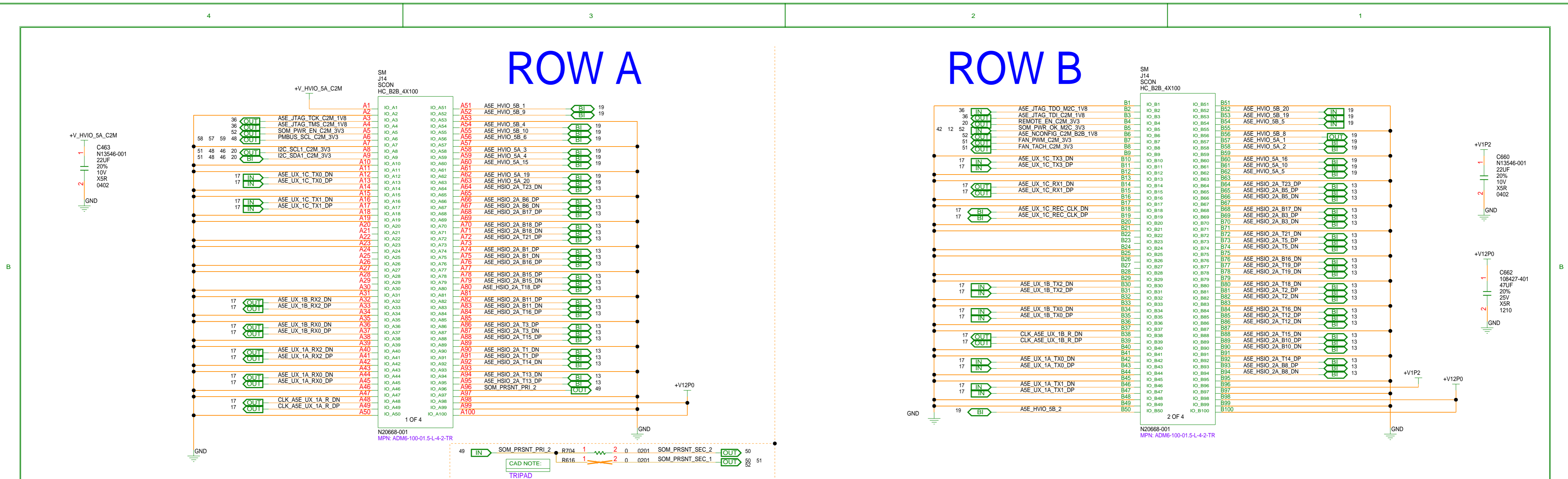
DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:	DO NOT SCALE DRAWING			SHEET	47 OF 62

ROW A

ROW B

ROW C

ROW D

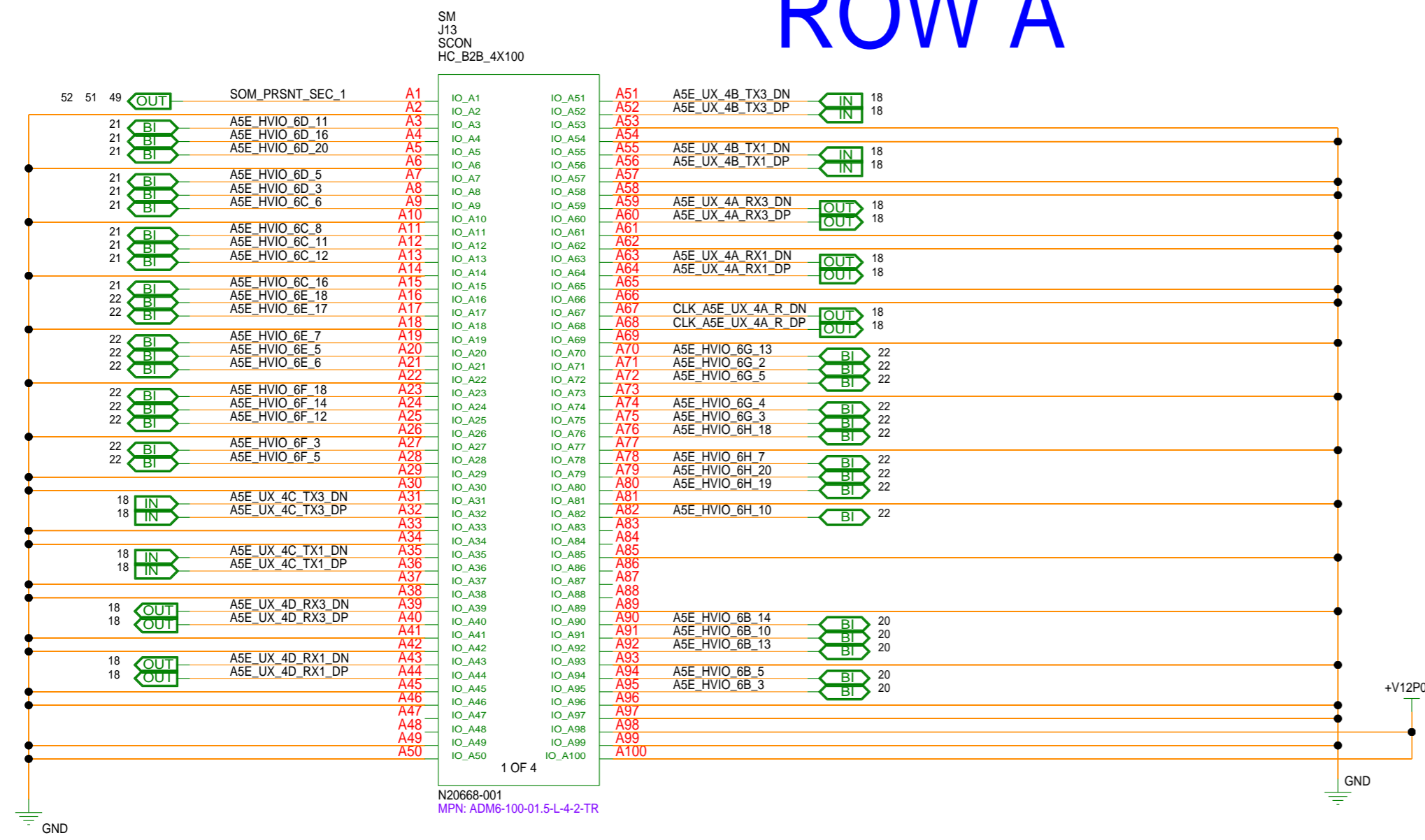


Mon Oct 14 15:10:02 2024

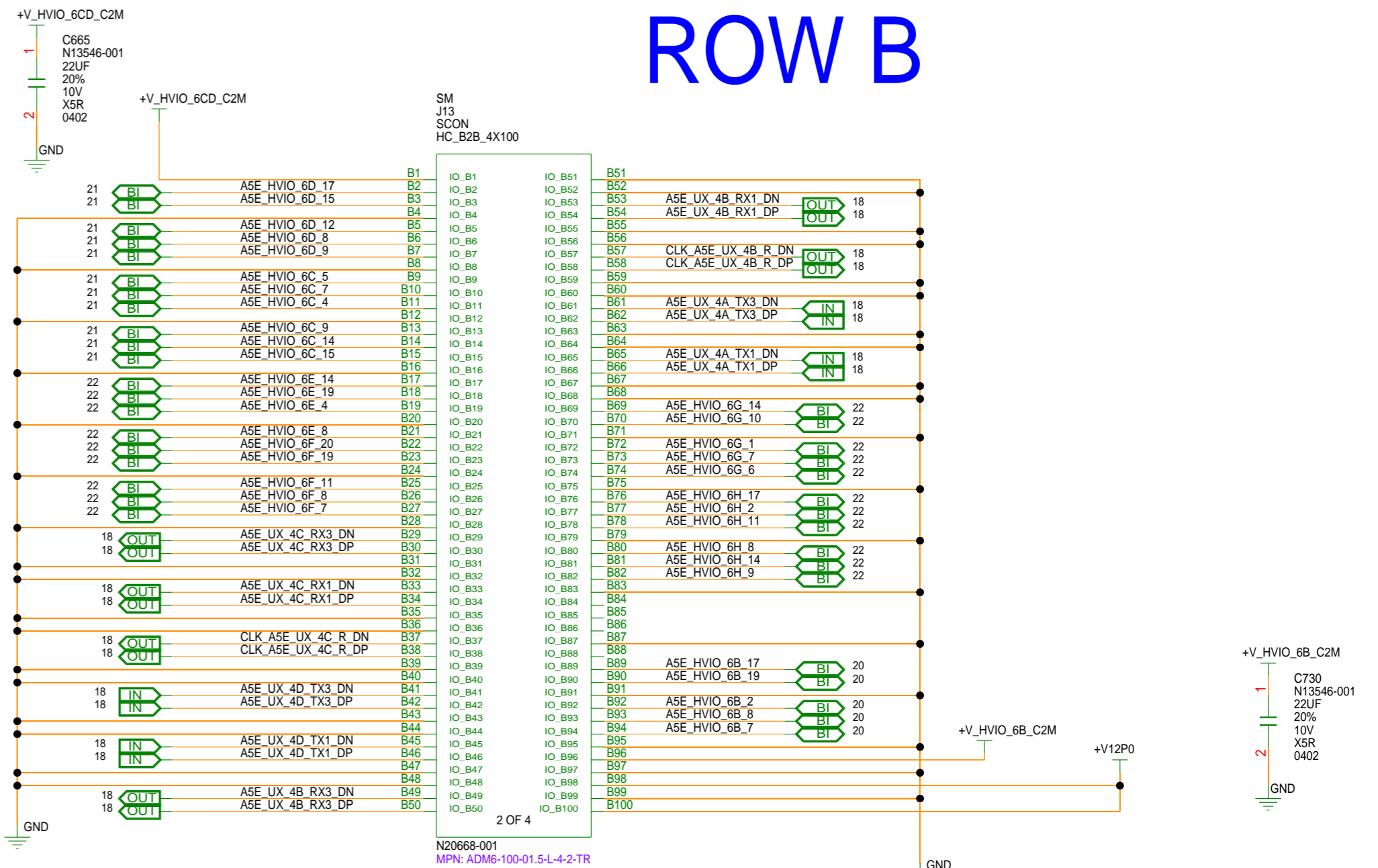
B2B_PRIMARY_CONN

DEPARTMENT	altera An Intel Company	SIZE C+	CODE 34649	DOCUMENT NUMBER 150-0330723-B1	REV 2.1
SCALE:		DO NOT SCALE DRAWING		SHEET 48 OF 62	

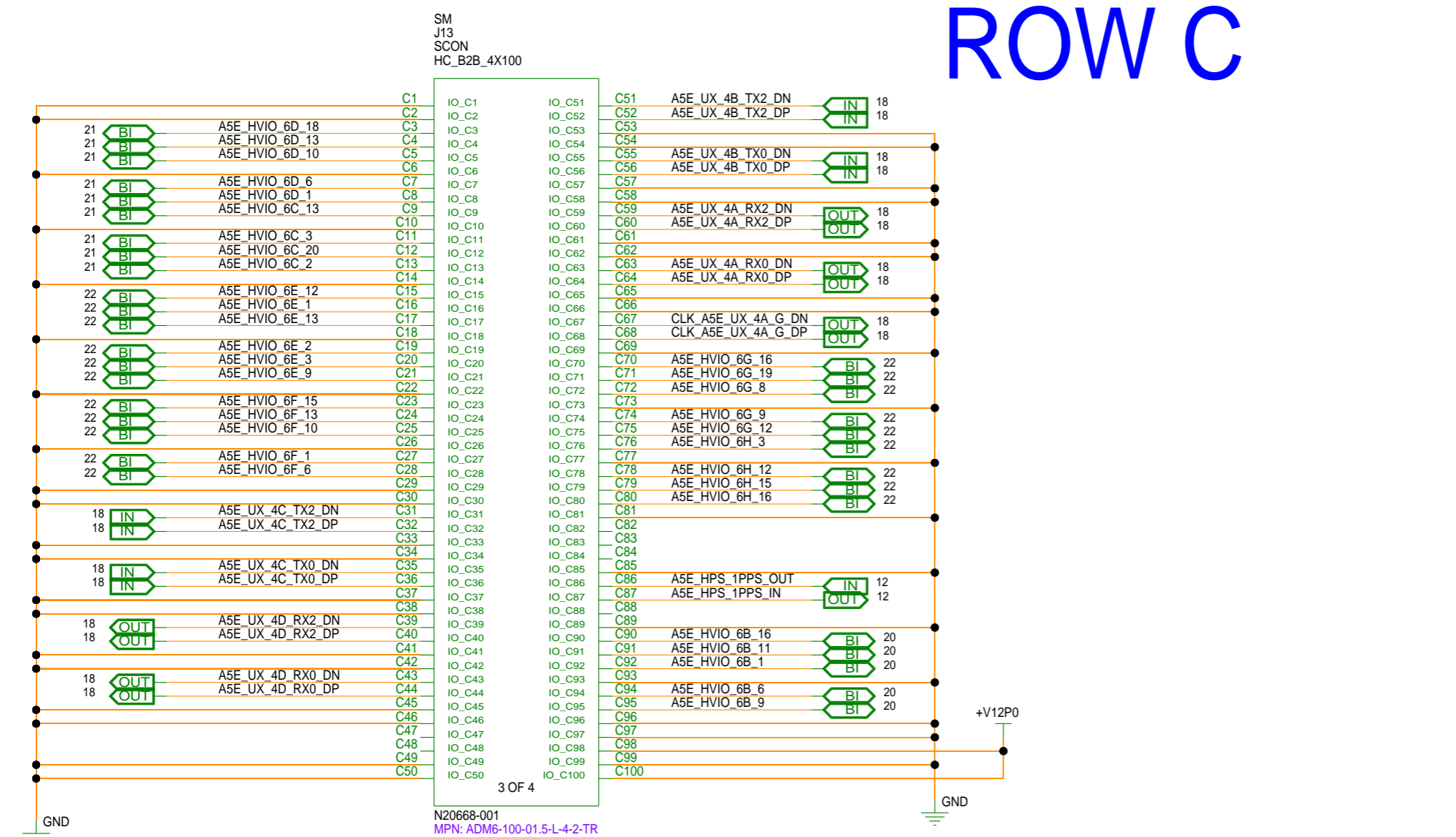
ROW A



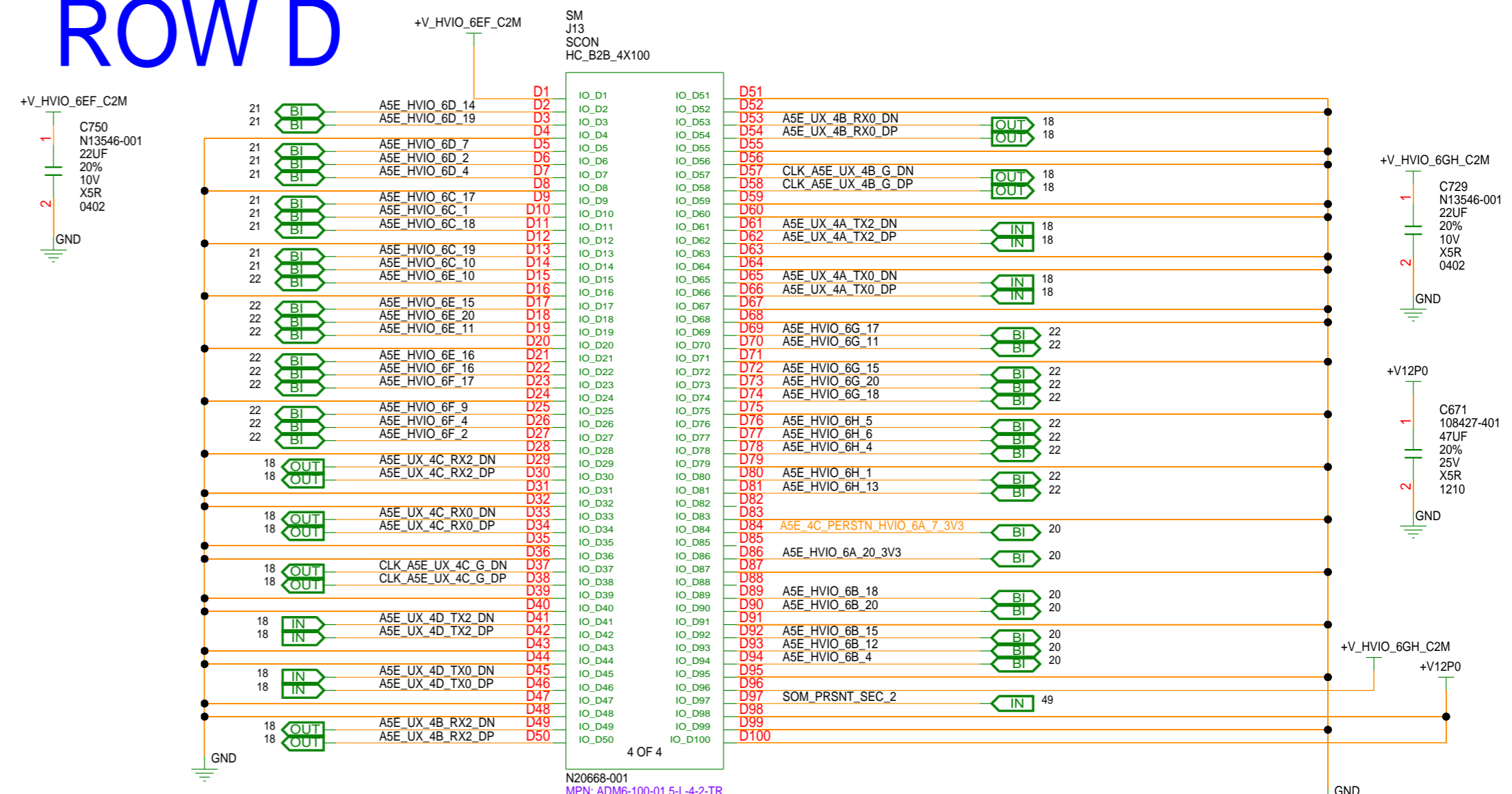
ROW B



ROW C



ROW D



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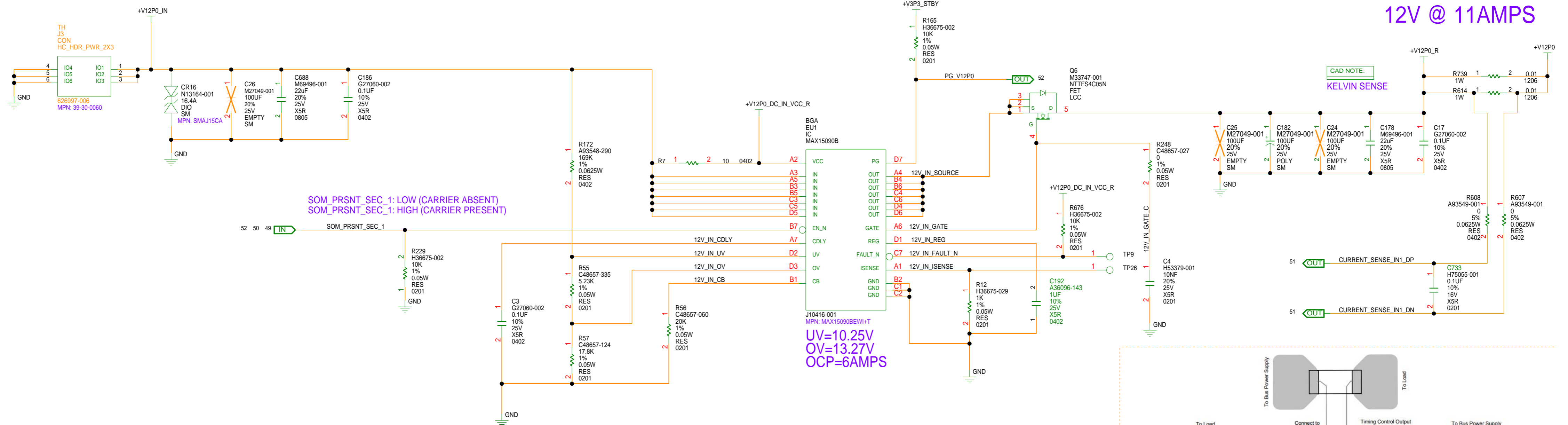
B2B_SECONDARY_CONN

DEPARTMENT

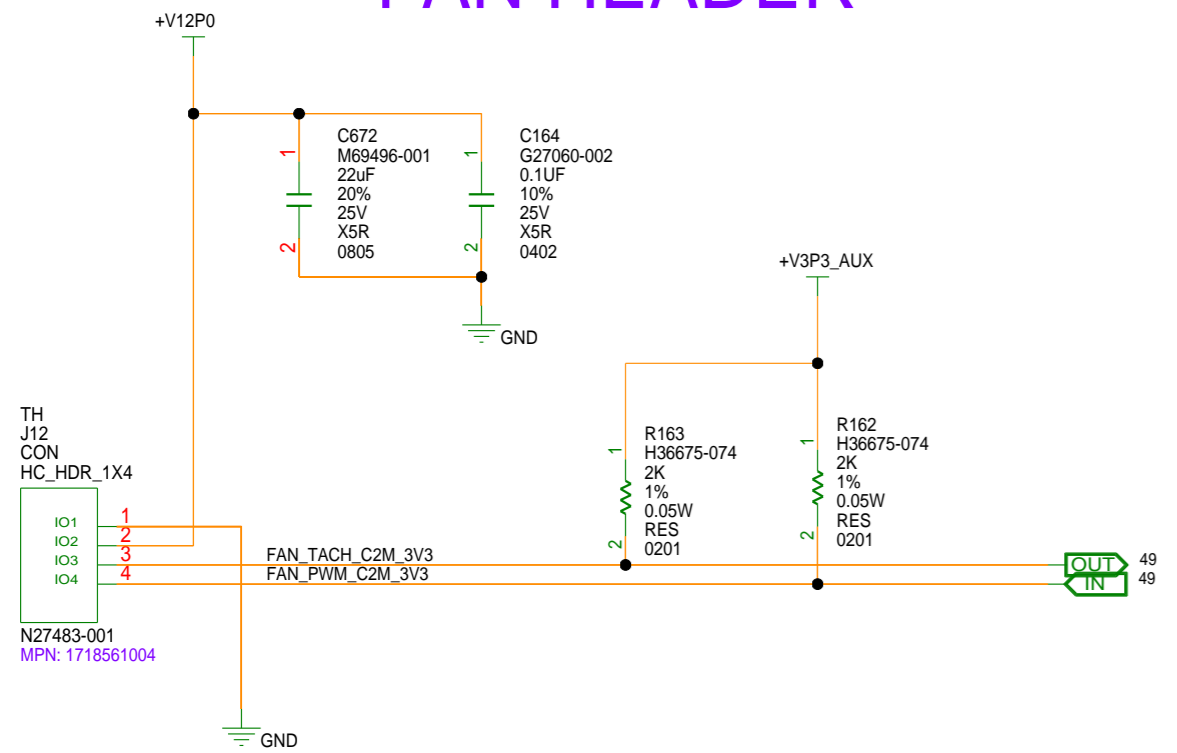


SIZE	CODE	DOCUMENT NUMBER	REV
C+	34649	150-0330723-B1	2.1
SCALE:	DO NOT SCALE DRAWING		SHEET 49 OF 62

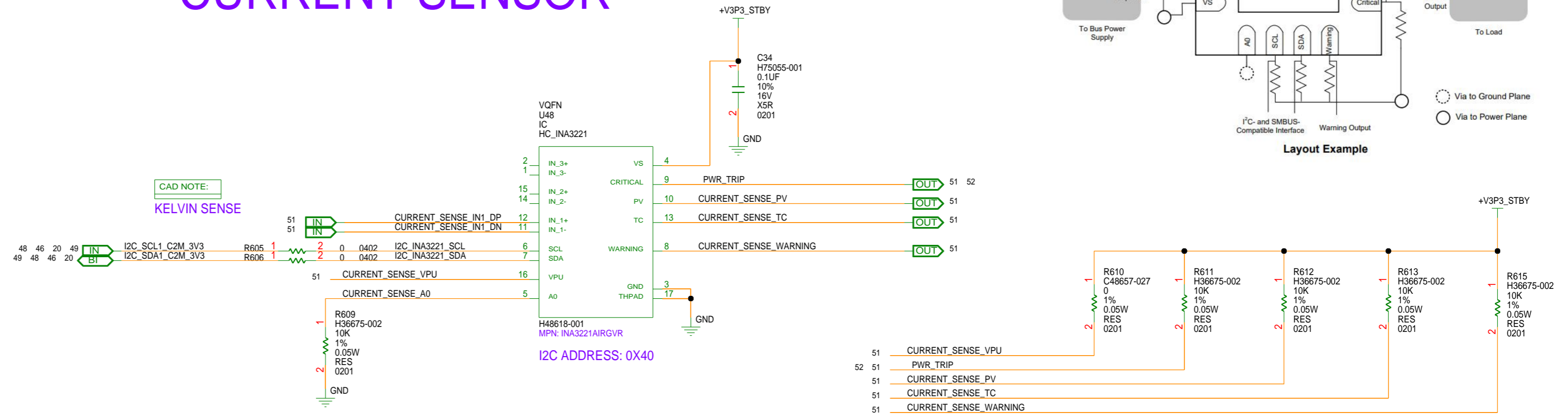
12V ATX CONN



FAN HEADER



CURRENT SENSOR

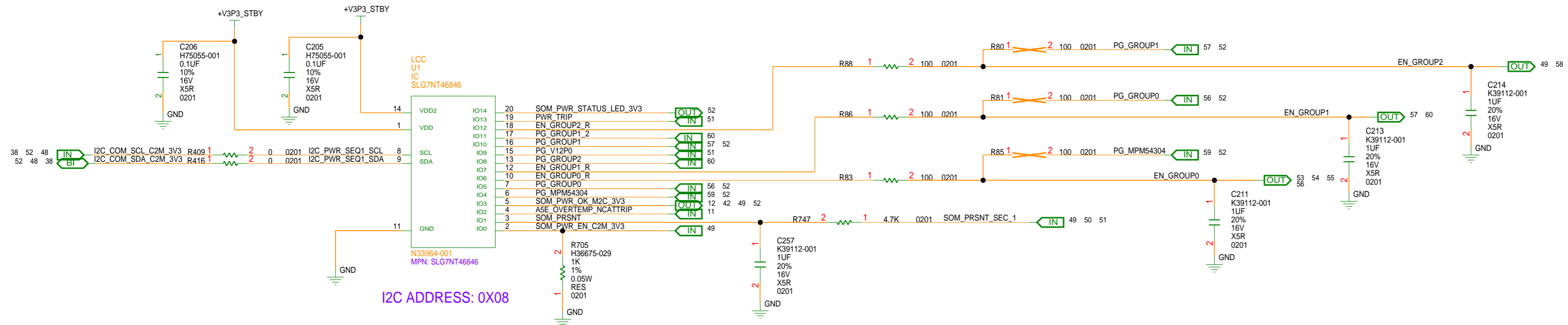


12V_POWER INPUT

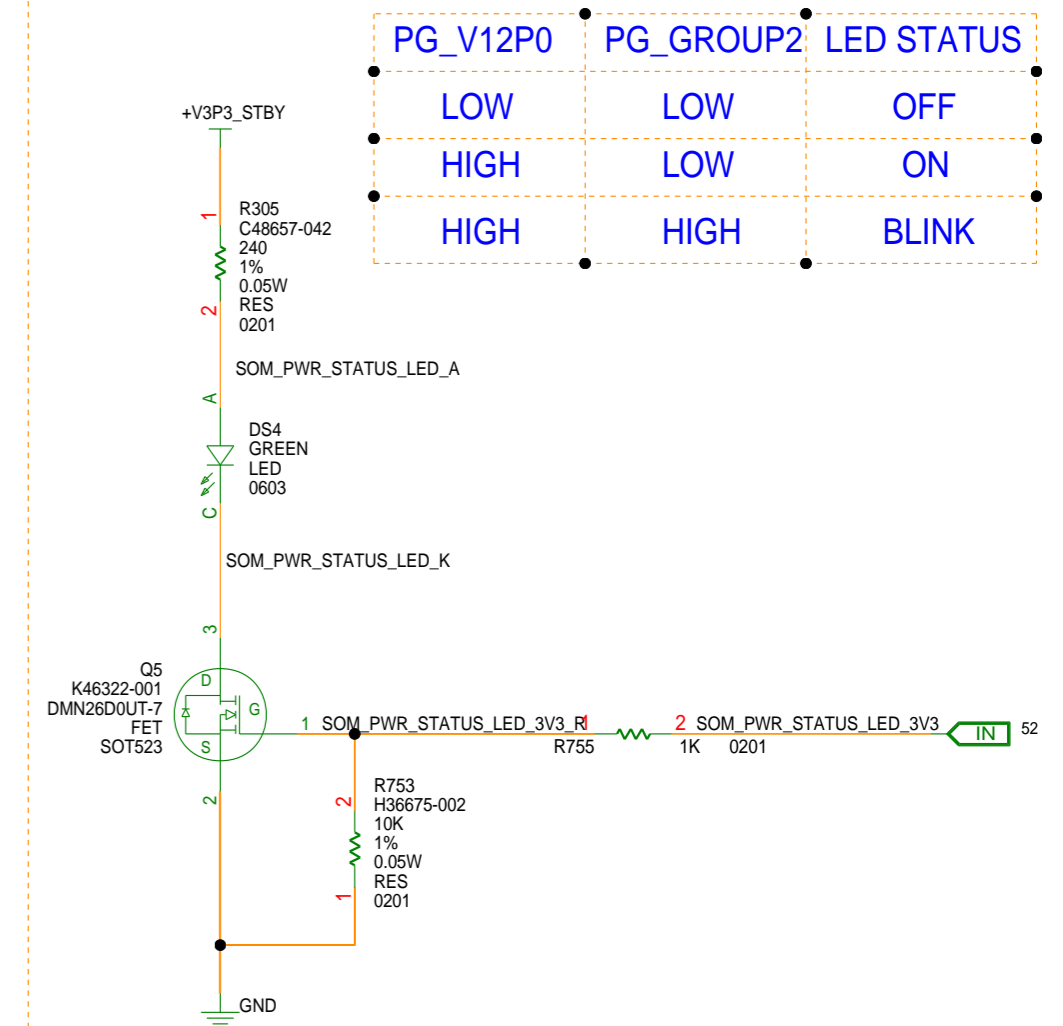
DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 50 OF 62

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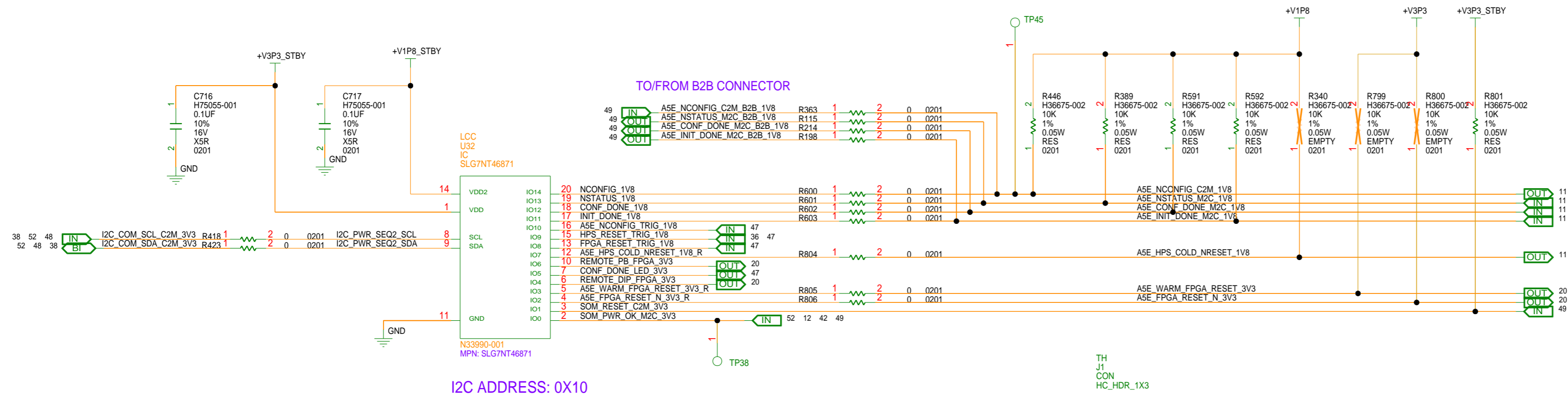
POWER SEQUENCER



POWER STATUS LED

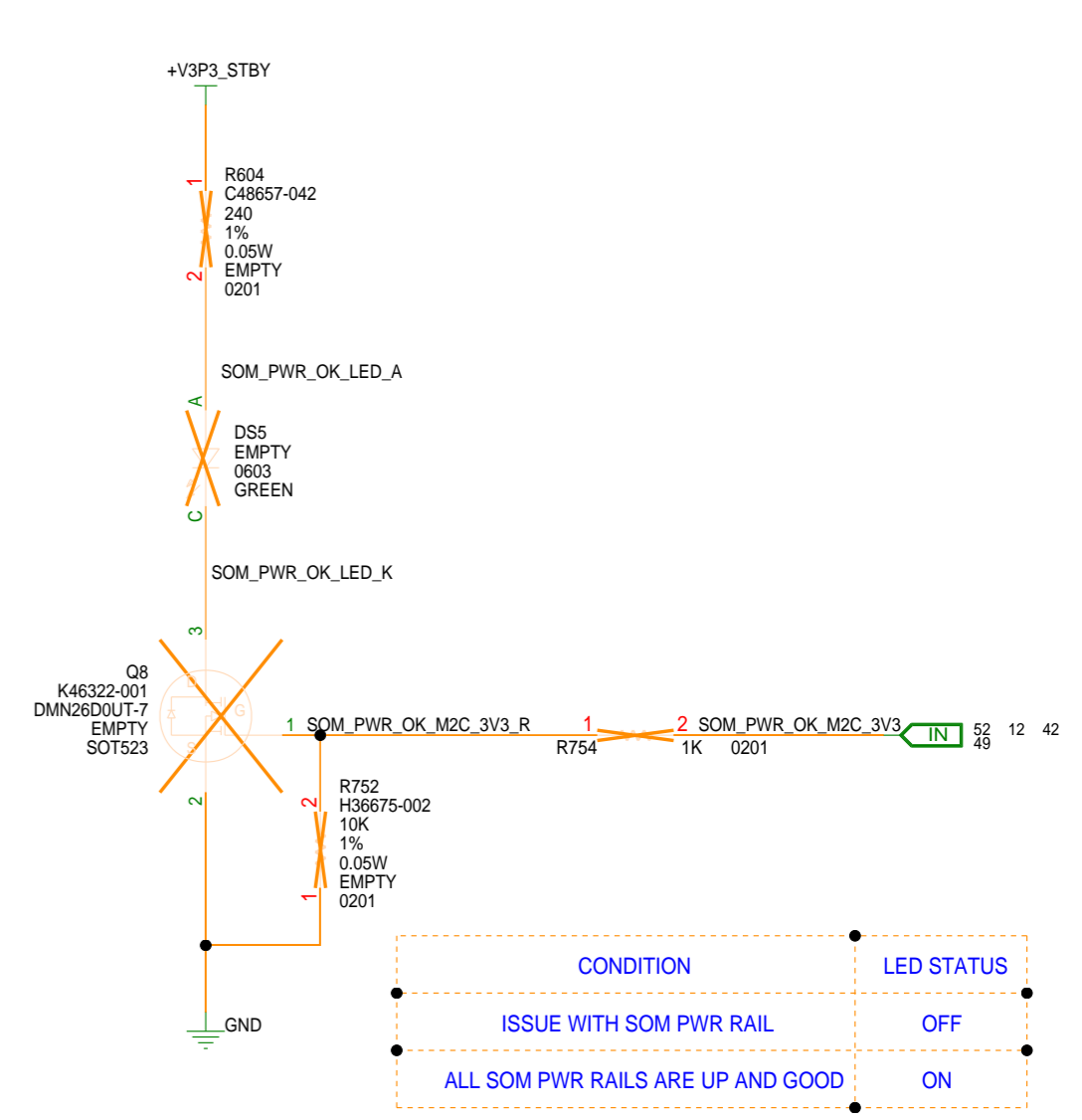


RESET AND CONFIG SEQUENCER



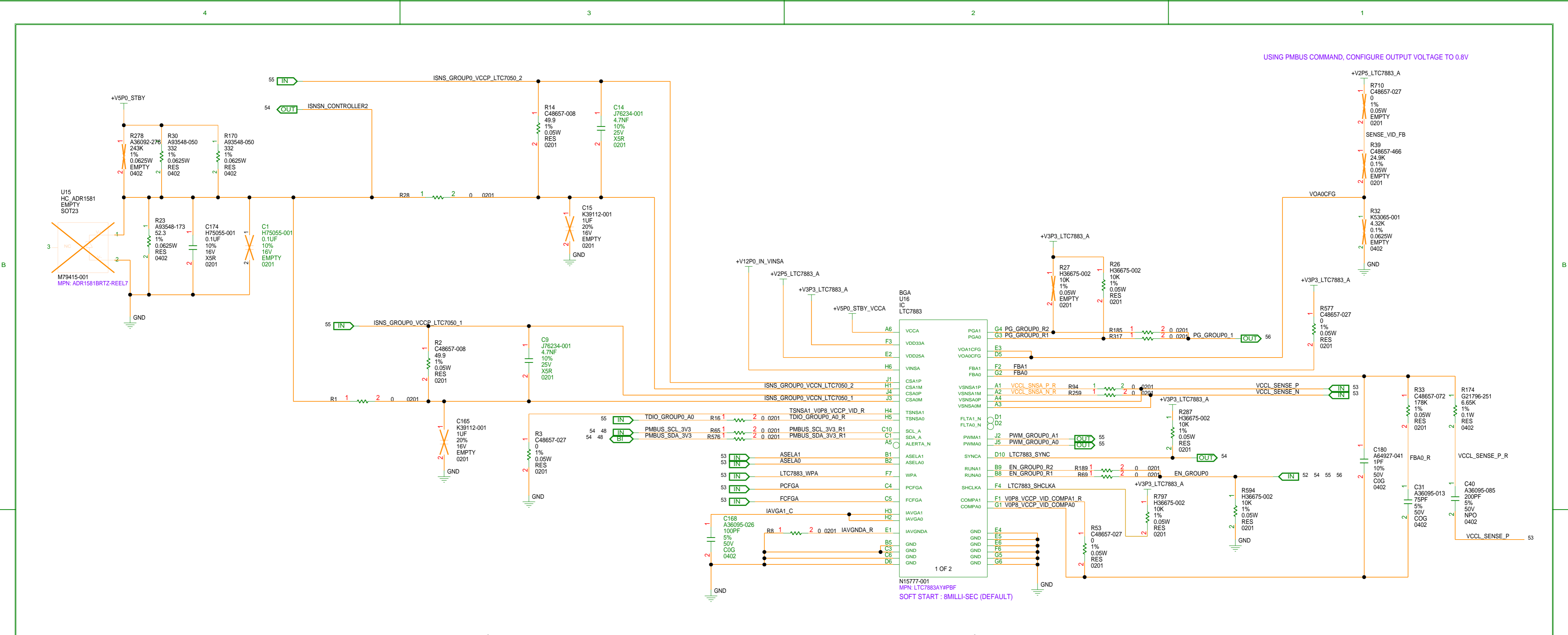
RESET SIGNAL	RESET TRIGGER CONDITION
FPGA FABRIC	WHEN PUSH BUTTON SWITCH "S5" IS PRESSED
HPS WARM	WHEN PUSH BUTTON SWITCH "S6" IS PRESSED FOR <3S
HPS COLD	WHEN PUSH BUTTON SWITCH "S6" IS PRESSED FOR >3S OR/AND WHEN "SOM_RST_C2M" SIGNAL GOES LOW

POWER OK LED

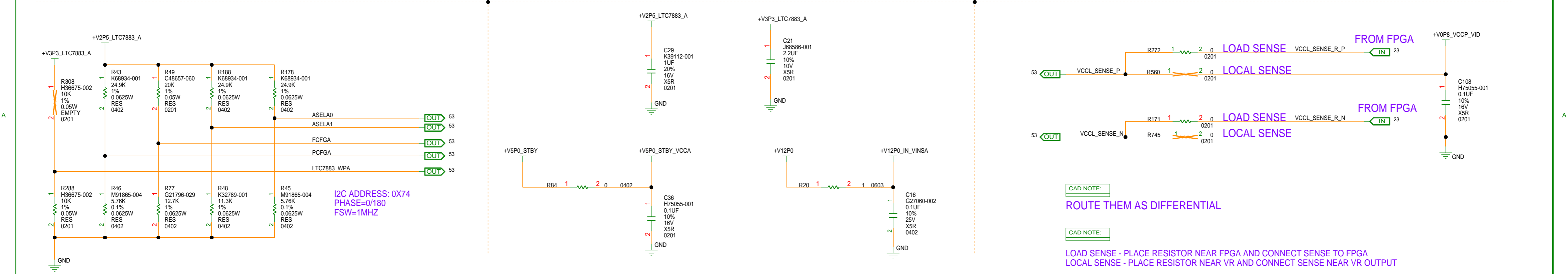


POWER SEQUENCER

Mon Oct 14 15:10:13 2024



USING PMBUS COMMAND, CONFIGURE OUTPUT VOLTAGE TO 0.8V



I2C ADDRESS: 0X74
PHASE=0/180
FSW=1MHZ

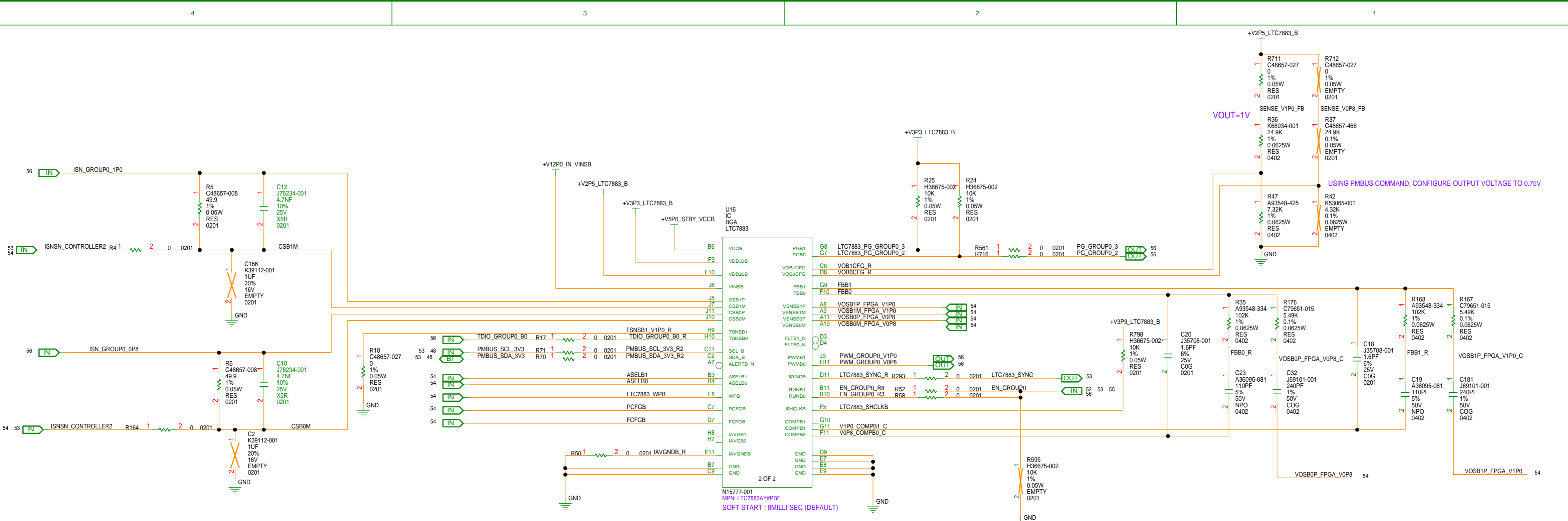
CAD NOTE:
ROUTE THEM AS DIFFERENTIAL

CAD NOTE:
LOAD SENSE - PLACE RESISTOR NEAR FPGA AND CONNECT SENSE TO FPGA
LOCAL SENSE - PLACE RESISTOR NEAR VR AND CONNECT SENSE NEAR VR OUTPUT

Mon Oct 14 15:10:14 2024

POWER-LTC7883-CONTROLLER

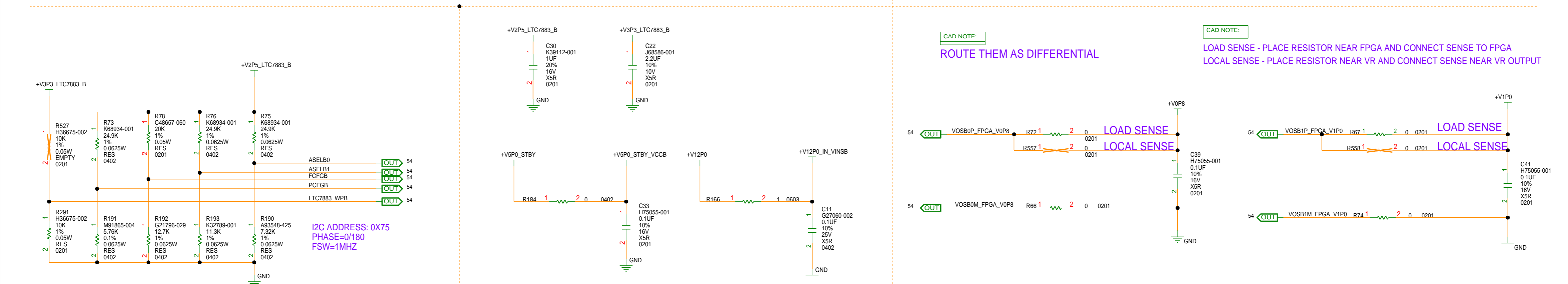
DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 52 OF 62



VO_{UT}=1V

USING PMBUS COMMAND, CONFIGURE OUTPUT VOLTAGE TO 0.75V

2 OF 2
N15777-001
MPN: LTC7883AY#PBF
SOFT START : 8MILLI-SEC (DEFAULT)



I2C ADDRESS: 0X75
PHASE=0/180
FSW=1MHZ

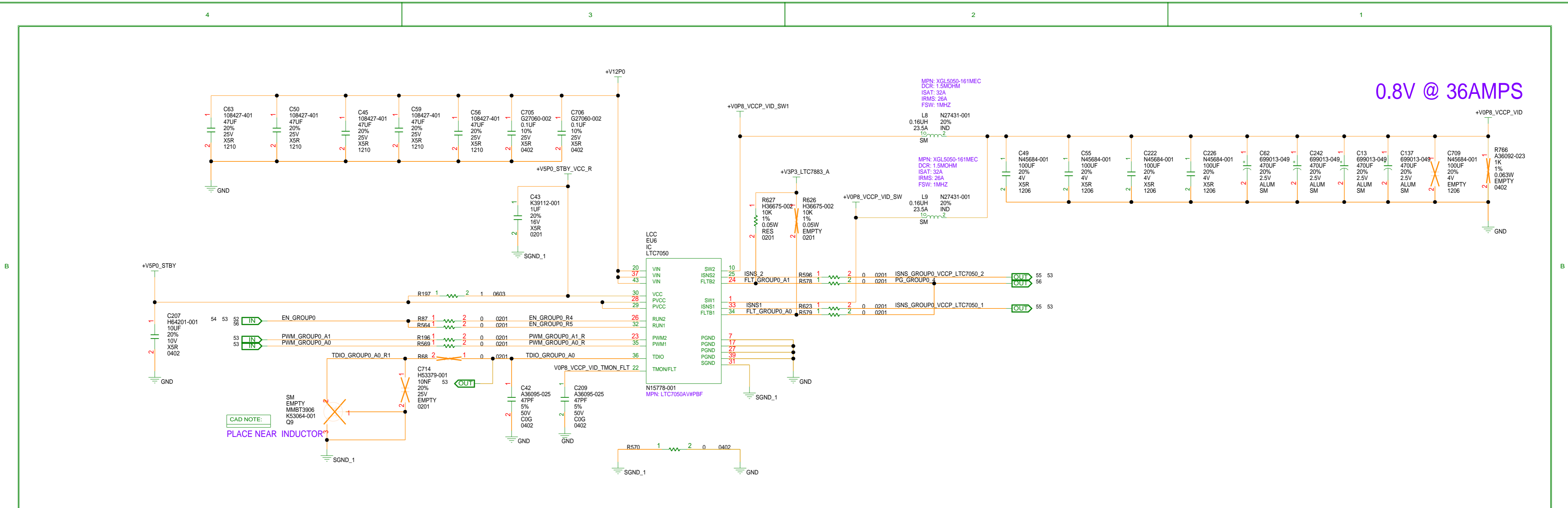
CAD NOTE:
ROUTE THEM AS DIFFERENTIAL

CAD NOTE:
LOAD SENSE - PLACE RESISTOR NEAR FPGA AND CONNECT SENSE TO FPGA
LOCAL SENSE - PLACE RESISTOR NEAR VR AND CONNECT SENSE NEAR VR OUTPUT

POWER-LTC7883-CONTROLLER

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:	DO NOT SCALE DRAWING			SHEET	53 OF 62

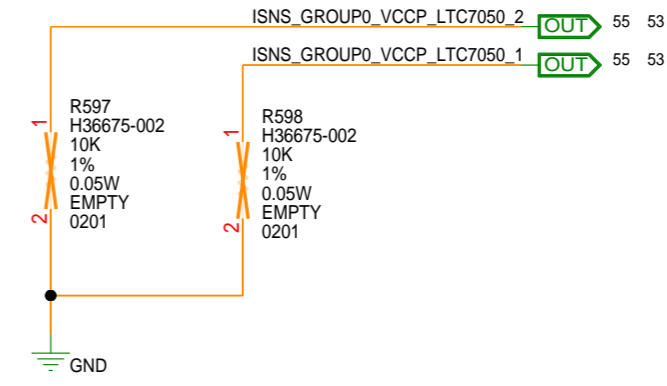
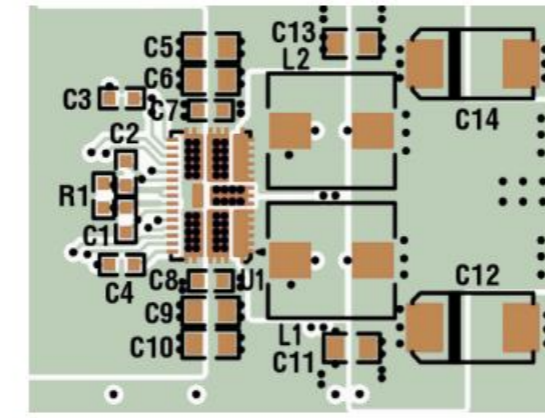
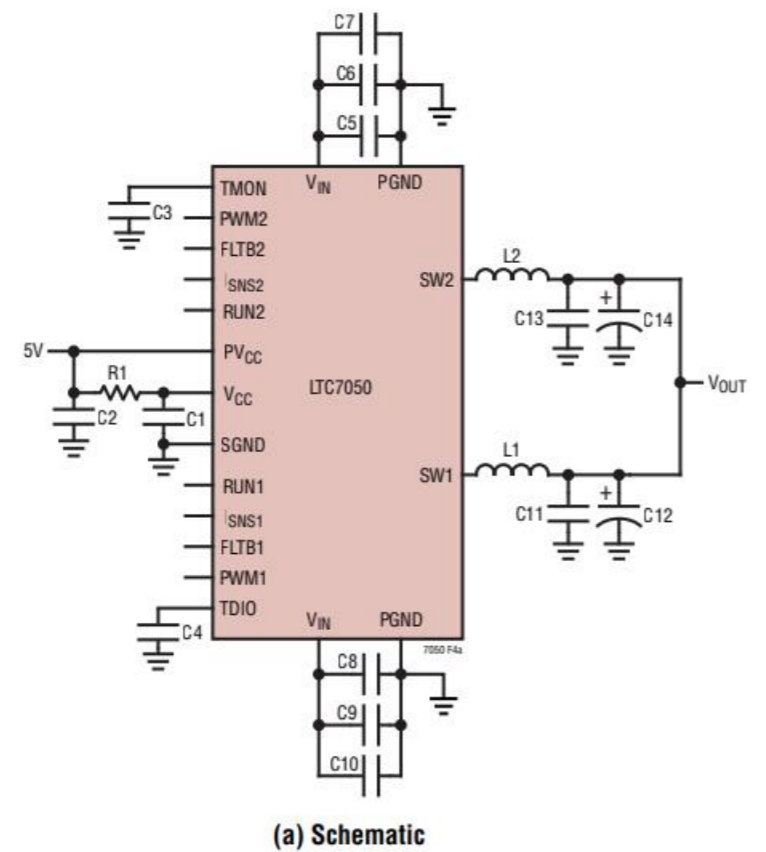
Mon Oct 14 15:10:16 2024



0.8V @ 36AMPS

CAD NOTE:
PLACE NEAR INDUCTOR

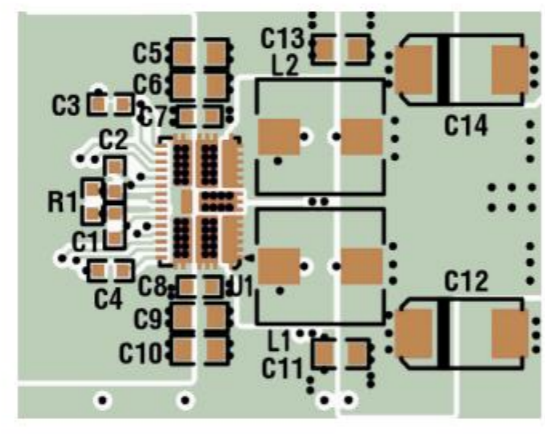
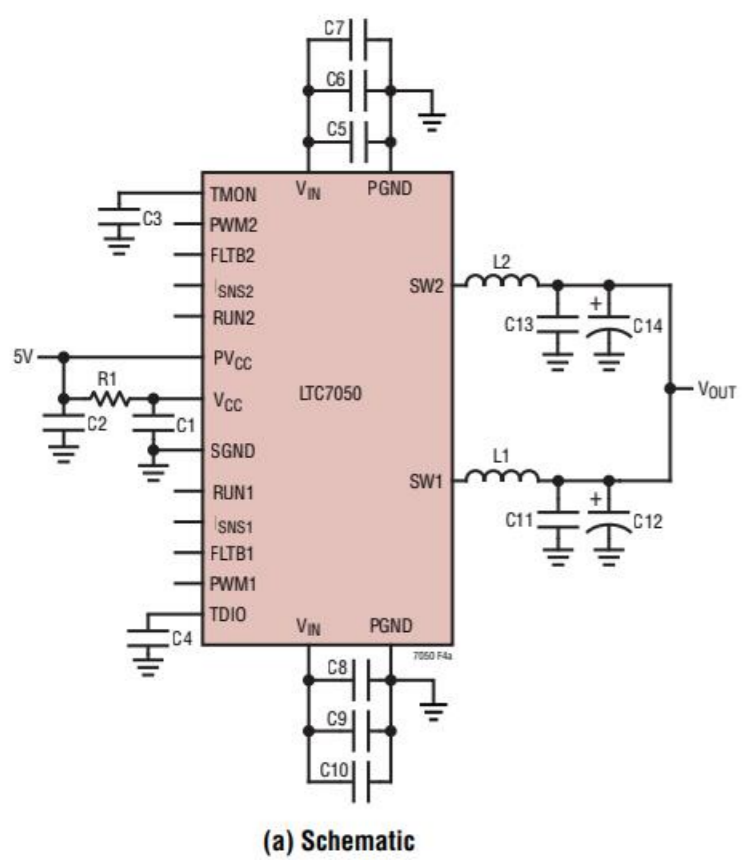
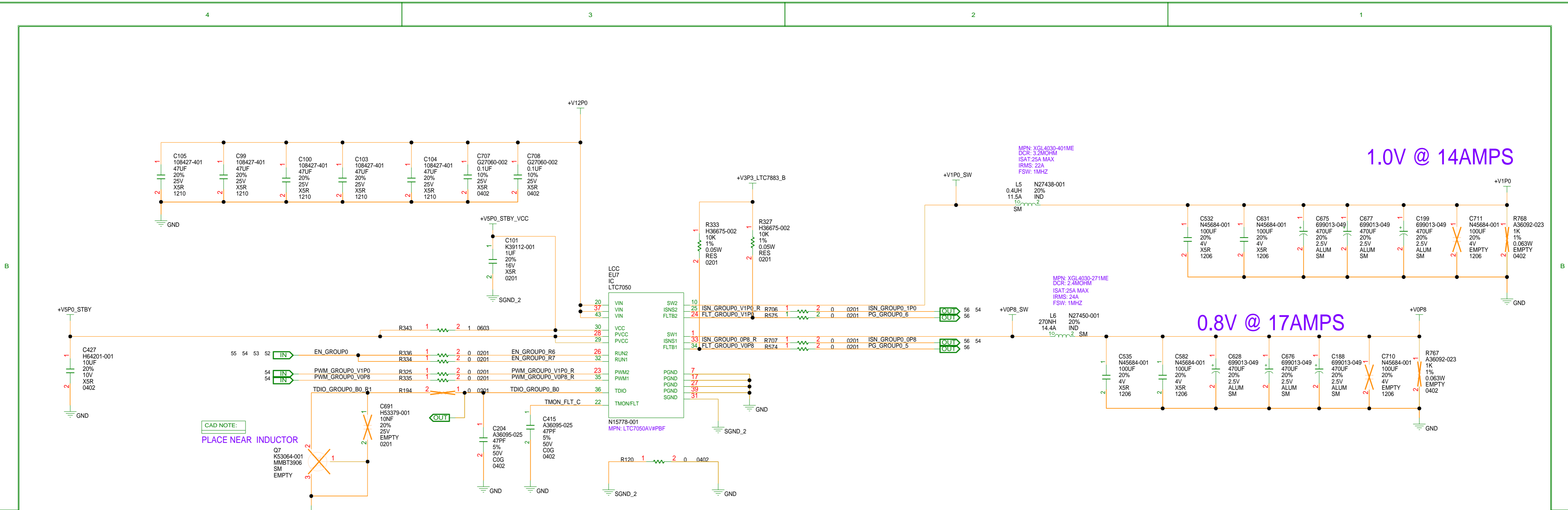
PROVISION TO REDUCE AN OFFSET ON THE CURRENT SENSE AT MID TO HEAVY LOADS DUE TO SWITCHING SPIKES



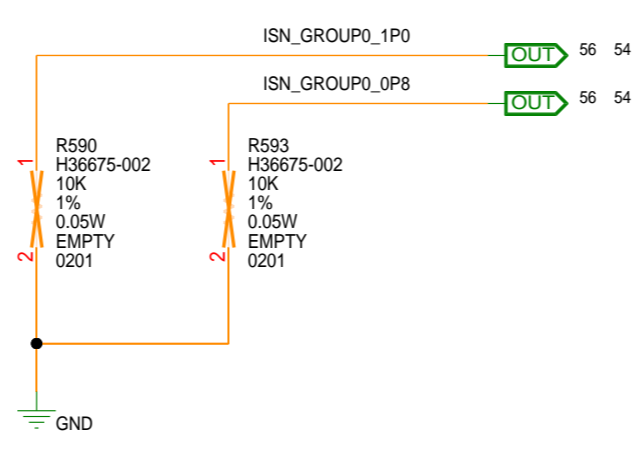
POWER-VCCP_VID

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
		SCALE:	DO NOT SCALE DRAWING		SHEET 54 OF 62

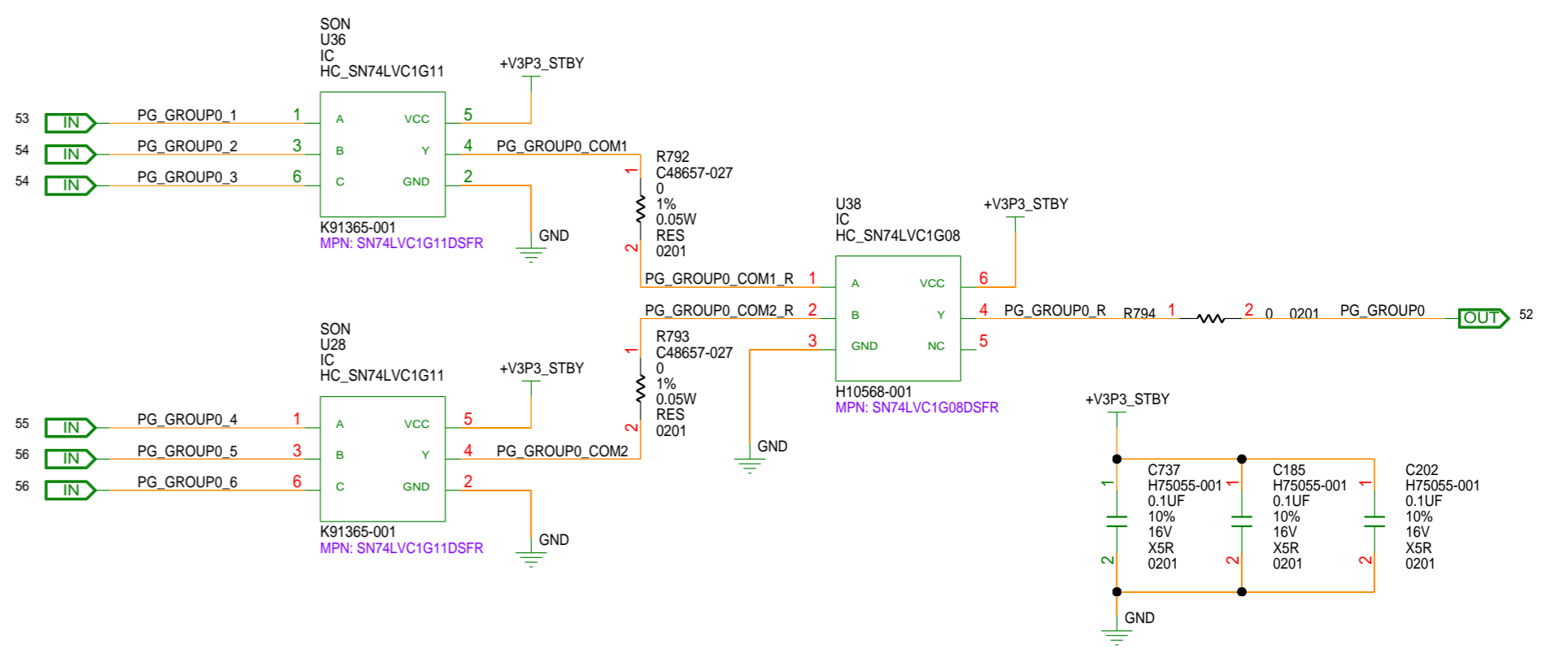
Mon Oct 14 15:10:19 2024



PROVISION TO REDUCE AN OFFSET ON THE CURRENT SENSE AT MID TO HEAVY LOADS DUE TO SWITCHING SPIKES



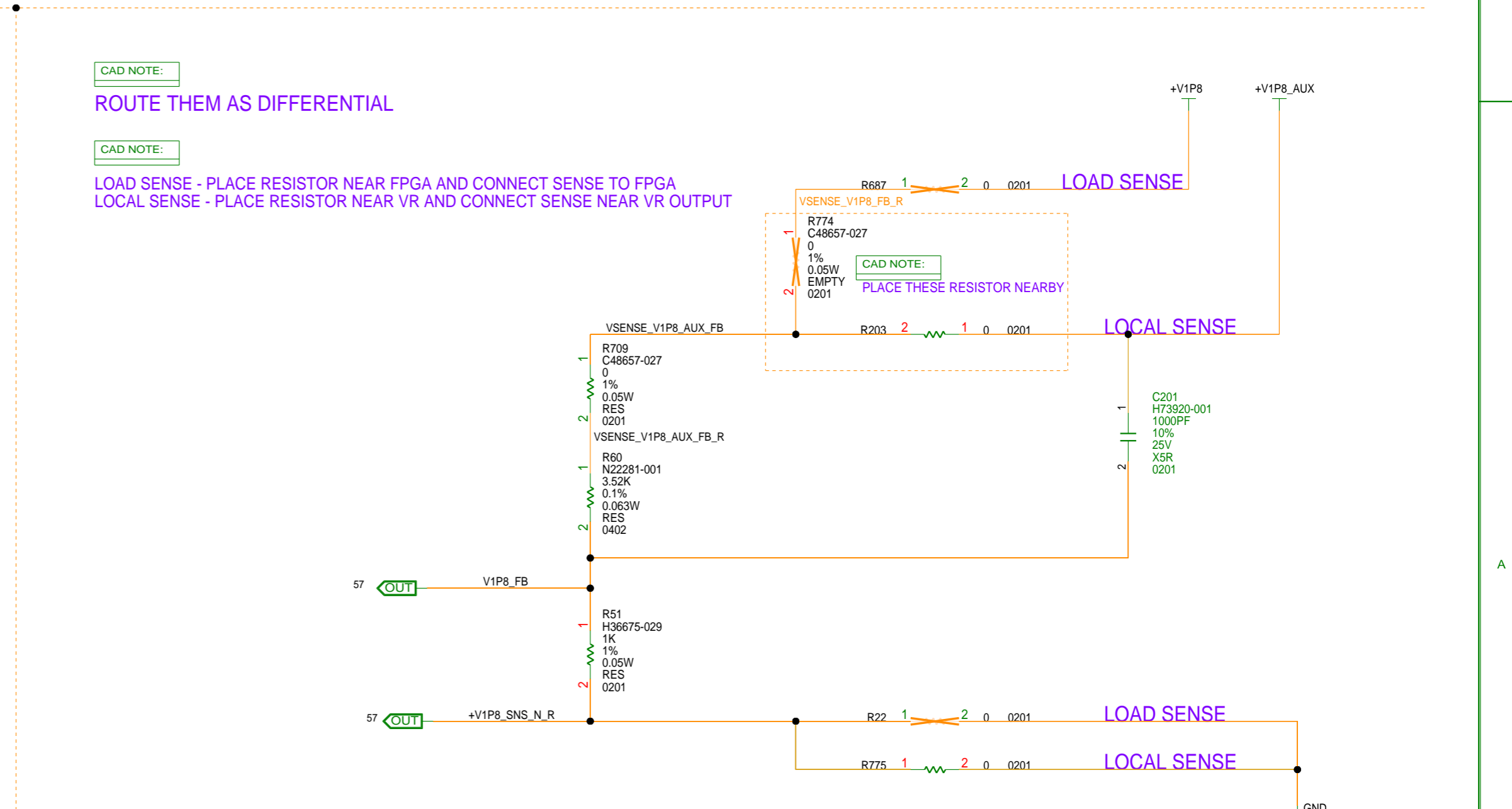
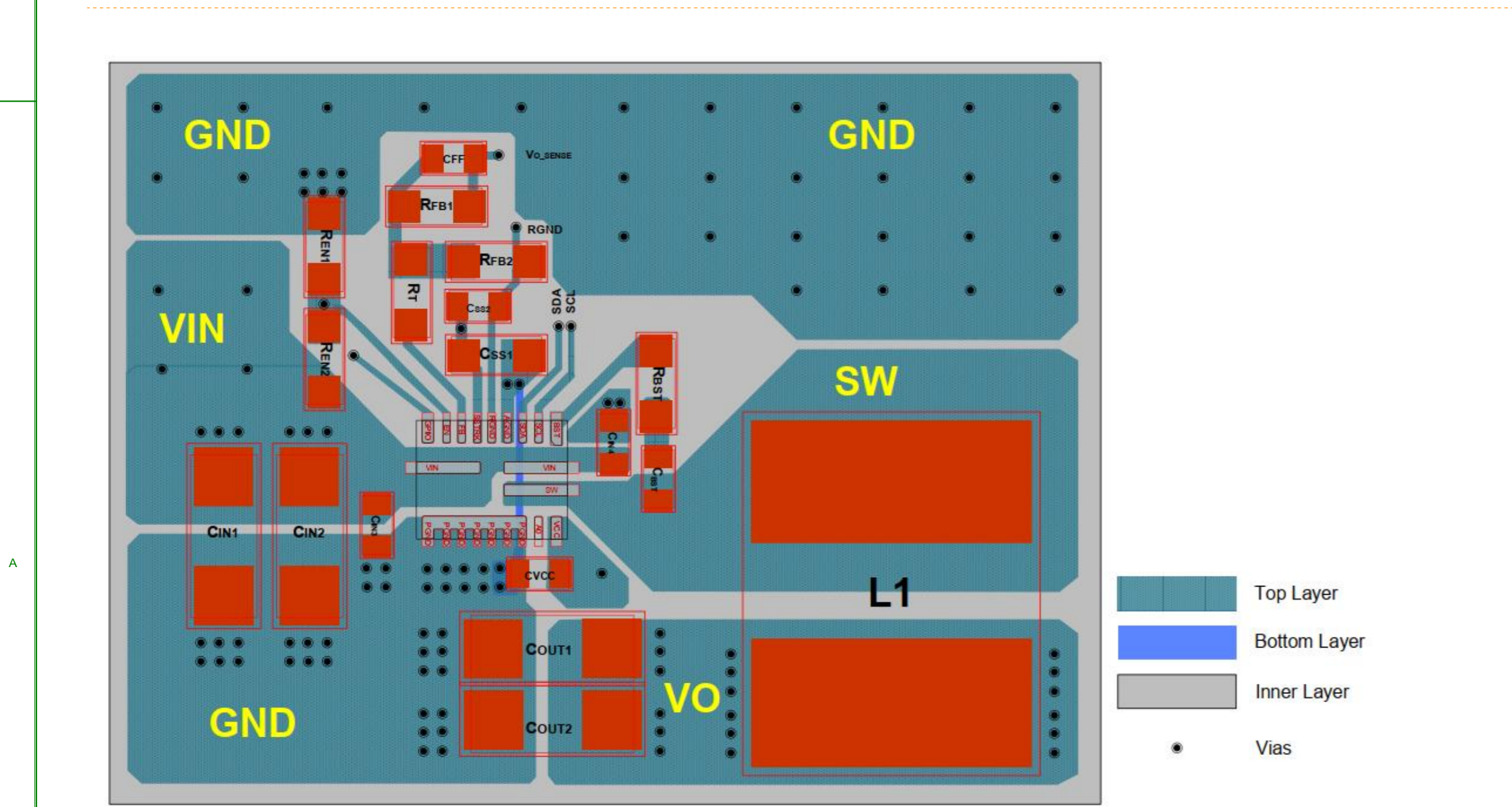
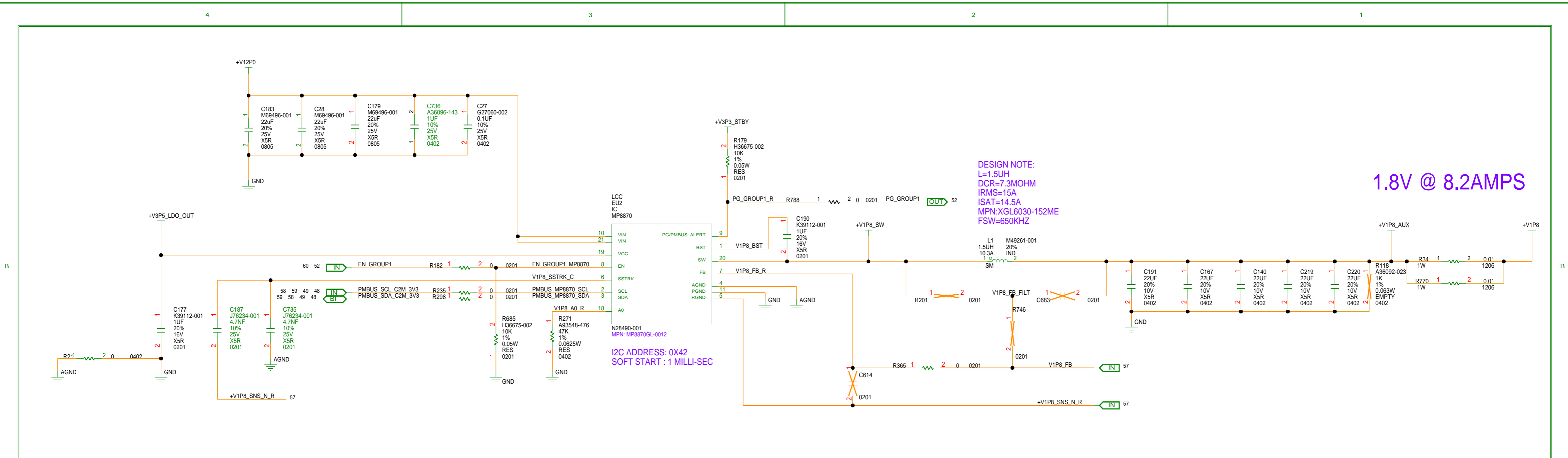
POWER GOOD



POWER - +V1P0, +V0P8

DEPARTMENT	altera An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 55 OF 62

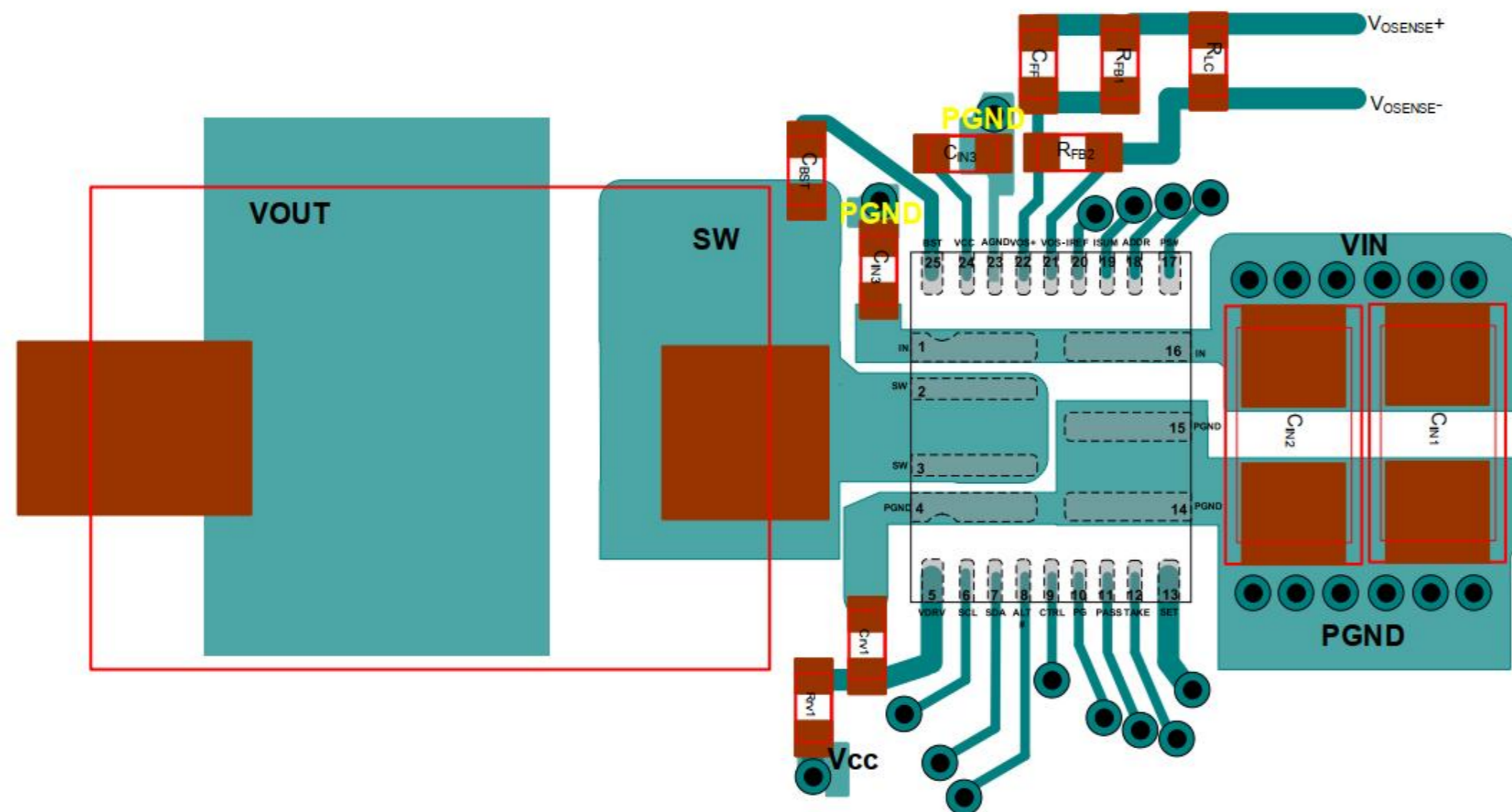
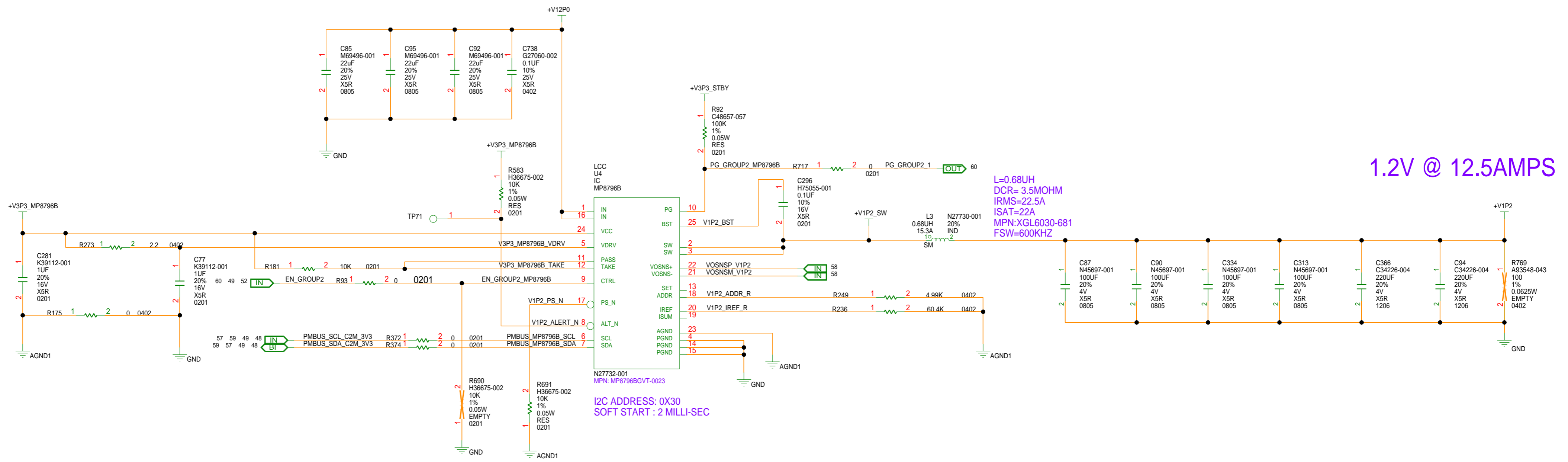
Mon Oct 14 15:10:20 2024



POWER - +V1P8

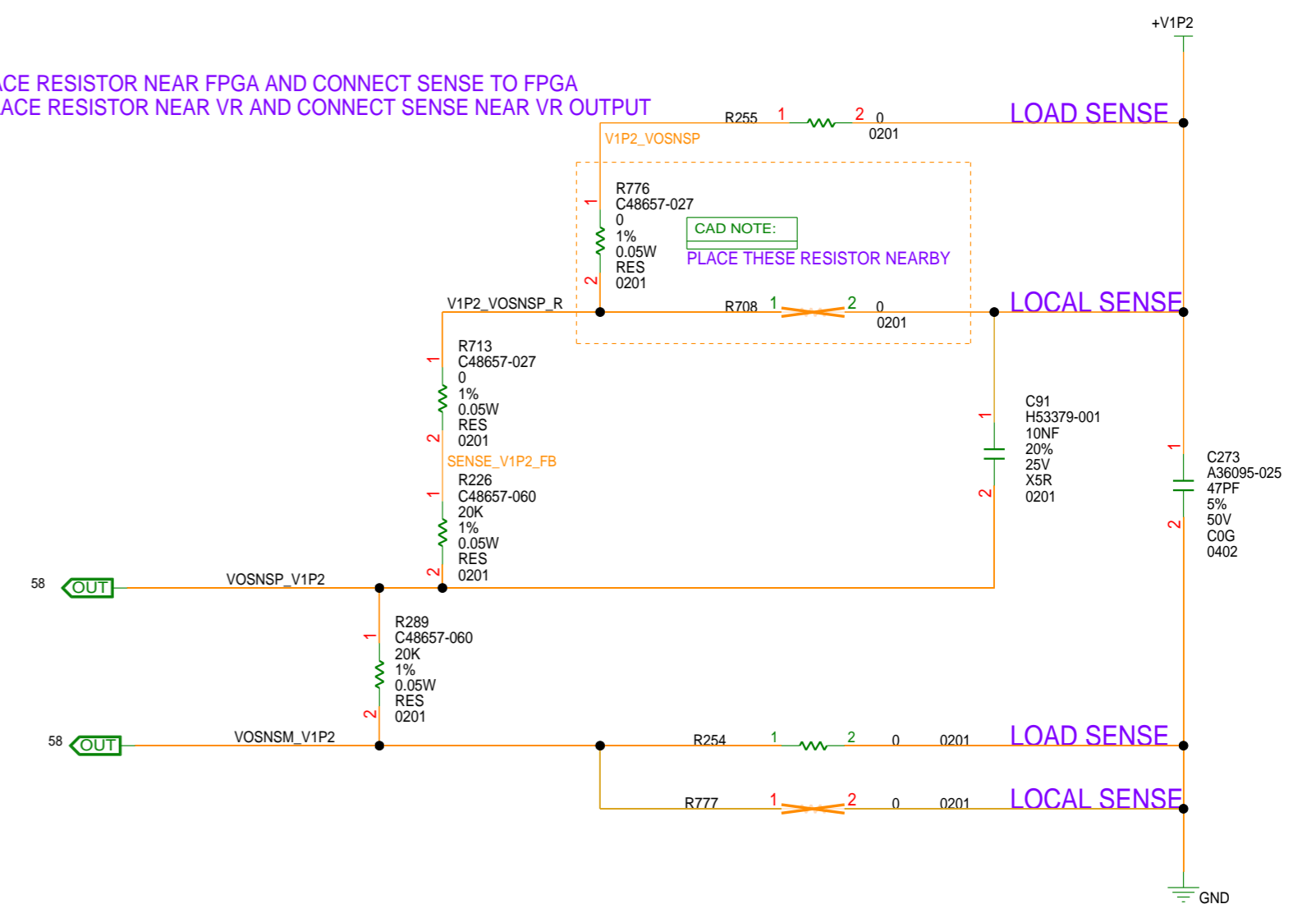
Mon Oct 14 15:10:21 2024

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:	DO NOT SCALE DRAWING			SHEET	56 OF 62



CAD NOTE:
ROUTE THEM AS DIFFERENTIAL

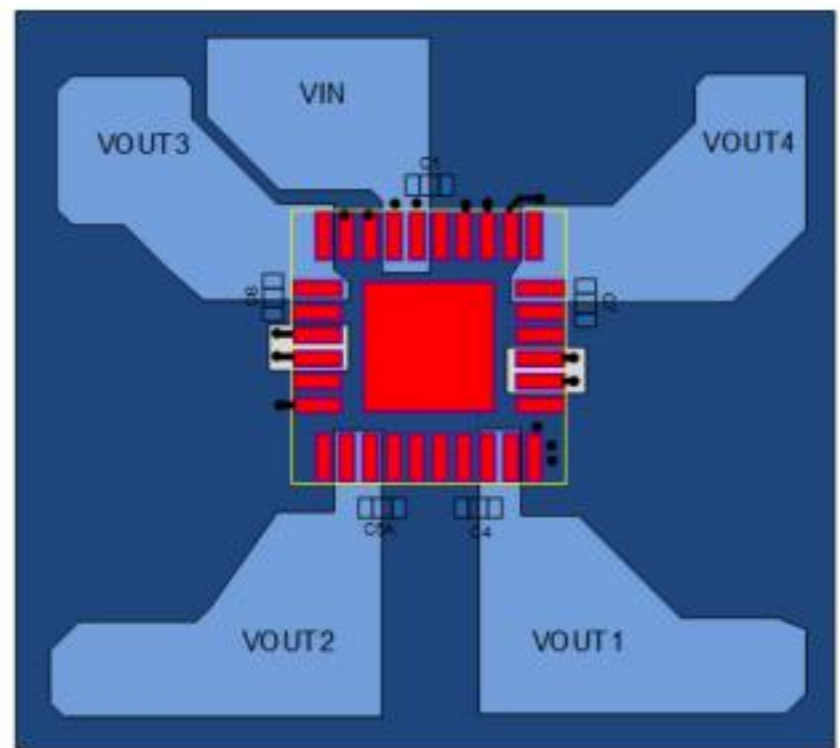
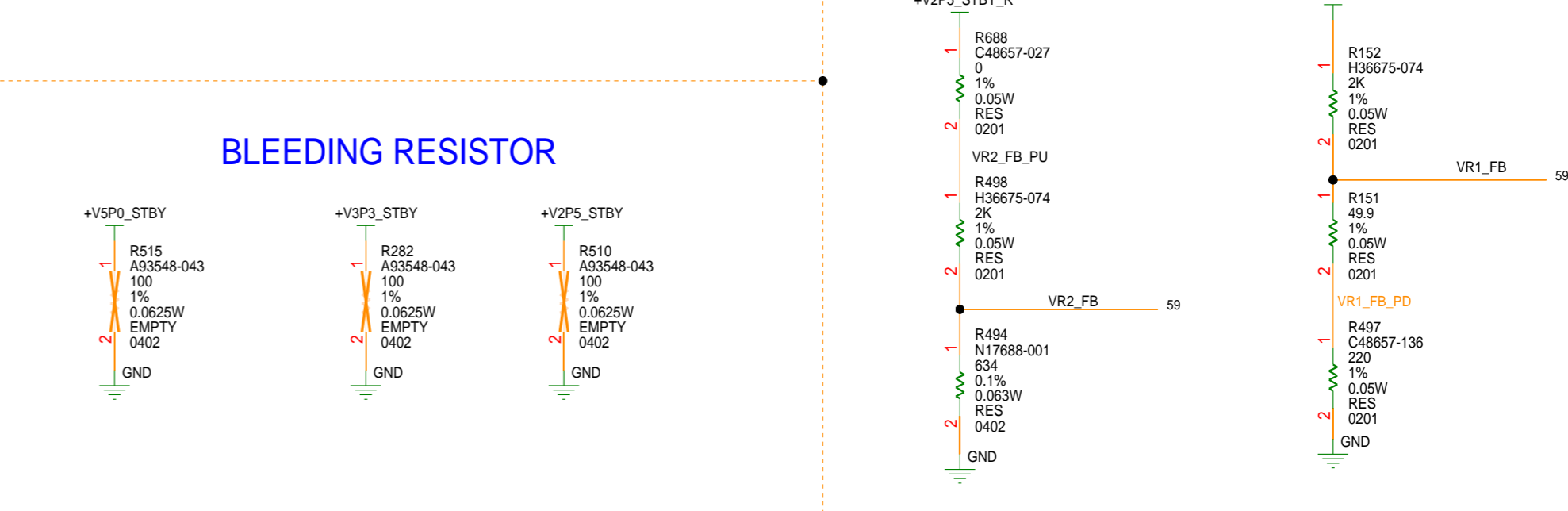
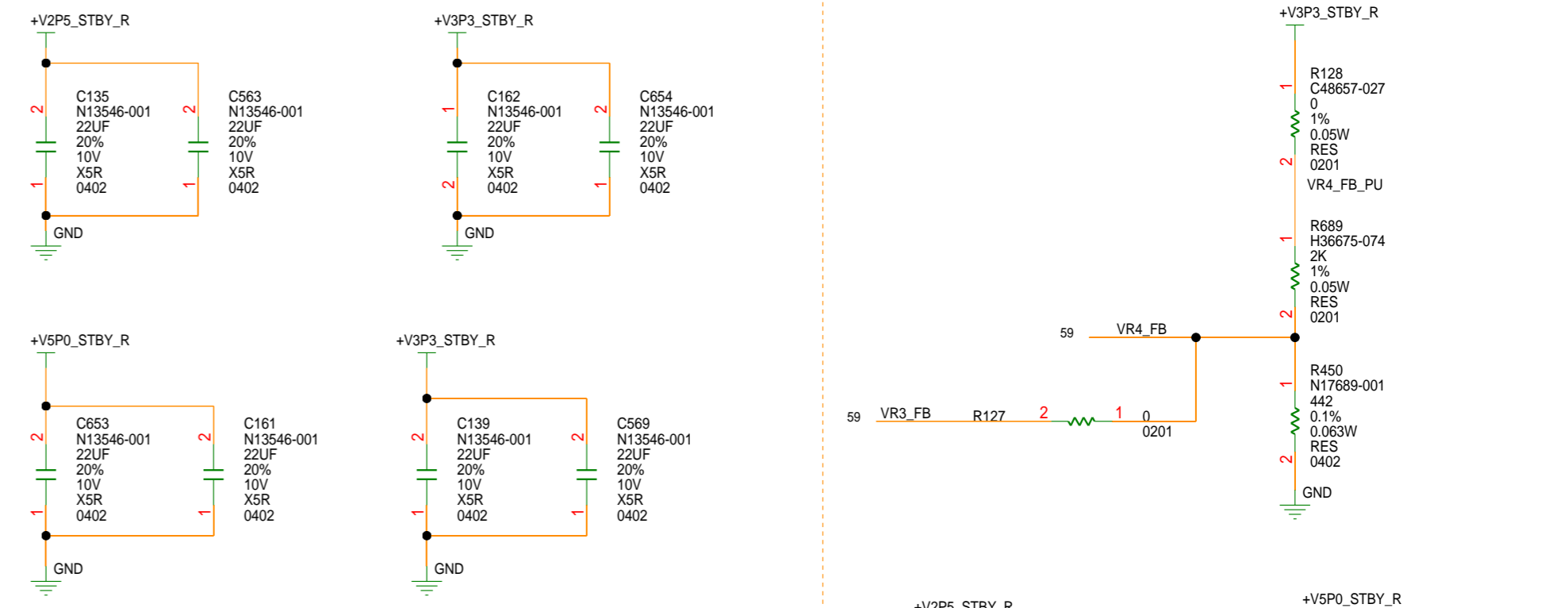
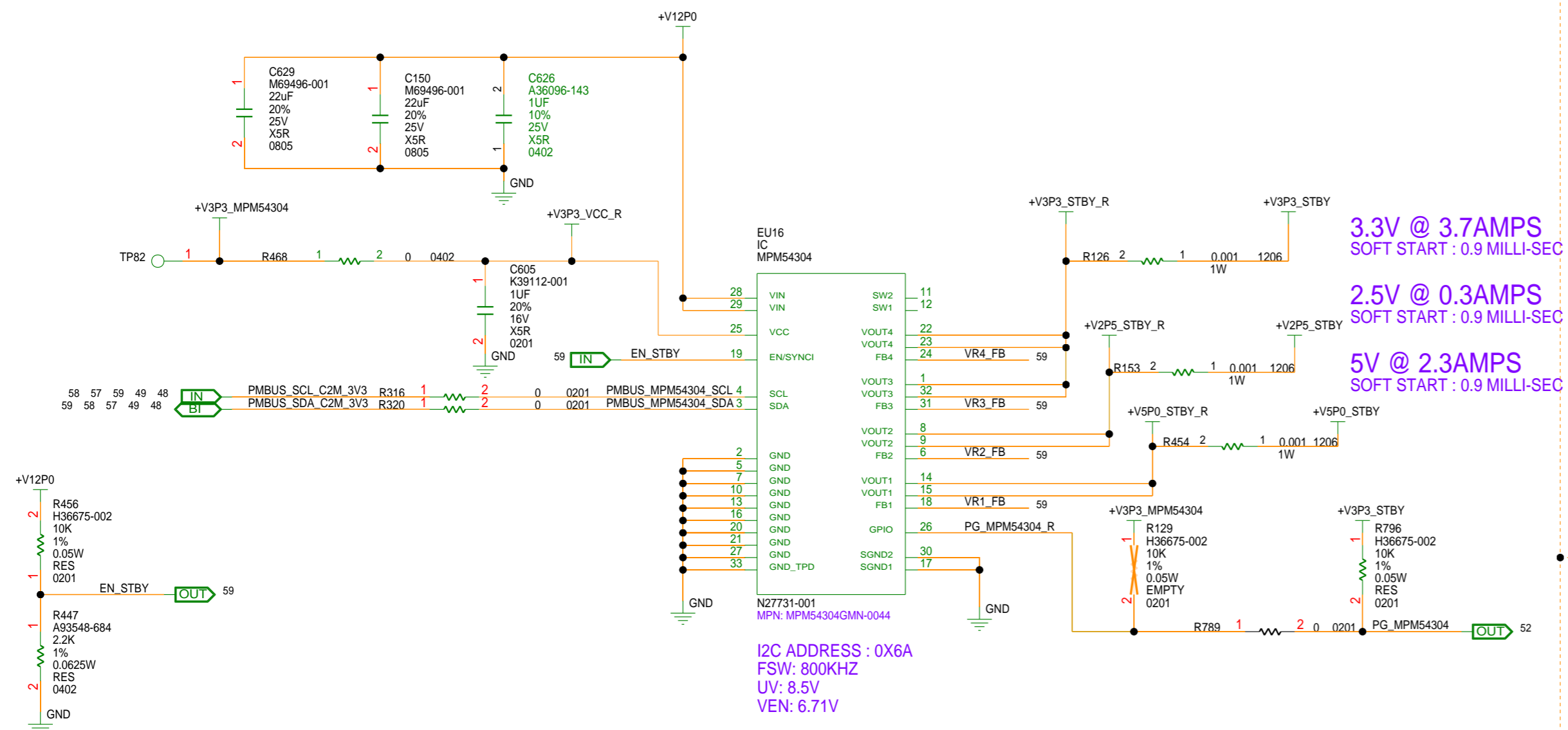
CAD NOTE:
LOAD SENSE - PLACE RESISTOR NEAR FPGA AND CONNECT SENSE TO FPGA
LOCAL SENSE - PLACE RESISTOR NEAR VR AND CONNECT SENSE NEAR VR OUTPUT



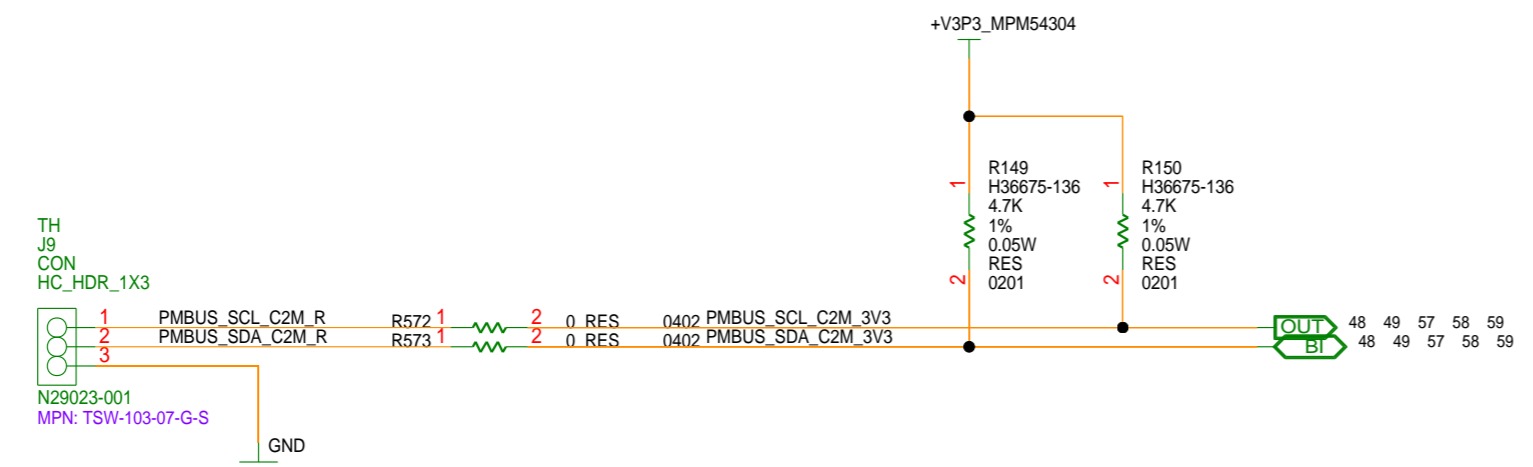
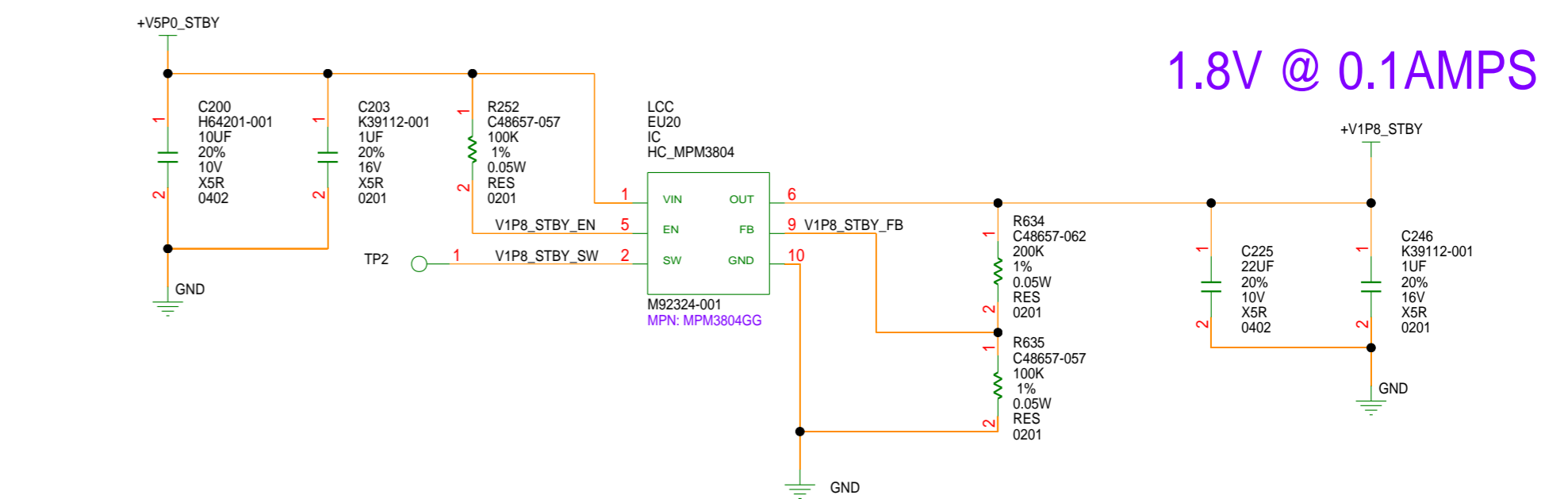
Mon Oct 14 15:10:22 2024

POWER - +V1P2

DEPARTMENT	altera An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 57 OF 62



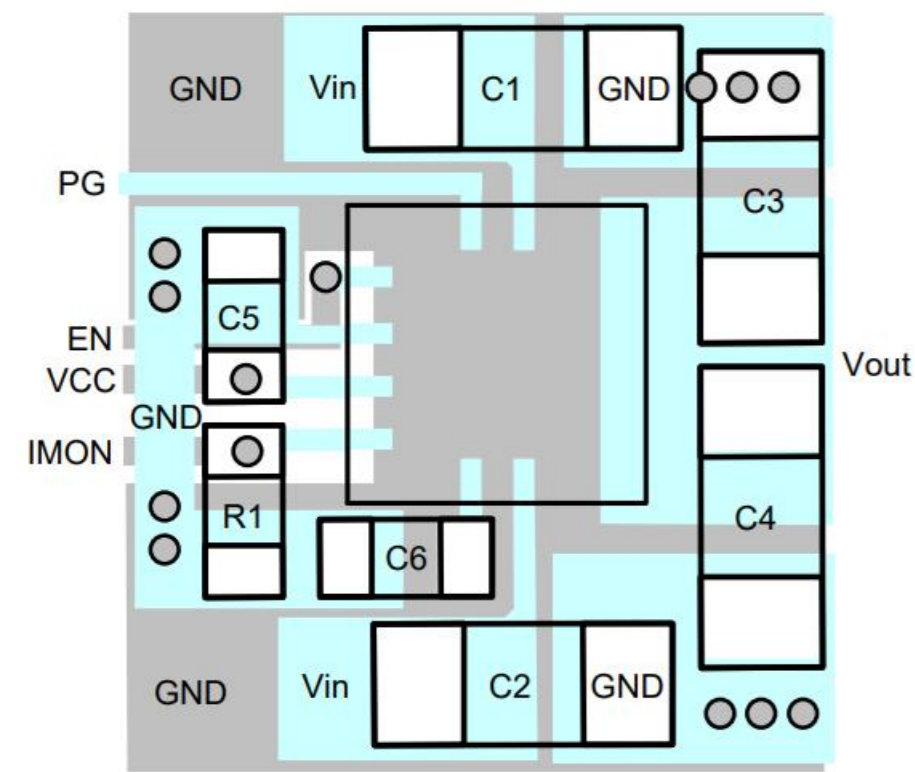
+V1P8_STBY SUPPLY



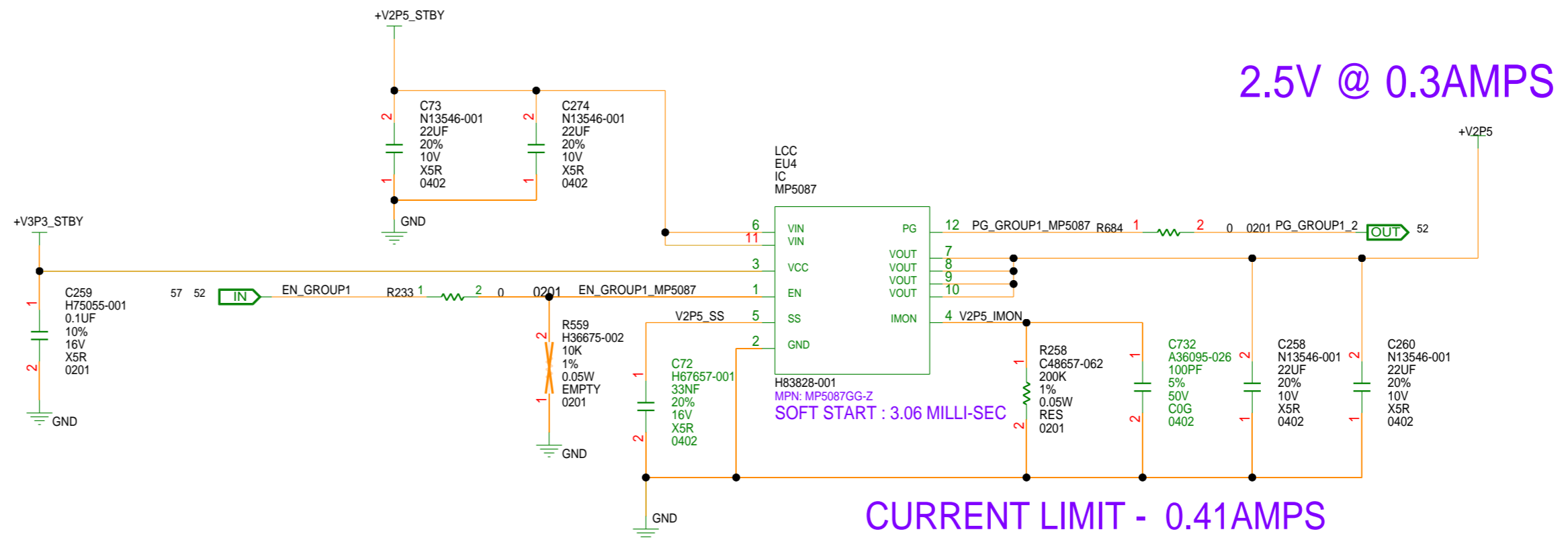
Mon Oct 14 15:10:23 2024

DEPARTMENT	altera An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
		SCALE:	DO NOT SCALE DRAWING		SHEET 58 OF 62

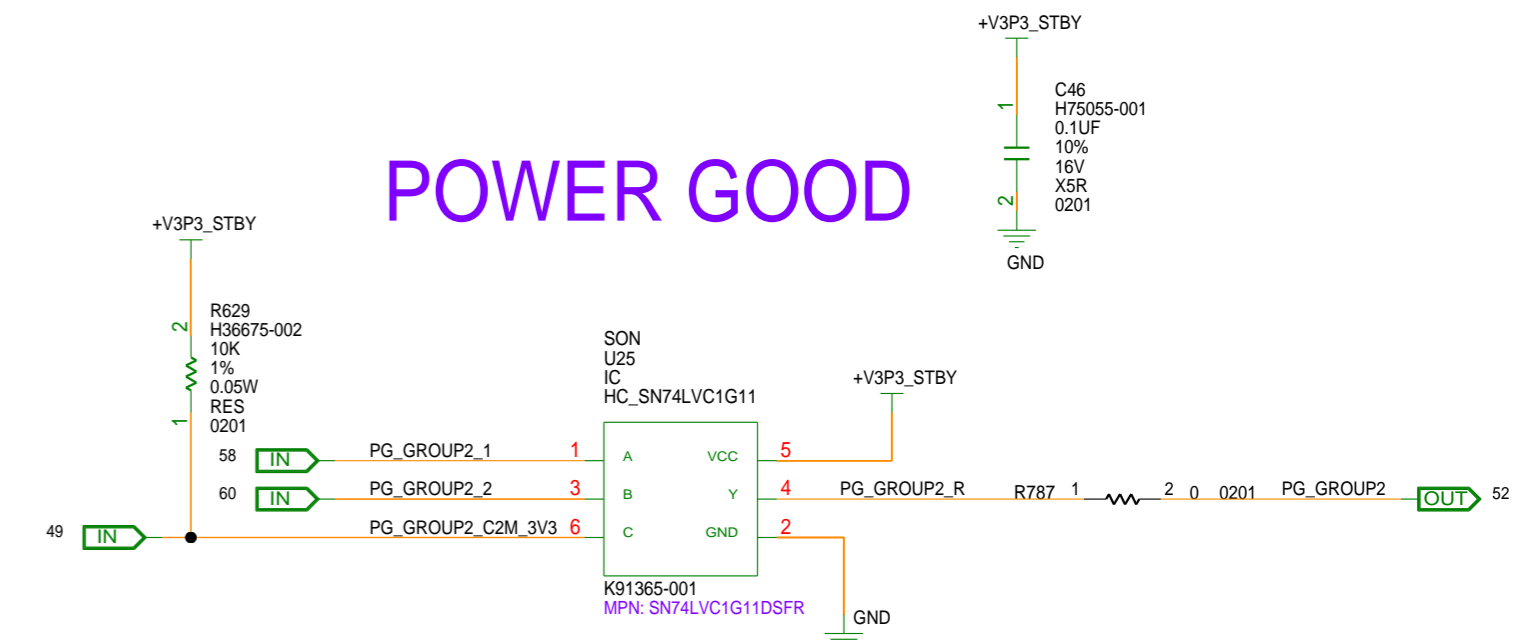
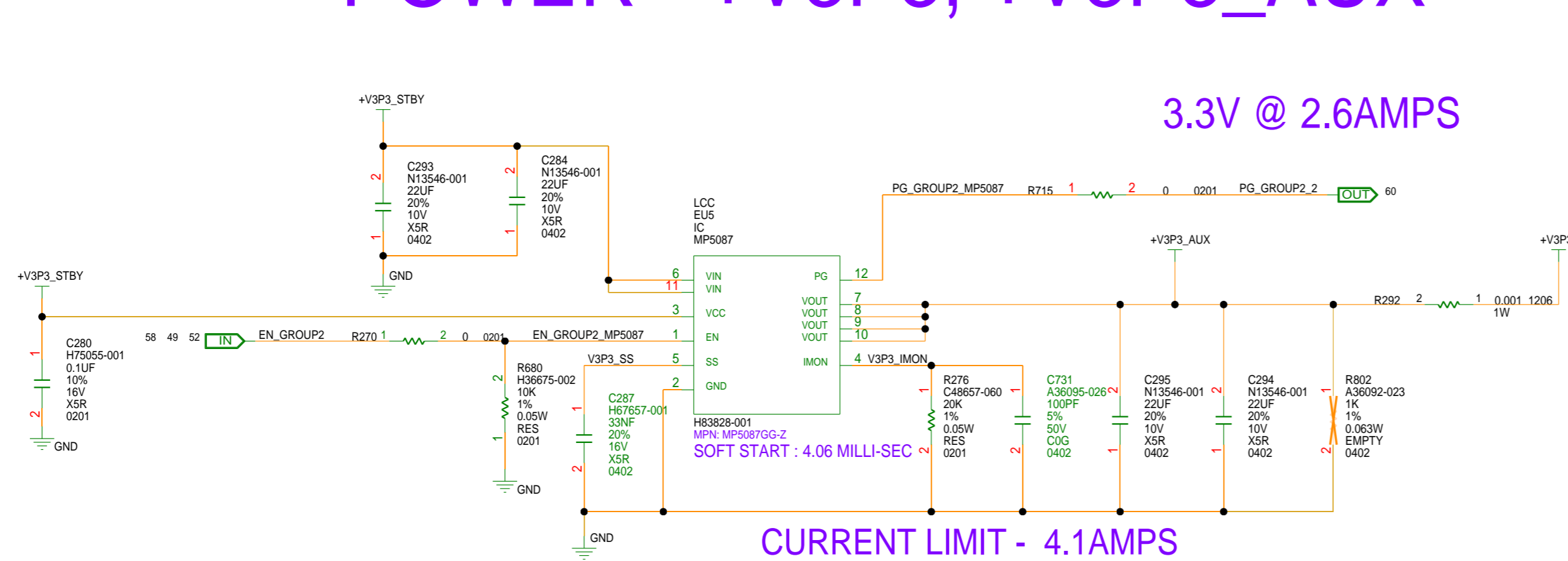
POWER - +V2P5



Recommended Layout



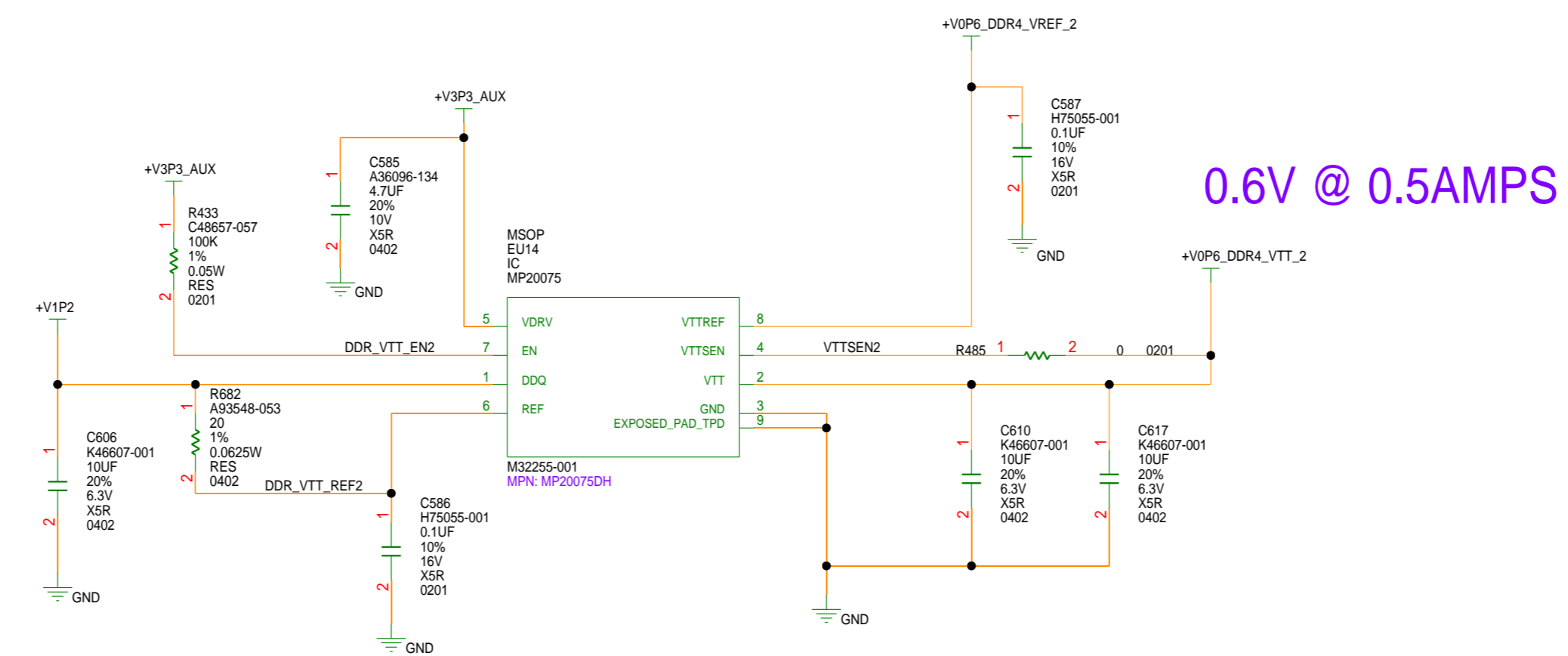
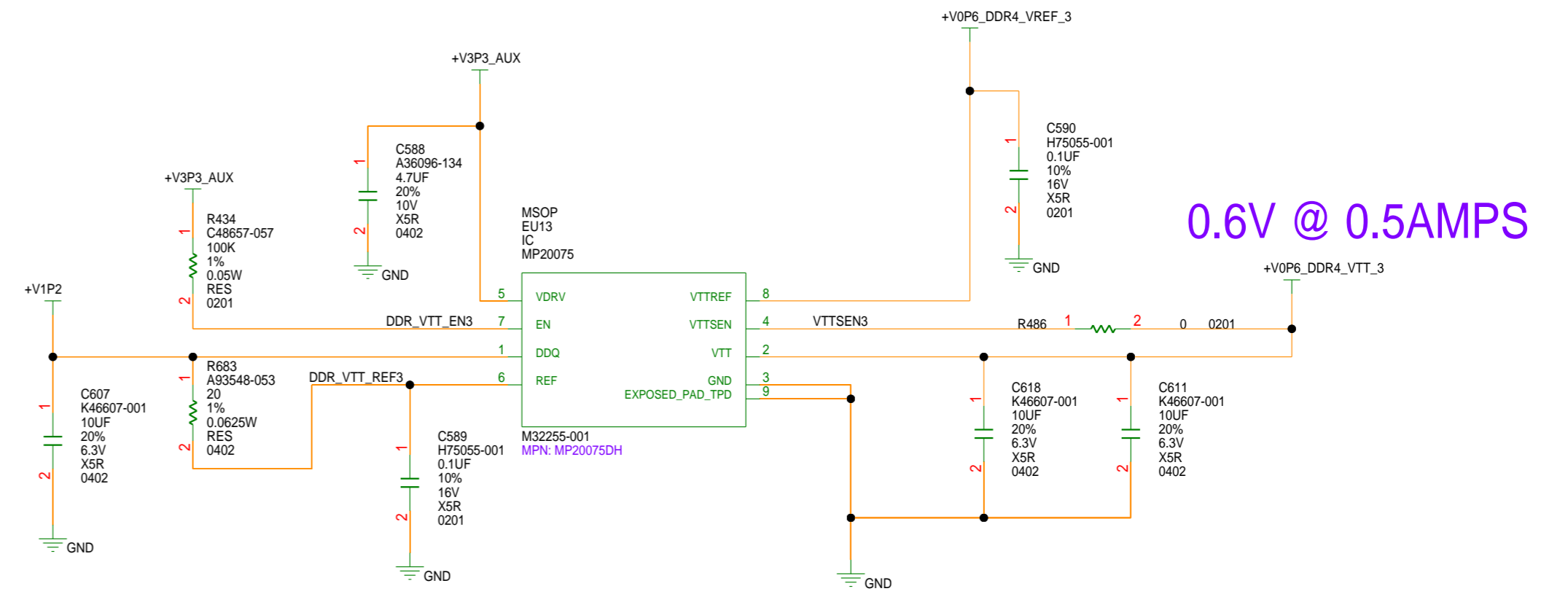
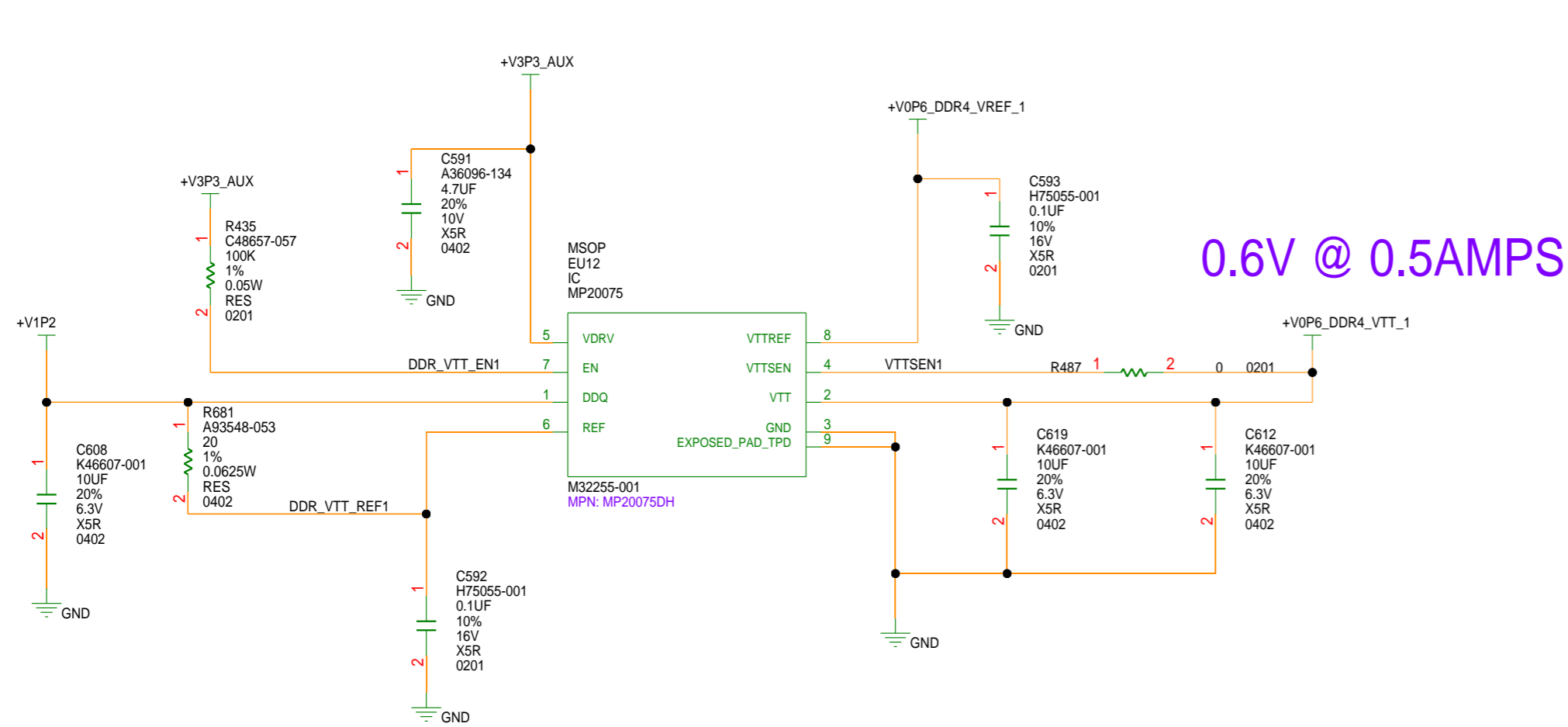
POWER - +V3P3, +V3P3_AUX



POWER - MP5087 LOAD SWITCH


DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 59 OF 62

Mon Oct 14 15:10:24 2024



POWER - +V0P6_DDR4_VTT

Mon Oct 14 15:10:35 2024

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING			SHEET 60 OF 62

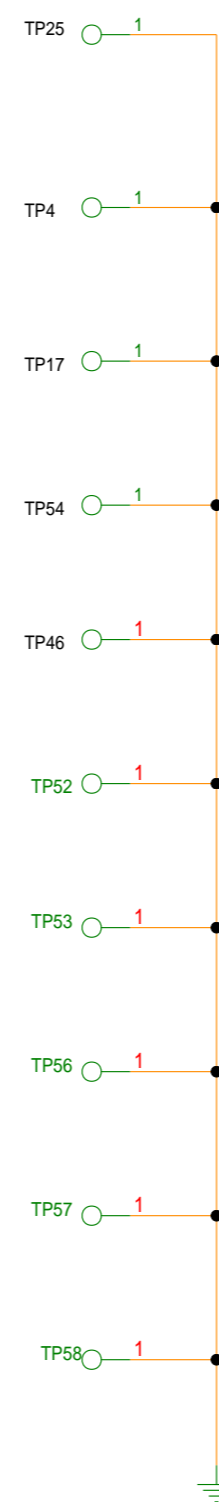
POWER PROBE POINTS



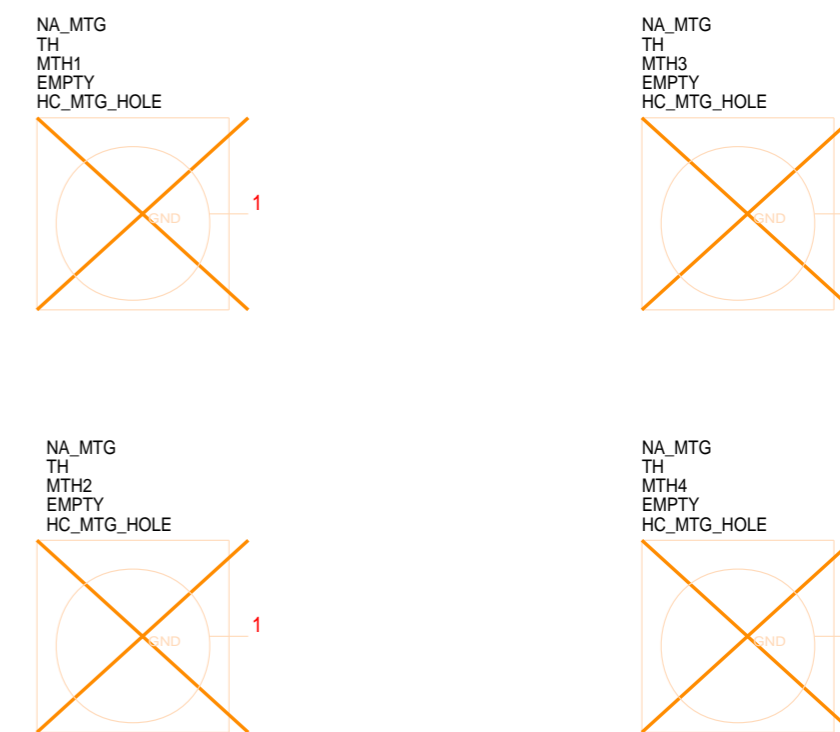
CAD NOTE:
PLACE NEAR PRIMARY LOAD POINTS FOR EACH RAIL
ADD SILK SCREEN LABEL WITH RAIL NAME FOR EACH TP

GND PROBE POINTS

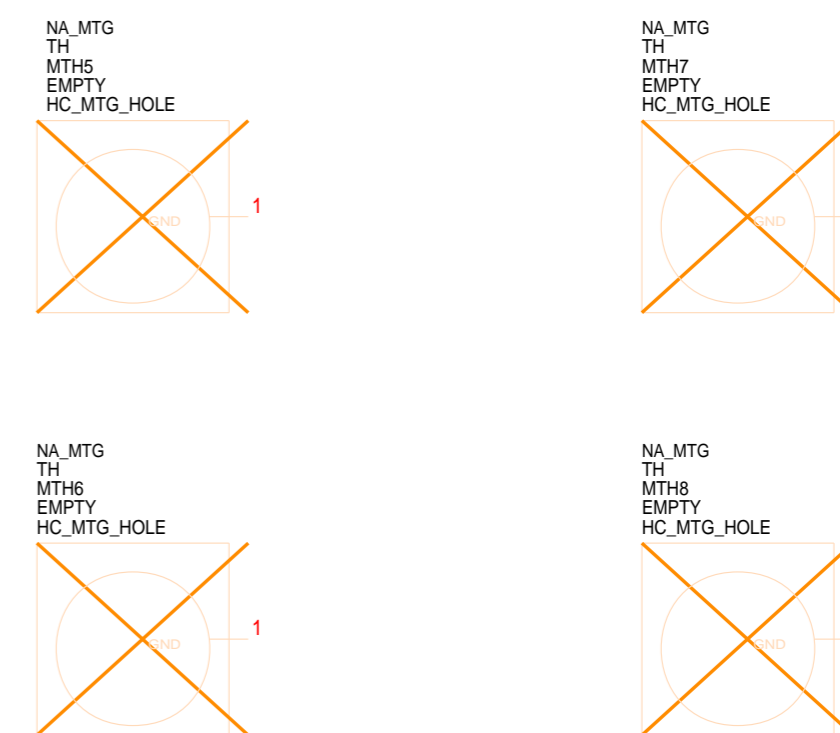
CAD NOTE:
SCATTER AROUND THE BOARD TOP SIDE



MOUNTING HOLE FOR HEAT SINK



MOUNTING HOLES FOR PCB



TEST POINT


Mon Oct 14 15:10:37 2024

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING		SHEET	61 OF 62

SR. NO.	REV	DATE	DESCRIPTION
1	1P0	AUG'23	INITIAL FAB - A RELEASE
2	2P0	MAR'24	FAB - B RELEASE
3	2P1	JUN'24	1. UPDATED HPS RESET CIRCUIT 2. UPDATED I2C TREE

Mon Sep 30 16:23:18 2024

REVISION HISTORY

DEPARTMENT	 An Intel Company	SIZE	CODE	DOCUMENT NUMBER	REV
		C+	34649	150-0330723-B1	2.1
SCALE:		DO NOT SCALE DRAWING		SHEET	62 OF 62