

# AGILEX™ 5 FPGA E-SERIES 065B


## MODULAR DEVELOPMENT KIT-CARRIER BOARD

PB :N19945-002 : FAB B  
 PBA:N19361-002 : ASSEMBLY FAB B  
 TA :N19359-002 : TA FAB B

Project Drawing Numbers:

|                           |               |
|---------------------------|---------------|
| RAW PCB                   | 100-330724-B1 |
| GERBER FILES              | 110-330724-B1 |
| PCB DESIGN FILES          | 120-330724-B1 |
| ASSEMBLY DRAWING          | 130-330724-B1 |
| FAB DRAWING               | 140-330724-B1 |
| SCHEMATIC DRAWING         | 150-330724-B1 |
| PCB FILM                  | 160-330724-B1 |
| BILL OF MATERIALS         | 170-330724-B1 |
| SCHEMATIC DESIGN FILES    | 180-330724-B1 |
| FUNCTIONAL SPECIFICATIONS | 210-330724-B1 |
| PCB LAYOUT GUIDELINES     | 220-330724-B1 |
| ASSEMBLY REWORK           | 320-330724-B1 |

Tue Oct 1 13:02:02 2024

|            |   |                      |       |                 |         |
|------------|---|----------------------|-------|-----------------|---------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV     |
|            |   | C+                   | 34649 | 150-330724-B1   | 2.0     |
| SCALE:     |   | DO NOT SCALE DRAWING |       | SHEET           | 1 OF 74 |

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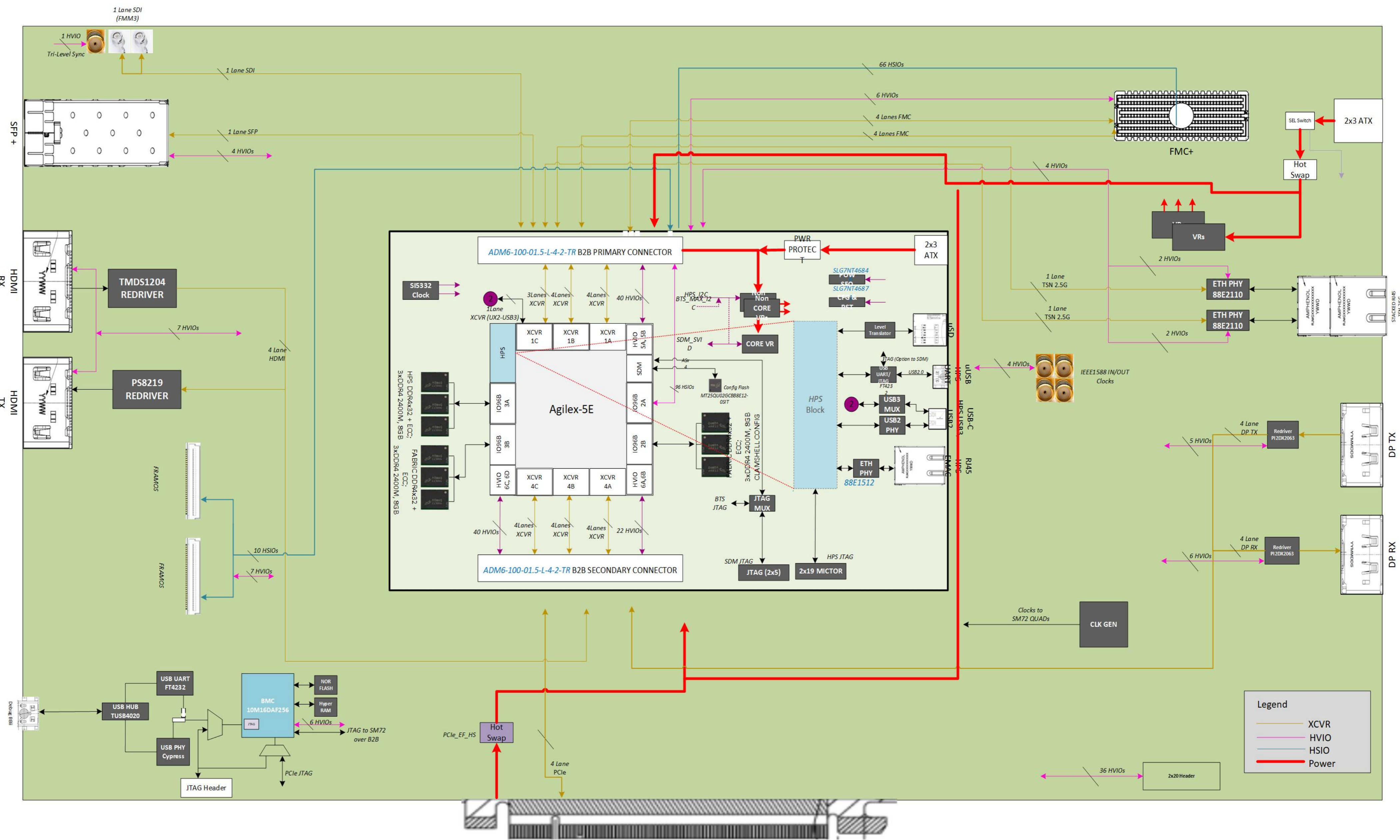
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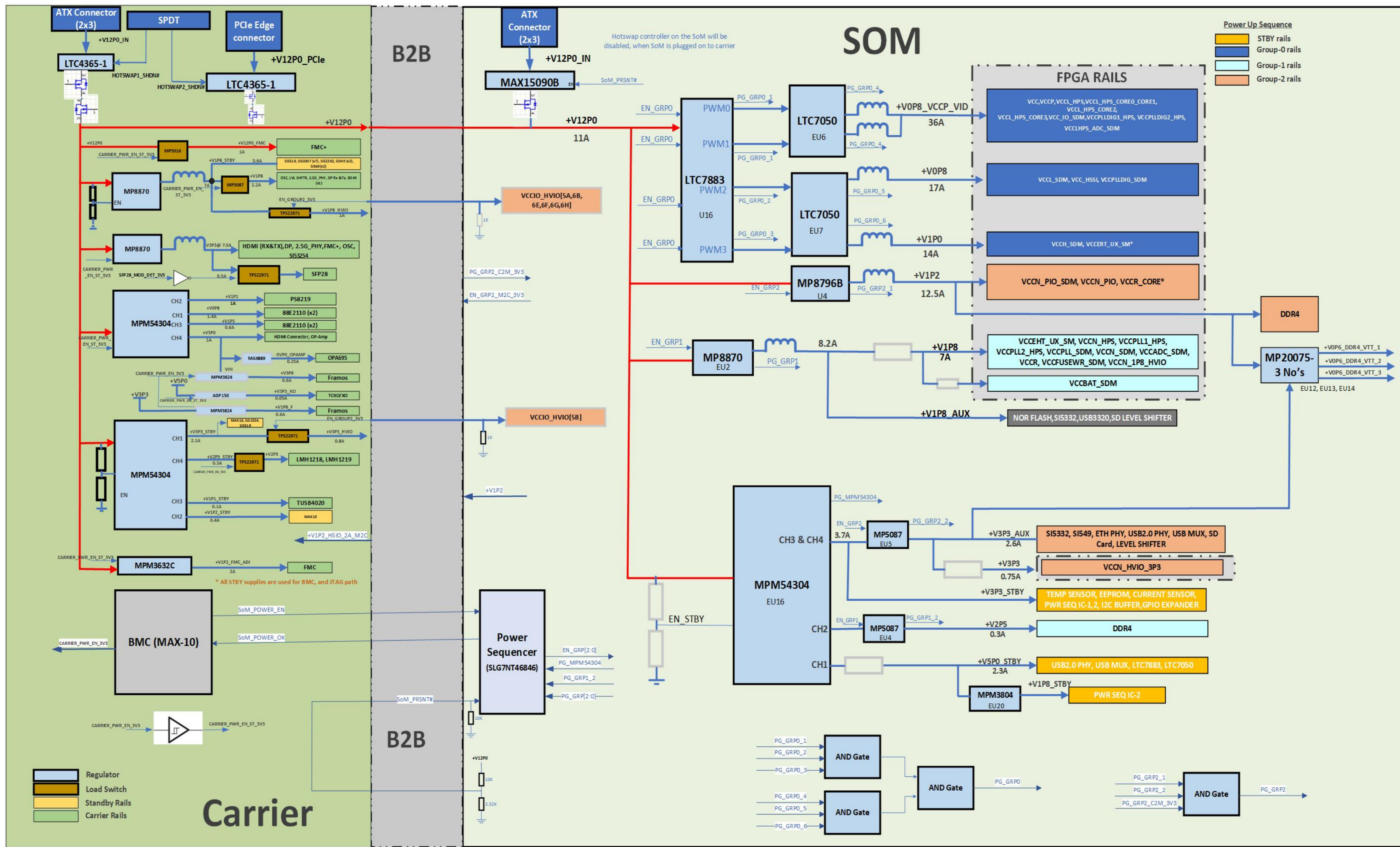
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|            |   | C+     | 34649                | 150-330724-B1   | 2.0           |
|            |   | SCALE: | DO NOT SCALE DRAWING |                 | SHEET 2 OF 74 |



# BLOCK DIAGRAM

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|            |   |      |       |                 |         |
|------------|---|------|-------|-----------------|---------|
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|            |   | C+   | 34649 | 150-330724-B1   | 2.0     |
| SCALE:     | DO NOT SCALE DRAWING  |      |       | SHEET           | 3 OF 74 |



**Power Up Sequence**

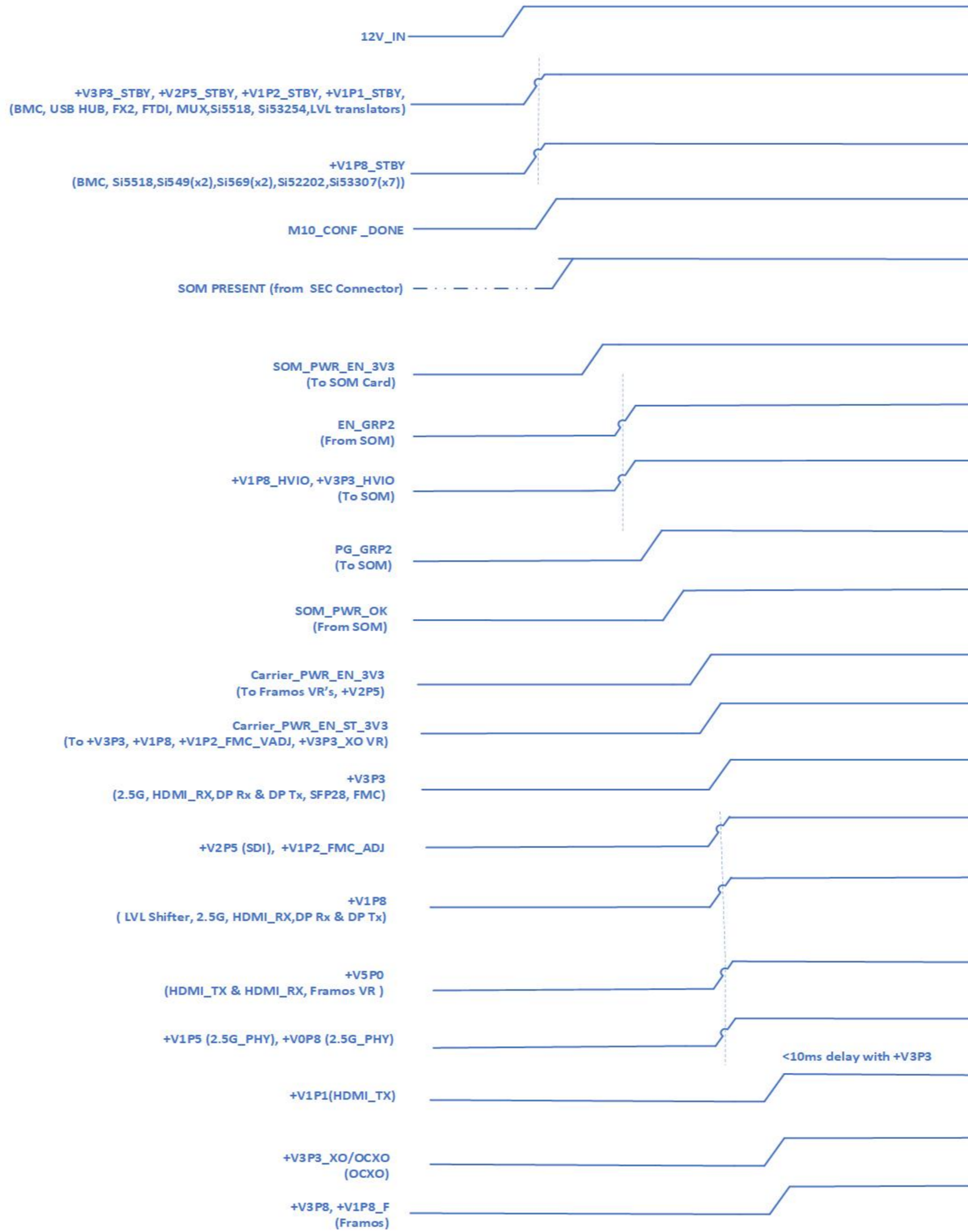
- STBY rails
- Group-0 rails
- Group-1 rails
- Group-2 rails

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# POWER TREE


|            |                                   |                      |       |                 |               |
|------------|-----------------------------------|----------------------|-------|-----------------|---------------|
| DEPARTMENT | <b>altera</b><br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV           |
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# AG5E CARRIER Board Power Sequence



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# POWER SEQUENCE

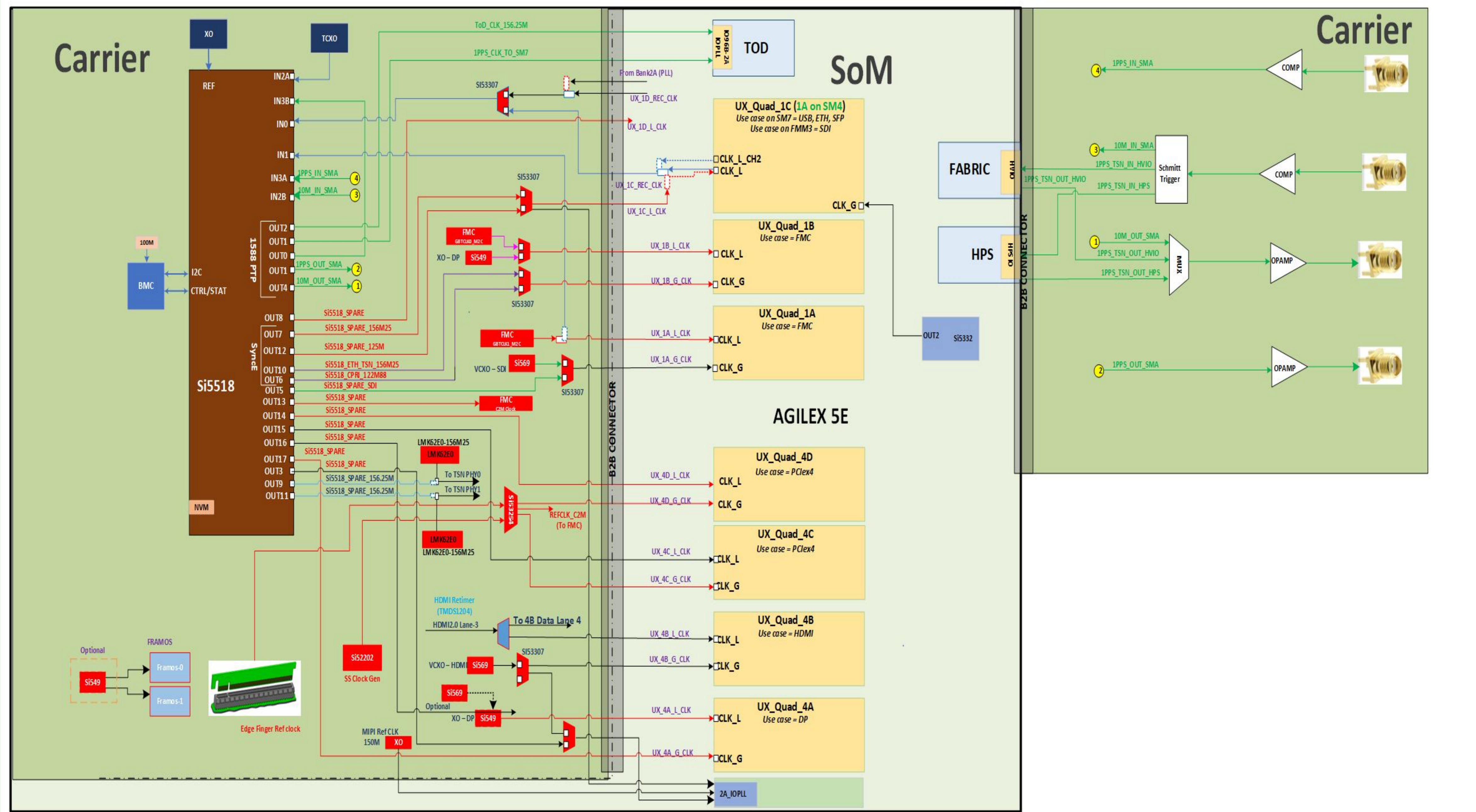
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|            |   | C+                   | 34649 | 150-330724-B1   | 2.0 |
| SCALE:     |   | DO NOT SCALE DRAWING |       | SHEET 5 OF 74   |     |

# Carrier

# Carrier


# SoM

# AGILEX 5E



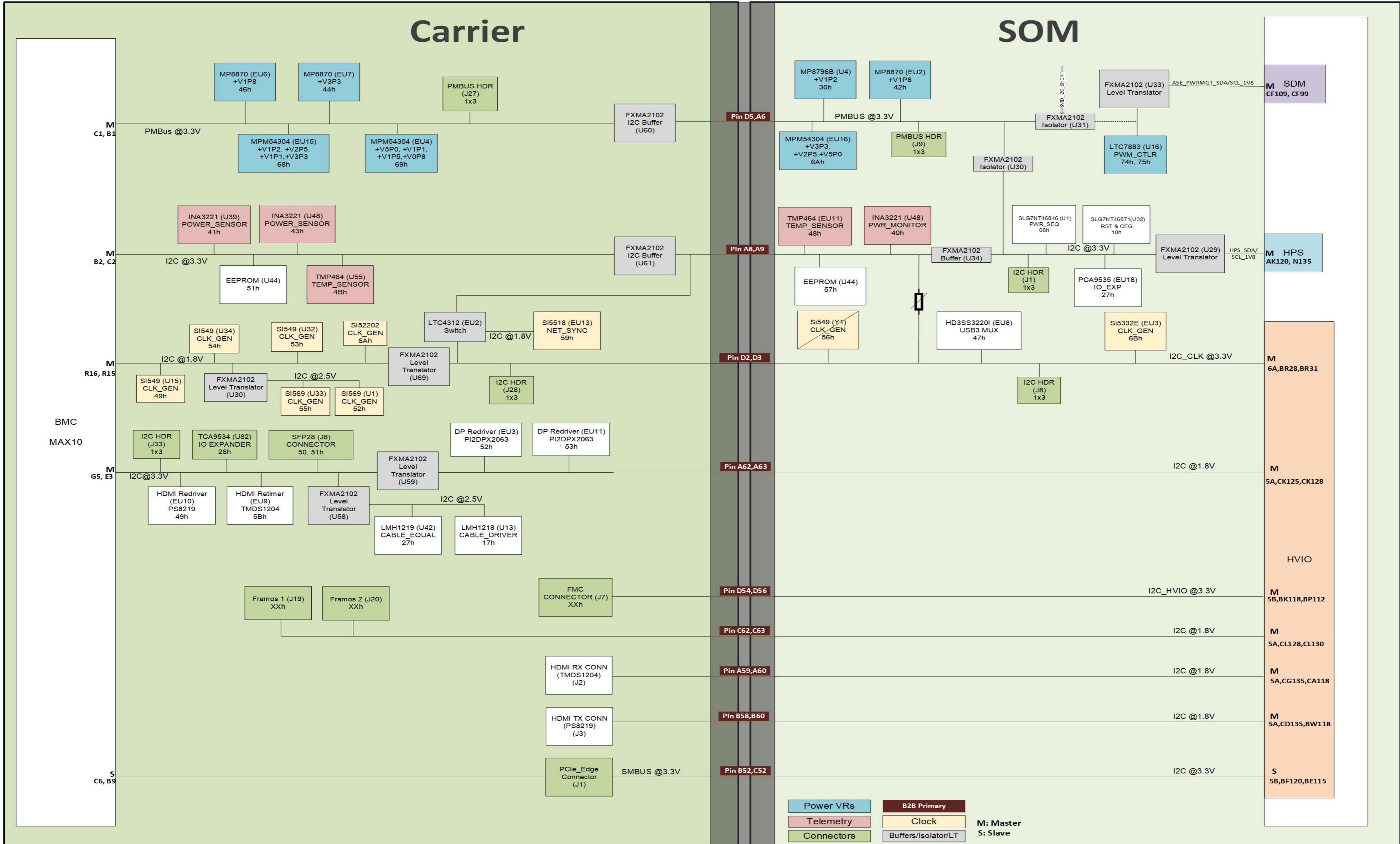
# CLOCK TREE

Mon Oct 14 18:00:19 2024

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# Carrier

# SOM



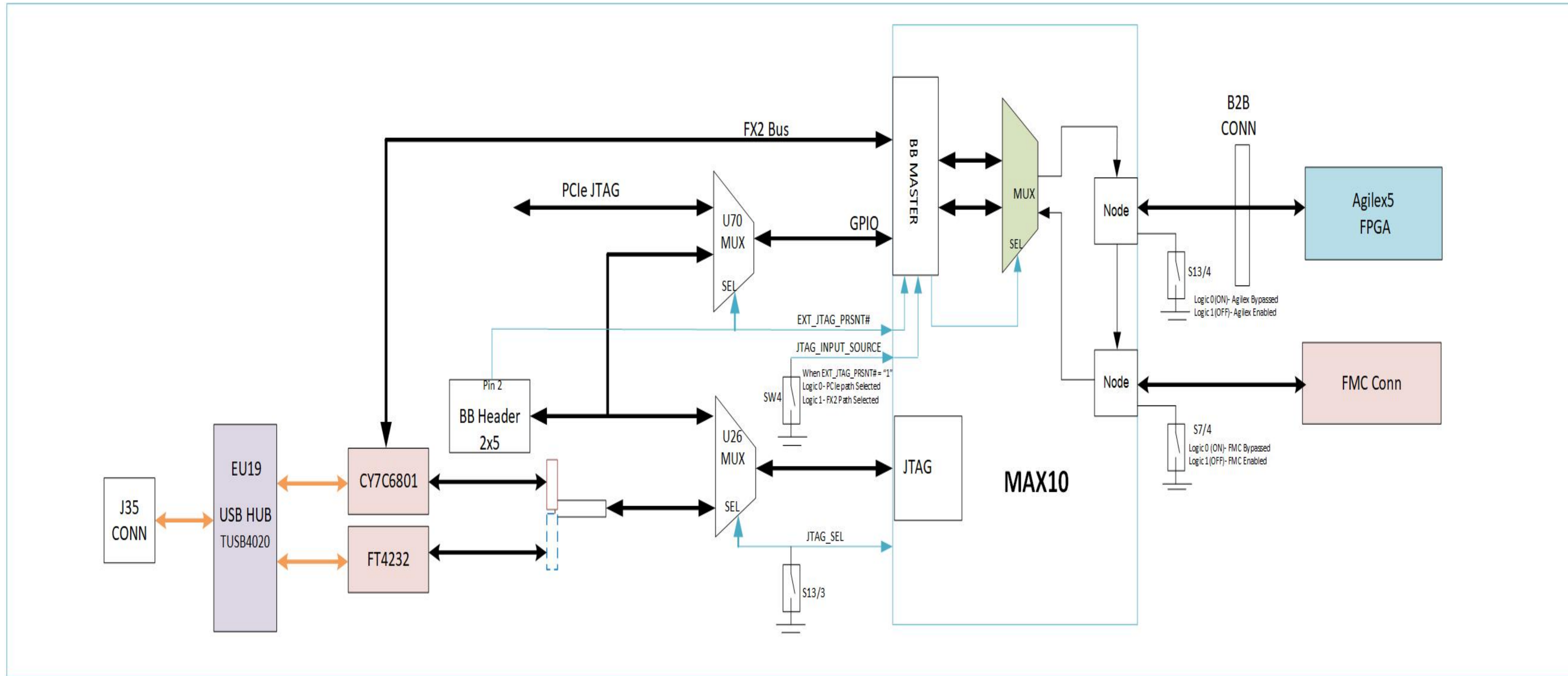
|            |                     |
|------------|---------------------|
| Power VRs  | B2B Primary         |
| Telemetry  | Clock               |
| Connectors | Buffers/Isolator/LT |

M: Master  
S: Slave

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# I2C TREE

|            |                         |                      |       |                 |         |
|------------|-------------------------|----------------------|-------|-----------------|---------|
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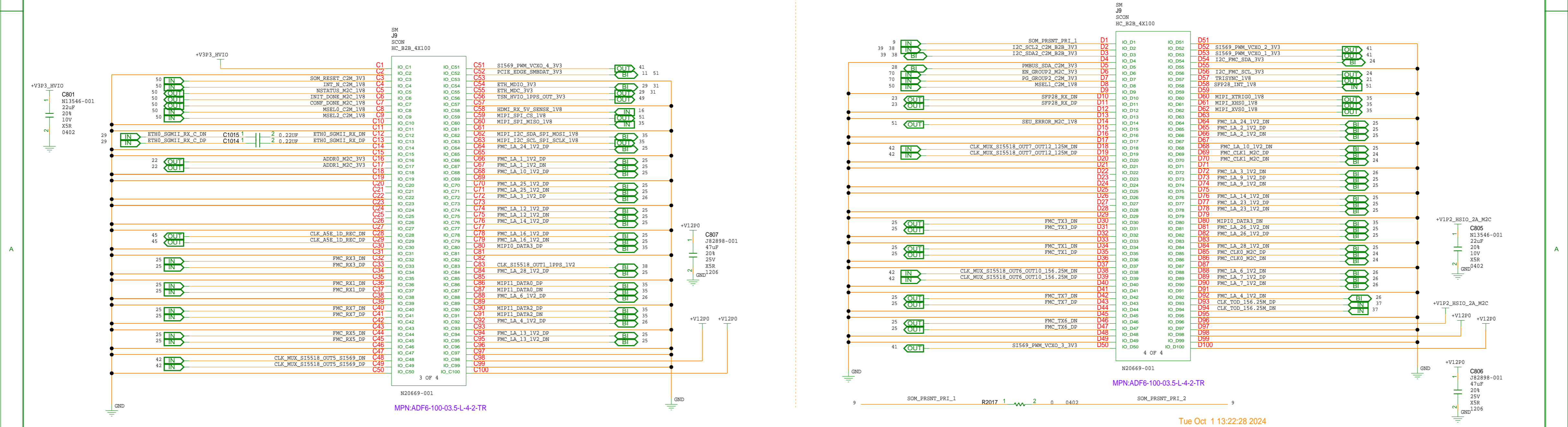
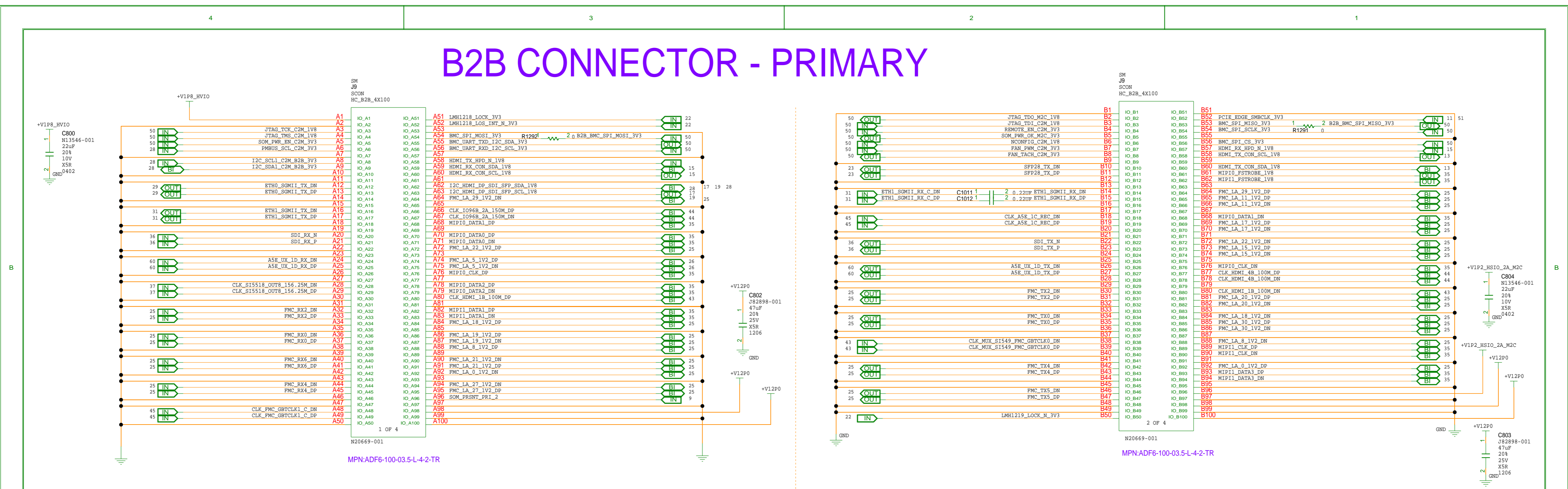
# JTAG TREE

Tue Oct 1 11:16:34 2024

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|            |   | C+                   | 34649 | 150-330724-B1   | 2.0     |
| SCALE:     |   | DO NOT SCALE DRAWING |       | SHEET           | 8 OF 74 |



# B2B CONNECTOR - PRIMARY

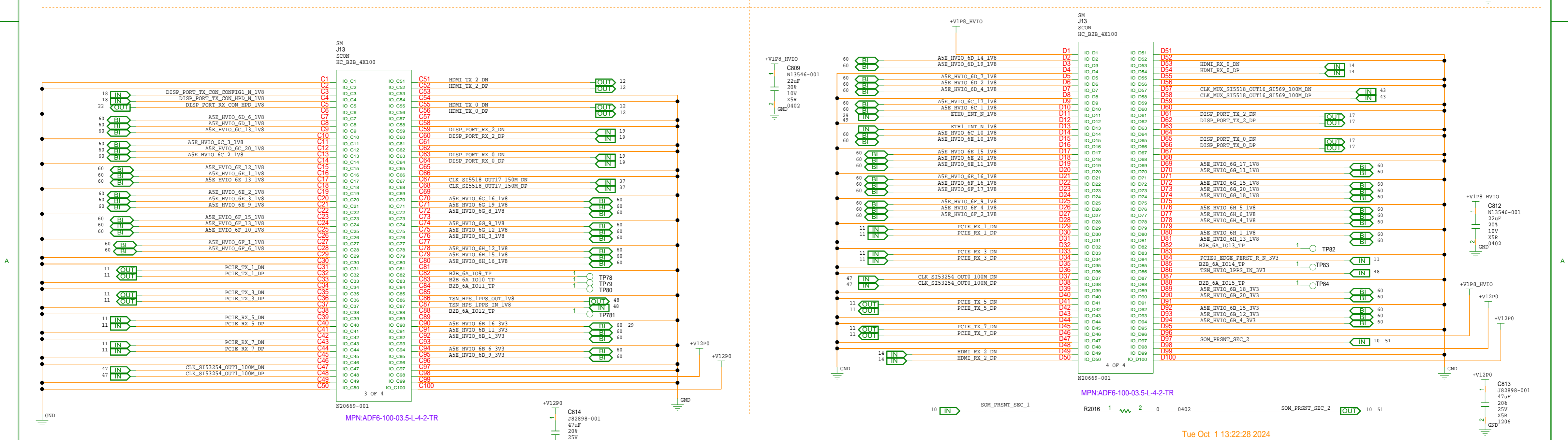
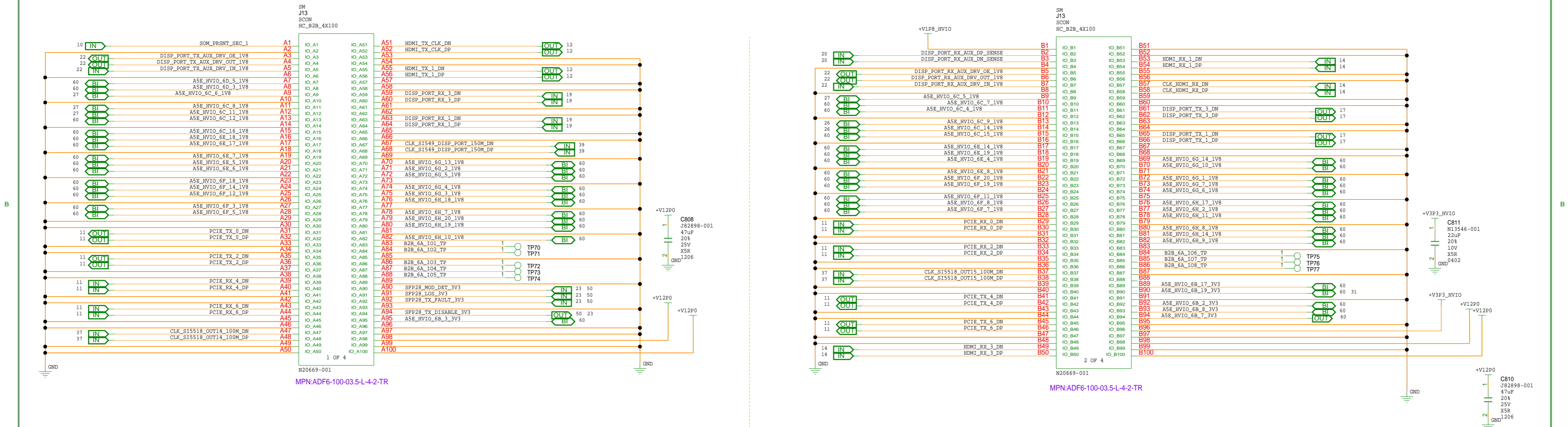


## B2B CONN-PRIMARY

|            |                            |                      |               |                                  |            |
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| SCALE:     |                            | DO NOT SCALE DRAWING |               | SHEET<br>9 OF 74                 |            |

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# B2B CONNECTOR - SECONDARY

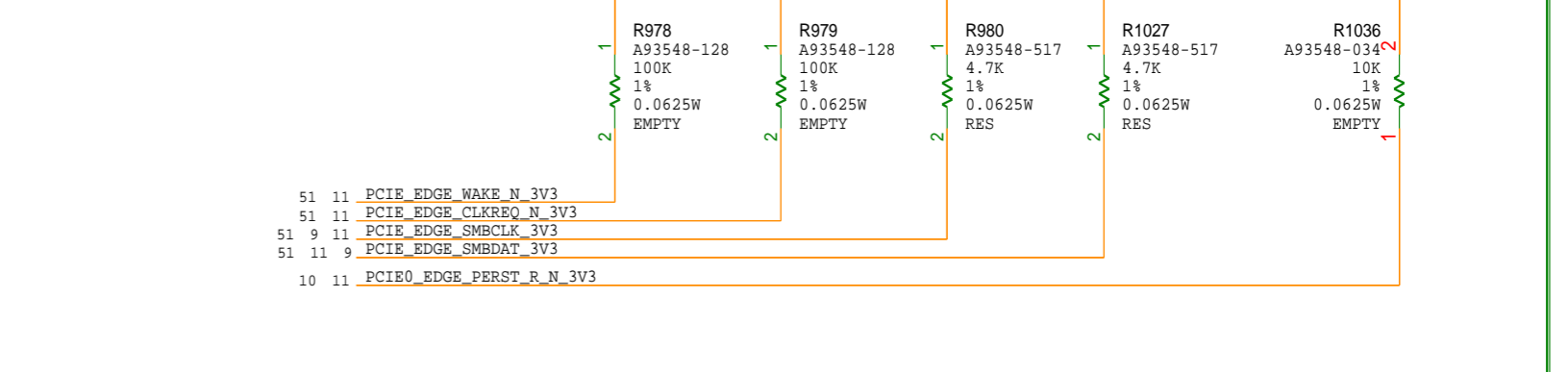
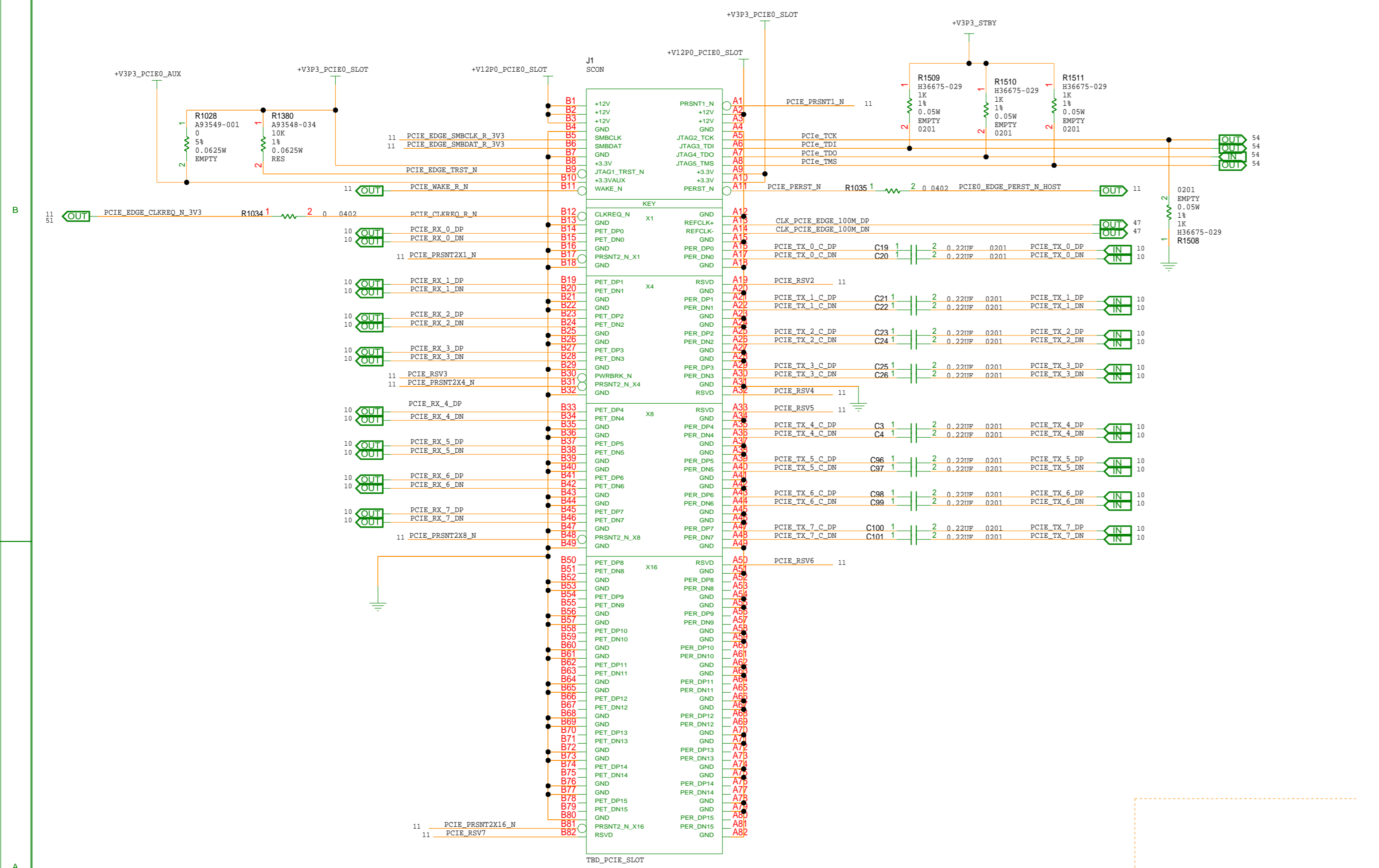


B2B CONN-SECONDARY

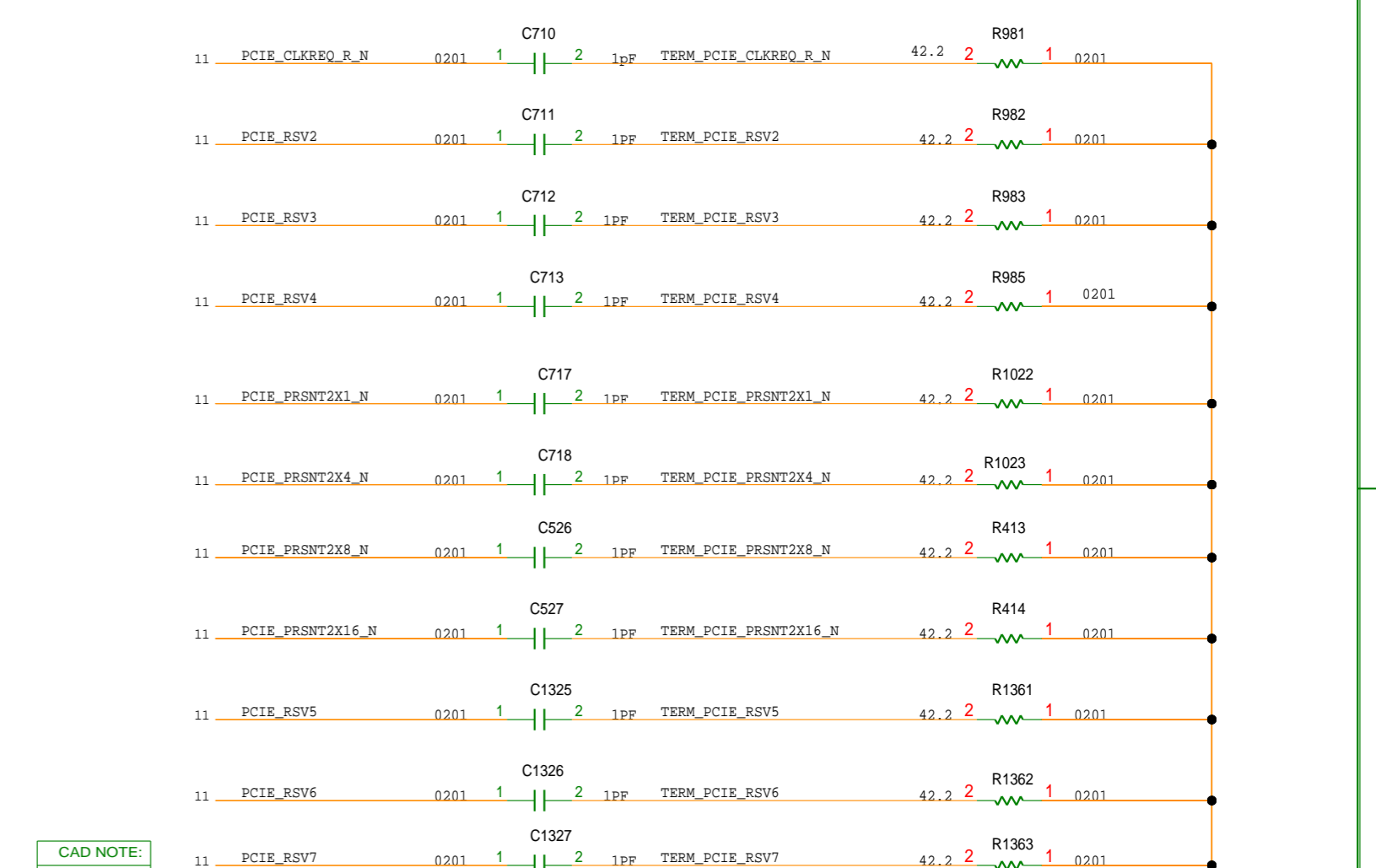
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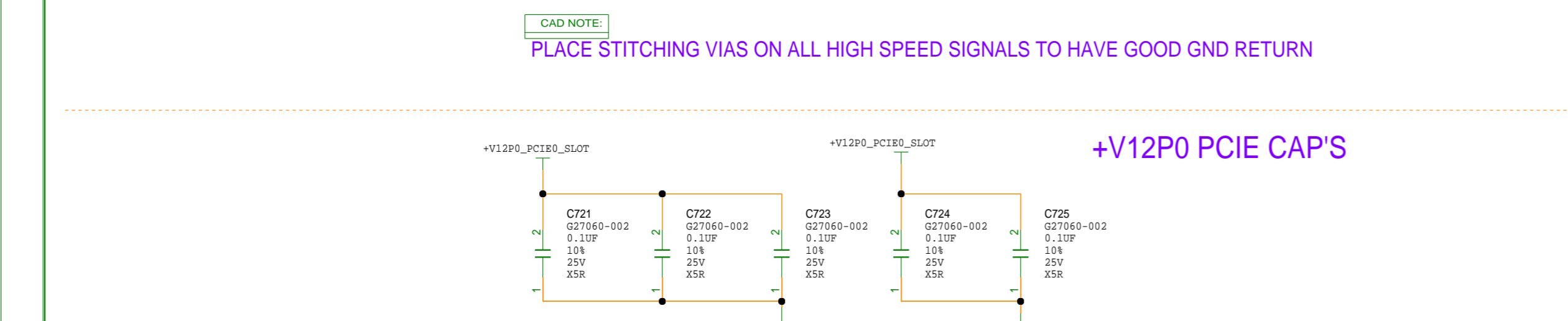
# PCIE EDGE GOLD FINGER



## AC MATCH TERMINATION FOR AUXILIARY SIGNALS

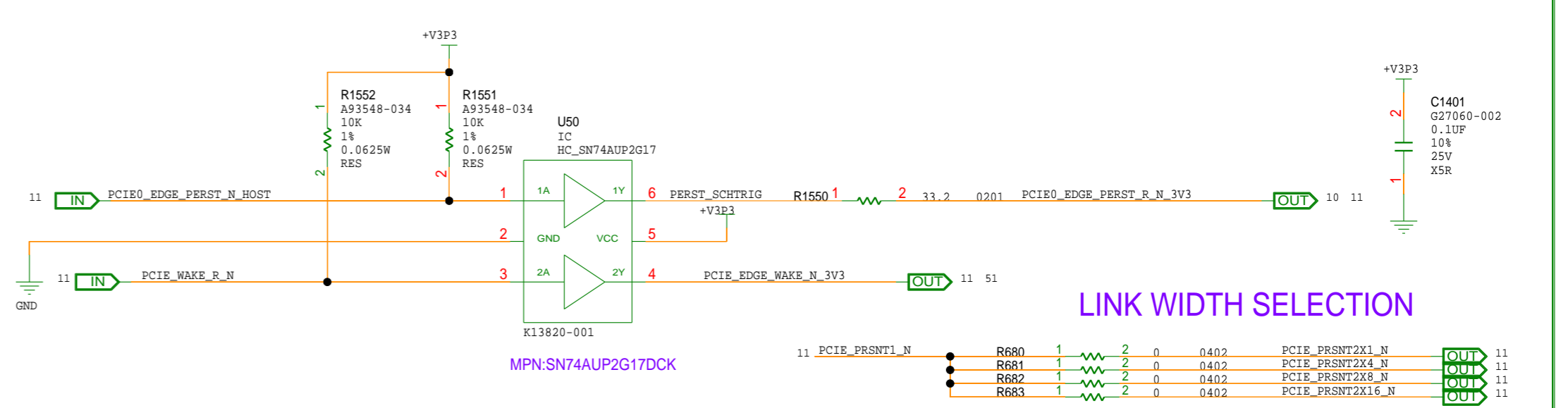


CAD NOTE:  
PLACE NEAR PCIE GOLD FINGER. MAX.500MIL AWAY.  
ENSURE NO STUBS ON PRIMARY ROUTING PATHS.



CAD NOTE:  
PLACE STITCHING VIAS ON ALL HIGH SPEED SIGNALS TO HAVE GOOD GND RETURN

## +V12P0 PCIe CAP'S



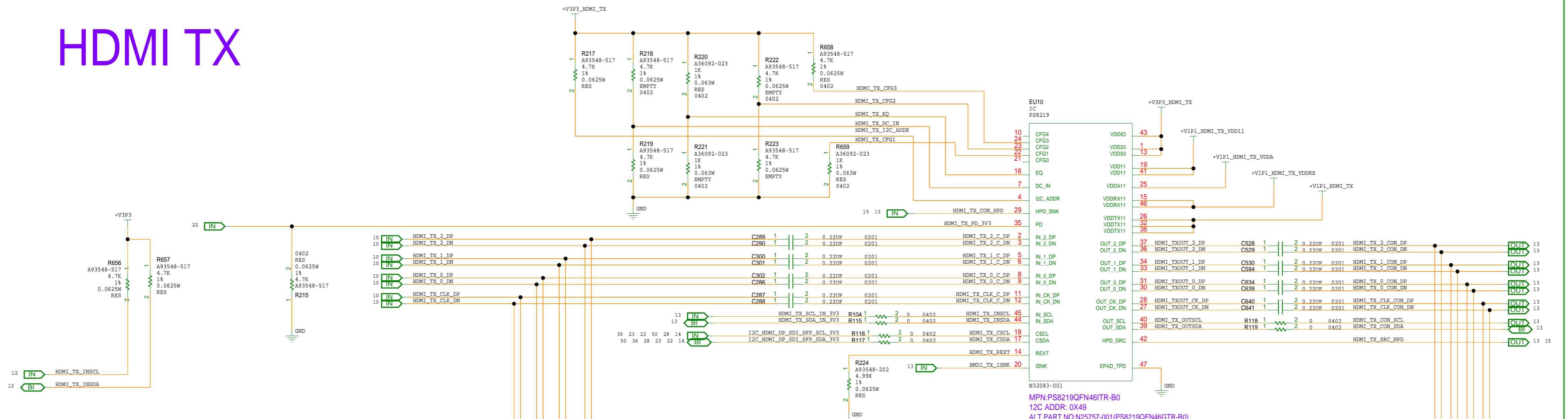
## LINK WIDTH SELECTION

Tue Oct 1 13:22:28 2024

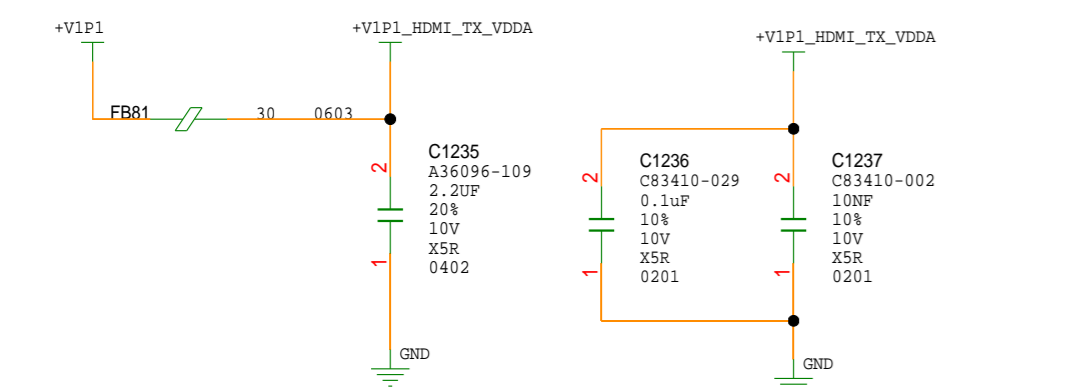
# PCIE X16

|            |                            |                      |       |                 |          |
|------------|----------------------------|----------------------|-------|-----------------|----------|
| DEPARTMENT | altera<br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV      |
|            |                            | C+                   | 34649 | 150-330724-B1   | 2.0      |
| SCALE:     |                            | DO NOT SCALE DRAWING |       | SHEET           | 11 OF 74 |

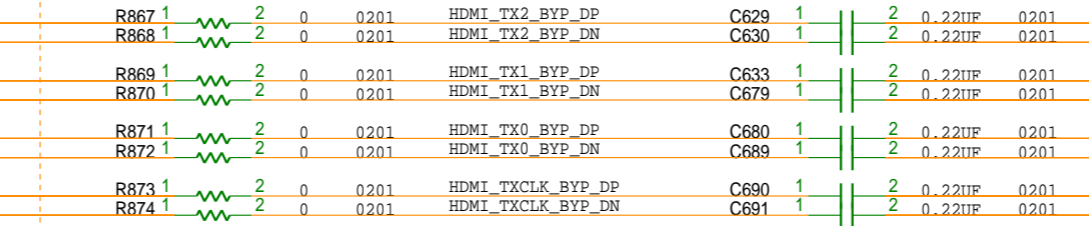
# HDMI TX



## +V1P1\_VDDA SUPPLY DE-CAP



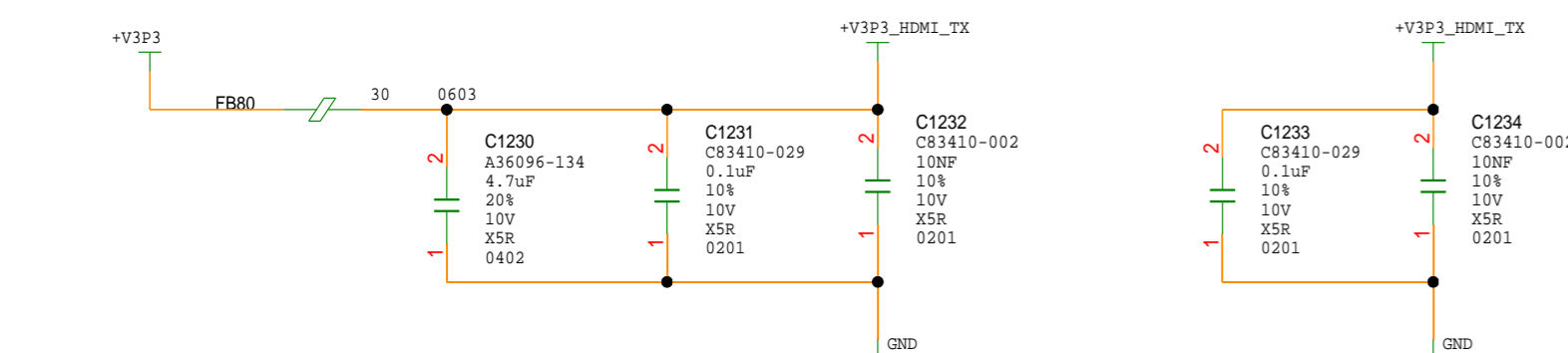
## HDMI TX REDRIVER BYPASS PATH



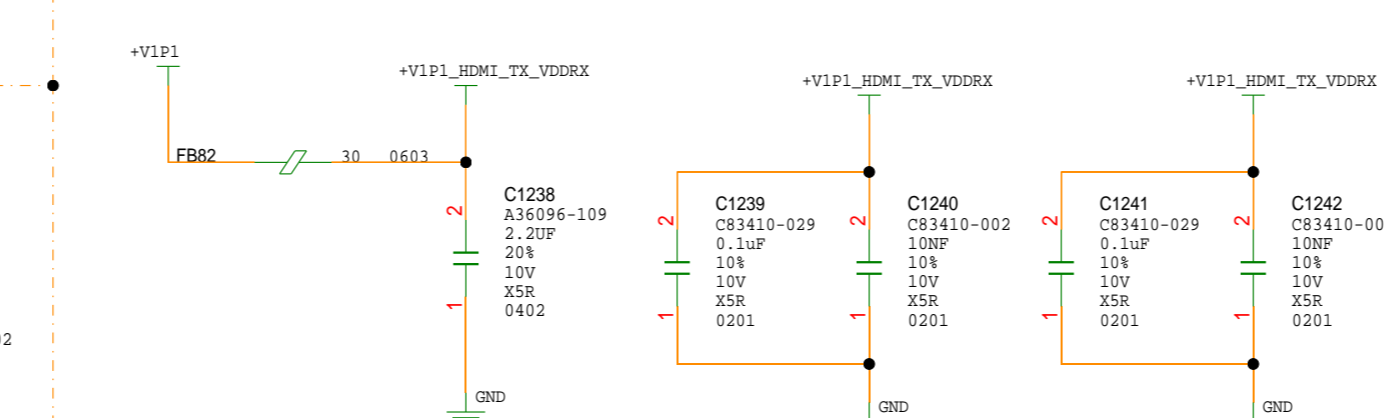
## TRIPAD OPTION TO BYPASS HDMI TX OUTPUT

|         | REDRIVER PATH  | BYPASS PATH  |
|---------|--|--|
| MOUNT   | R104&R105<br>C289, C290, C300, C301, C302, C286, C287, C288<br>C528, C529, C530, C594, C634, C639, C640, C641    | R867, R868 AND C629, C630<br>R869, R870 AND C633, C679<br>R871, R872 AND C680, C689<br>R873, R874 AND C690, C691 |
| UNMOUNT | R867, R868 AND C629, C630<br>R869, R870 AND C633, C679<br>R871, R872 AND C680, C689<br>R873, R874 AND C690, C691 | R104&R105<br>C289, C290, C300, C301, C302, C286, C287, C288<br>C528, C529, C530, C594, C634, C639, C640, C641    |

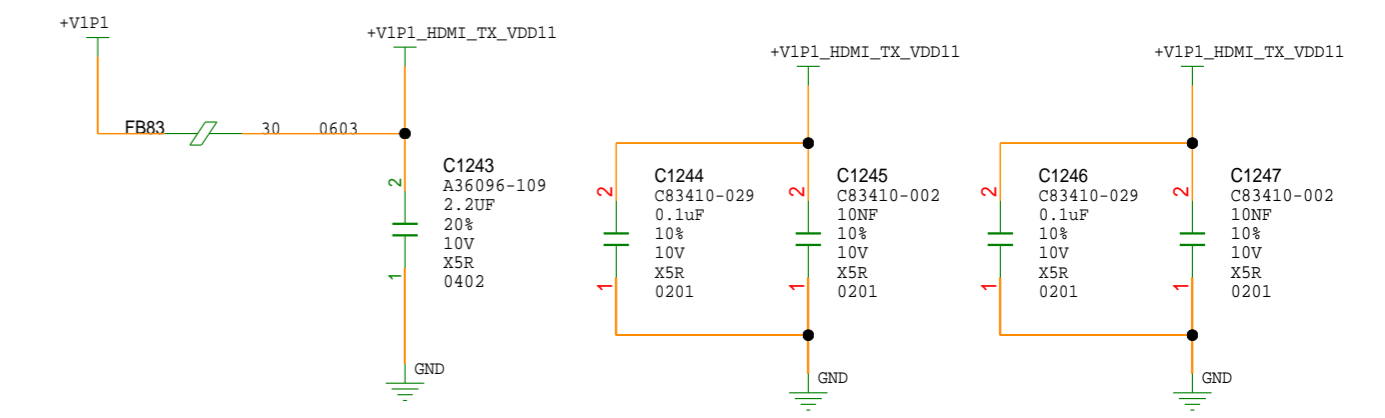
## +V3P3\_TX SUPPLY DE-CAP



## +V1P1\_TX\_VDDRX SUPPLY DE-CAP



## +V1P1\_VDD11 SUPPLY DE-CAP

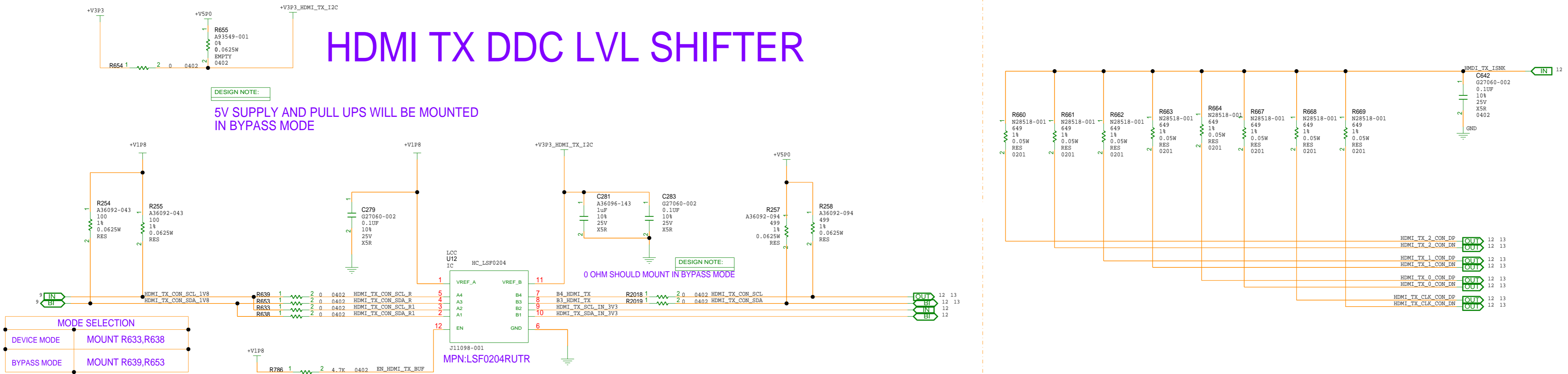


# HDMI TX REDRIVER

|            |                      |      |       |                 |          |
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| DEPARTMENT | <br>An Intel Company | SIZE | CODE  | DOCUMENT NUMBER | REV      |
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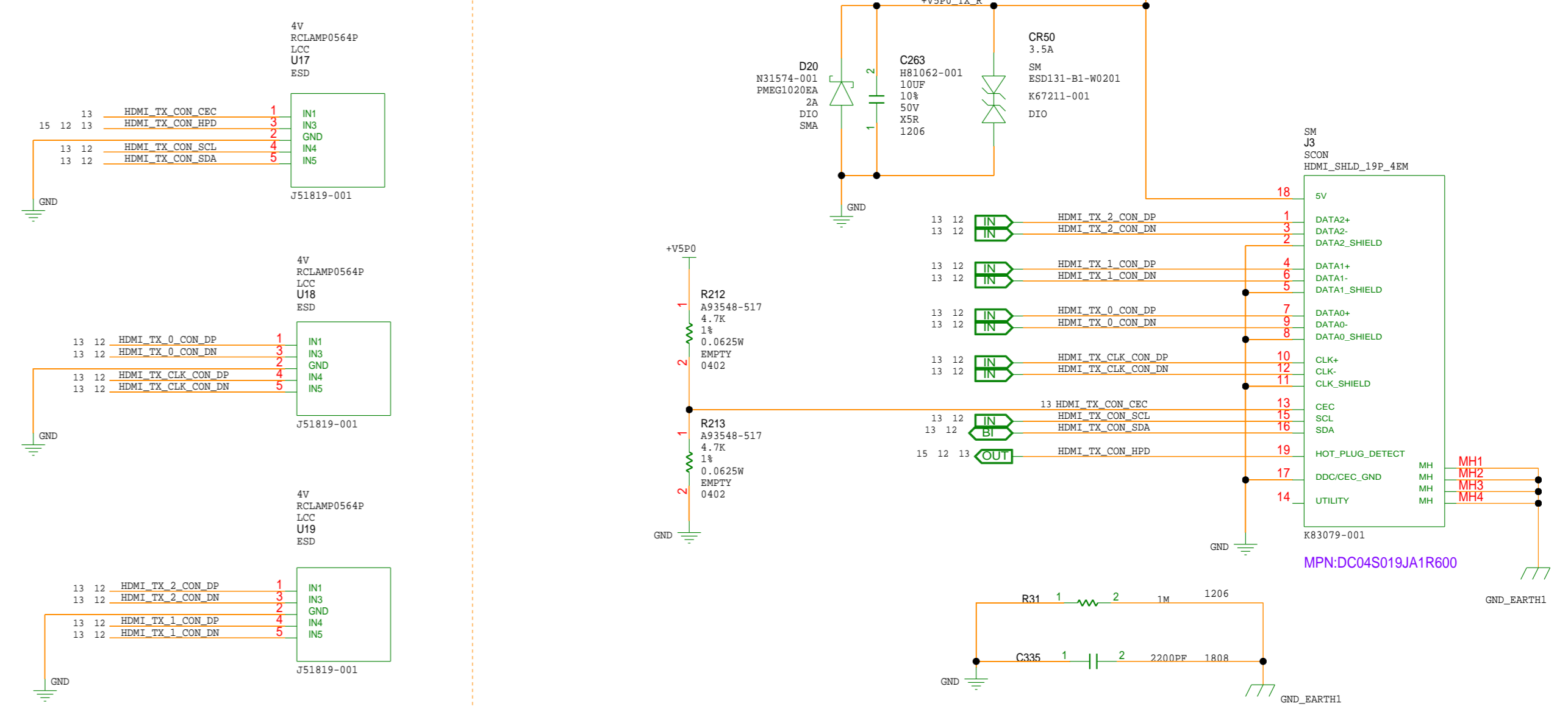
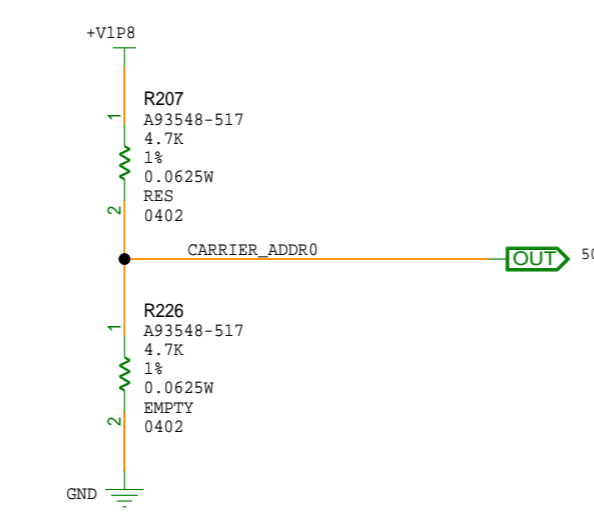
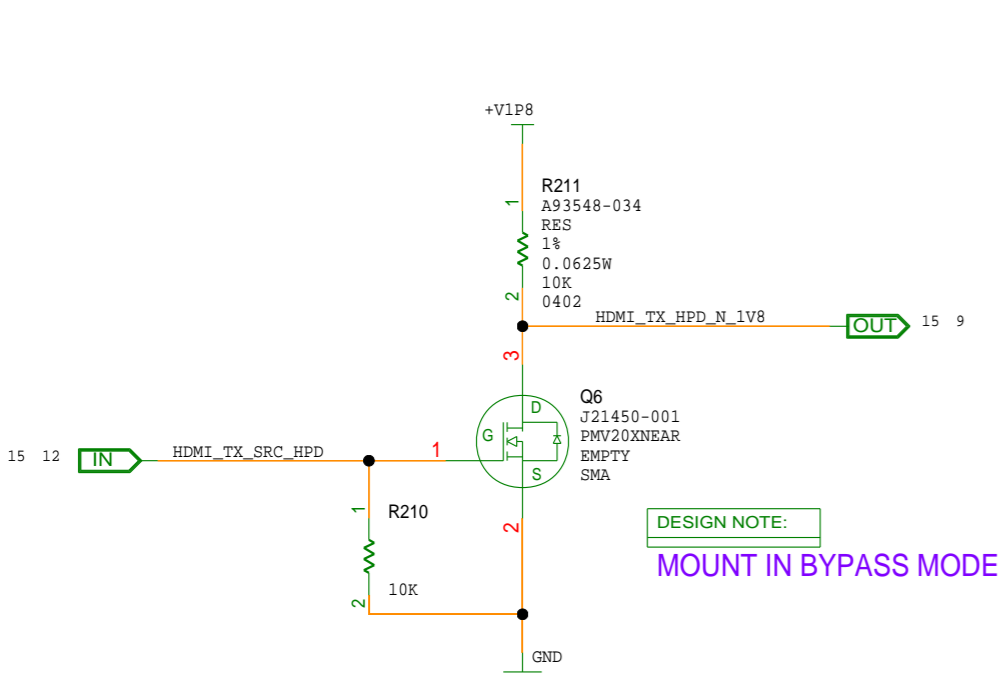
Tue Oct 1 13:22:29 2024

# HDMI TX DDC LVL SHIFTER



# HDMI ESD & TX CONNECTOR

## HDMI TX HPD SENSE

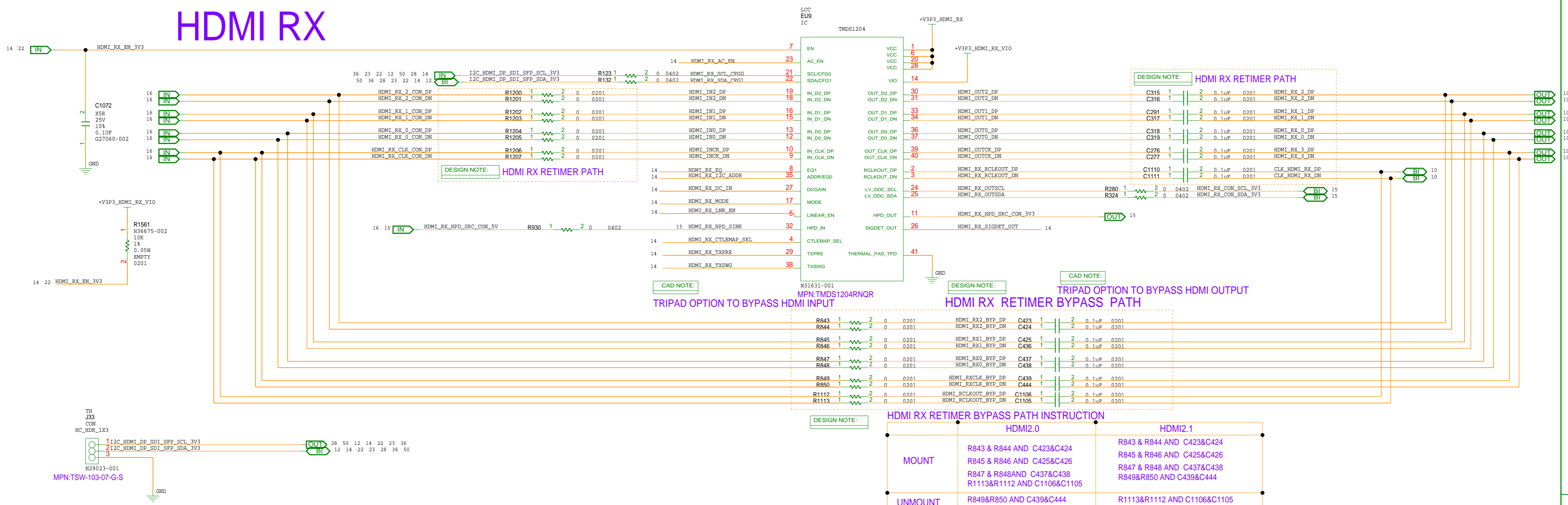


# HDMI TX CONTROL

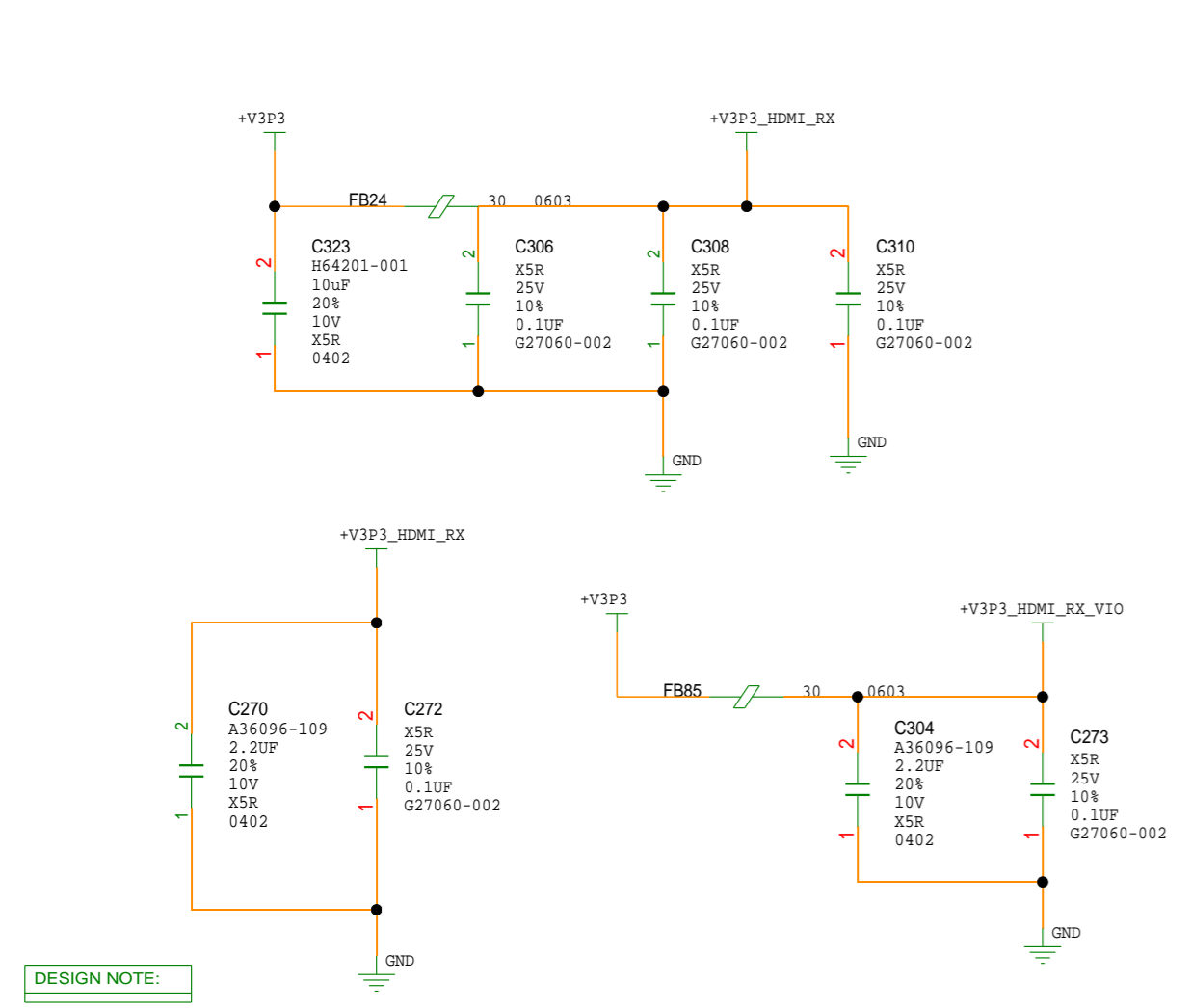
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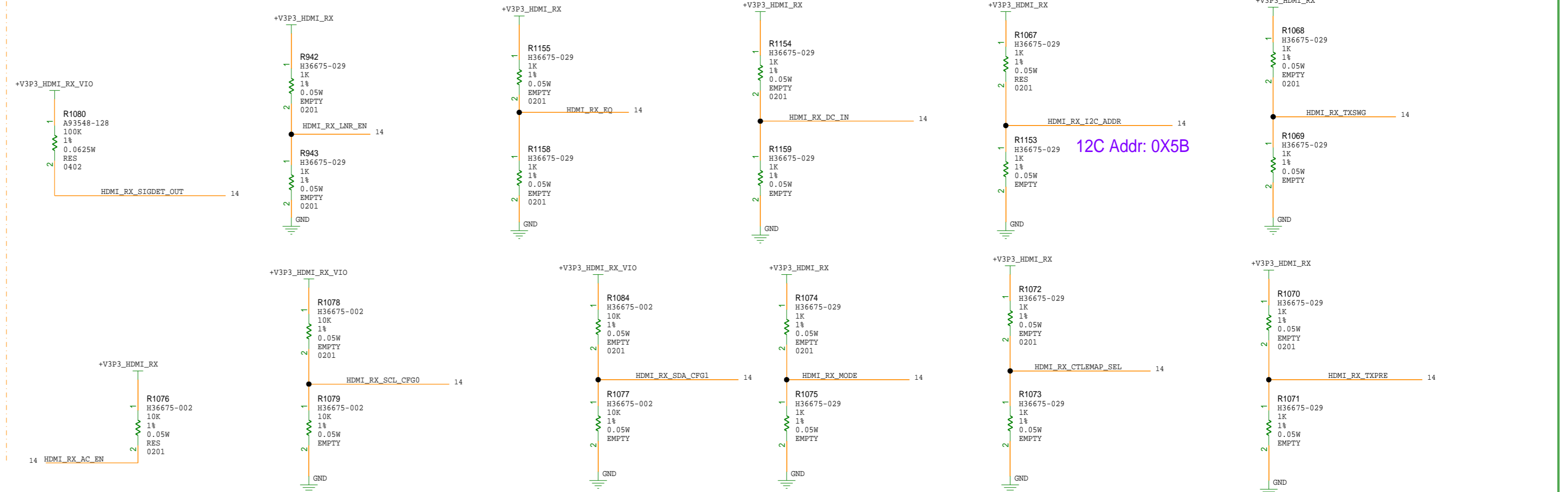
# HDMI RX



## SUPPLY DE-CAP



## TMS1204 CONTROL LINES SETTINGS



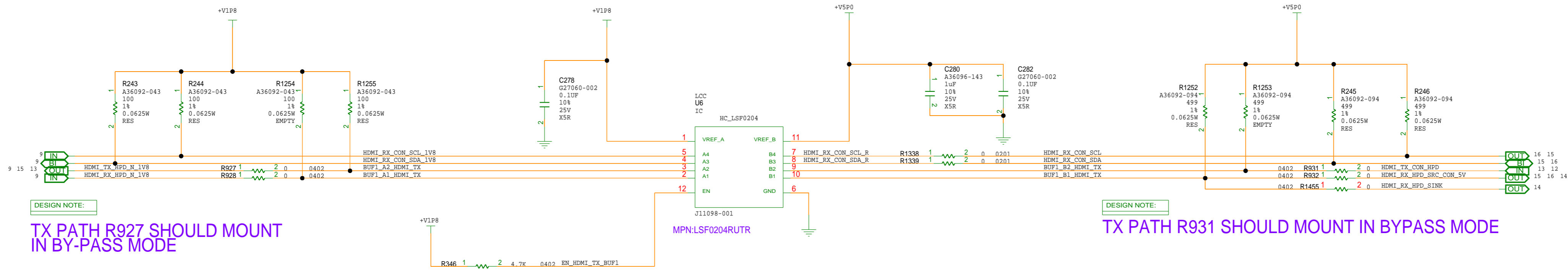
I2C MODE IS SELECTED & ALL EQ, SWING AND OTHER FEATURES CAN SELECT THROUGH INTERNAL REGISTERS

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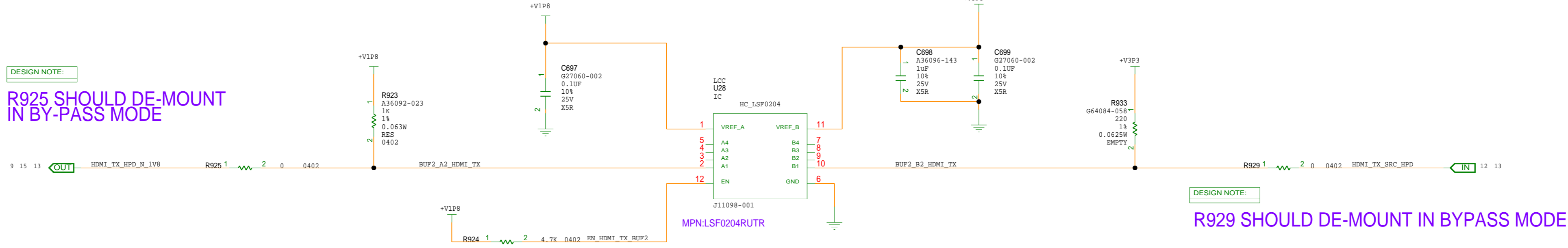
# HDMI RX RETIMER

|            |                      |                      |       |                 |                |
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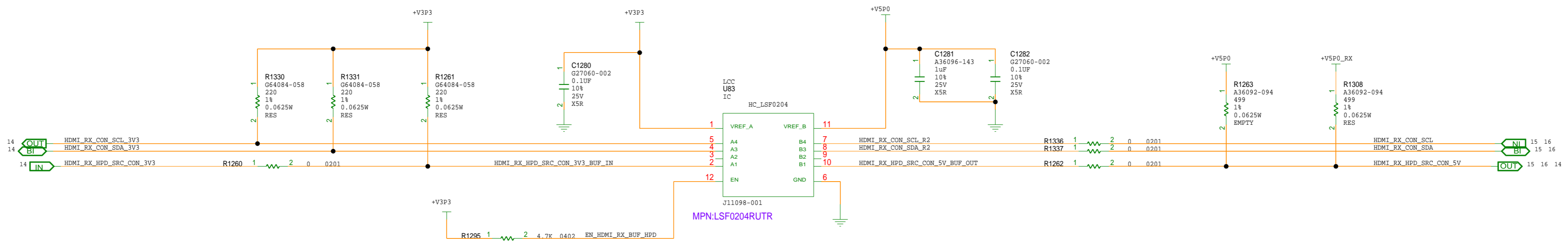
# HDMI RX DDC AND HPD BYPASS CONTROL



## HDMI TX HPD 3V3 TO 1V8



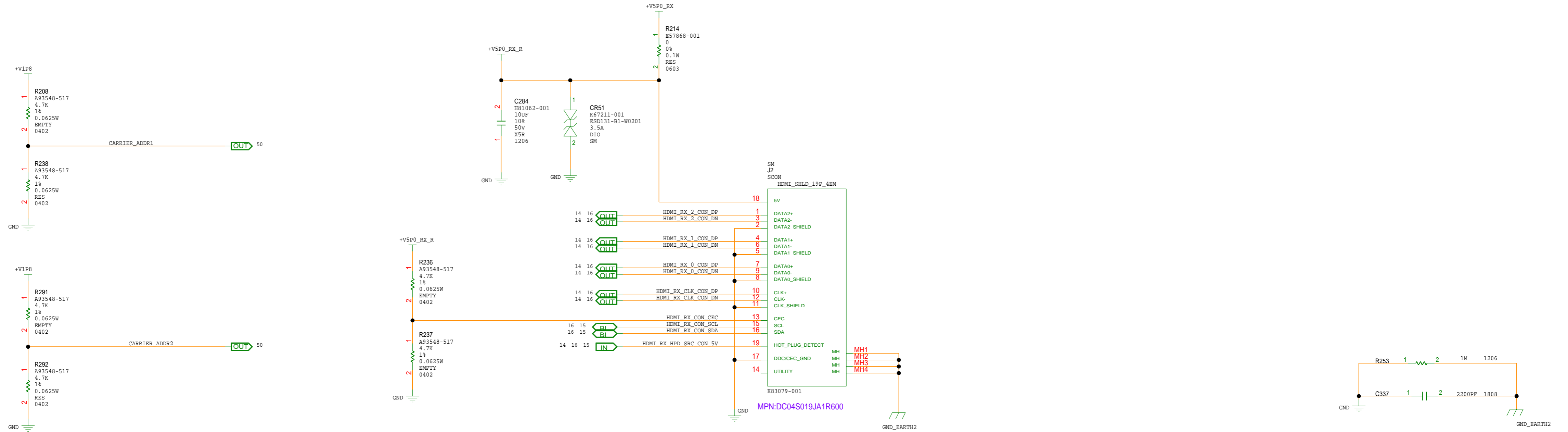
## HDMI RX HPD & DDC (3V3 TO 5V)



Tue Oct 1 13:22:29 2024

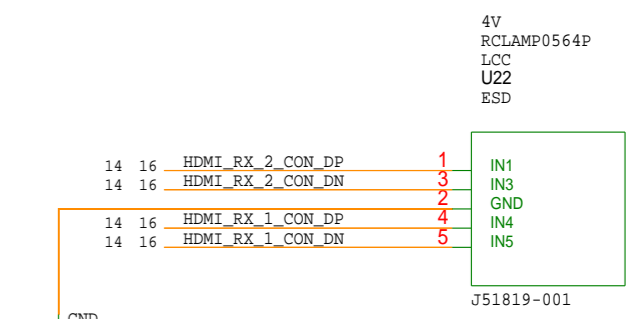
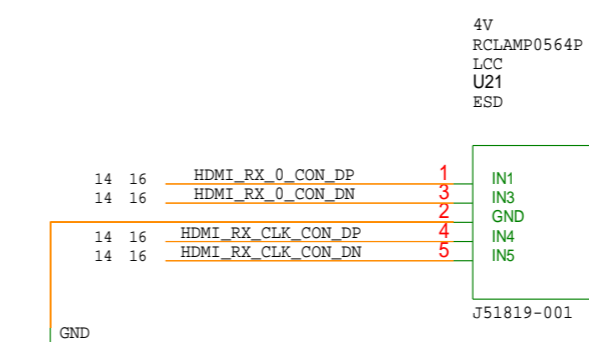
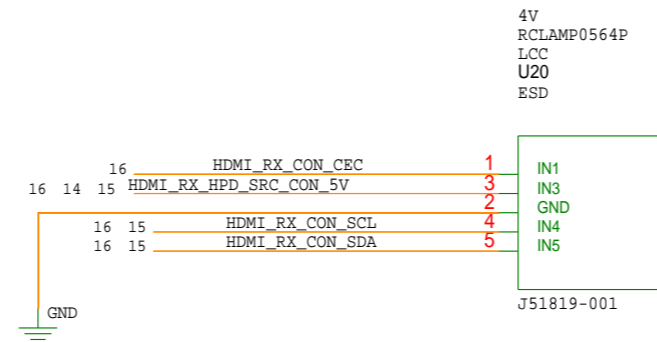
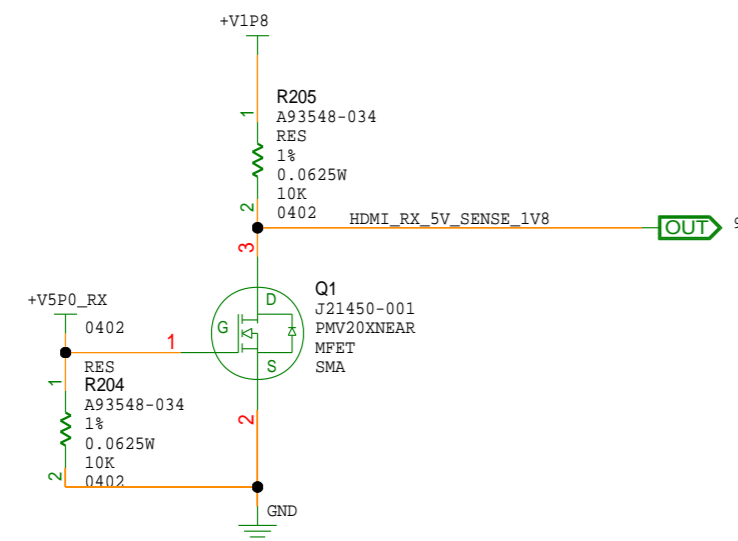
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|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0      |
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# HDMI RX CONNECTOR



## ESD

### HDMI RX 5V SENSE



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# HDMI RX CONNECTOR

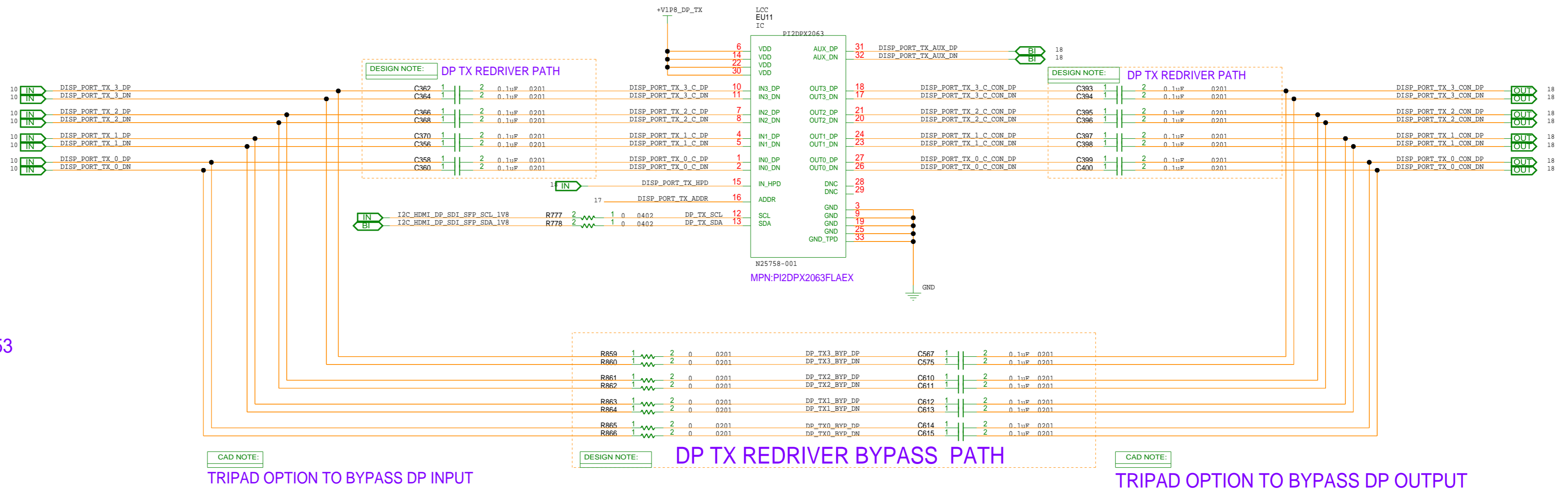
DEPARTMENT



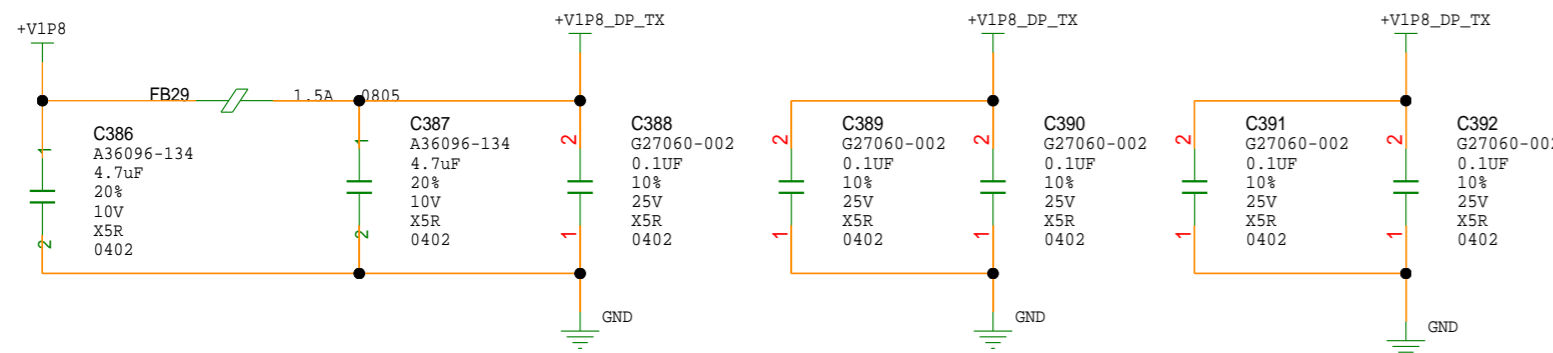
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| SCALE: | DO NOT SCALE DRAWING |                 | SHEET 16 OF 74 |



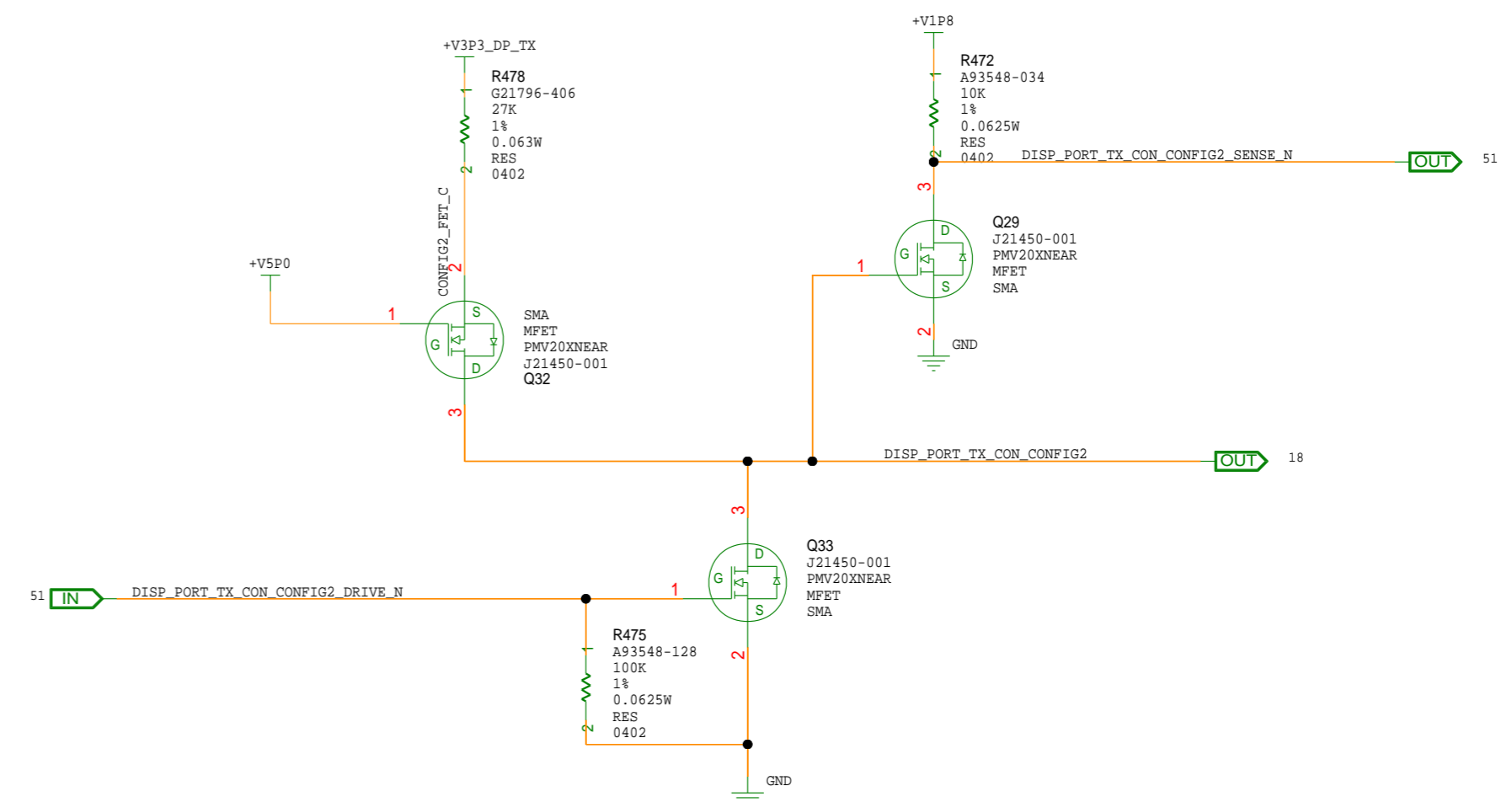
# DP TX



## SUPPLY DE-CAP



## DP TX CEC SENSE/DRIVE

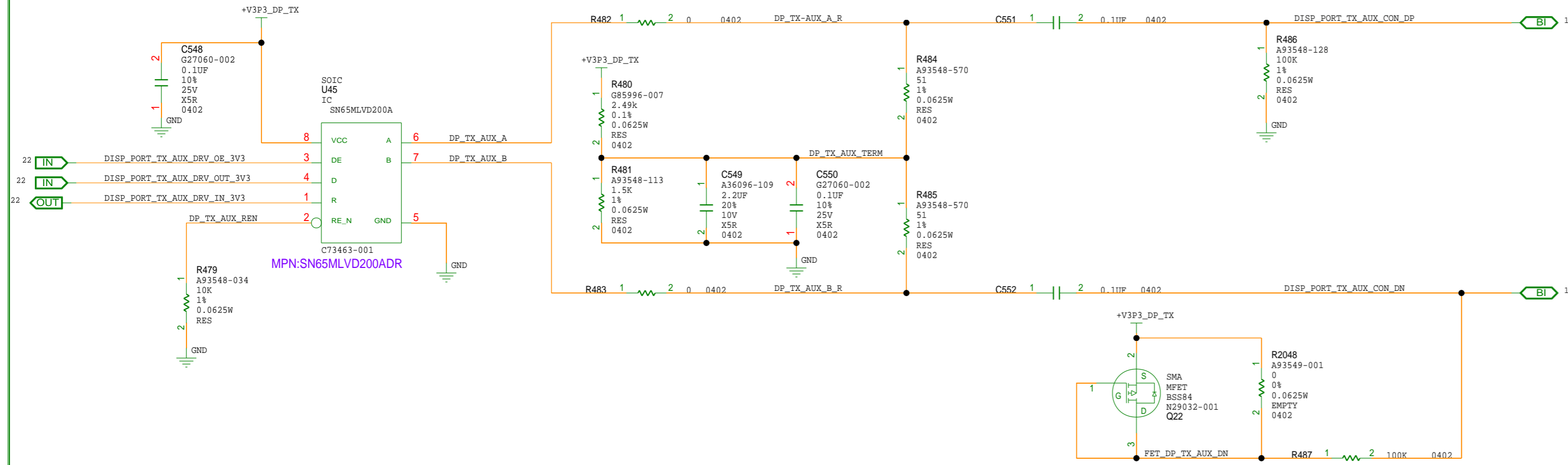


Tue Oct 1 13:22:30 2024

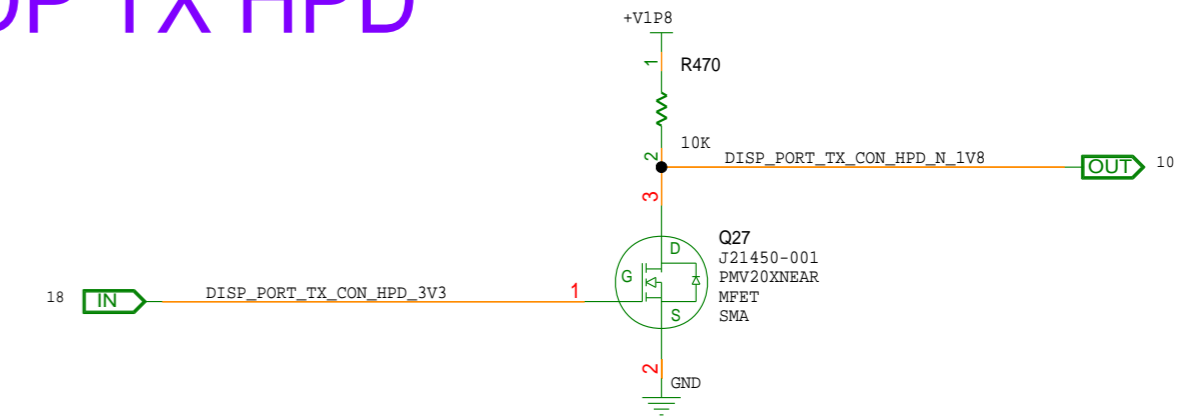
# DP TX REDRIVER

|            |                            |                      |       |                 |          |
|------------|----------------------------|----------------------|-------|-----------------|----------|
| DEPARTMENT | altera<br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV      |
|            |                            | C+                   | 34649 | 150-330724-B1   | 2.0      |
| SCALE:     |                            | DO NOT SCALE DRAWING |       | SHEET           | 17 OF 74 |

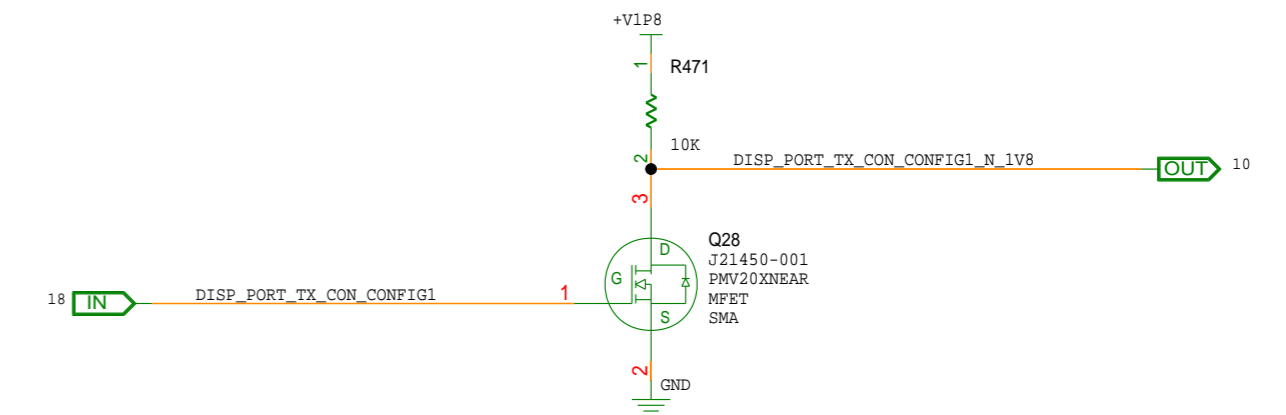
# DP TX AUX



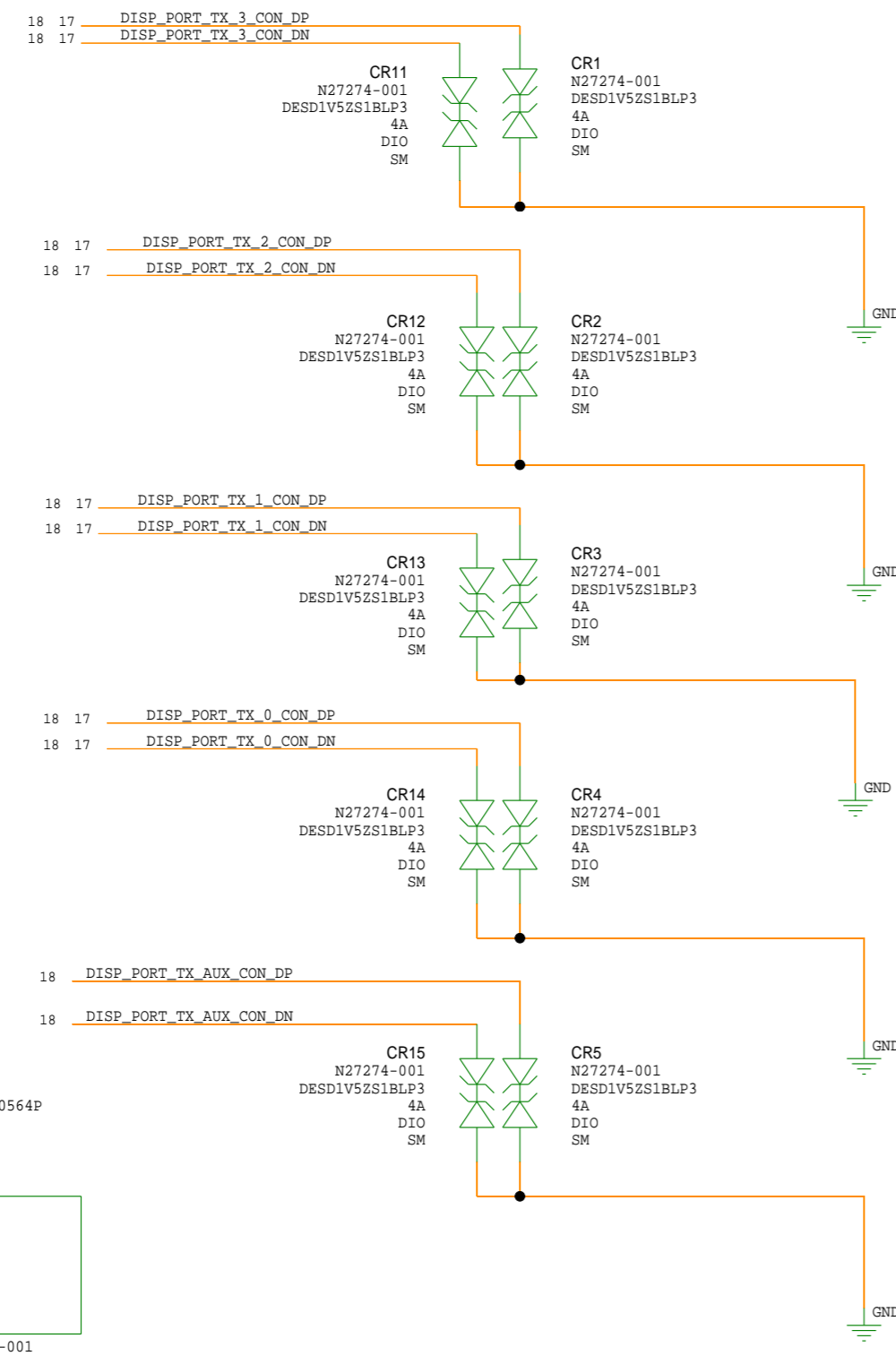
# DP TX HPD



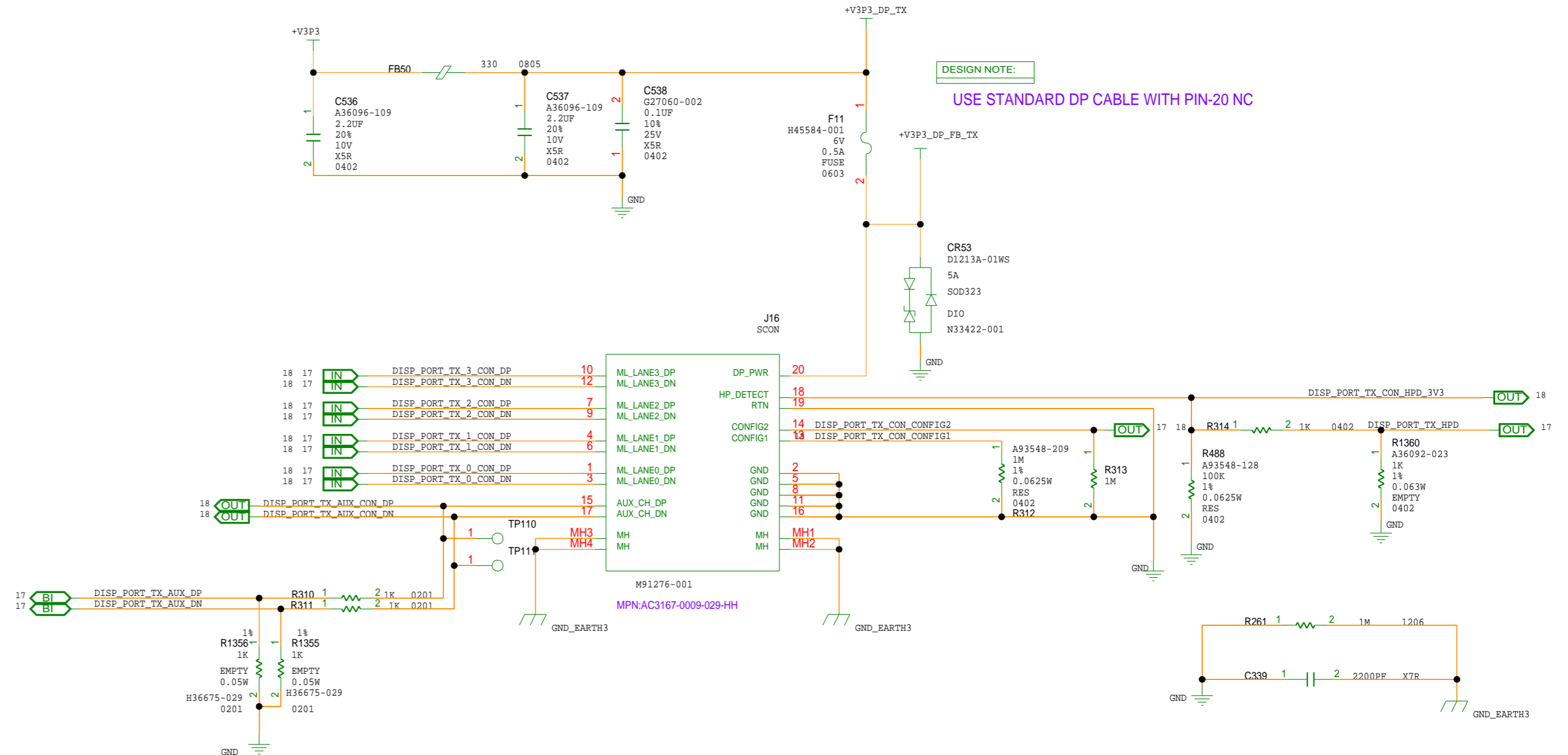
# DP TX CABLE DETECT



# ESD



# DP CONNECTOR

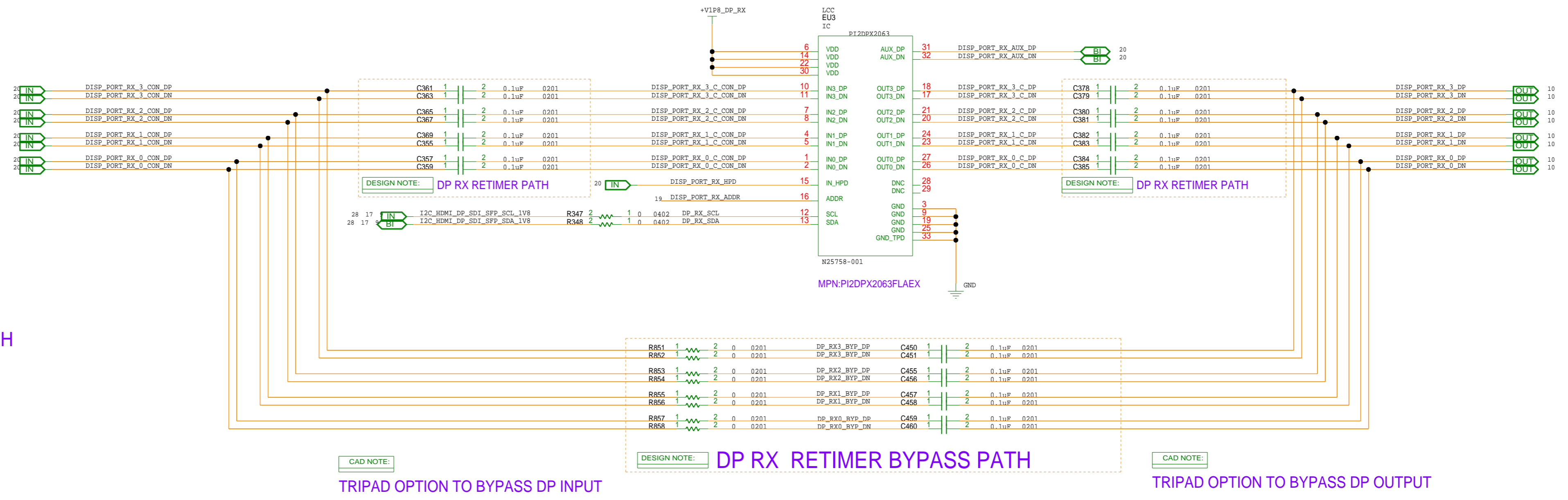


# DP TX CONNECTOR

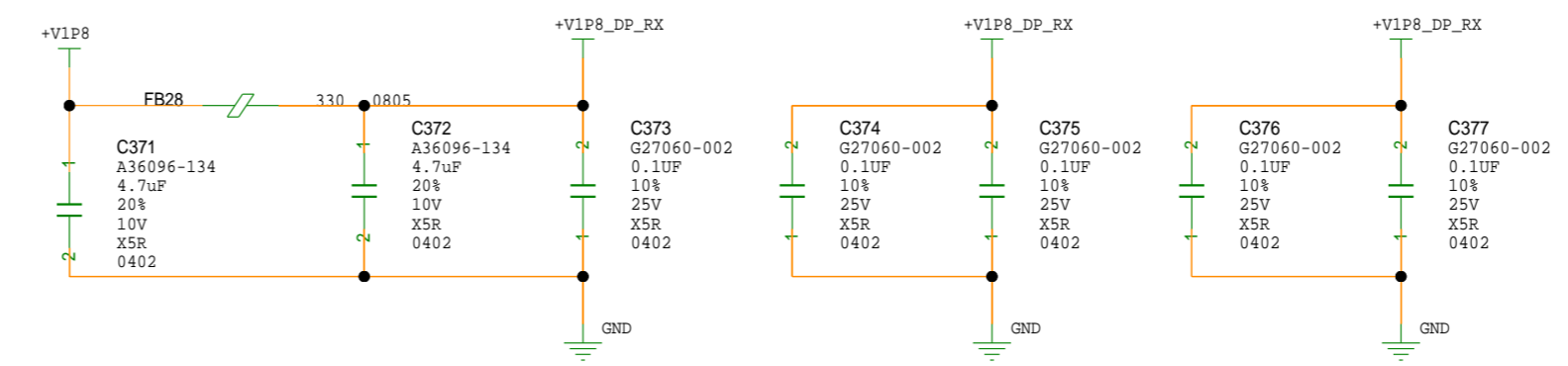
|            |                      |                      |       |                 |                |
|------------|----------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                      | DO NOT SCALE DRAWING |       |                 | SHEET 18 OF 74 |

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# DP RX



# SUPPLY DE-CAP

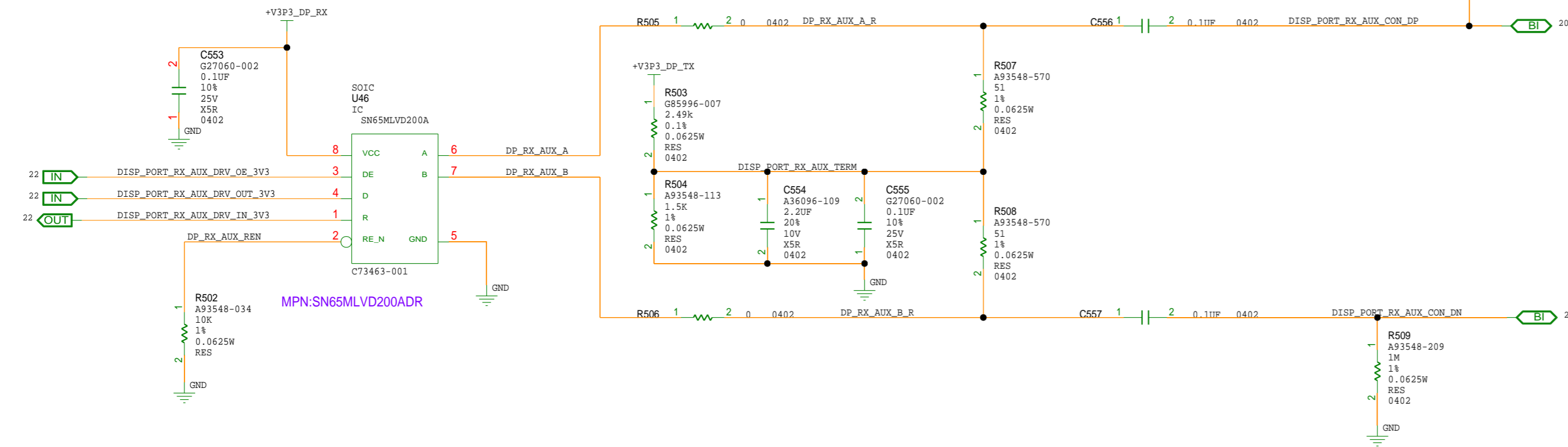


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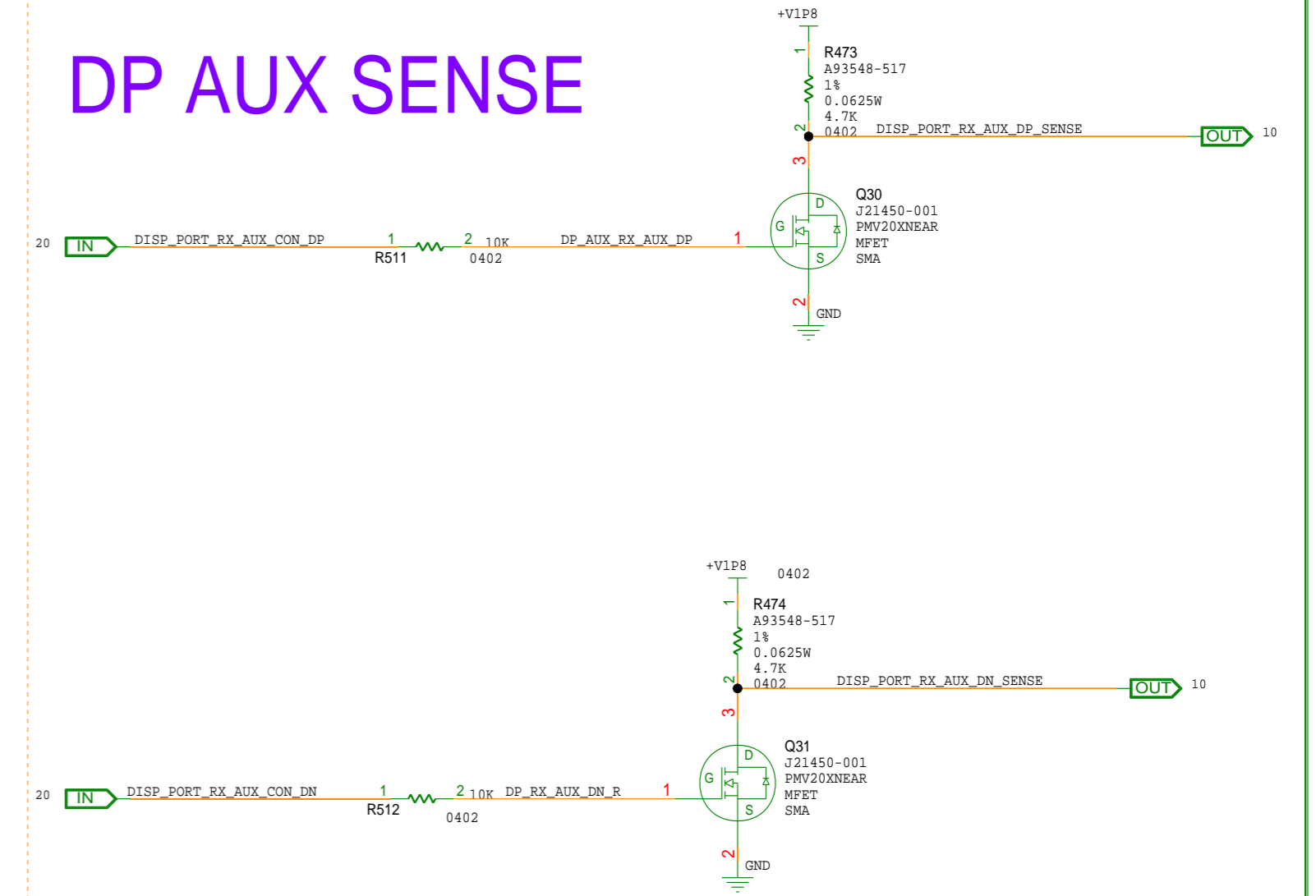
# DP RX REDRIVER

|            |                      |        |                      |                 |                |
|------------|----------------------|--------|----------------------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE   | CODE                 | DOCUMENT NUMBER | REV            |
|            |                      | C+     | 34649                | 150-330724-B1   | 2.0            |
|            |                      | SCALE: | DO NOT SCALE DRAWING |                 | SHEET 19 OF 74 |

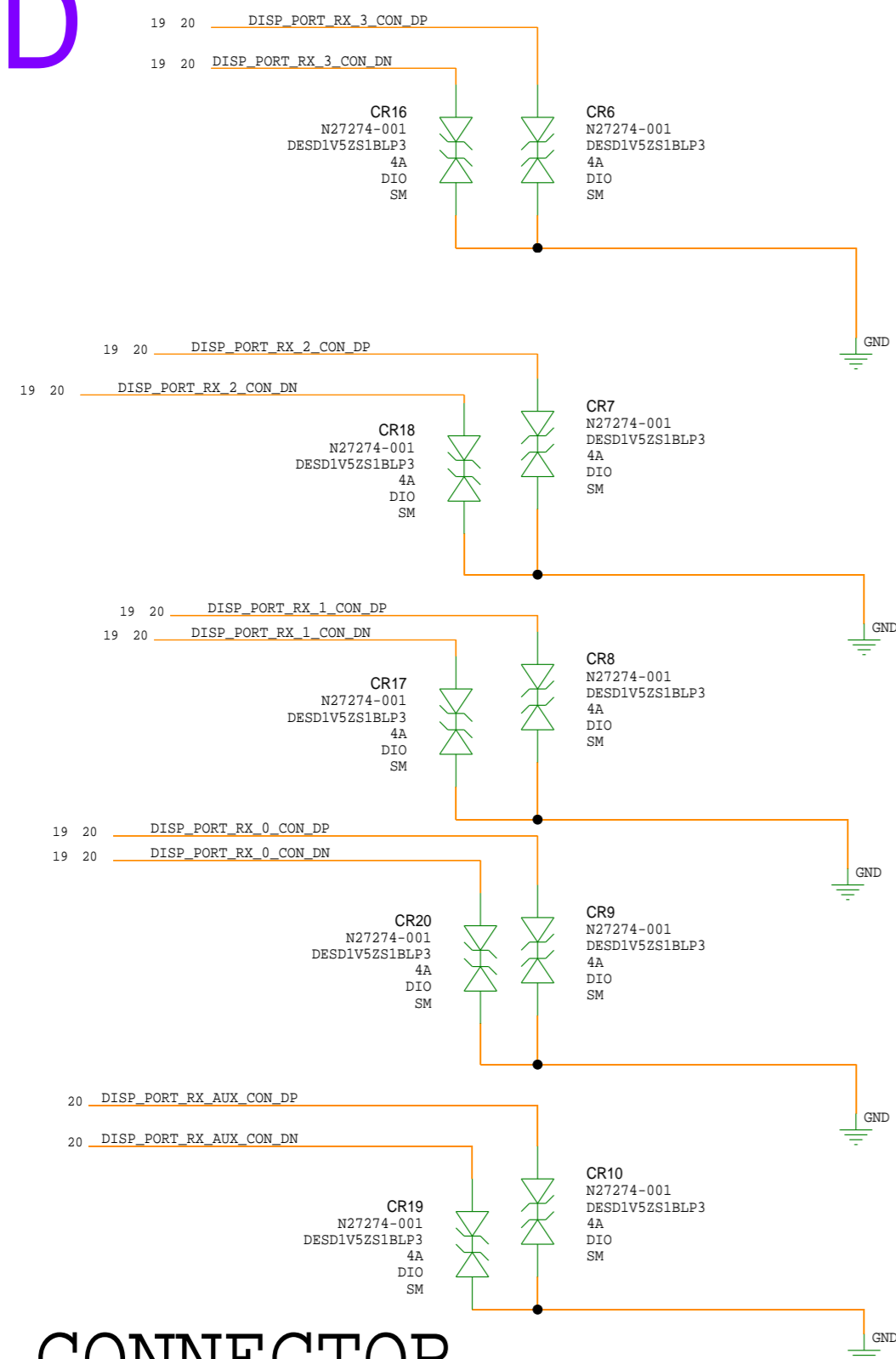
# DP RX AUX



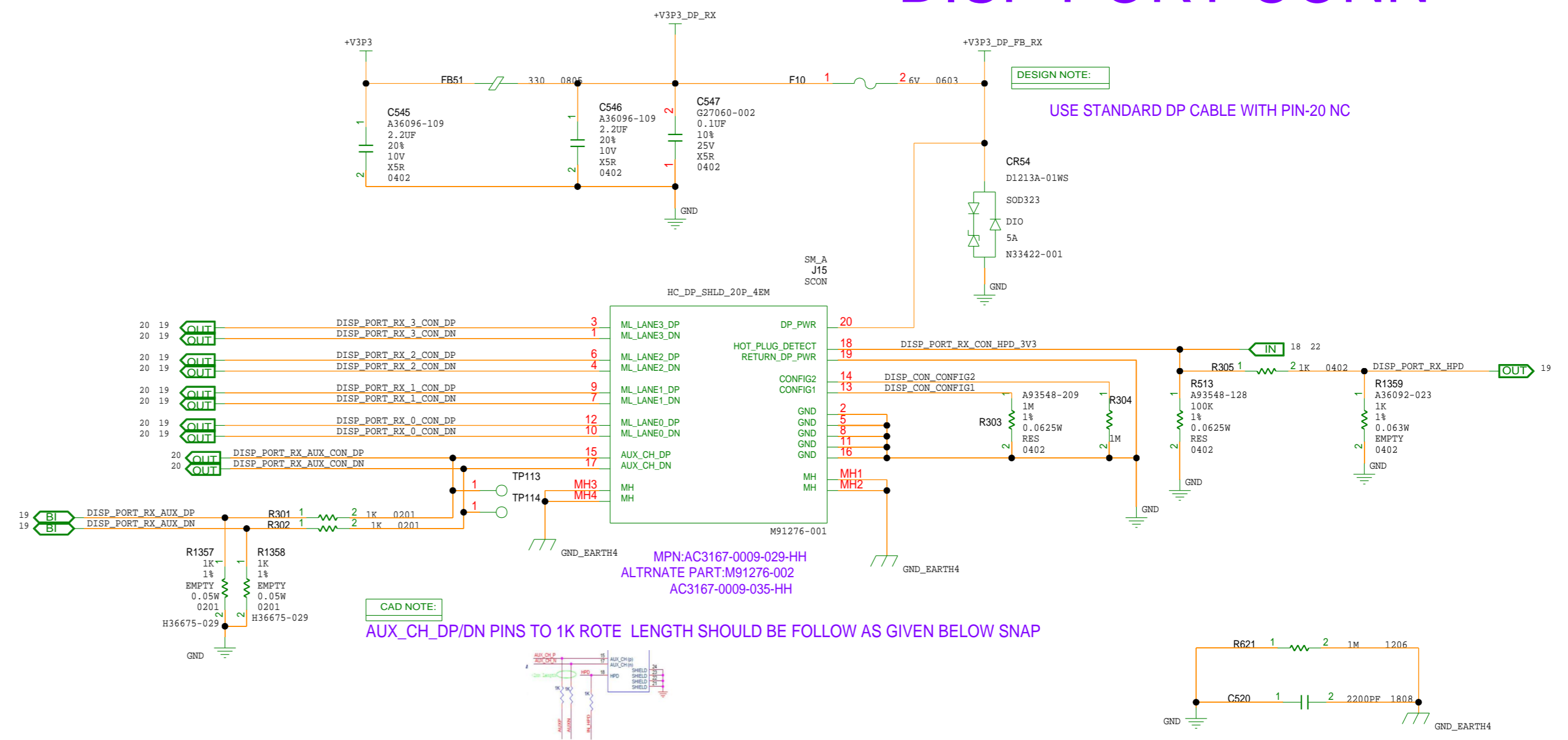
# DP AUX SENSE



# ESD



# DISP PORT CONN

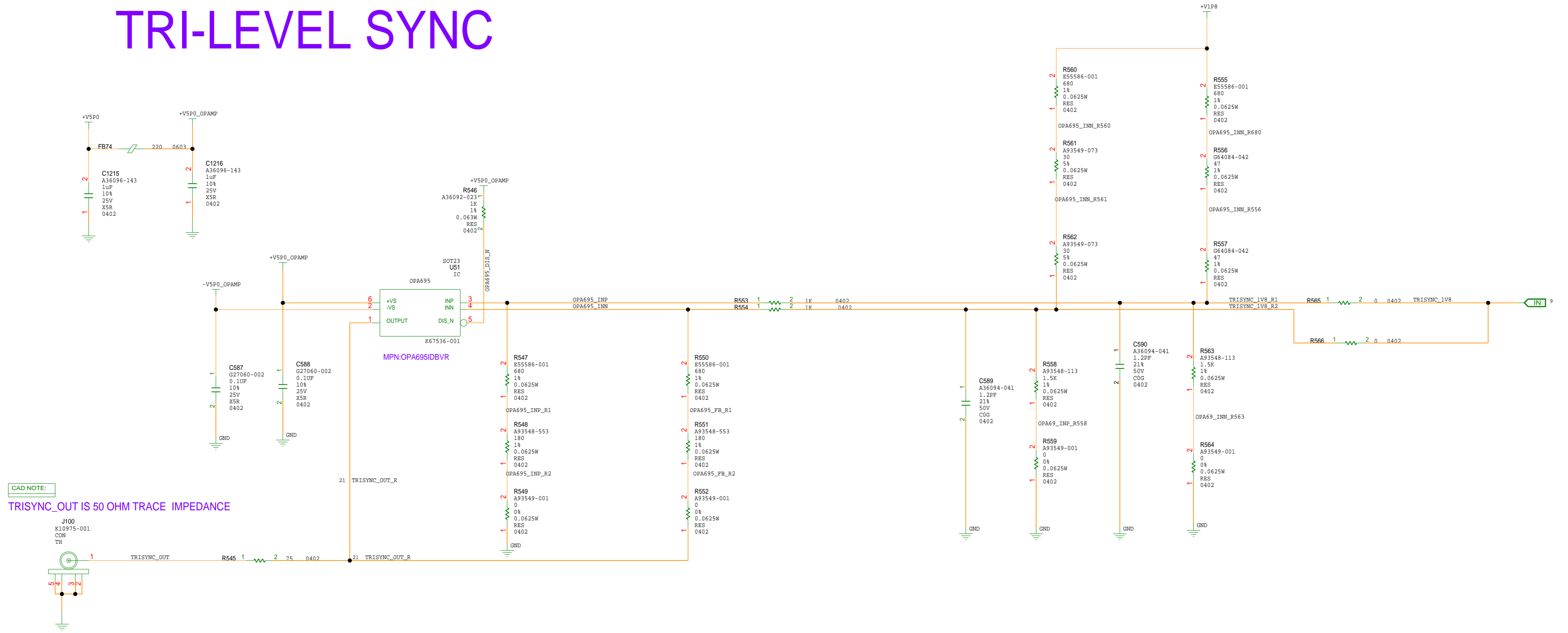


# DP RX CONNECTOR

|            |                      |                      |       |                 |     |
|------------|----------------------|----------------------|-------|-----------------|-----|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0 |
| SCALE:     |                      | DO NOT SCALE DRAWING |       | SHEET 20 OF 74  |     |

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# TRI-LEVEL SYNC



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# TRI-LEVEL SYNC

DEPARTMENT



SIZE  
C+

CODE  
34649

DOCUMENT NUMBER

150-330724-B1

REV  
2.0

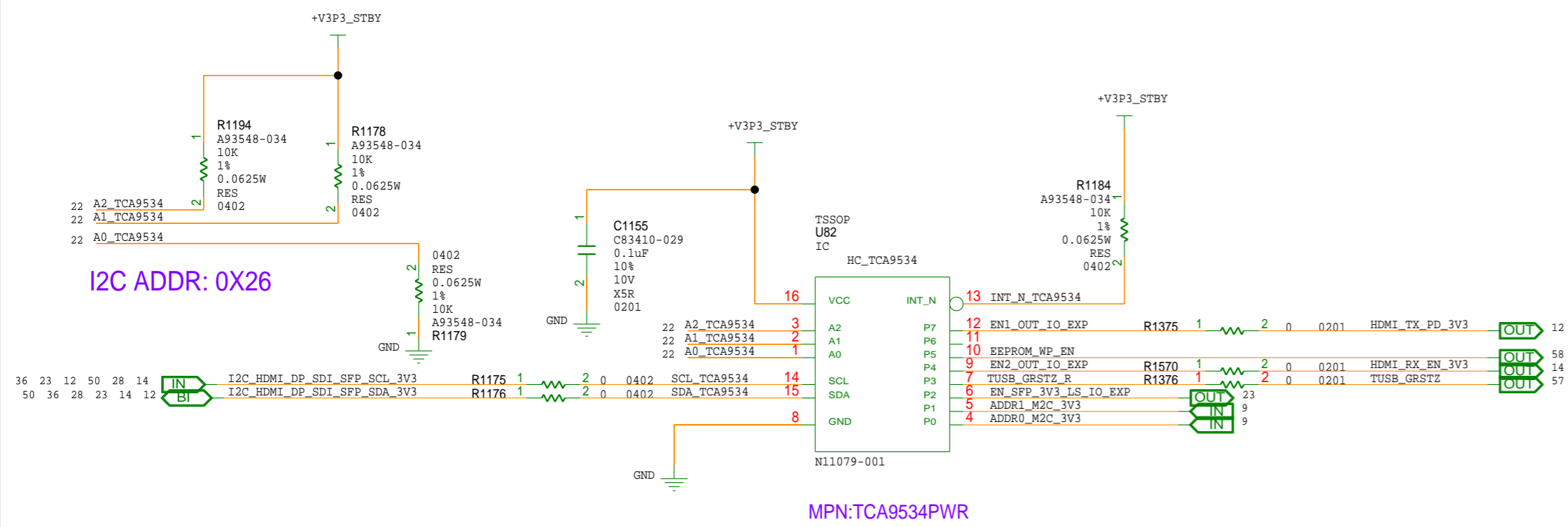
SCALE:

DO NOT SCALE DRAWING

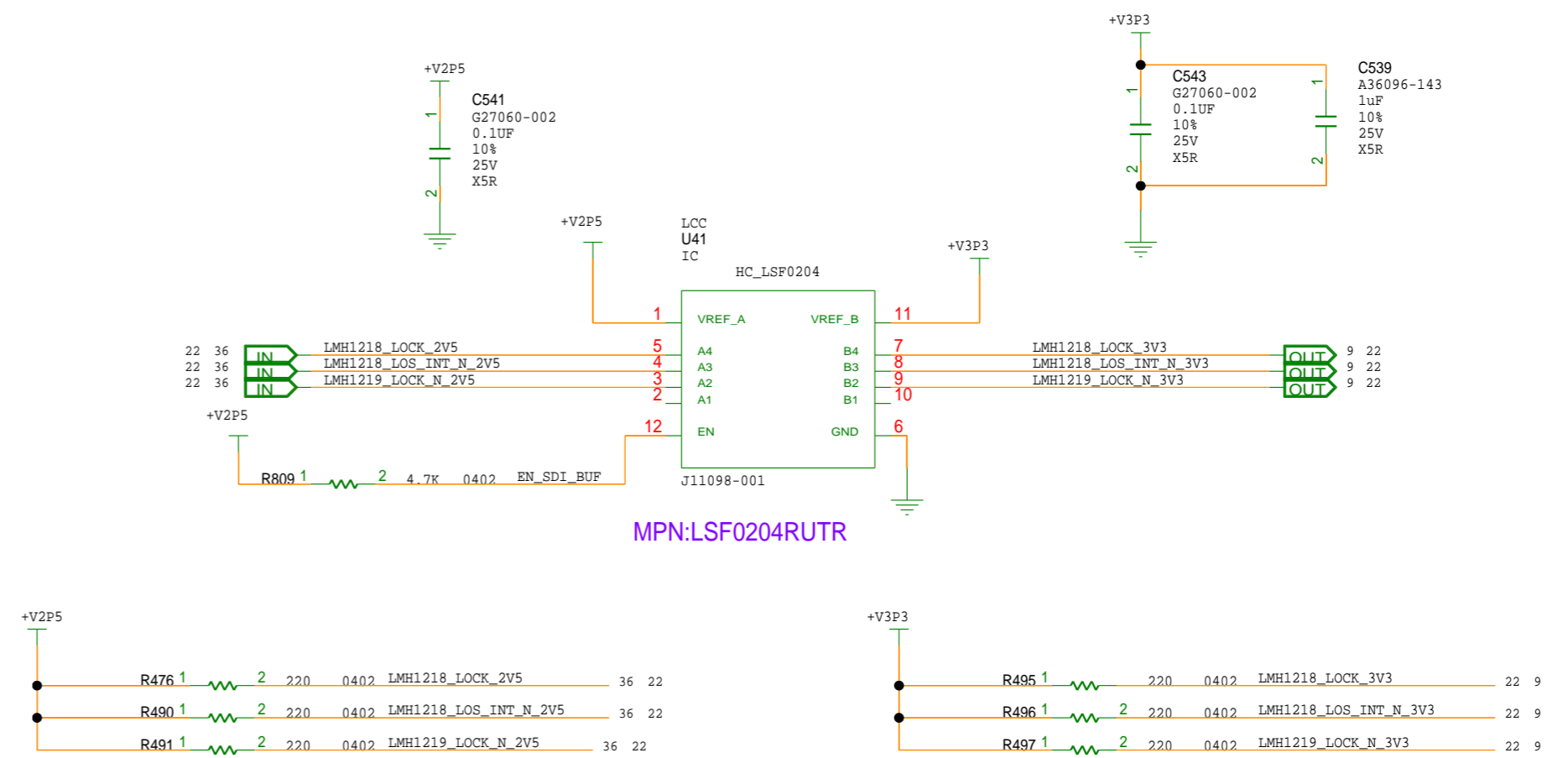
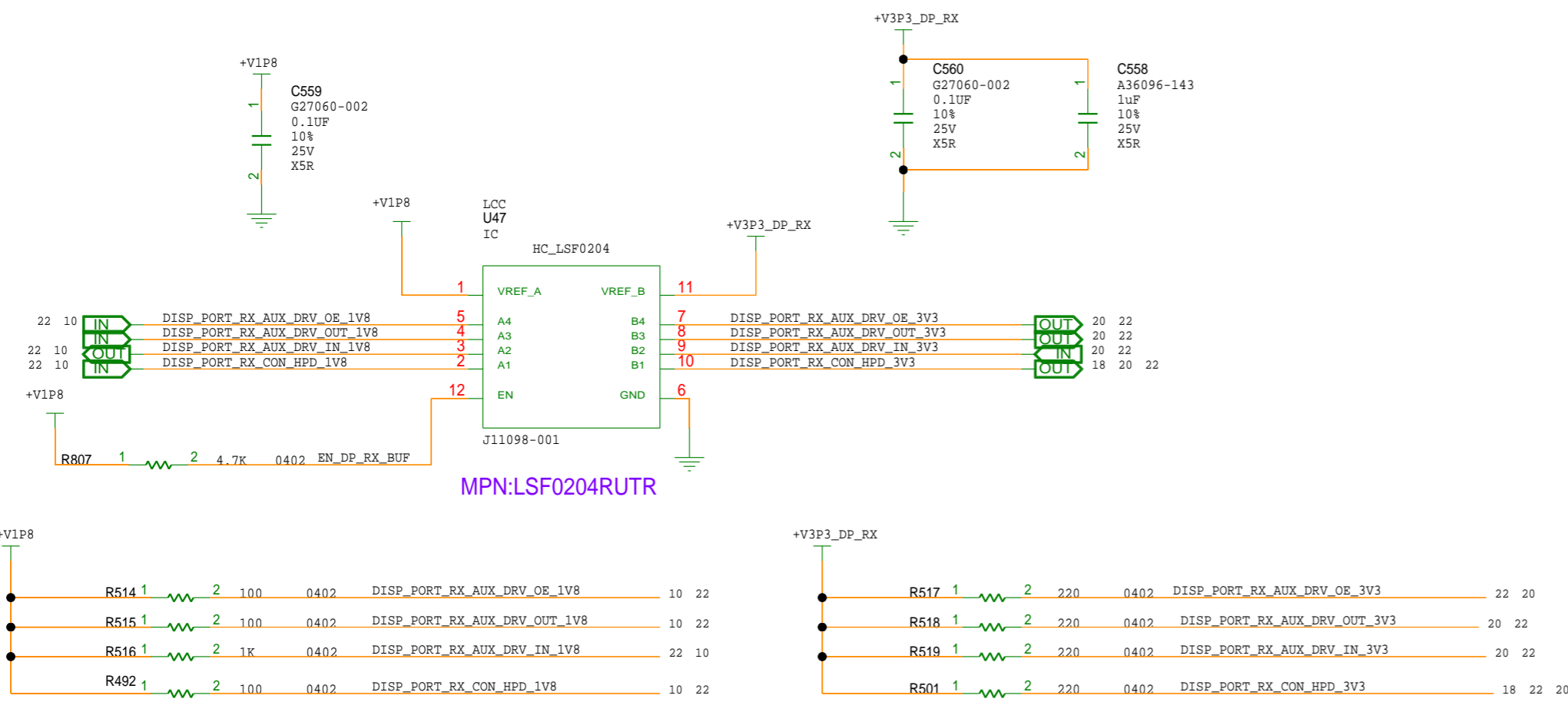
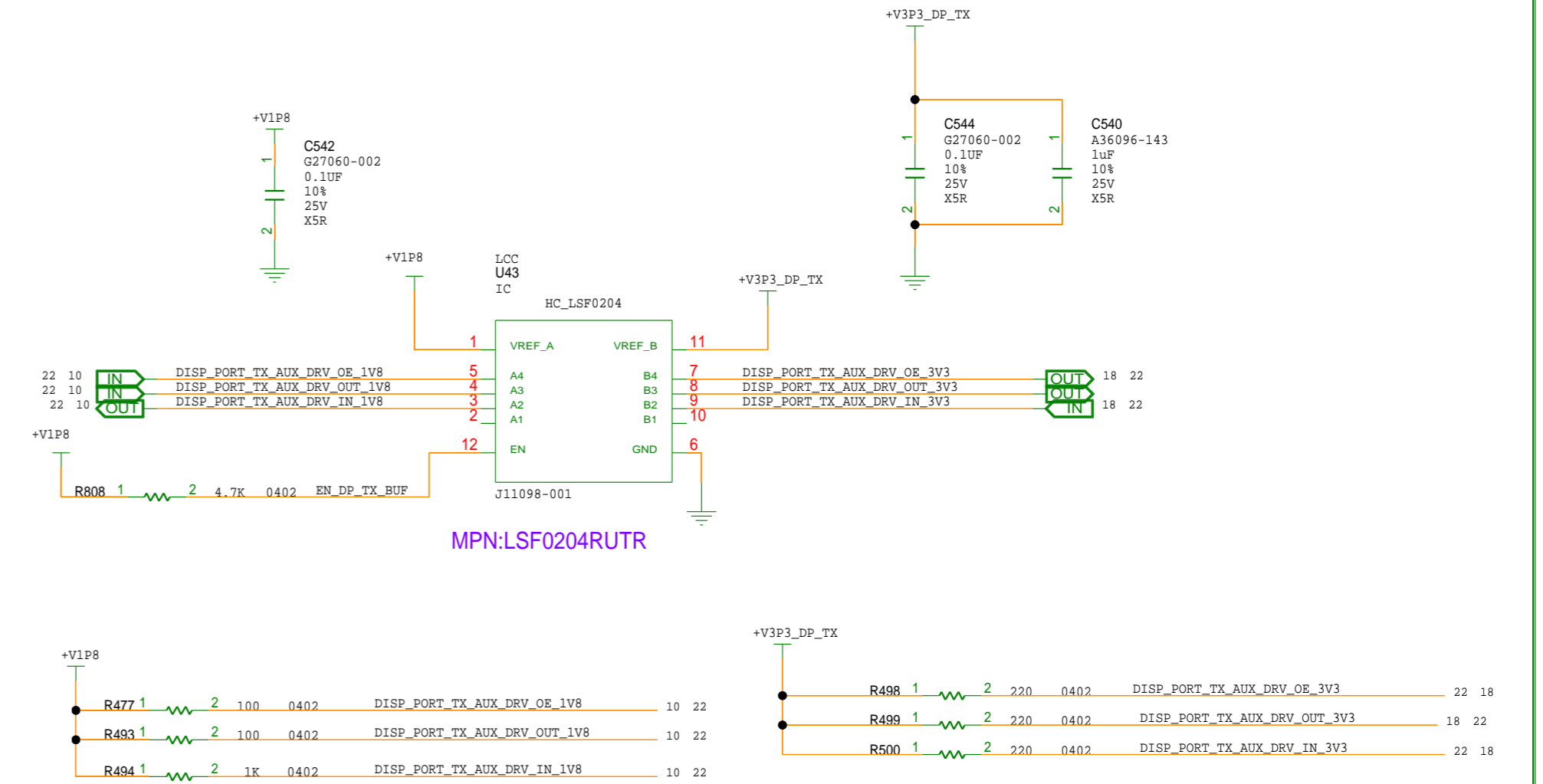
SHEET

21 OF 74

# GPIO EXPANDER



# LVL SHIFTER FOR DP TX CONTROLS



# LVL SHIFTER FOR DP RX CONTROLS

# LVL SHIFTER FOR SDI CONTROLS

LEVEL SHIFTER-DP, SDI

DEPARTMENT



SIZE  
C+

CODE  
34649

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DOCUMENT NUMBER

150-330724-B1

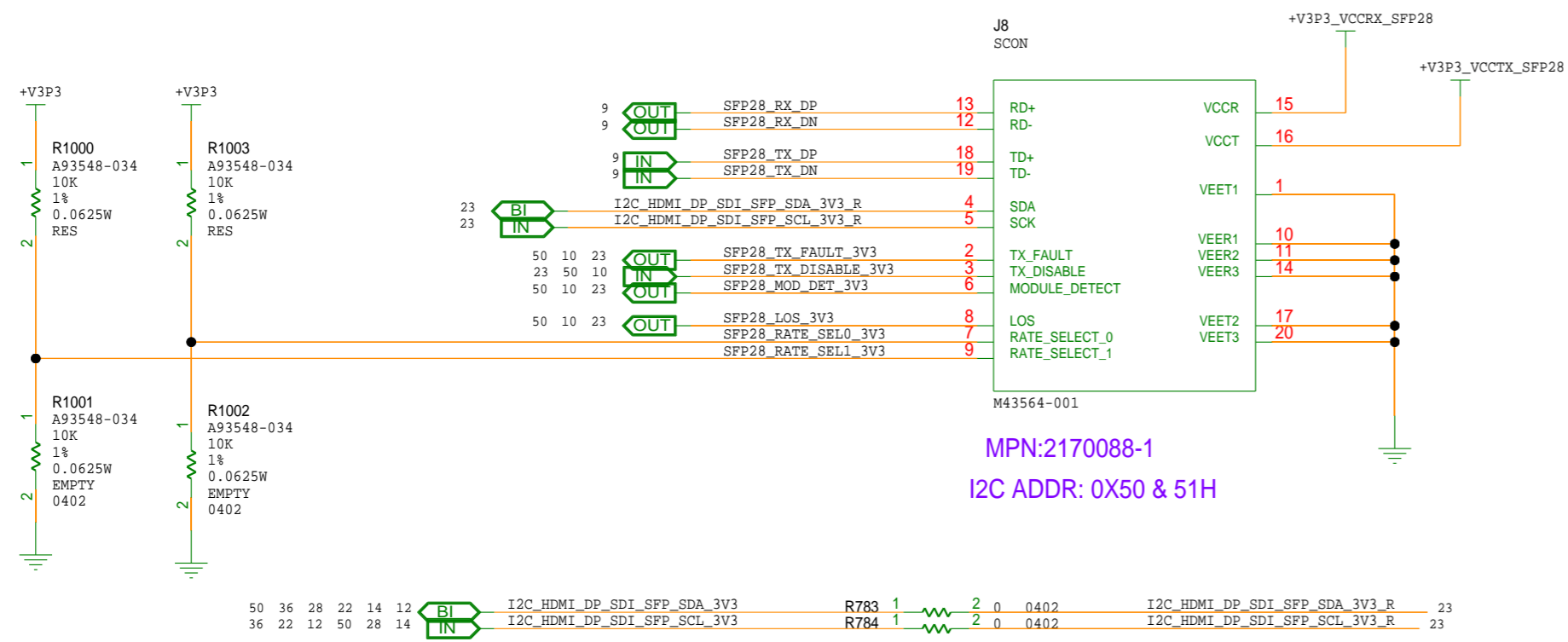
REV  
2.0

SCALE:

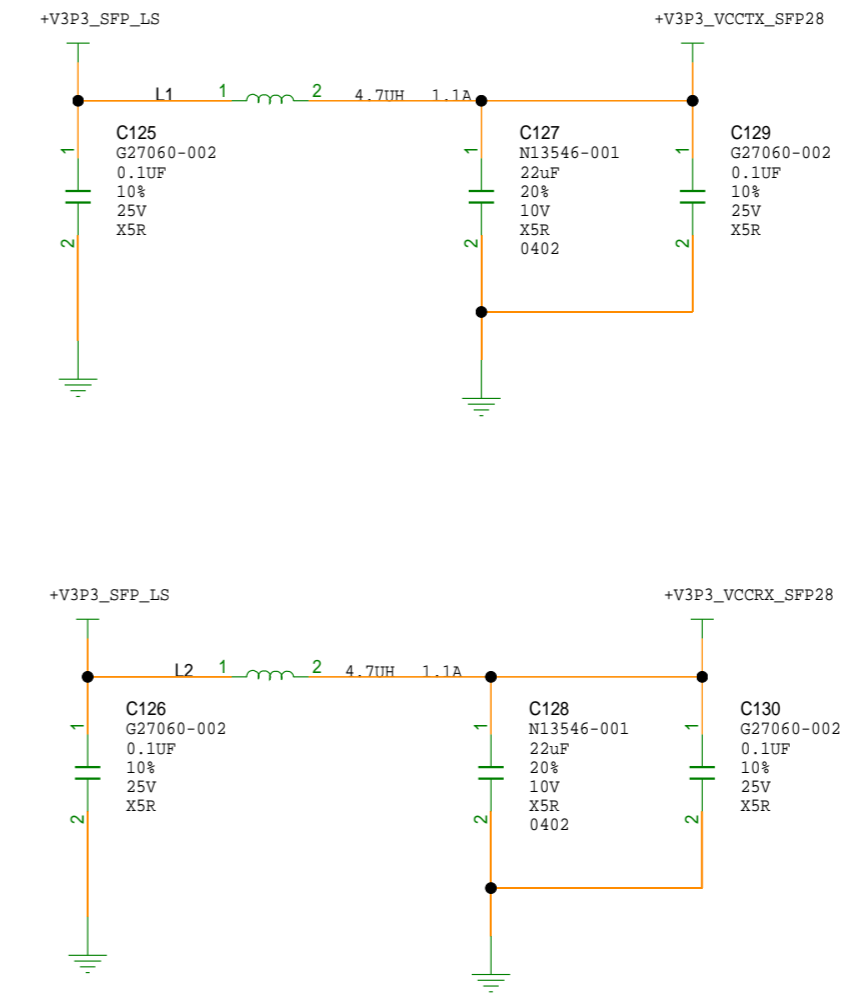
DO NOT SCALE DRAWING

SHEET 22 OF 74

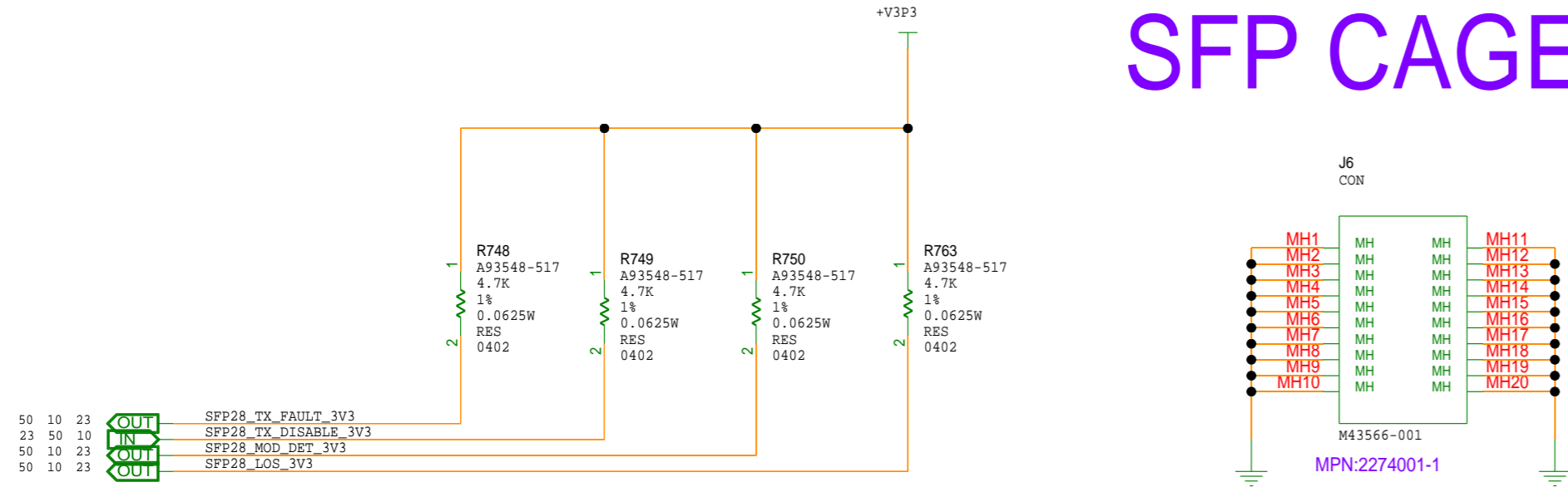
# SFP RECEPTACLE



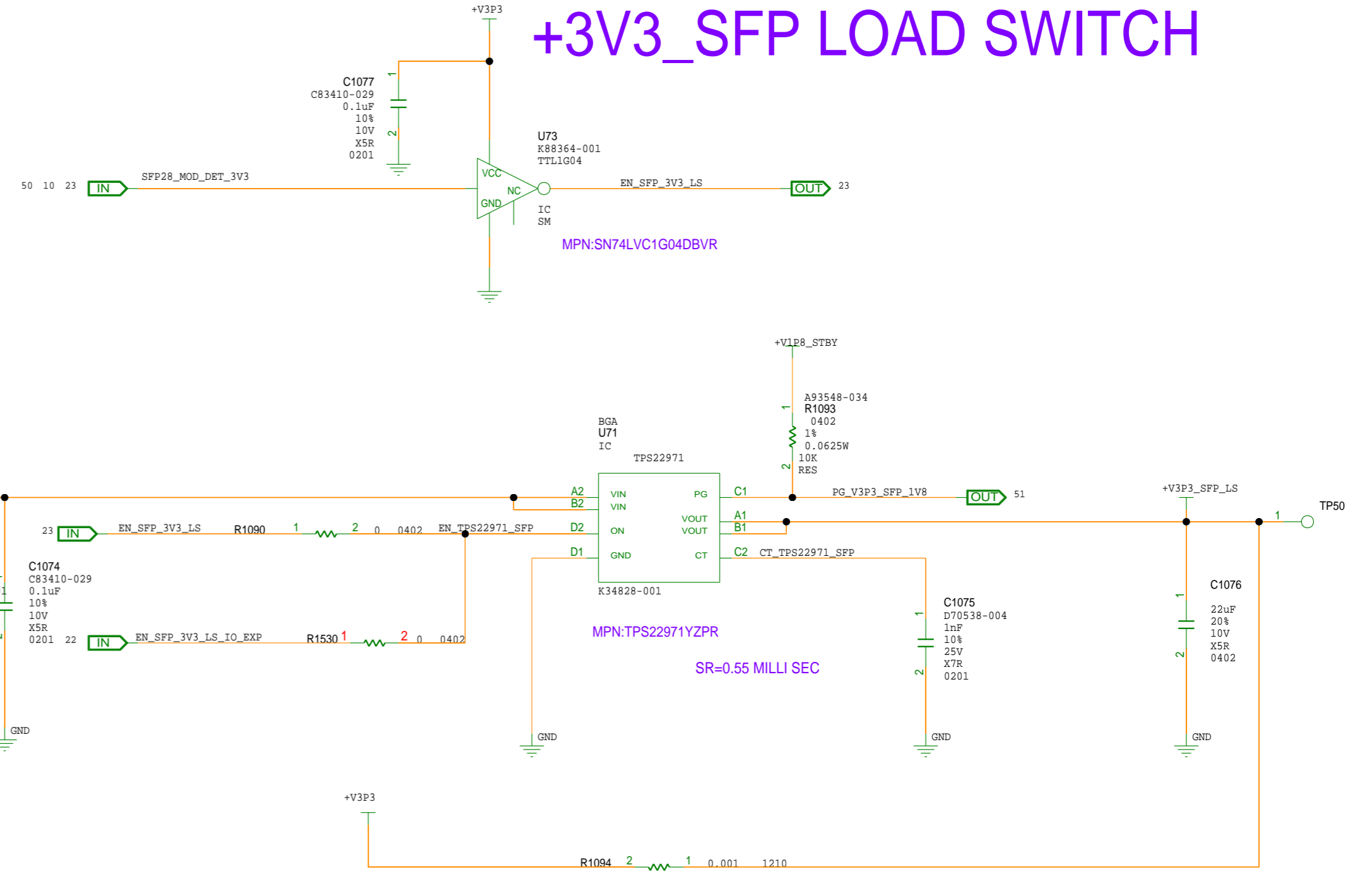
# SUPPLY DE-CAP



# SFP CAGE



# +3V3\_SFP LOAD SWITCH



# 3.3V LOAD SWITCH BY-PASS PATH

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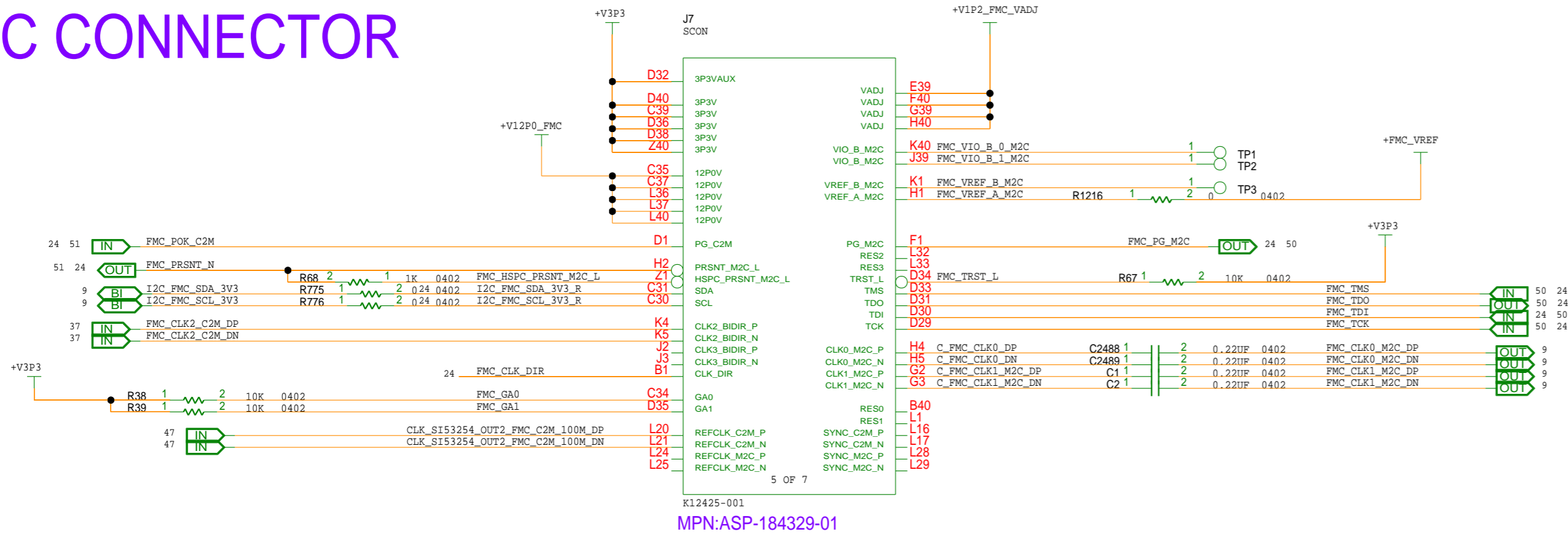
# SFP

DEPARTMENT

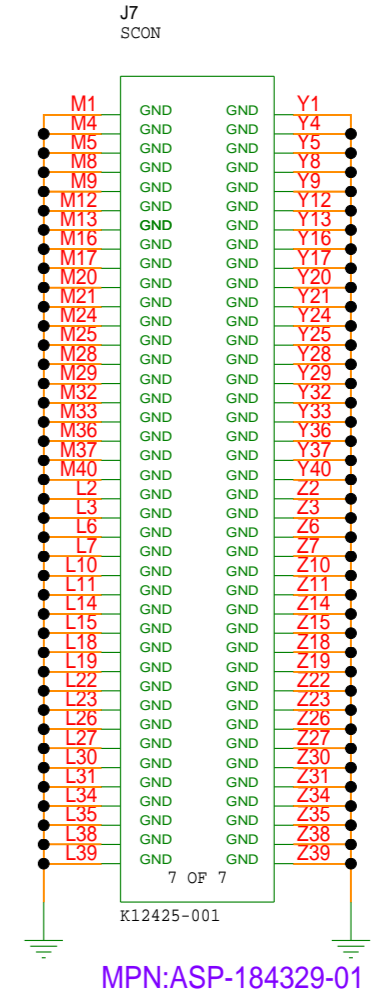
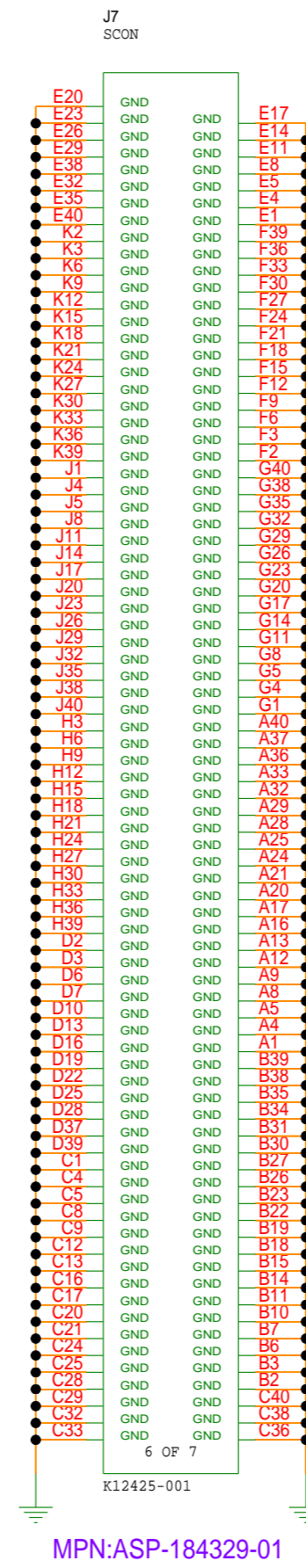
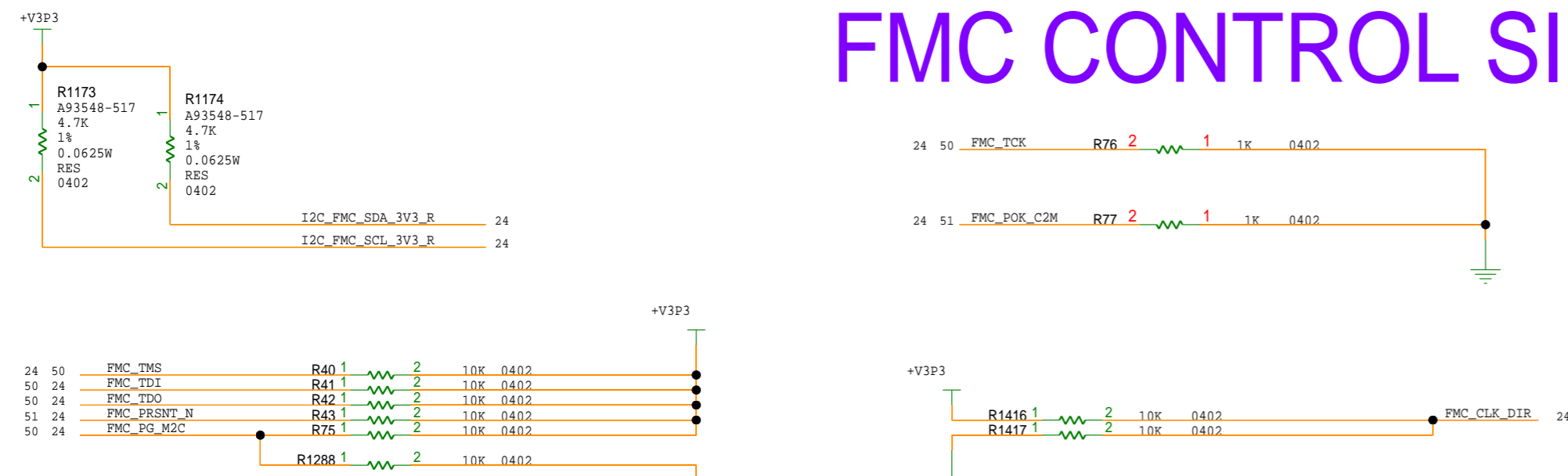


|        |                      |                 |                |
|--------|----------------------|-----------------|----------------|
| SIZE   | CODE                 | DOCUMENT NUMBER | REV            |
| C+     | 34649                | 150-330724-B1   | 2.0            |
| SCALE: | DO NOT SCALE DRAWING |                 | SHEET 23 OF 74 |

# FMC CONNECTOR



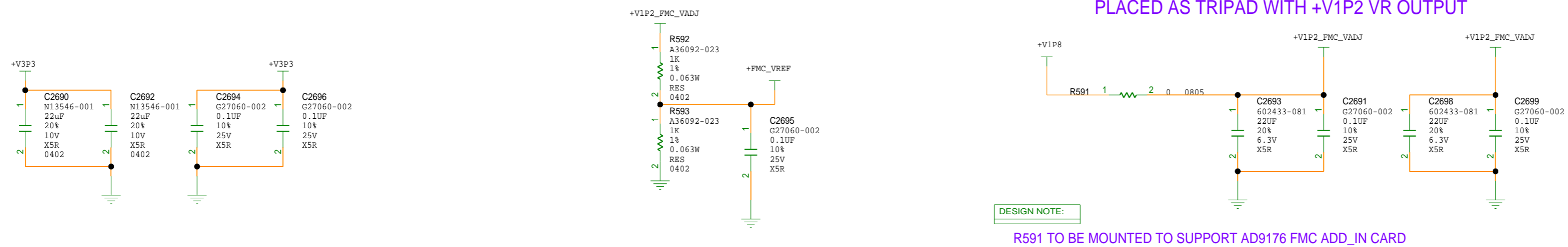
# FMC CONTROL SIGNALS



| Voltage Supply | Allowable Voltage Range | No Pins | Max Amps | Tolerance |
|----------------|-------------------------|---------|----------|-----------|
| VADJ           | 0 - 3.3V                | 2       | 2        | +/- 5%    |
| VIO B M2C      | NC                      | 0       | 0        | n/a       |
| VREF A M2C     | 0 - VADJ                | 1       | 1mA      | +/- 2%    |
| VREF B M2C     | NC                      | 0       | 0        | n/a       |
| 3P3VAUX        | 3.3V                    | 1       | 20mA     | +/- 5%    |
| 3P3V           | 3.3V                    | 4       | 3        | +/- 5%    |
| 12P0V          | 12V                     | 2       | 1        | +/- 5%    |

Table 12. Power Supply Voltages for LPC connector

# SUPPLY DE-CAP

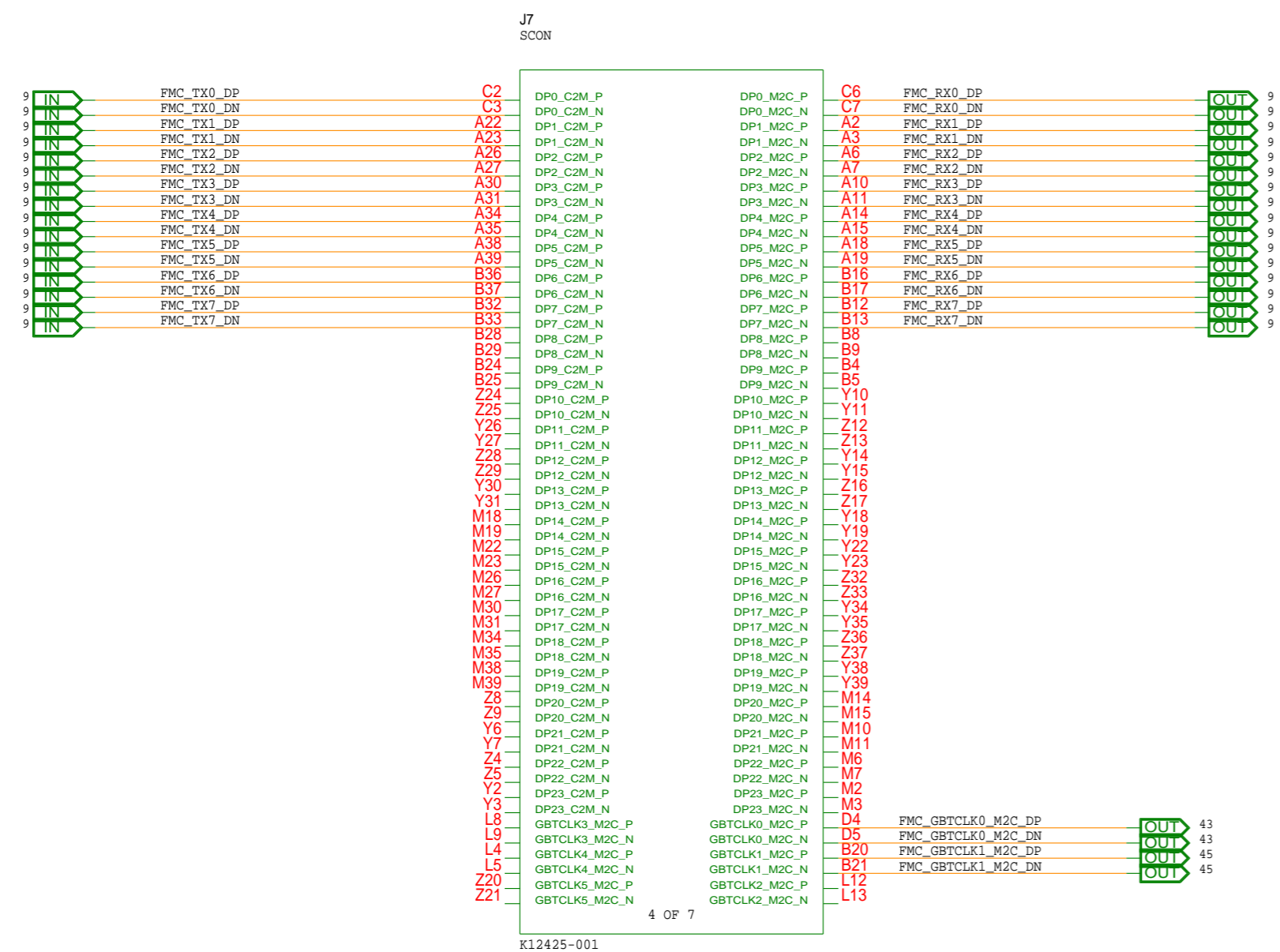


CAD NOTE:  
PLACED AS TRIPAD WITH +V1P2 VR OUTPUT

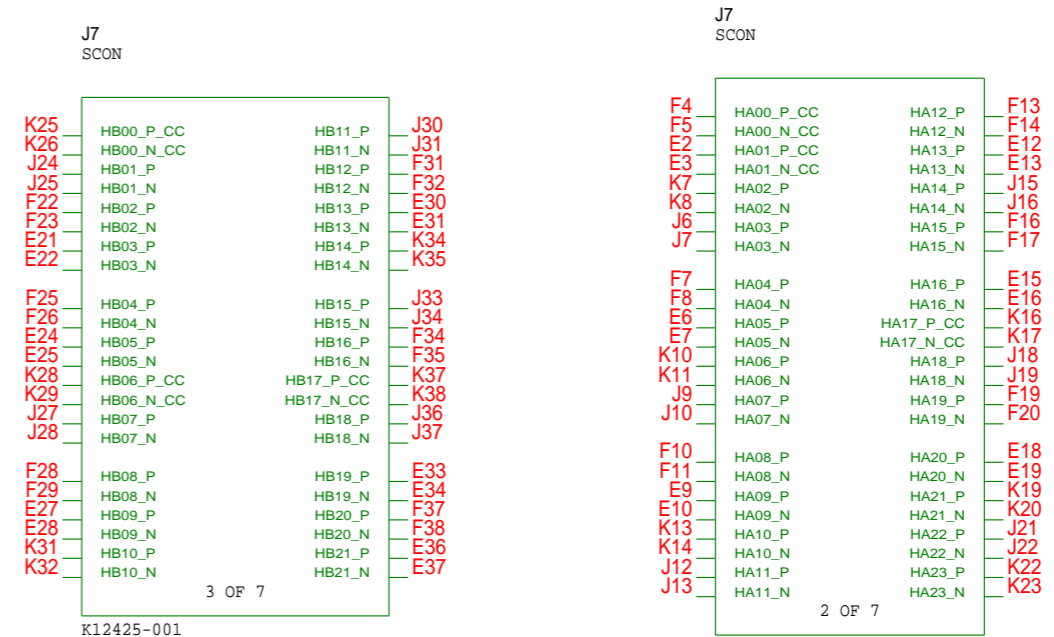
DESIGN NOTE:  
R591 TO BE MOUNTED TO SUPPORT AD9176 FMC ADD\_IN CARD



# FMC CONNECTOR

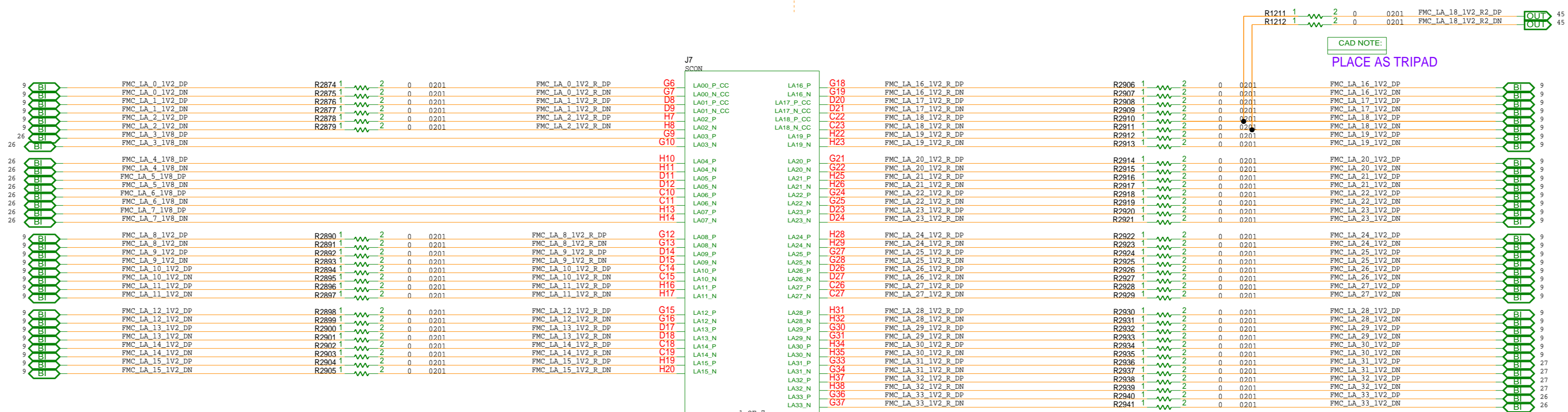


MPN:ASP-184329-01



MPN:ASP-184329-01

MPN:ASP-184329-01



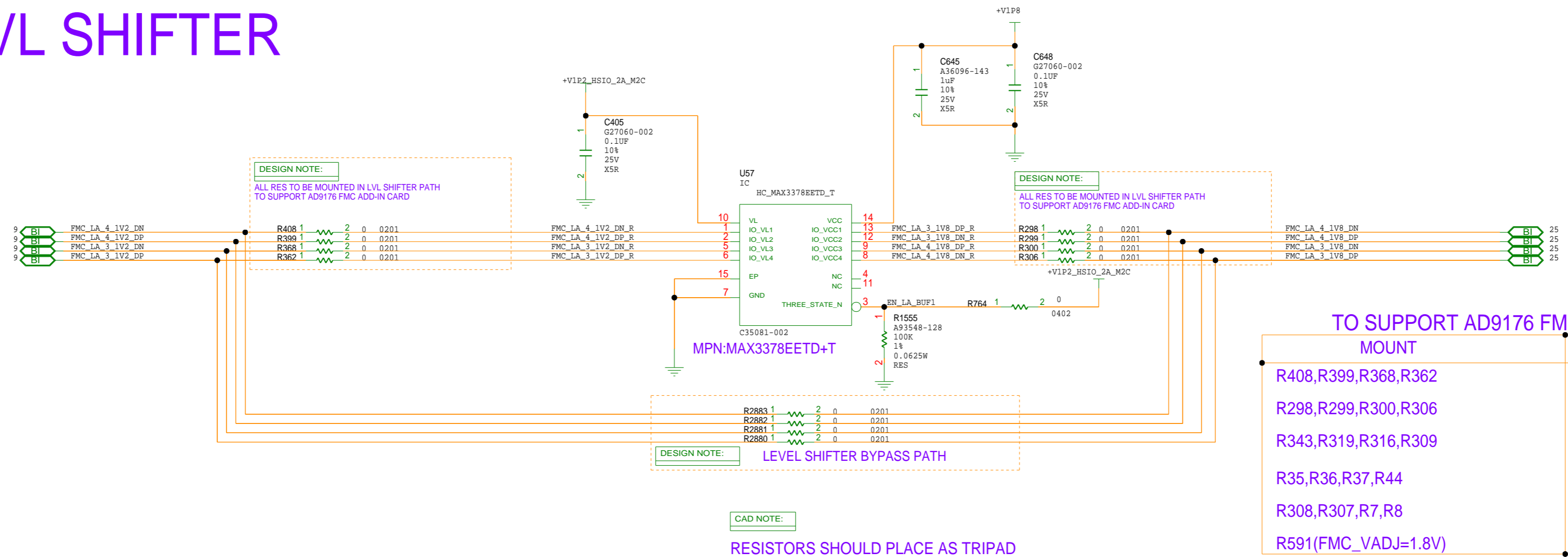
MPN:ASP-184329-01

Tue Oct 1 13:22:31 2024

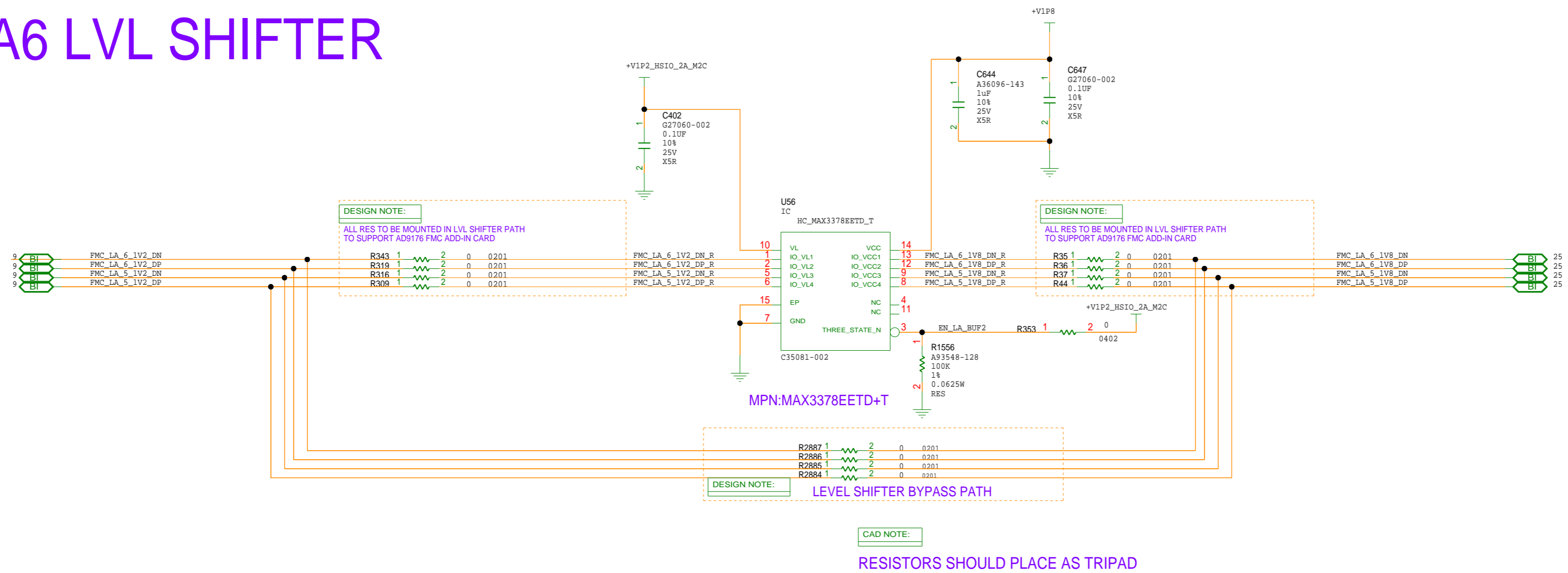
# FMC CONNECTOR

|            |                            |                      |               |                                  |            |
|------------|----------------------------|----------------------|---------------|----------------------------------|------------|
| DEPARTMENT | altera<br>An Intel Company | SIZE<br>C+           | CODE<br>34649 | DOCUMENT NUMBER<br>150-330724-B1 | REV<br>2.0 |
| SCALE:     |                            | DO NOT SCALE DRAWING |               | SHEET                            | 25 OF 74   |

# LA3 & LA4 LVL SHIFTER



# LA5 & LA6 LVL SHIFTER

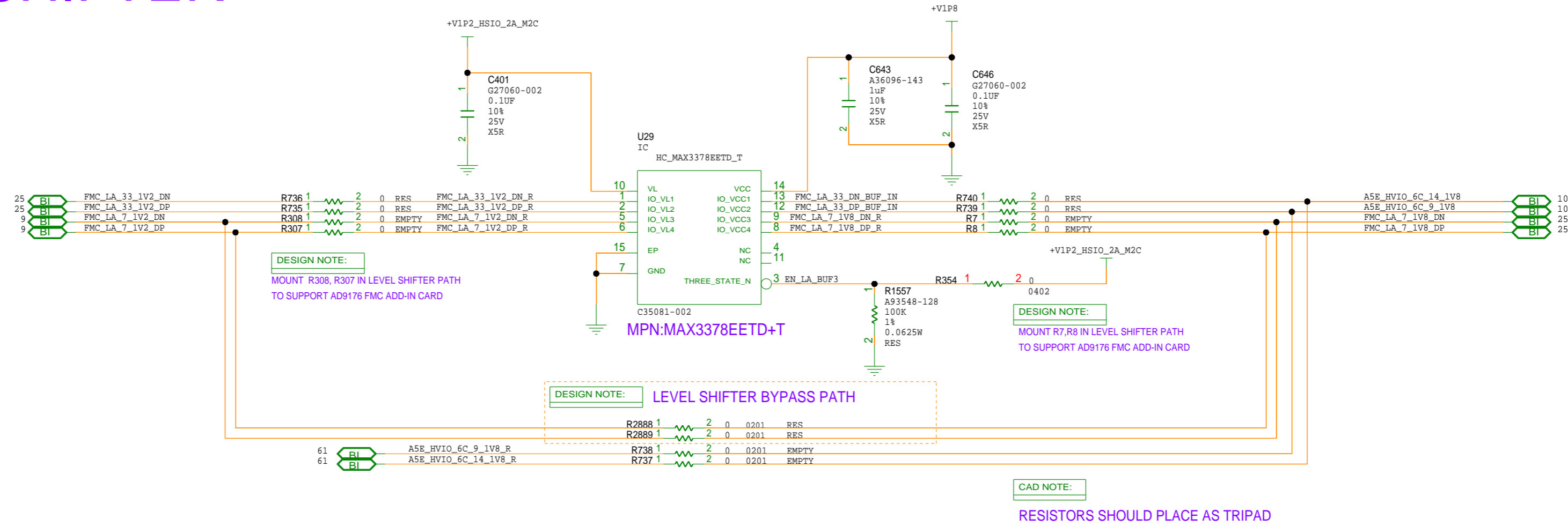


LEVEL SHIFTER\_LA SIG

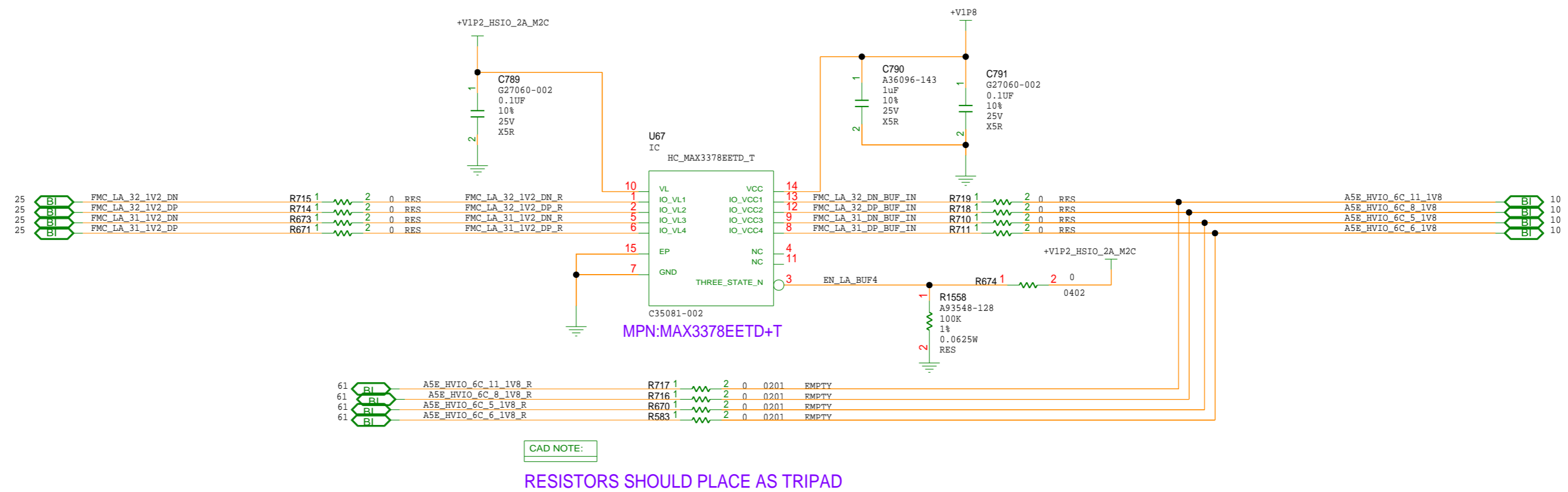
|            |                      |                      |       |                 |          |
|------------|----------------------|----------------------|-------|-----------------|----------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV      |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0      |
| SCALE:     |                      | DO NOT SCALE DRAWING |       | SHEET           | 26 OF 74 |

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# LA7 & LA33 LVL SHIFTER



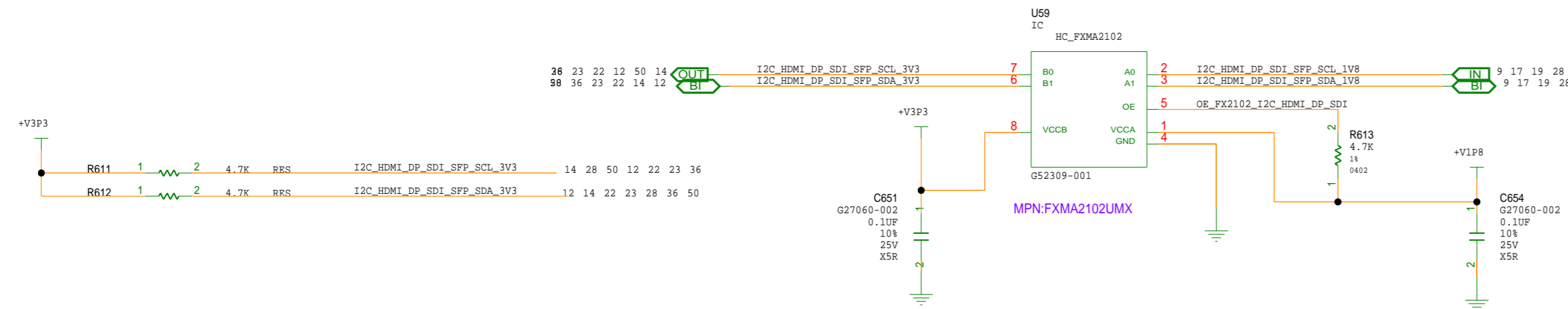
# LA31 & LA32 LVL SHIFTER



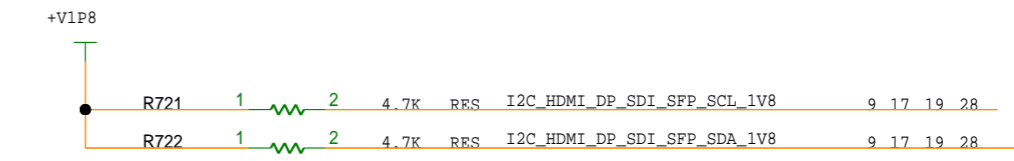
Tue Oct 1 13:22:32 2024

|            |   |                      |       |                 |                |
|------------|---|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |   | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |   | DO NOT SCALE DRAWING |       |                 | SHEET 27 OF 74 |

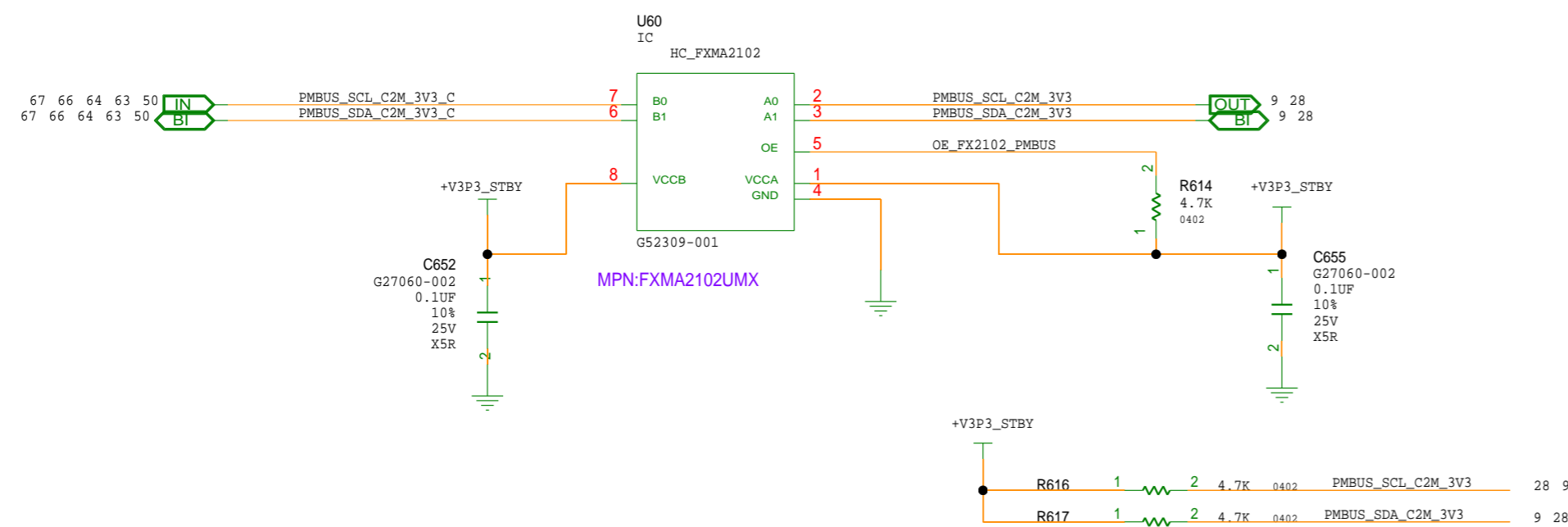
# SDI/SFP/HDMI/DP I2C



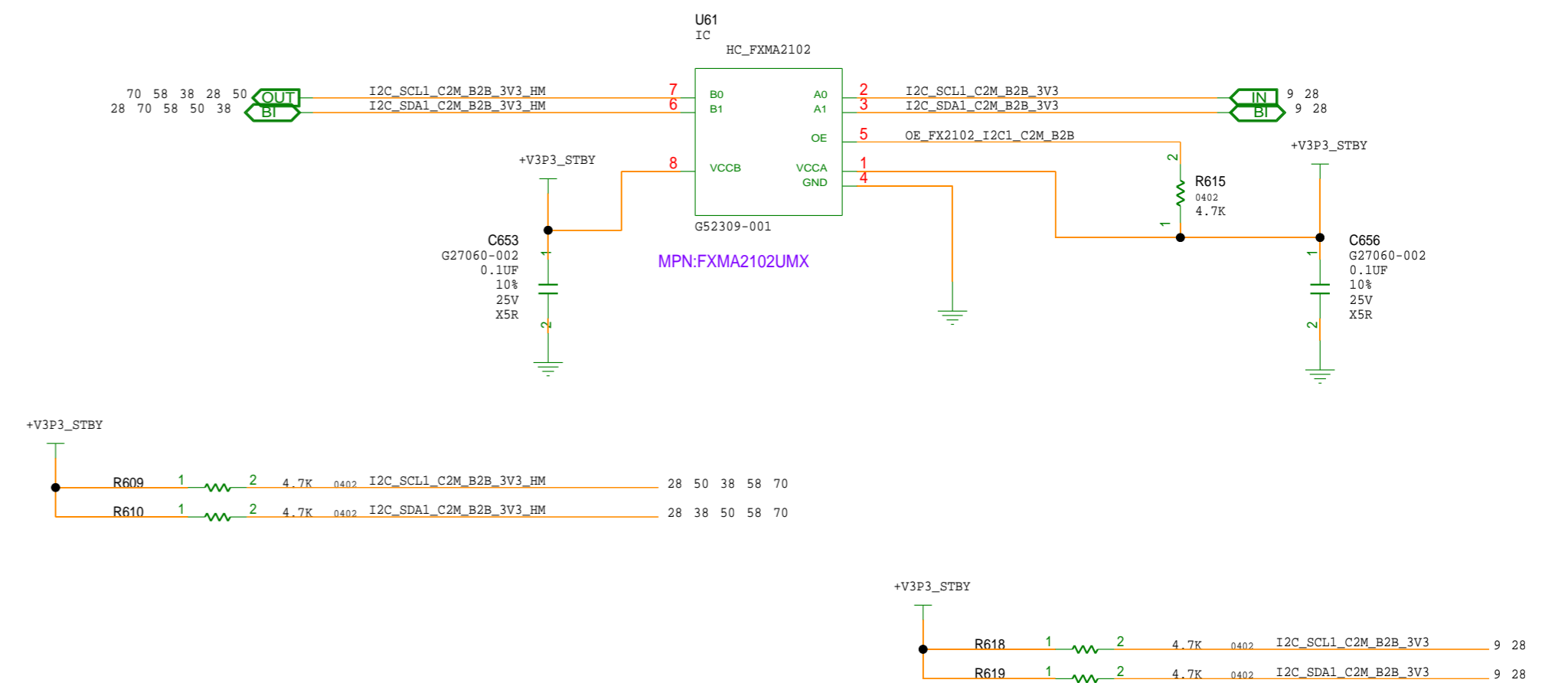
# I2C ISOLATORS



# PMBUS I2C FOR VRM ACCESS




# TEMP & CURRENT MONITORING I2C

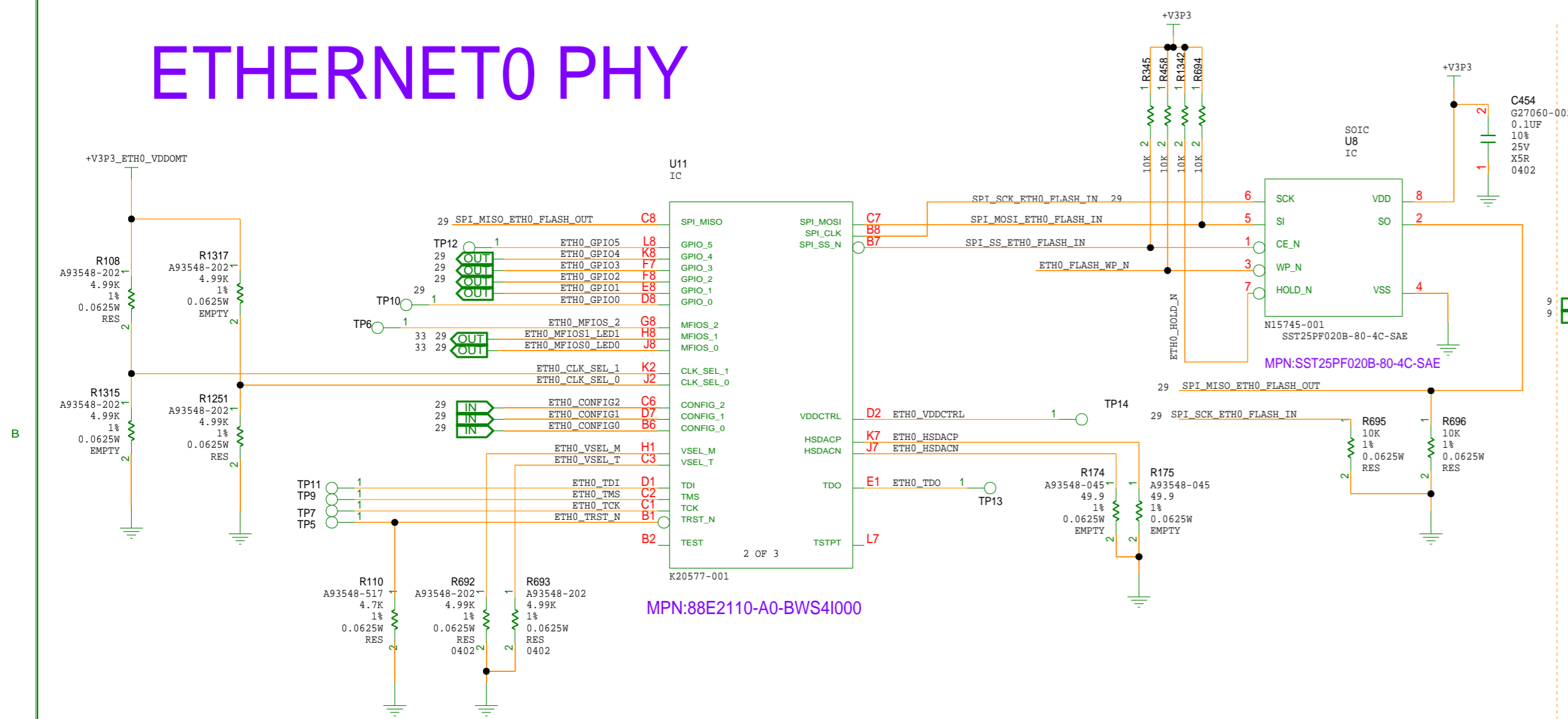


# LEVEL SHIFTER\_I2C

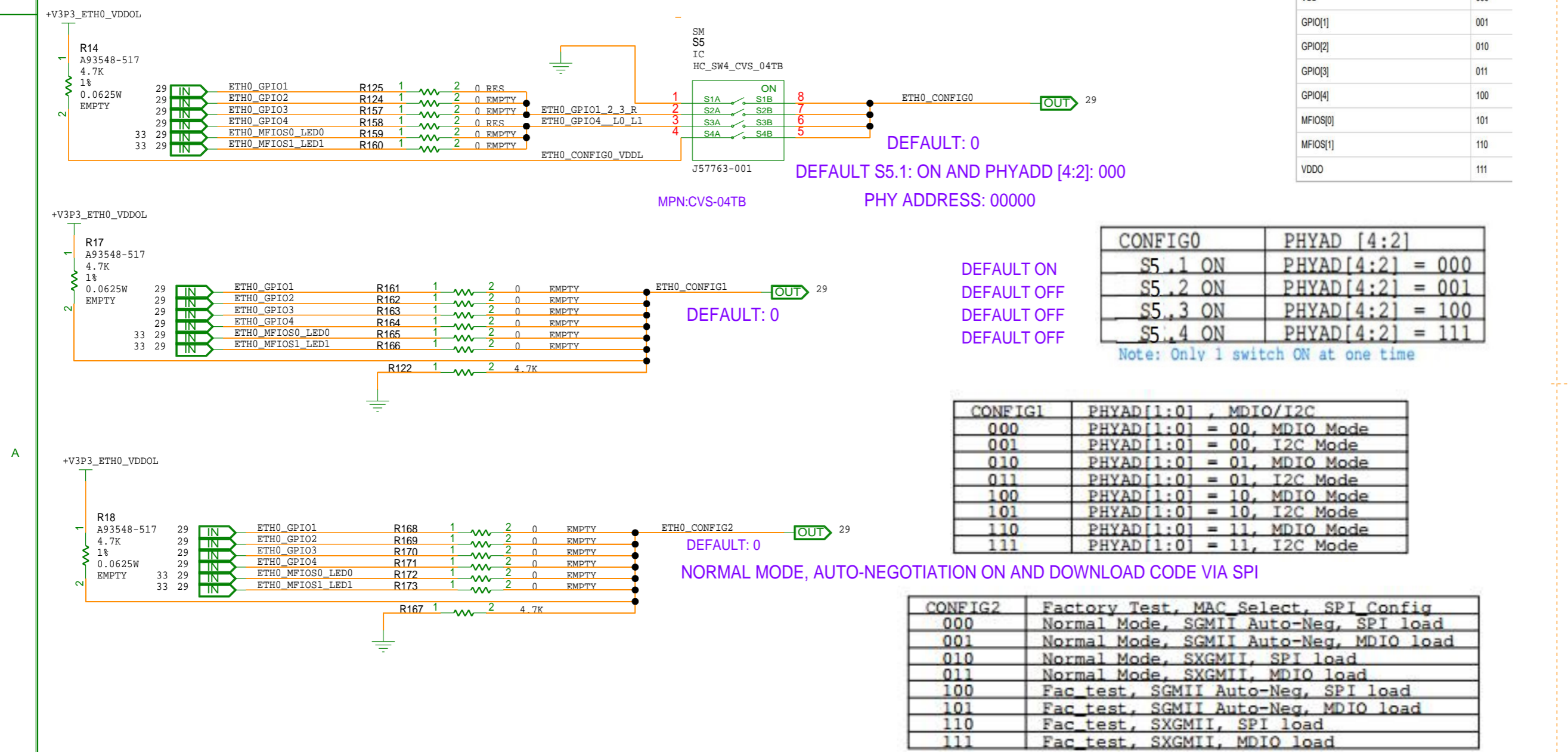
Tue Oct 1 13:22:32 2024

|            |   |                      |       |                 |          |
|------------|---|----------------------|-------|-----------------|----------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV      |
|            |   | C+                   | 34649 | 150-330724-B1   | 2.0      |
| SCALE:     |   | DO NOT SCALE DRAWING |       | SHEET           | 28 OF 74 |

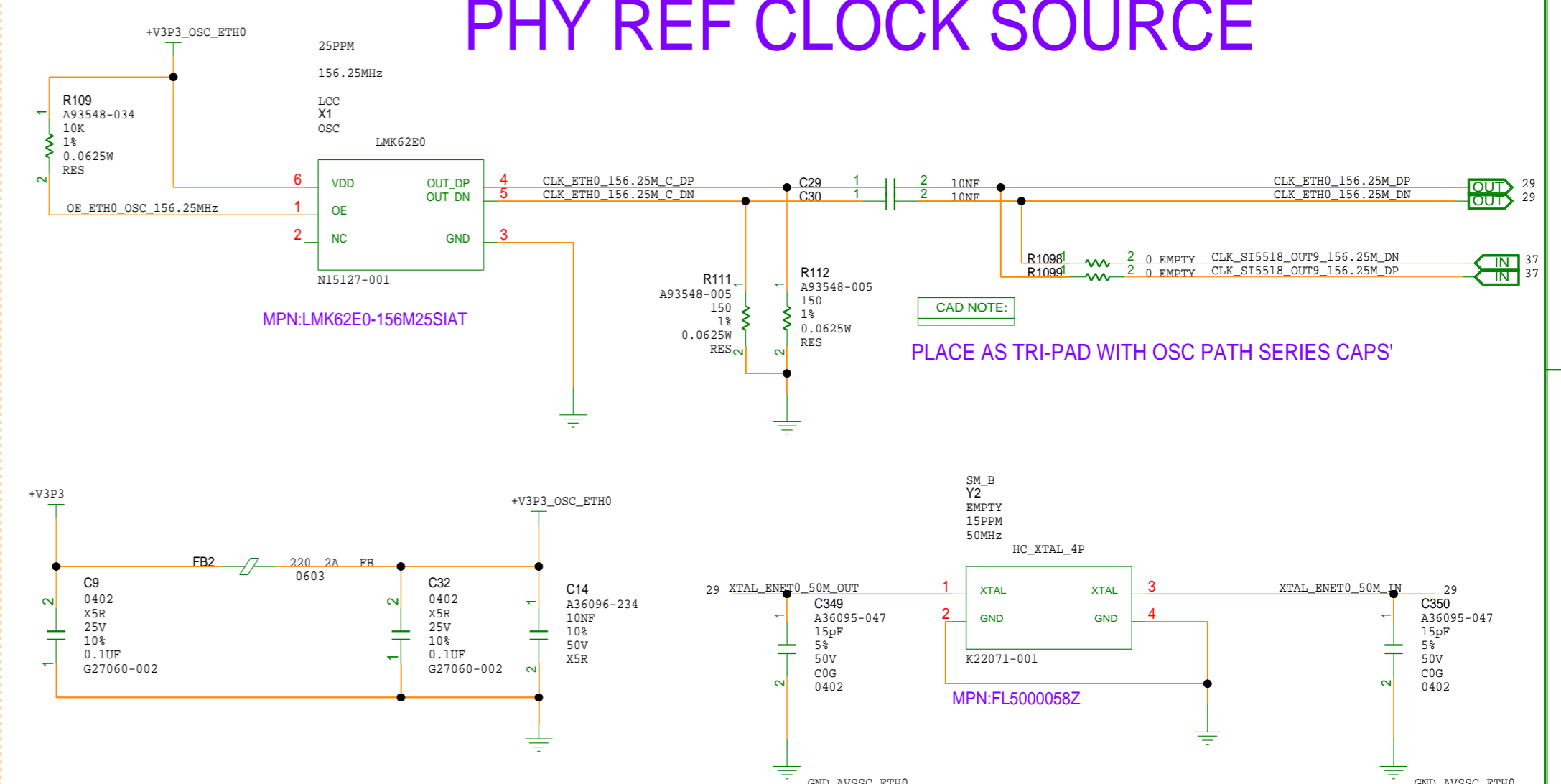
# ETHERNET0 PHY



# PHY BOOTSTRAP SETTINGS

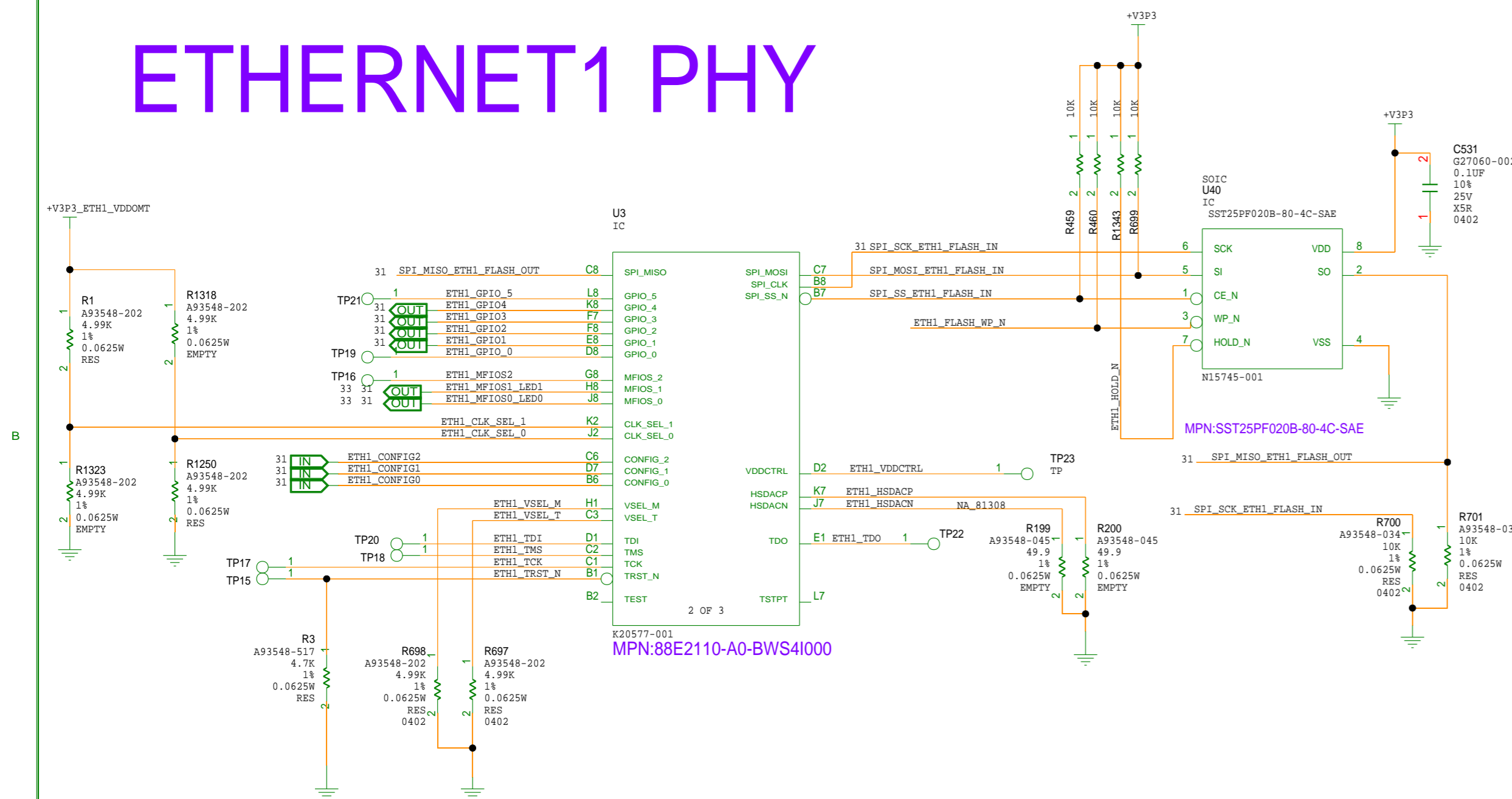


# PHY REF CLOCK SOURCE





# ETHERNET1 PHY



## PHY BOOTSTRAP SETTINGS

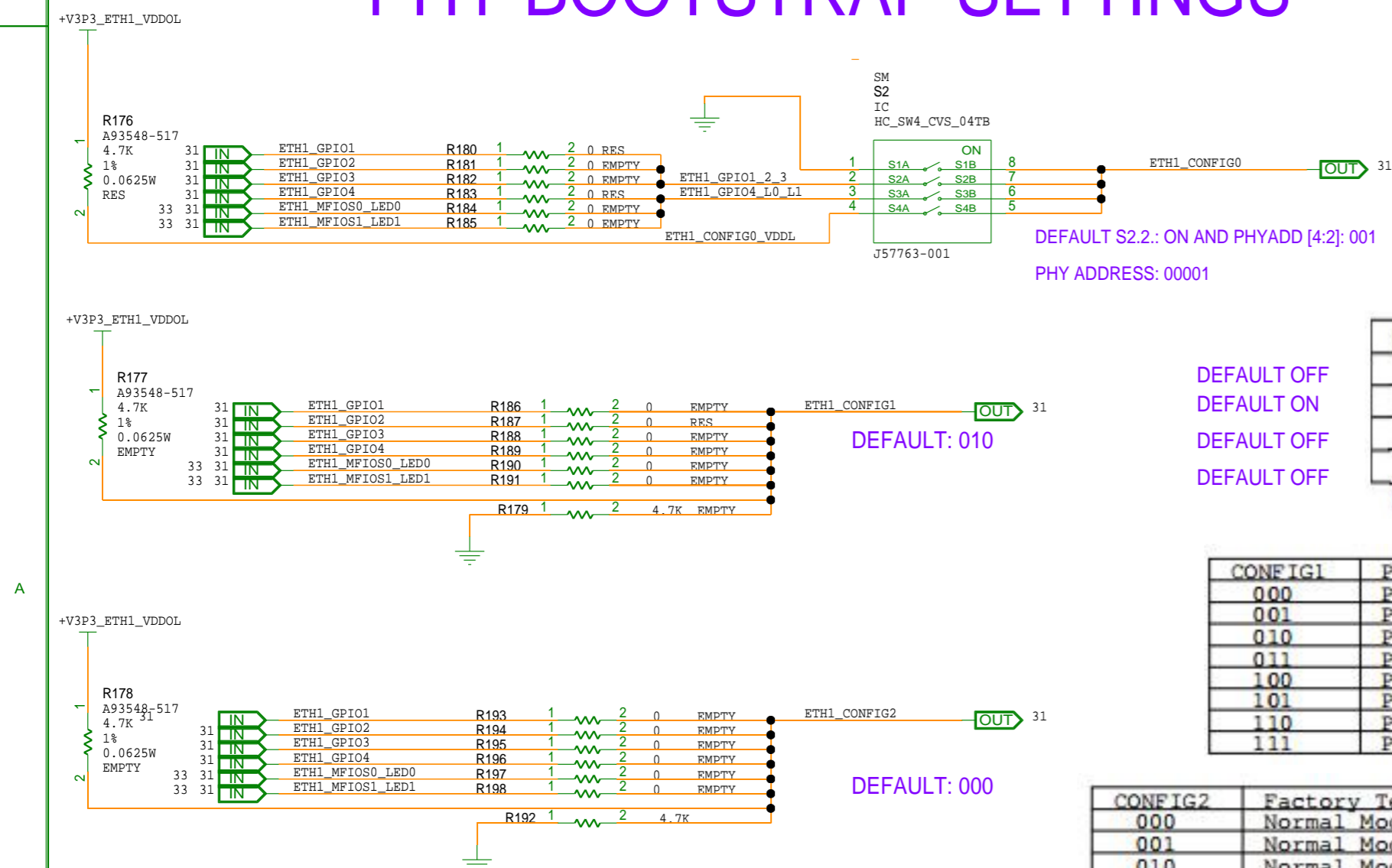


Table 30: 88E2110 Device Three Bit Mapping

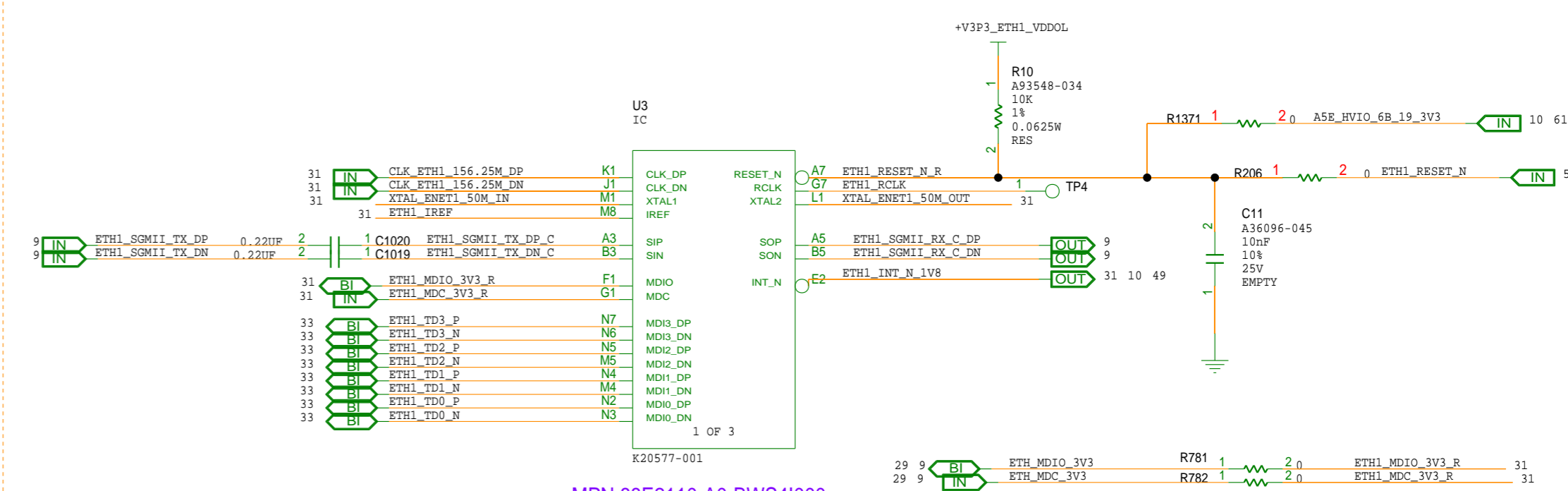
| Pin      | Bit[2:0] |
|----------|----------|
| VSS      | 000      |
| GPIO[1]  | 001      |
| GPIO[2]  | 010      |
| GPIO[3]  | 011      |
| GPIO[4]  | 100      |
| MFIOS[0] | 101      |
| MFIOS[1] | 110      |
| VDDO     | 111      |

| CONFIG0 | PHYAD [4:2]      |
|---------|------------------|
| S2.1 ON | PHYAD[4:2] = 000 |
| S2.2 ON | PHYAD[4:2] = 001 |
| S2.3 ON | PHYAD[4:2] = 100 |
| S2.4 ON | PHYAD[4:2] = 111 |

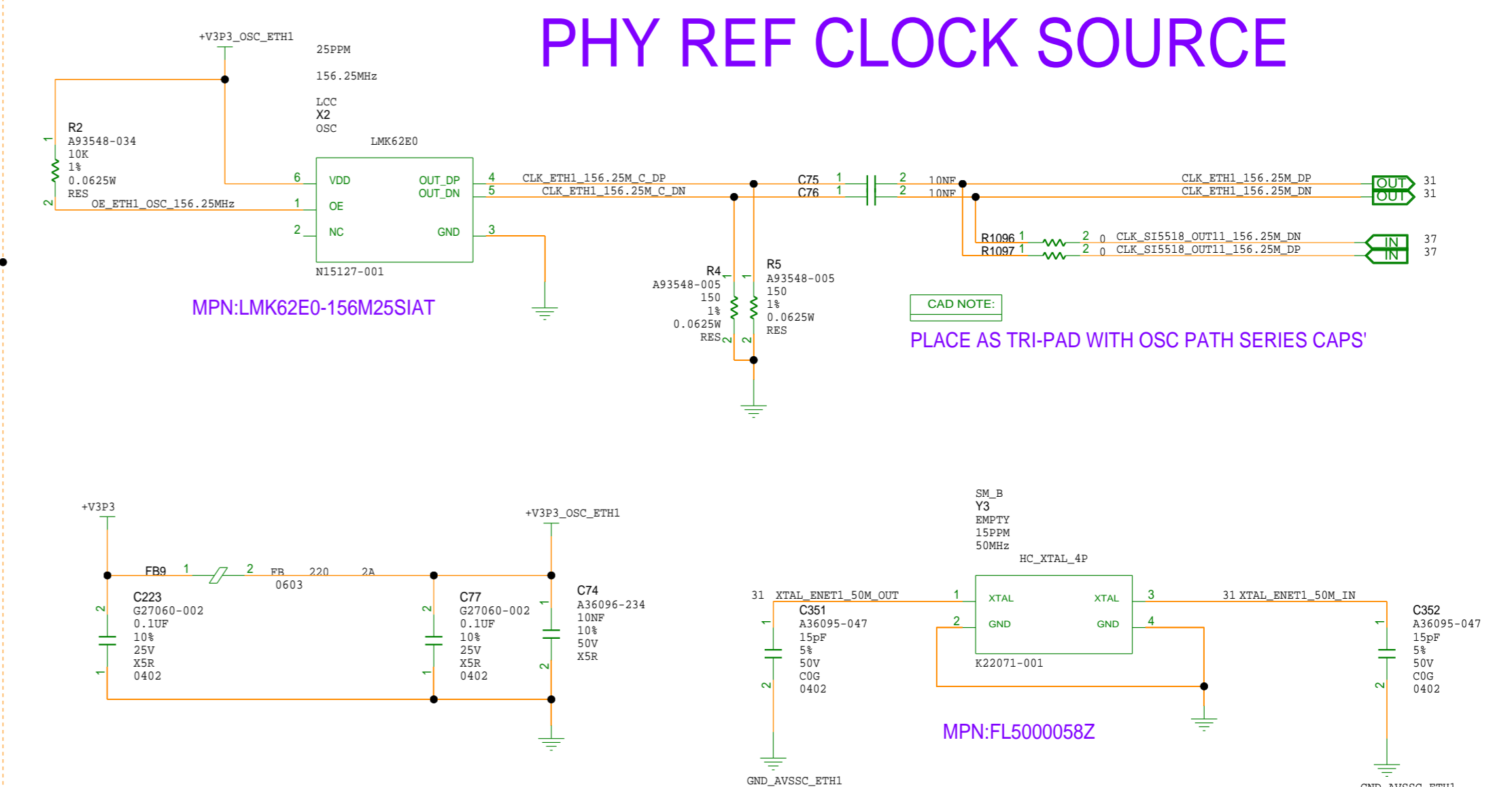
Note: Only 1 switch ON at one time

| CONFIG1 | PHYAD[1:0], MDIO/I2C       |
|---------|----------------------------|
| 000     | PHYAD[1:0] = 00, MDIO Mode |
| 001     | PHYAD[1:0] = 00, I2C Mode  |
| 010     | PHYAD[1:0] = 01, MDIO Mode |
| 011     | PHYAD[1:0] = 01, I2C Mode  |
| 100     | PHYAD[1:0] = 10, MDIO Mode |
| 101     | PHYAD[1:0] = 10, I2C Mode  |
| 110     | PHYAD[1:0] = 11, MDIO Mode |
| 111     | PHYAD[1:0] = 11, I2C Mode  |

| CONFIG2 | Factory Test, MAC Select, SPI Config   |
|---------|--|
| 000     | Normal Mode, SGMII Auto-Neg, SPI load  |
| 001     | Normal Mode, SGMII Auto-Neg, MDIO load |
| 010     | Normal Mode, SXGMII, SPI load          |
| 011     | Normal Mode, SXGMII, MDIO load         |
| 100     | Fac test, SGMII Auto-Neg, SPI load     |
| 101     | Fac test, SGMII Auto-Neg, MDIO load    |
| 110     | Fac test, SXGMII, SPI load             |
| 111     | Fac test, SXGMII, MDIO load            |



## PHY REF CLOCK SOURCE

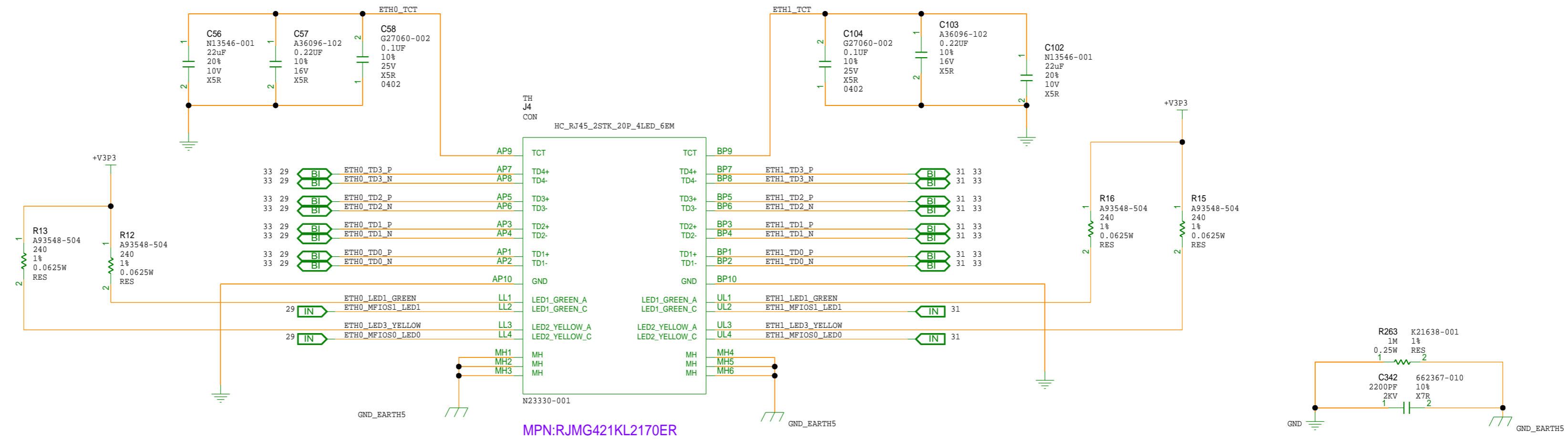


CAD NOTE: PLACE AS TRI-PAD WITH OSC PATH SERIES CAPS

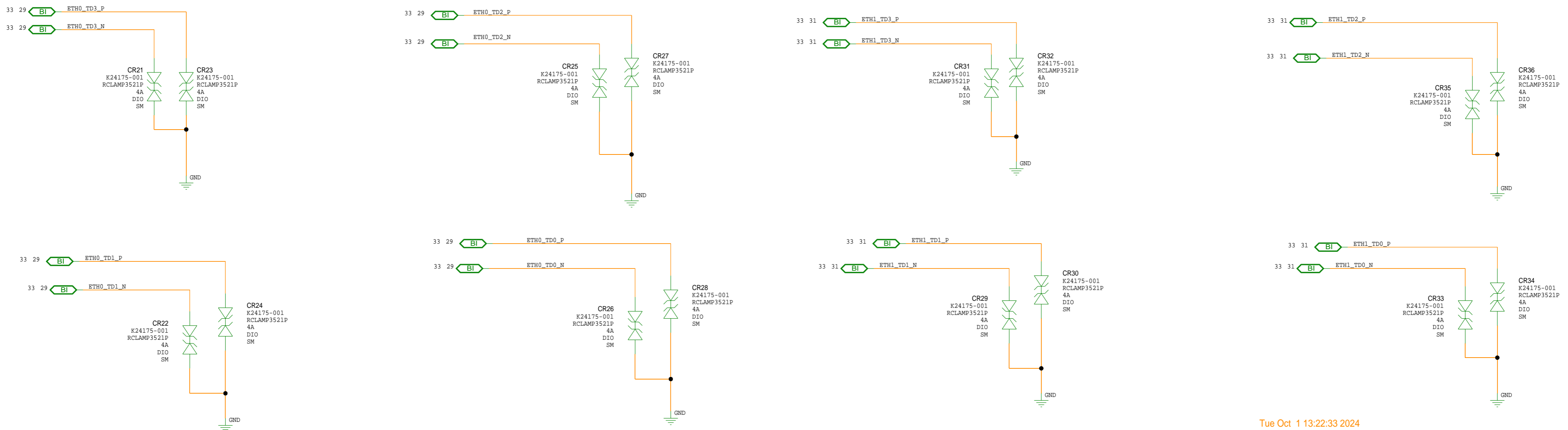




# ETHERNET RJ45 CONN



MPN:RJMG421KL2170ER



Tue Oct 1 13:22:33 2024

# ETHERNET RJ45 CONN

|            |                      |                      |       |                 |                |
|------------|----------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                      | DO NOT SCALE DRAWING |       |                 | SHEET 33 OF 74 |


# FRAMOS PINOUT DETAILS (NATIVE MIPI)

| Pin # | PixelMateC Name | Native MIPI         | SLVS-MIPI Name      |
|-------|-----------------|---------------------|---------------------|
| 1     | 3V8_VDD         | 3V8_VDD             | 3V8_VDD             |
| 3     | 3V8_VDD         | 3V8_VDD             | 3V8_VDD             |
| 5     | V_ANA           | AUX_ANA             | NC                  |
| 7     | V_ANA           | AUX_ANA             | NC                  |
| 9     | V_IF            | AUX_IF              | NC                  |
| 11    | GND             | GND                 | GND                 |
| 13    | GND             | GND                 | GND                 |
| 15    | RST_0           | RST_0               | RST_0               |
| 17    | SPI_MISO        | GPIO14              | EE_MISO             |
| 19    | XMASTER0        | GPIO0(XMASTER0)     | GPIO0(XMASTER0)     |
| 21    | I2C_0_SCL       | I2C_0_SCL(SPI_SCK)  | I2C_0_SCL(SPI_SCK)  |
| 23    | SPI_CS          | GPIO17(SPI_CS)      | GPIO17(SPI_CS)      |
| 25    | XVS0            | GPIO1(XVS0)         | GPIO1(XVS0)         |
| 27    | I2C_0_SDA       | I2C_0_SDA(SPI_MOSI) | I2C_0_SDA(SPI_MOSI) |
| 29    | XHS0            | GPIO2(XHS0)         | GPIO2(XHS0)         |
| 31    | XTRIG0          | GPIO3(XTRIG0)       | GPIO3(XTRIG0)       |
| 33    | PW_EN_0         | PW_EN_0             | PW_EN               |
| 35    | SLAMODE1        | GPIO6               | GPIO6               |
| 37    | GND             | GND                 | GND                 |
| 39    | MCLK_0          | MCLK_0              | MCLK_0              |
| 41    | MCKL_1          | MCKL_1              | MCKL_1              |
| 43    | GND             | GND                 | GND                 |
| 45    | D_CLK_1_P       | D_CLK_1_P           | NC                  |
| 47    | D_CLK_1_N       | D_CLK_1_N           | NC                  |
| 49    | GND             | GND                 | GND                 |
| 51    | D_DATA_0_N      | D_DATA_0_N          | D_DATA_0_N          |
| 53    | D_DATA_0_P      | D_DATA_0_P          | D_DATA_0_P          |
| 55    | GND             | GND                 | GND                 |
| 57    | D_DATA_2_P      | D_DATA_2_P          | D_DATA_2_P          |
| 59    | D_DATA_2_N      | D_DATA_2_N          | D_DATA_2_N          |

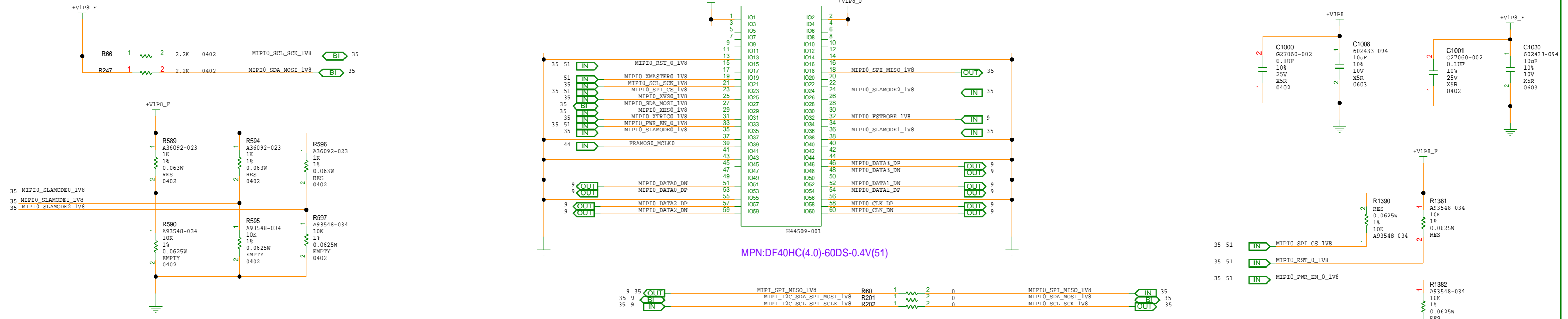
| Pin # | PixelMateC Name | Native MIPI      | SLVS-MIPI Name   |
|-------|-----------------|------------------|------------------|
| 2     | 1V8_VDD         | 1V8_VDD          | 1V8_VDD          |
| 4     | 1V8_VDD         | 1V8_VDD          | 1V8_VDD          |
| 6     | V_DIG           | AUX_DIG          | NC               |
| 8     | V_DIG           | AUX_DIG          | NC               |
| 10    | V_AUX           | AUX_V            | NC               |
| 12    | GND             | GND              | GND              |
| 14    | GND             | GND              | GND              |
| 16    | RST_1           | RST_1            | RST_1            |
| 18    | SPI_MOSI        | GPIO15(SPI_MISO) | GPIO15(SPI_MISO) |
| 20    | XMASTER1        | GPIO8            | EE_MOSI          |
| 22    | I2C_1_SCL       | I2C_1_SCL        | NC               |
| 24    | SPI_CLK         | GPIO16(SW_PW_EN) | GPIO16(SW_PW_EN) |
| 26    | XVS1            | GPIO9            | EE_SCK           |
| 28    | I2C_1_SDA       | I2C_1_SDA        | NC               |
| 30    | XHS1            | GPIO10           | EE_SS            |
| 32    | XTRIG1/FSTROBE  | GPIO11(FSTROBE)  | GPIO11           |
| 34    | PW_EN_1         | PW_EN_1          | CRESET_B         |
| 36    | SLAMODE2        | GPIO7            | GPIO7            |
| 38    | GND             | GND              | GND              |
| 40    | GPIO4(MCLK2)    | GPIO4(MCLK2)     | GPIO4(MCLK2)     |
| 42    | GPIO5(MCLK3)    | GPIO5(MCLK3)     | GPIO5(MCLK3)     |
| 44    | GND             | GND              | GND              |
| 46    | D_DATA_3_P      | D_DATA_3_P       | D_DATA_3_P       |
| 48    | D_DATA_3_N      | D_DATA_3_N       | D_DATA_3_N       |
| 50    | GND             | GND              | GND              |
| 52    | D_DATA_1_N      | D_DATA_1_N       | D_DATA_1_N       |
| 54    | D_DATA_1_P      | D_DATA_1_P       | D_DATA_1_P       |
| 56    | GND             | GND              | GND              |
| 58    | D_DATA_0_P      | D_DATA_0_P       | D_DATA_0_P       |
| 60    | D_DATA_0_N      | D_DATA_0_N       | D_DATA_0_N       |

## MIPI CONN DETAILS

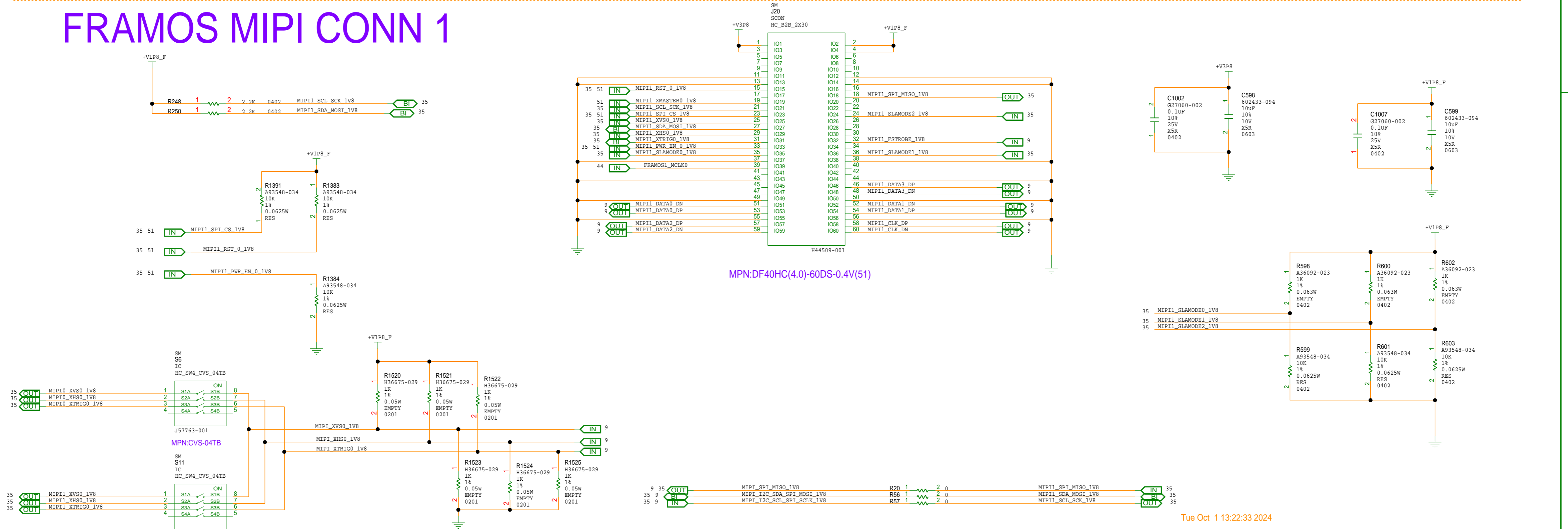
Tue Oct 1 11:17:06 2024

|            |   |                      |       |                 |     |
|------------|---|----------------------|-------|-----------------|-----|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV |
|            |   | C+                   | 34649 | 150-330724-B1   | 2.0 |
| SCALE:     |   | DO NOT SCALE DRAWING |       | SHEET 34 OF 74  |     |

# FRAMOS MIPI CONN 0



# FRAMOS MIPI CONN 1

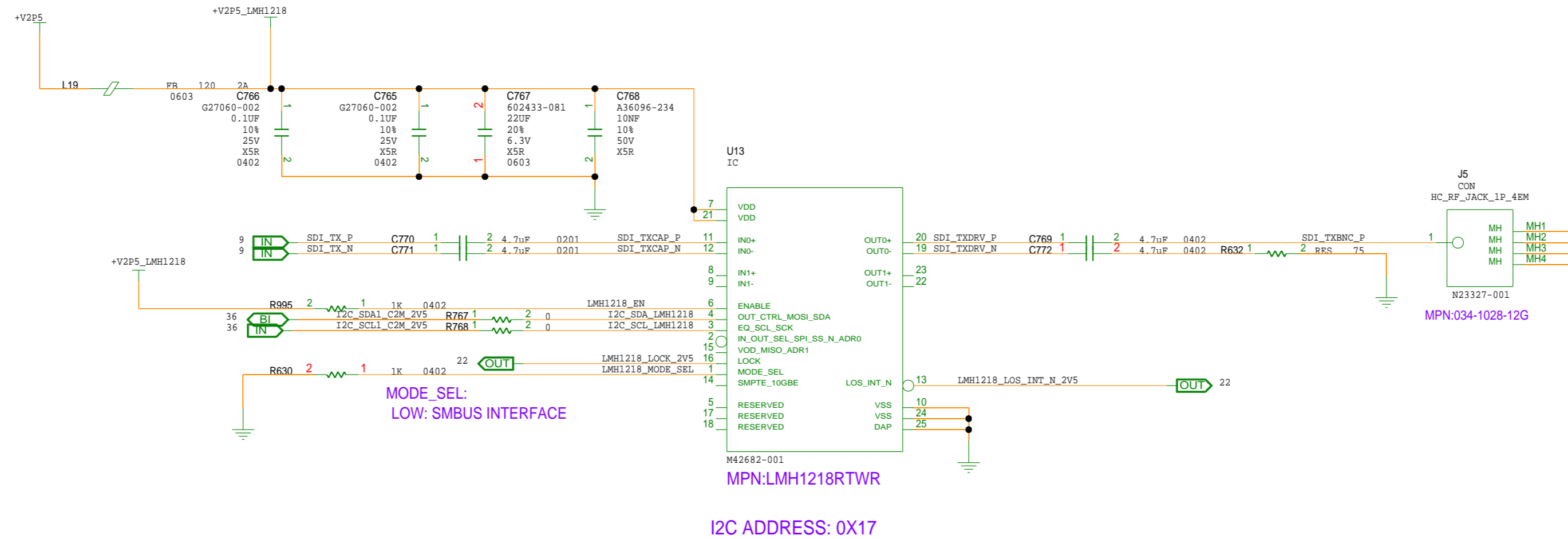


# FRAMOS CONNECTOR

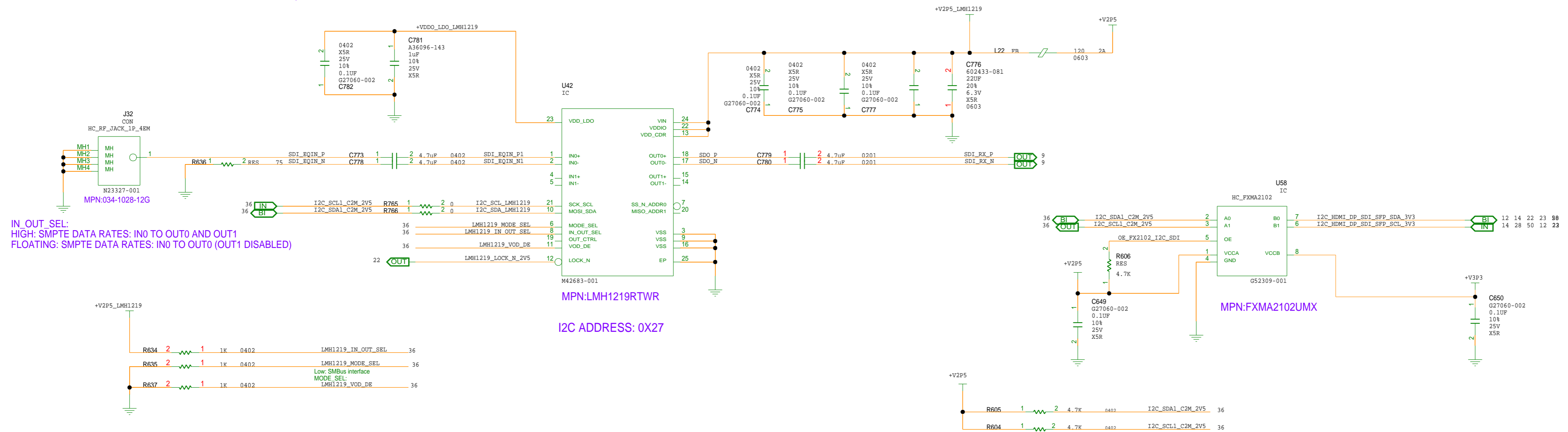
|            |                            |                      |               |                                  |            |
|------------|----------------------------|----------------------|---------------|----------------------------------|------------|
| DEPARTMENT | altera<br>An Intel Company | SIZE<br>C+           | CODE<br>34649 | DOCUMENT NUMBER<br>150-330724-B1 | REV<br>2.0 |
| SCALE:     |                            | DO NOT SCALE DRAWING |               | SHEET                            | 35 OF 74   |

Tue Oct 1 13:22:33 2024

# CABLE DRIVER



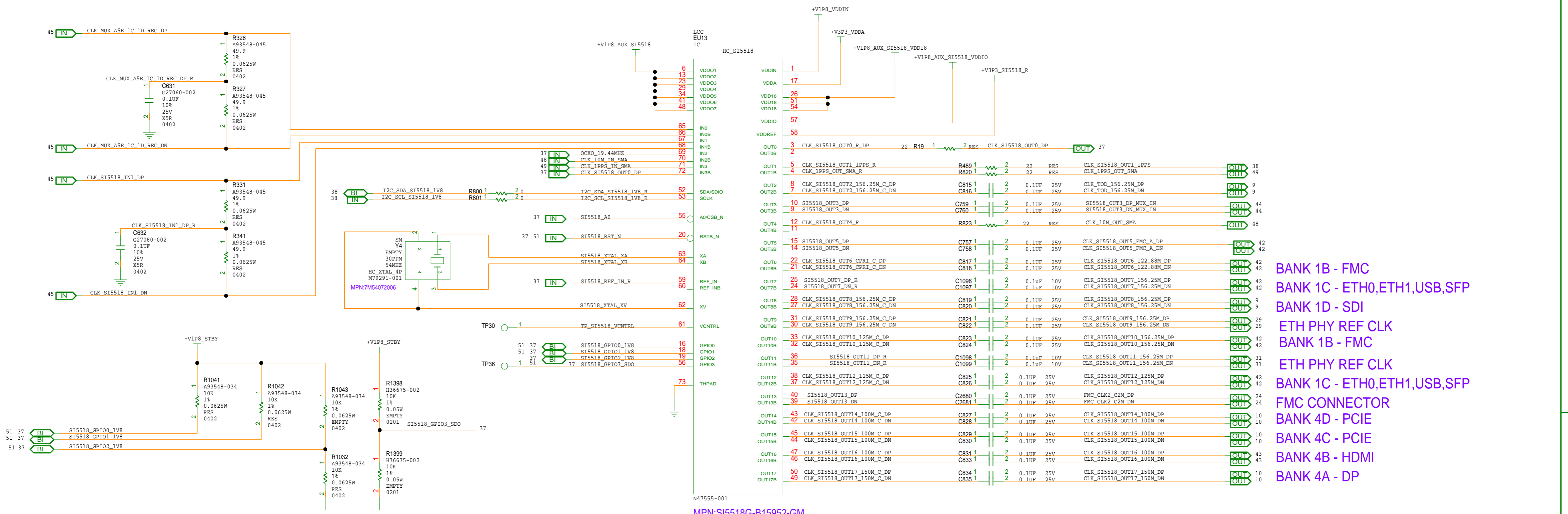
# CABLE EQUALIZER



Tue Oct 1 13:22:34 2024

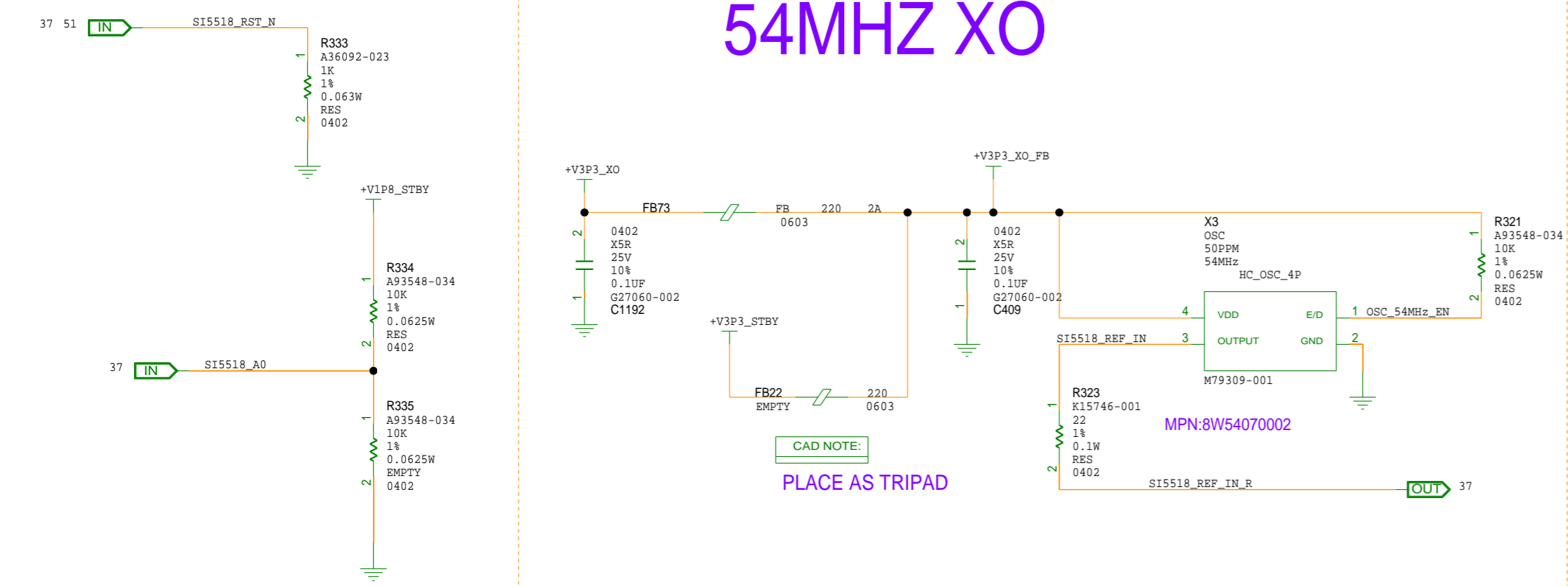
|            |                            |                      |       |                 |                |
|------------|----------------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | altera<br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                            | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                            | DO NOT SCALE DRAWING |       |                 | SHEET 36 OF 74 |

# CLOCK - SI5518

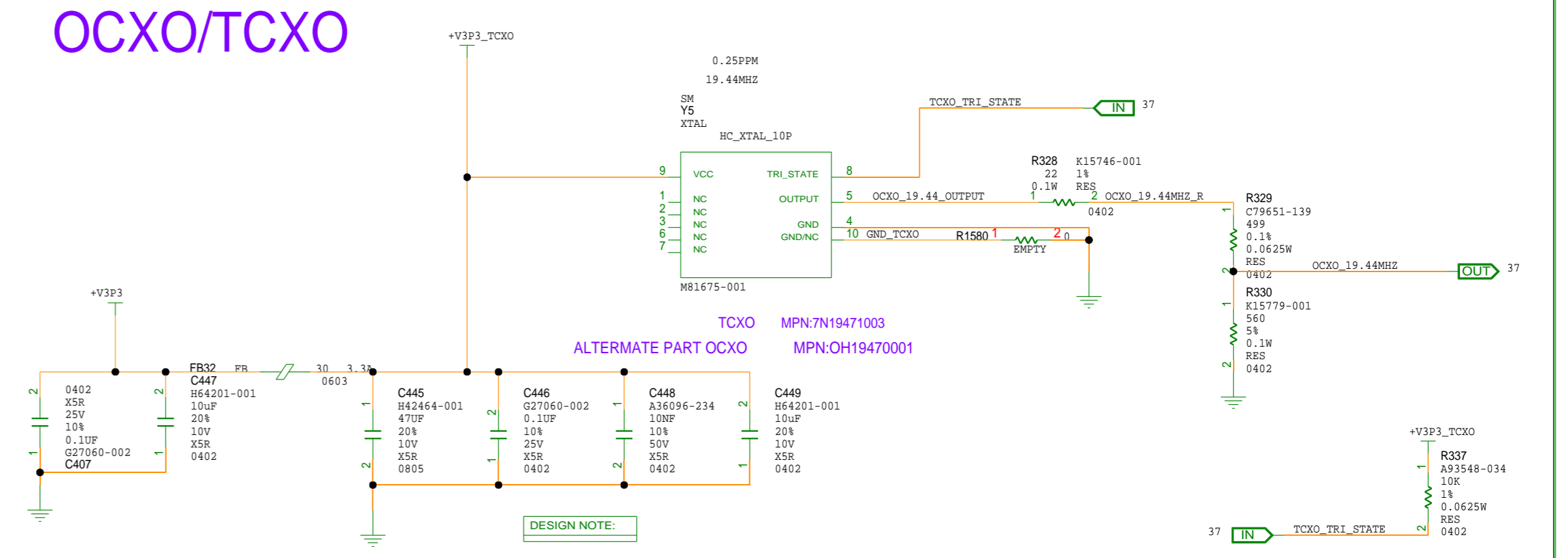


- BANK 1B - FMC
- BANK 1C - ETH0,ETH1,USB,SFP
- BANK 1D - SDI
- ETH PHY REF CLK
- BANK 1B - FMC
- ETH PHY REF CLK
- BANK 1C - ETH0,ETH1,USB,SFP
- FMC CONNECTOR
- BANK 4D - PCIE
- BANK 4C - PCIE
- BANK 4B - HDMI
- BANK 4A - DP

## 54MHZ XO



## OCXO/TCXO

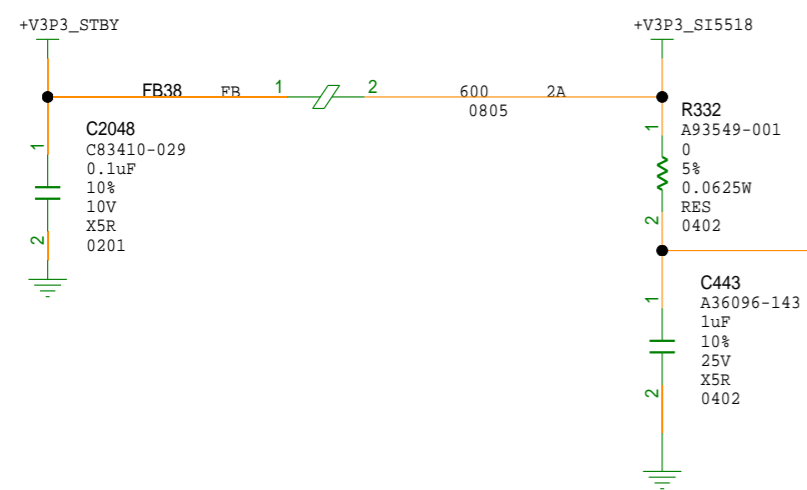
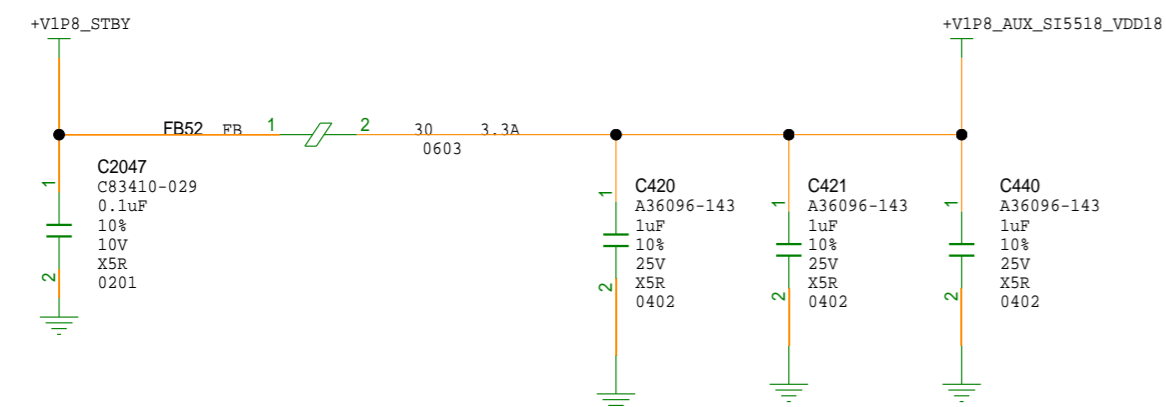
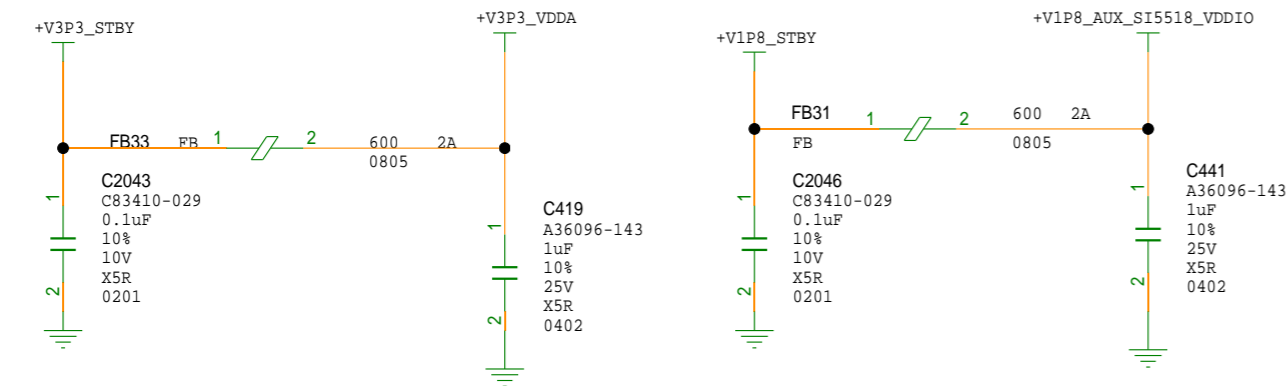
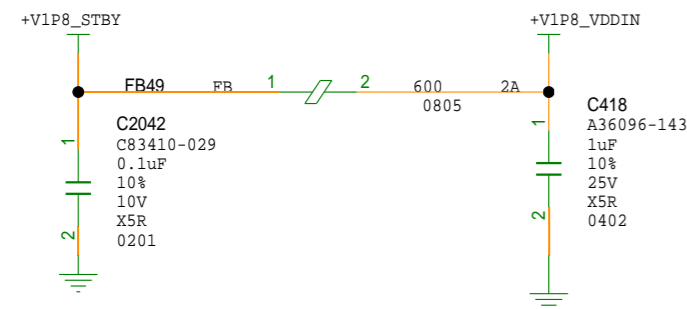
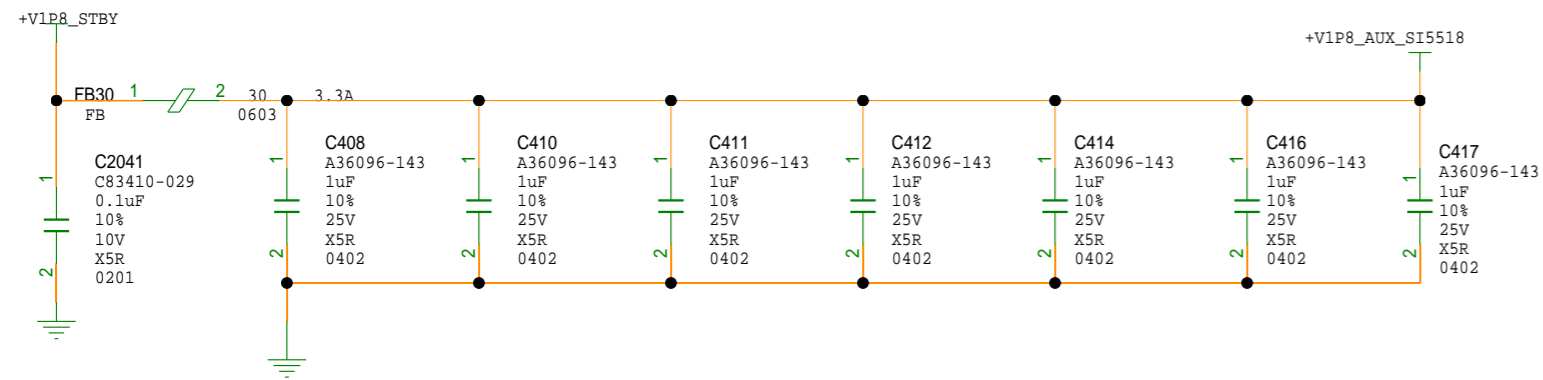


# CLOCK-SI5518

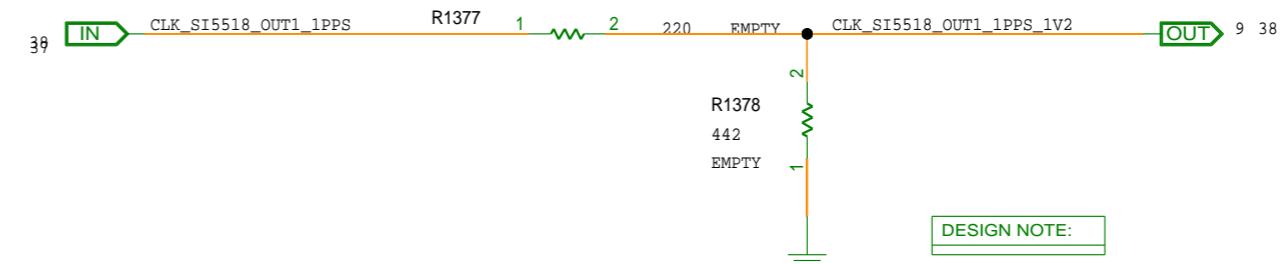
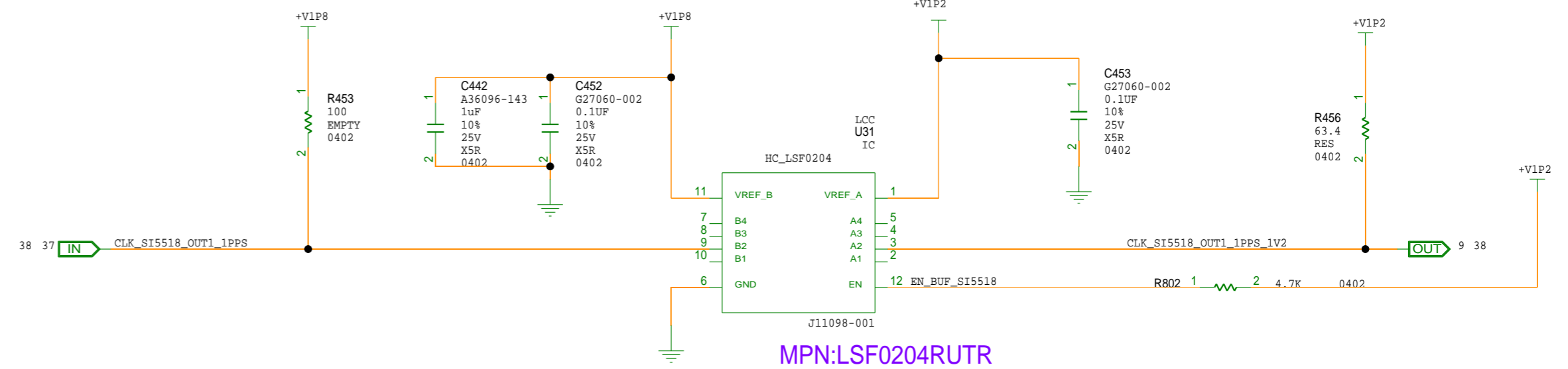
|            |                            |                      |               |                                  |            |
|------------|----------------------------|----------------------|---------------|----------------------------------|------------|
| DEPARTMENT | altera<br>An Intel Company | SIZE<br>C+           | CODE<br>34649 | DOCUMENT NUMBER<br>150-330724-B1 | REV<br>2.0 |
| SCALE:     |                            | DO NOT SCALE DRAWING |               | SHEET 37 OF 74                   |            |

Tue Oct 1 13:22:34 2024

# SUPPLY DE-CAP

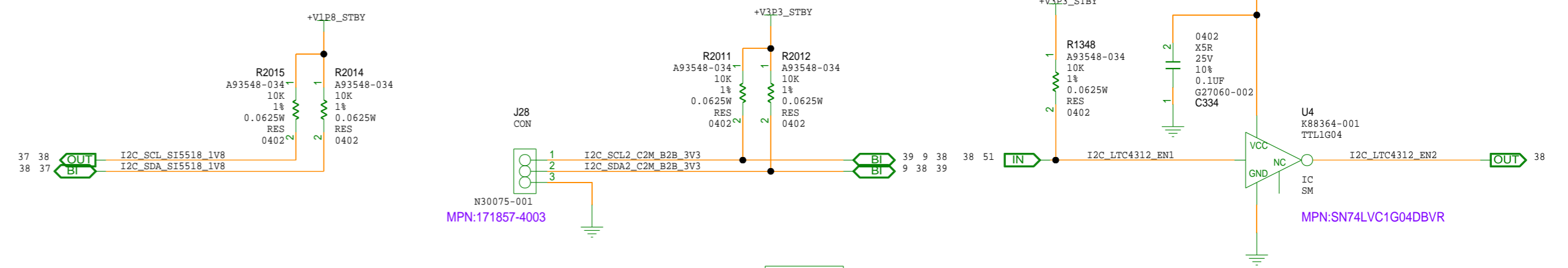


# LEVEL SHIFTER

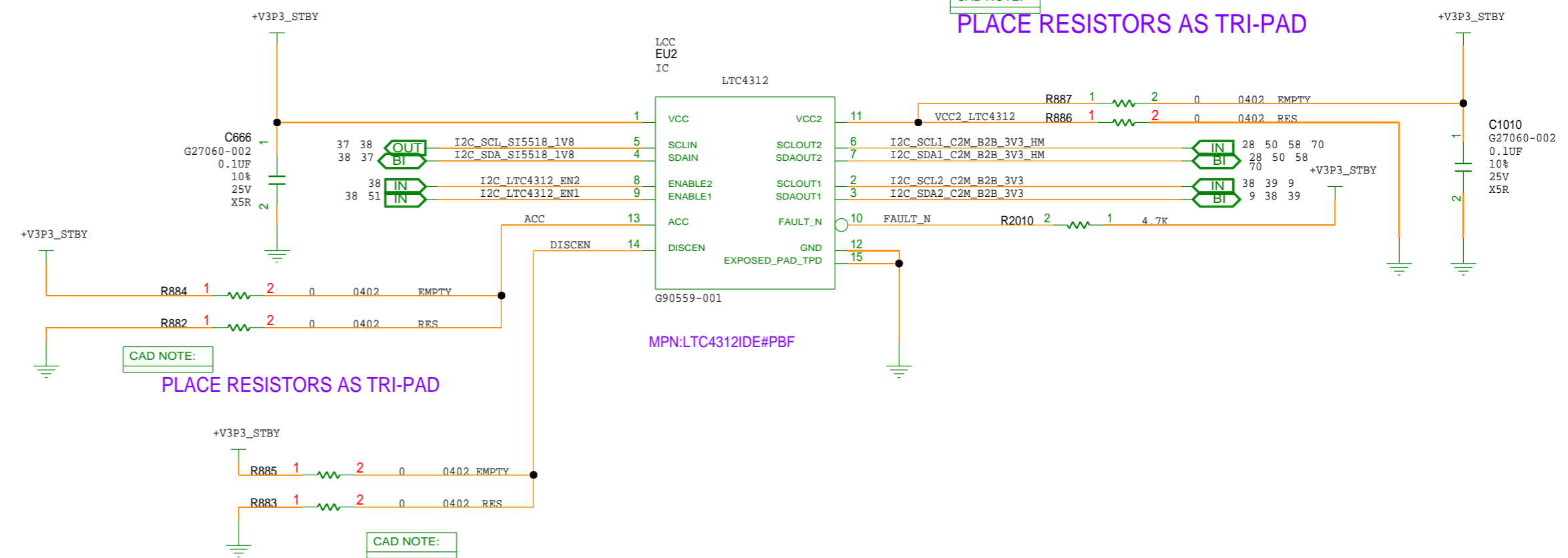


DESIGN NOTE:  
BYPASS PATH FOR 1PPS OUT

# PROGRAMING HEADER



CAD NOTE:  
PLACE RESISTORS AS TRI-PAD



CAD NOTE:  
PLACE RESISTORS AS TRI-PAD

CAD NOTE:  
PLACE RESISTORS AS TRI-PAD

# CLOCK-SI5518

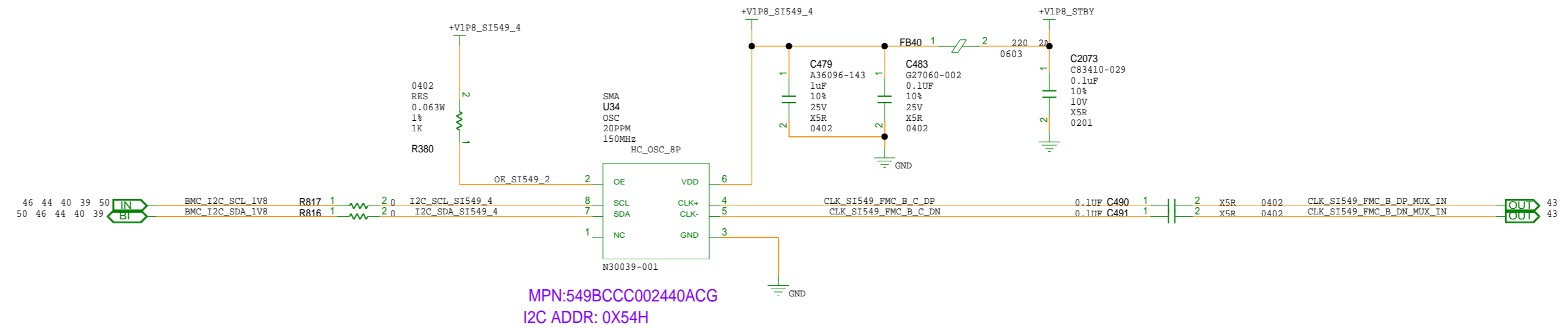
Tue Oct 1 13:22:34 2024

|            |                      |                      |       |                 |                |
|------------|----------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                      | DO NOT SCALE DRAWING |       |                 | SHEET 38 OF 74 |

# FMC-B CLOCK - SI549

DESIGN NOTE:

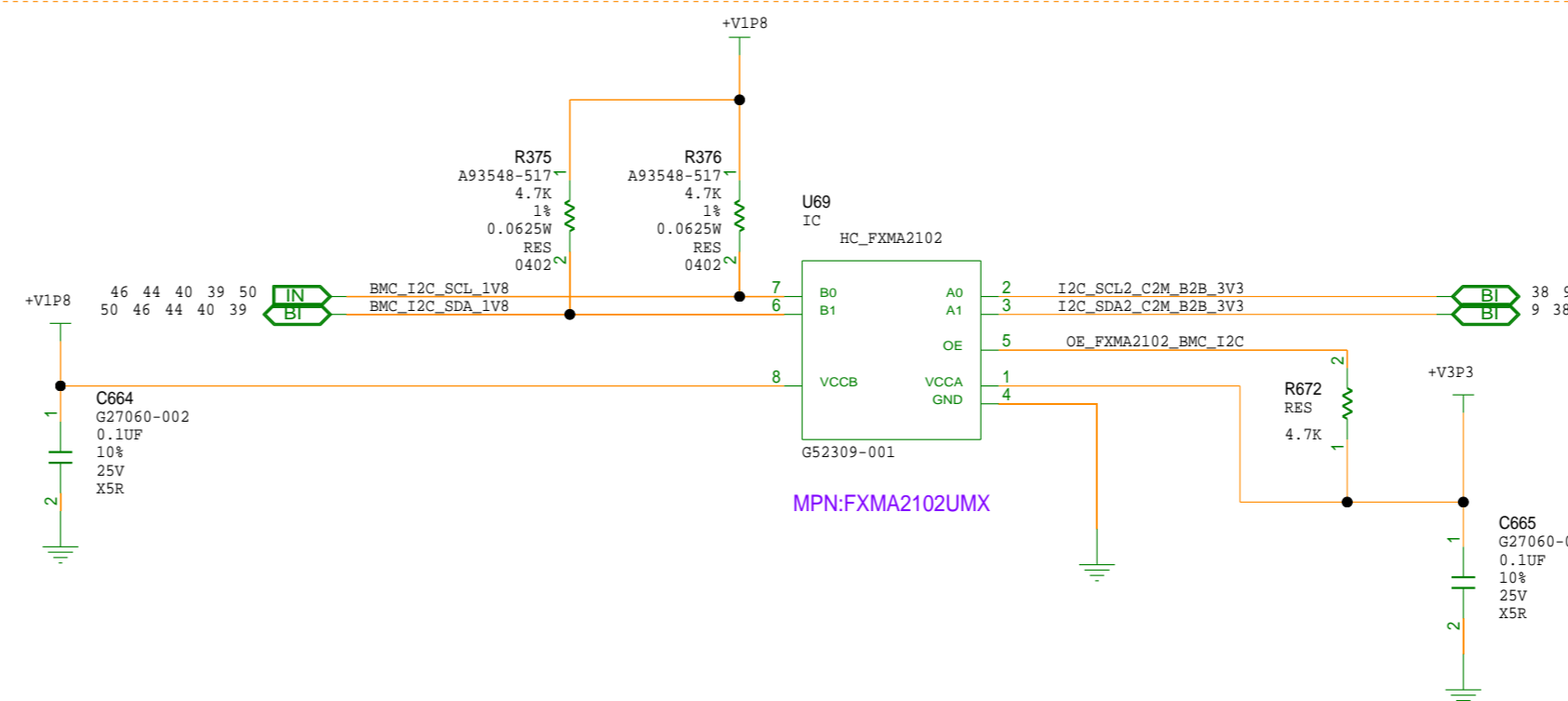
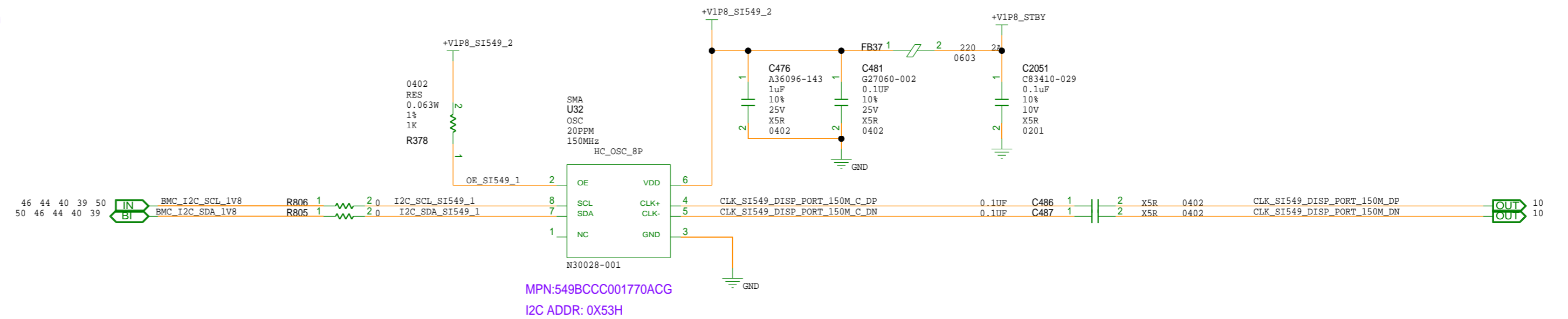
|   |   |
|---|---|
| Part Number                             | 549BCCC002440ACG                          |
| Model Number                            | Si549                                     |
| Startup Frequency (MHz)                 | 150.000000                                |
| I2C Address                             | 54 (Hex)                                  |
| Output Format and Supply Voltage        | LVDS: 1.8 V, 2.5 V, 3.3 V                 |
| Temperature Stability / Total Stability | +/- 7 ppm / 20 ppm                        |
| OE Pin Location and Polarity            | OE Pin2, Active High                      |
| Frequency Range                         | 0.2 - 325 MHz (CMOS available to 250 MHz) |
| Package Option                          | 5x7 mm                                    |
| Operating Temp Range (°C):              | -40 to +85                                |



# DP CLOCK - SI549

DESIGN NOTE:

|   |   |
|---|---|
| Part Number                             | 549BCCC001770ACG                          |
| Model Number                            | Si549                                     |
| Startup Frequency (MHz)                 | 150.000000                                |
| I2C Address                             | 53 (Hex)                                  |
| Output Format and Supply Voltage        | LVDS: 1.8 V, 2.5 V, 3.3 V                 |
| Temperature Stability / Total Stability | +/- 7 ppm / 20 ppm                        |
| OE Pin Location and Polarity            | OE Pin2, Active High                      |
| Frequency Range                         | 0.2 - 325 MHz (CMOS available to 250 MHz) |
| Package Option                          | 5x7 mm                                    |
| Operating Temp Range (°C):              | -40 to +85                                |



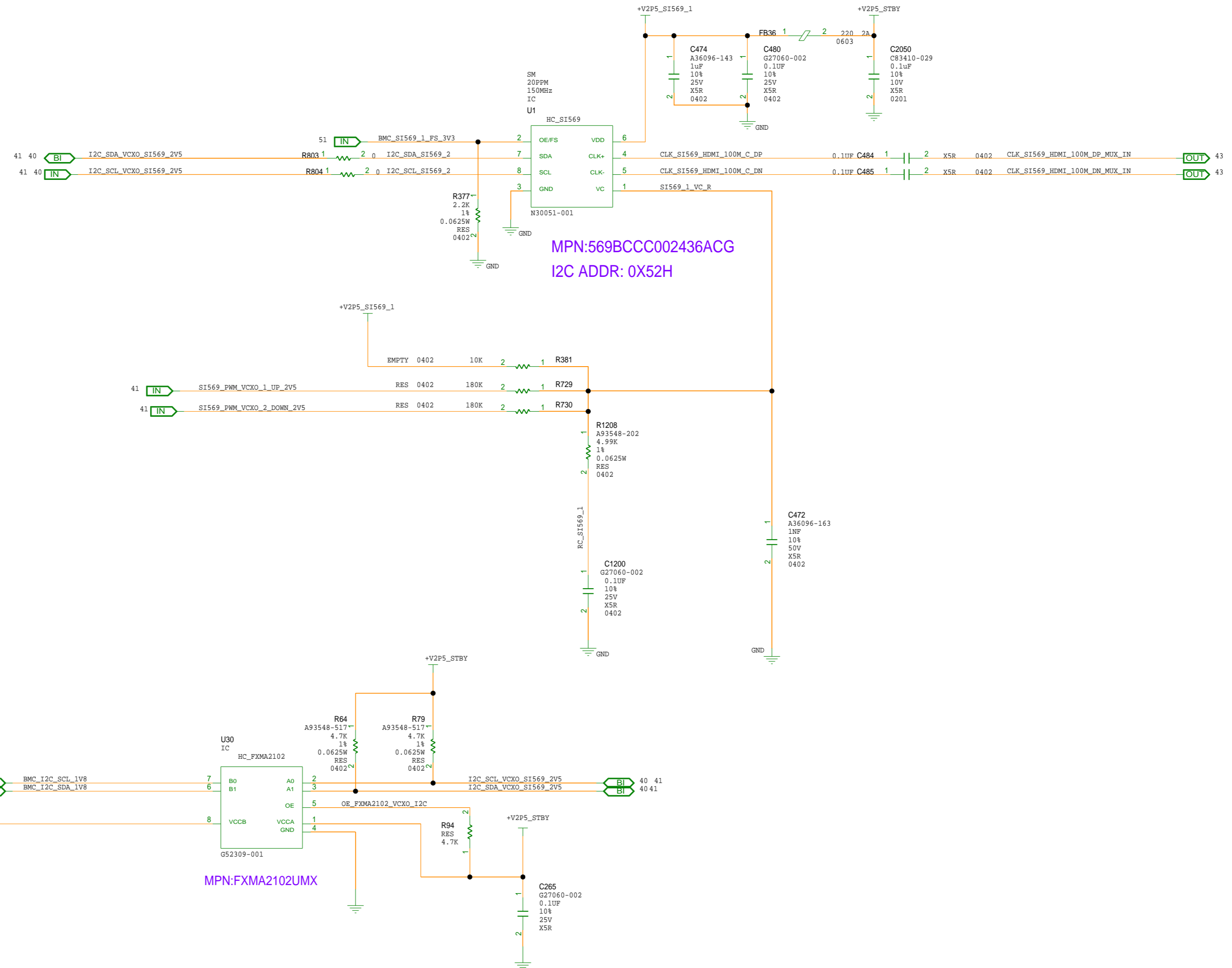
Tue Oct 1 13:22:34 2024

# CLOCK-SI569

|            |                      |      |       |                 |          |
|------------|----------------------|------|-------|-----------------|----------|
| DEPARTMENT | <br>An Intel Company | SIZE | CODE  | DOCUMENT NUMBER | REV      |
|            |                      | C+   | 34649 | 150-330724-B1   | 2.0      |
| SCALE:     | DO NOT SCALE DRAWING |      |       | SHEET           | 39 OF 74 |


# HDMI CLOCK - SI569

|                                  |                           |
|----------------------------------|---------------------------|
| Part Number                      | 569BCCC002436ACG          |
| Model Number                     | SI569                     |
| Startup Frequency (MHz):         |                           |
| FS=0:                            | 100.000000                |
| FS=1:                            | 150.000000                |
| I2C Address                      | 52 (Hex)                  |
| Output Format and Supply Voltage | LVDS: 1.8 V, 2.5 V, 3.3 V |
| Temperature Stability            | +/- 20 ppm                |
| Tuning Slope                     | 105 ppm/V                 |
| OE Pin Location and Polarity     | No OE Pin, FS0 Pin2       |
| Frequency Range                  | 0.2 - 800 MHz             |
| Package Option                   | 5x7 mm                    |
| Operating Temp Range (°C):       | -40 to +85                |



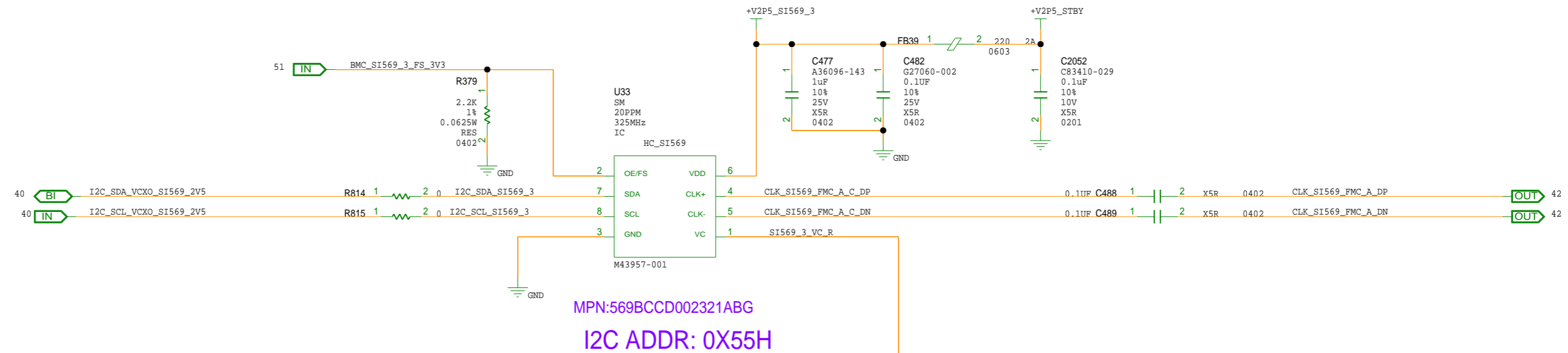
Tue Oct 1 13:22:35 2024

## CLOCK\_HDMI\_SI569

|            |   |                      |       |                 |                |
|------------|---|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |   | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |   | DO NOT SCALE DRAWING |       |                 | SHEET 40 OF 74 |



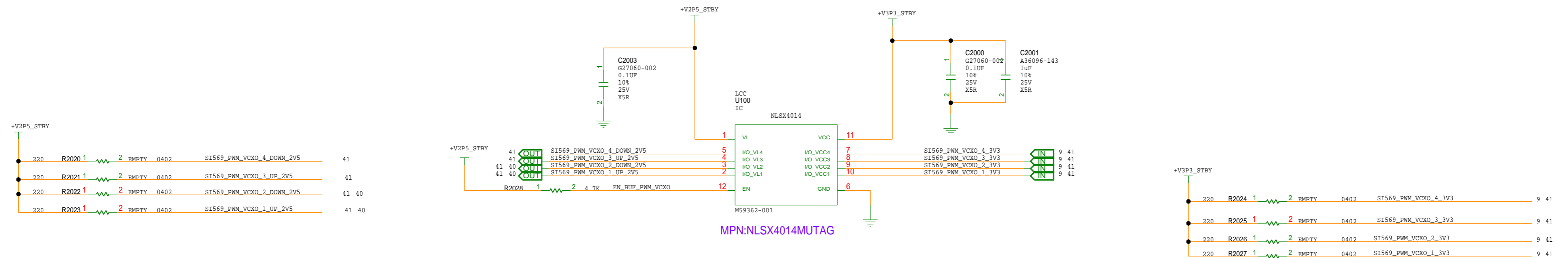
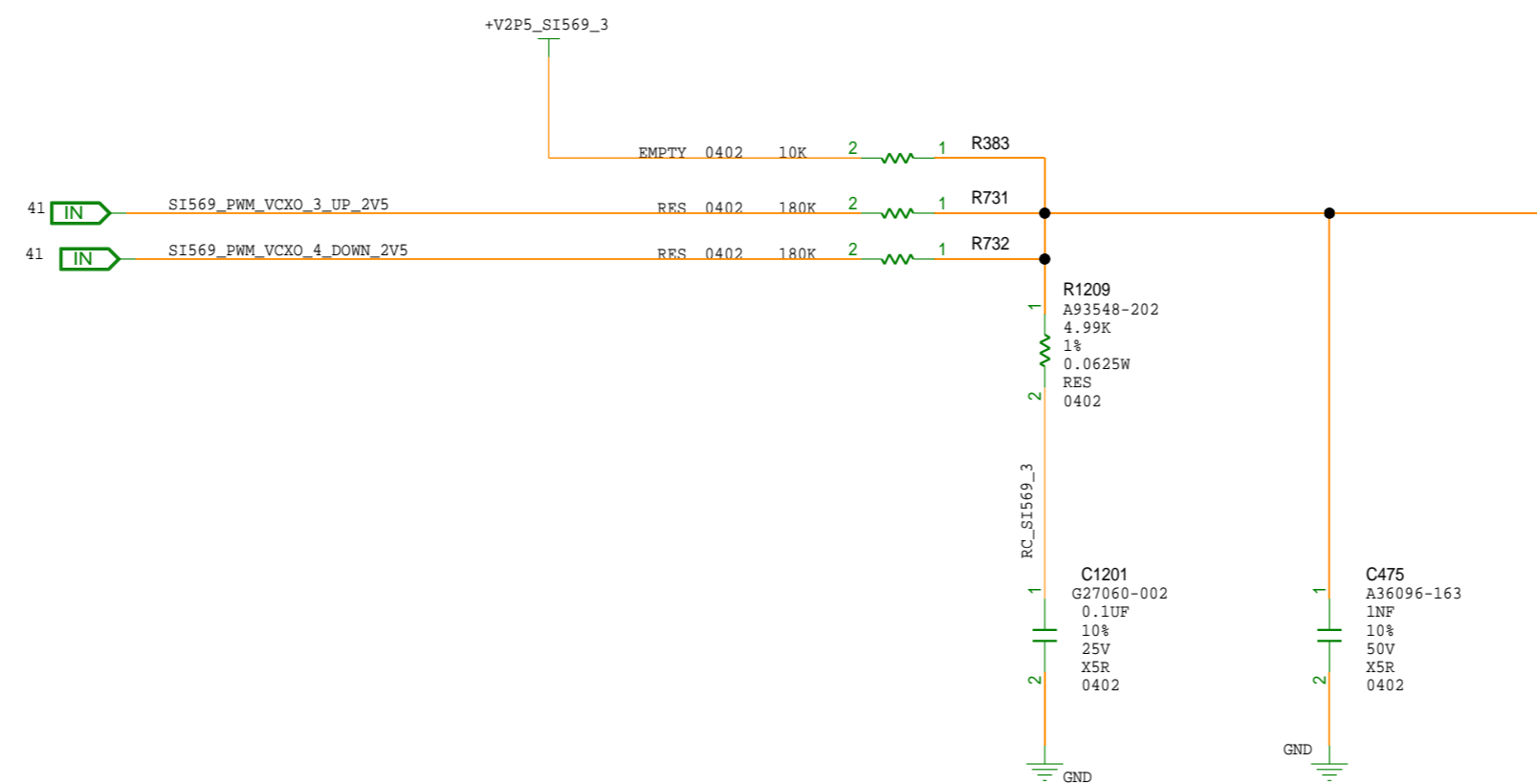
# FMC-A CLOCK - SI569



DESIGN NOTE:

Frequency A 148.35 MHz If Fs=0

Frequency B 148.5 MHz If Fs=1

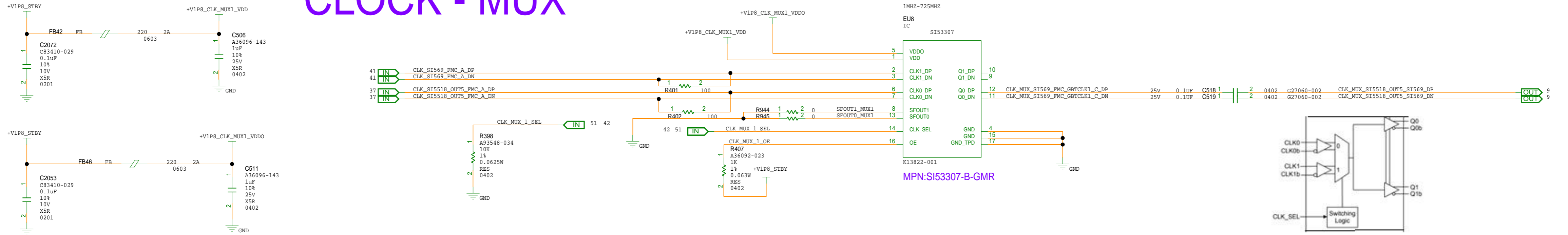


Tue Oct 1 13:22:35 2024

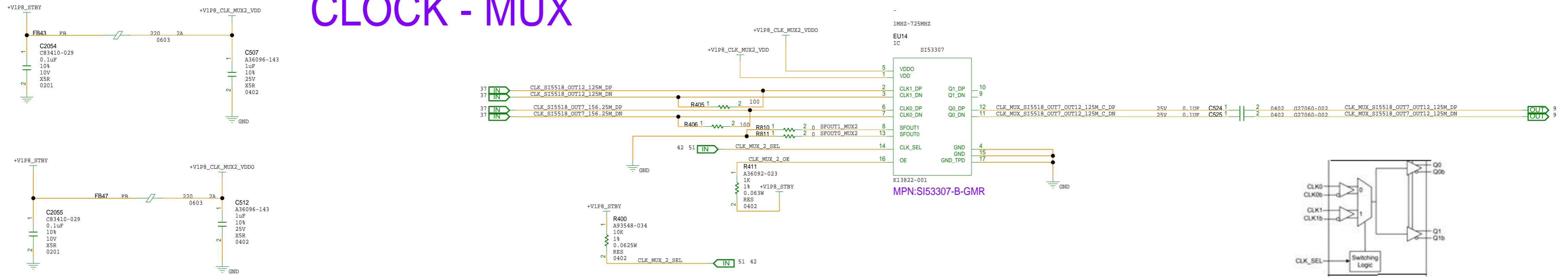
# CLOCK-SI569

|            |                      |                      |       |                 |                |
|------------|----------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                      | DO NOT SCALE DRAWING |       |                 | SHEET 41 OF 74 |

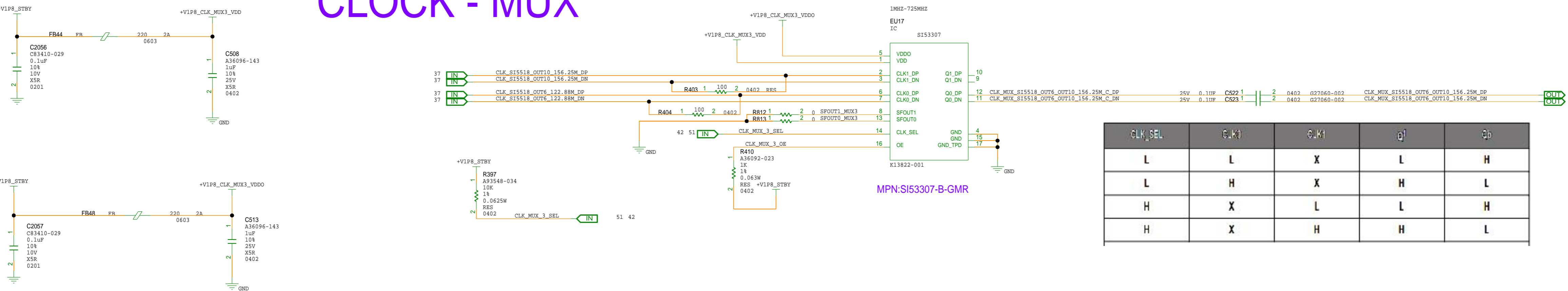
# CLOCK - MUX



# CLOCK - MUX




# CLOCK - MUX

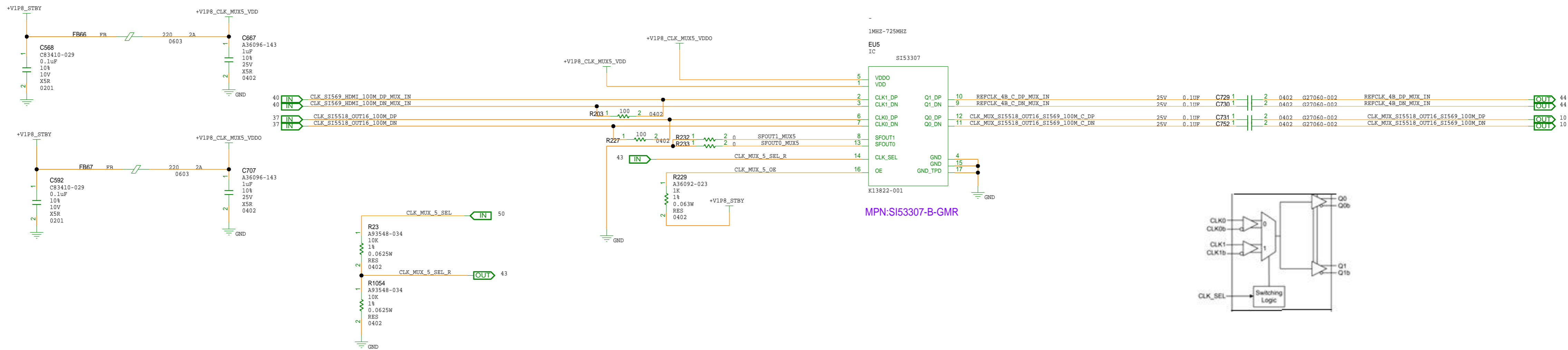


# CLOCK - MUX

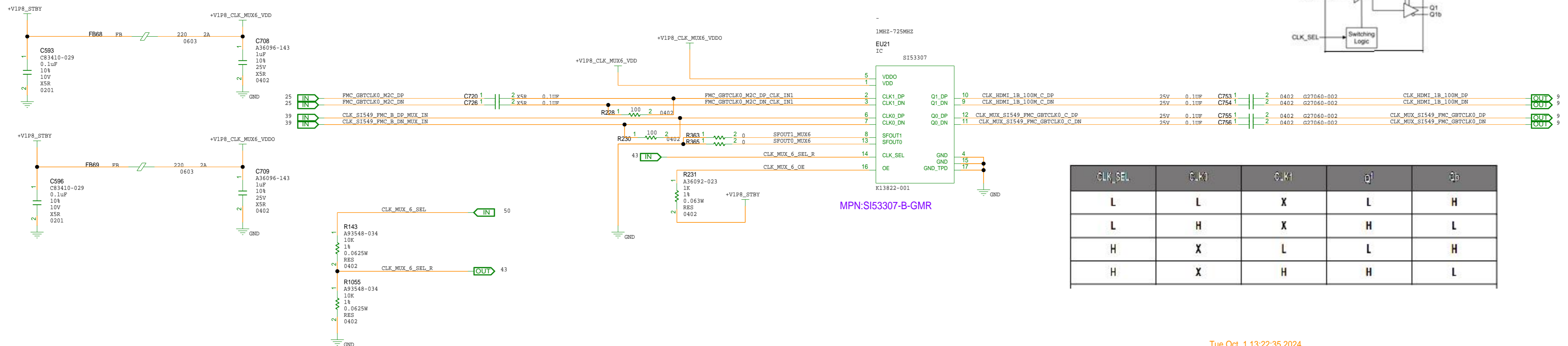
Tue Oct 1 13:22:35 2024

|            |   |                      |       |                 |          |
|------------|---|----------------------|-------|-----------------|----------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV      |
|            |   | C+                   | 34649 | 150-330724-B1   | 2.0      |
| SCALE:     |   | DO NOT SCALE DRAWING |       | SHEET           | 42 OF 74 |

# CLOCK - MUX



# CLOCK - MUX



| CLK_SEL | CLK0 | CLK1 | Q1 | Qb |
|---------|------|------|----|----|
| L       | L    | X    | L  | H  |
| L       | H    | X    | H  | L  |
| H       | X    | L    | L  | H  |
| H       | X    | H    | H  | L  |

Tue Oct 1 13:22:35 2024

# CLOCK - MUX

DEPARTMENT



SIZE  
C+

CODE  
34649

DOCUMENT NUMBER

150-330724-B1

REV  
2.0

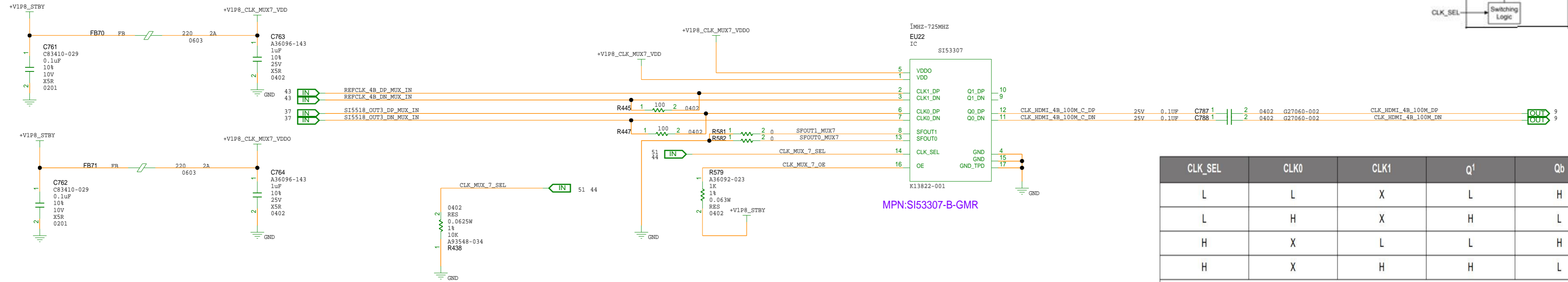
SCALE:

DO NOT SCALE DRAWING

SHEET

43 OF 74

# CLOCK - MUX

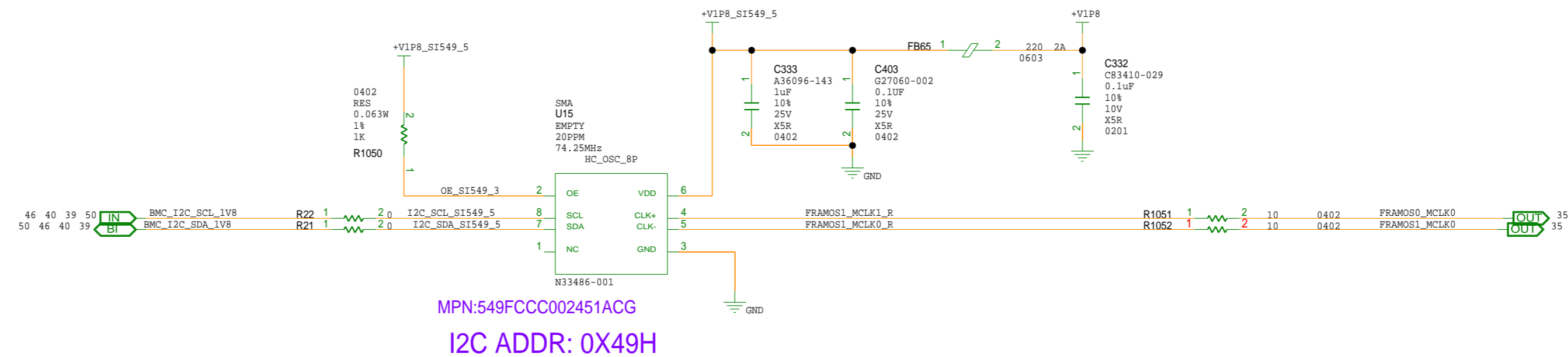


# FRAMOS MCLK SOURCE

Created part number 549FCCC002451ACG

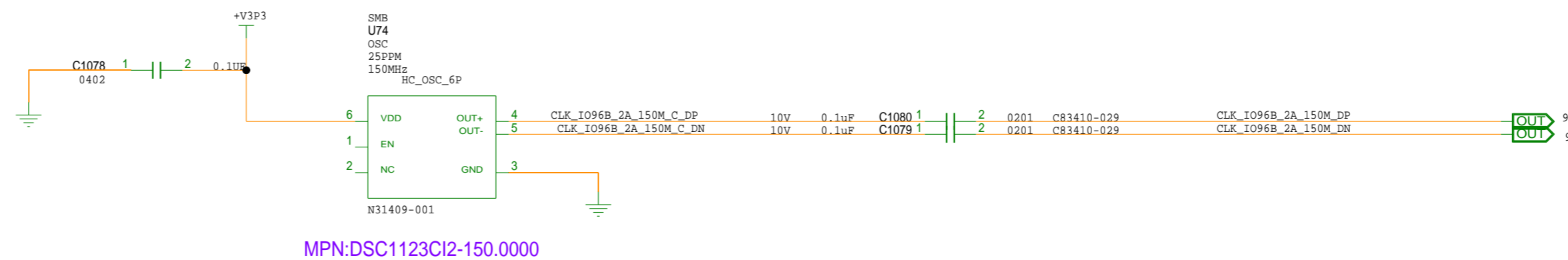
**Custom Part Number Specification:**

Part Number 549FCCC002451ACG  
 Model Number SI549  
 Startup Frequency (MHz) 74.2500000  
 I2C Address 49 (Hex)  
 Output Format and Supply Voltage In-phase dual CMOS: 1.8 V, 2.5 V, 3.3 V  
 Temperature Stability / Total Stability +/- 7 ppm / 20 ppm  
 OE Pin Location and Polarity OE Pin2, Active High  
 Frequency Range 0.2 - 325 MHz (CMOS available to 250 MHz)  
 Package Option 5x7 mm  
 Operating Temp Range (°C): -40 to +85



MPN:549FCCC002451ACG  
 I2C ADDR: 0X49H

# 150MHZ XO FOR 2A BANK



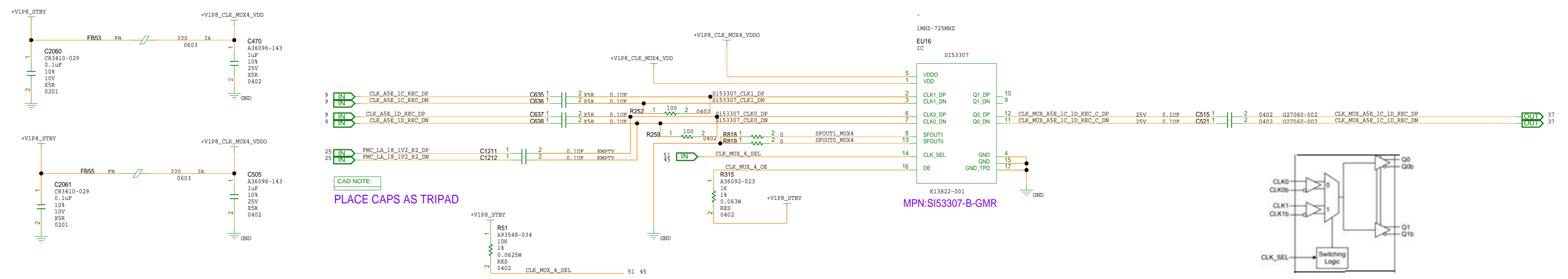
MPN:DSC1123CI2-150.0000

Tue Oct 1 13:22:36 2024

# CLOCK - MUX

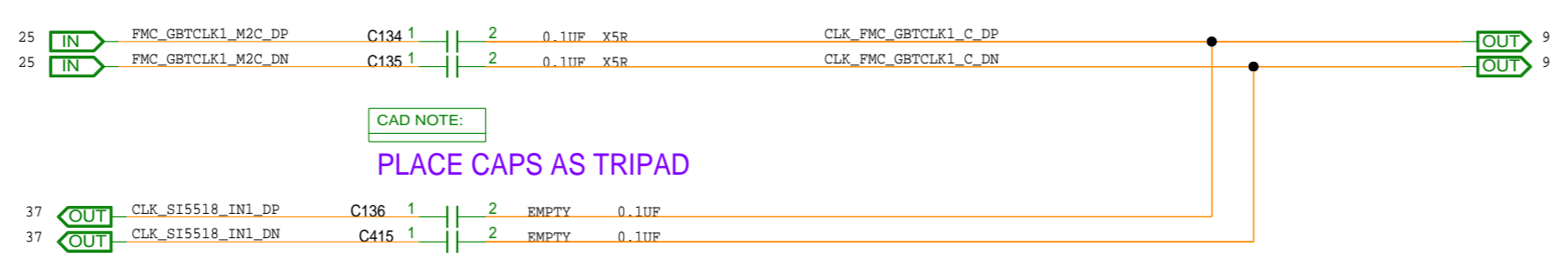
|            |                      |                      |       |                 |                |
|------------|----------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                      | DO NOT SCALE DRAWING |       |                 | SHEET 44 OF 74 |

# CLOCK - MUX



CAD NOTE:  
PLACE CAPS AS TRIPAD

MPN:SI53307-B-GMR



CAD NOTE:  
PLACE CAPS AS TRIPAD

# CLOCK MUX TABLE

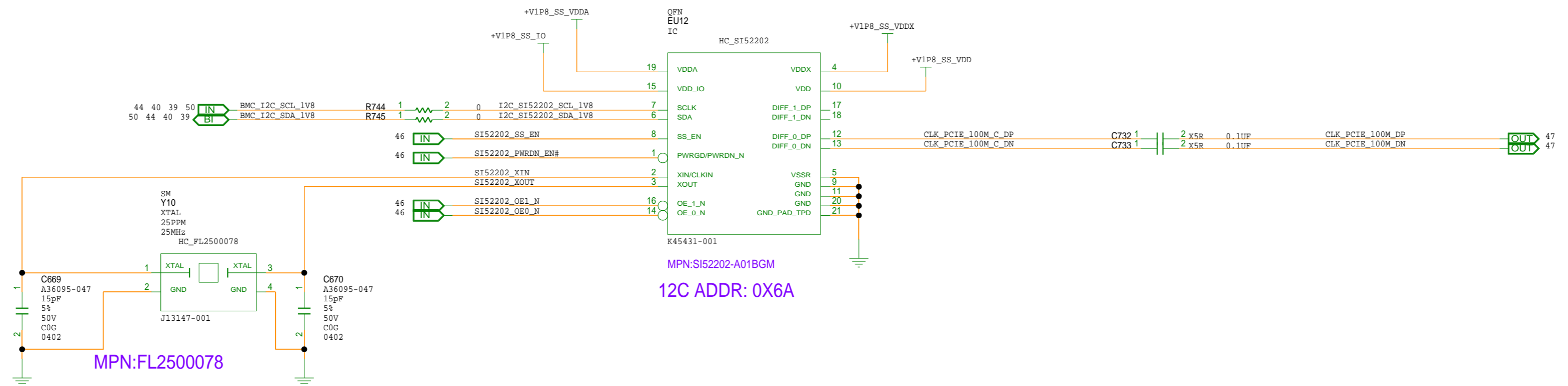
Table 2.5. Input Mux Logic

| CLK_SEL | CLK0 | CLK1 | Q <sup>1</sup> | Q <sup>b</sup> |
|---------|------|------|----------------|----------------|
| L       | L    | X    | L              | H              |
| L       | H    | X    | H              | L              |
| H       | X    | L    | L              | H              |
| H       | X    | H    | H              | L              |

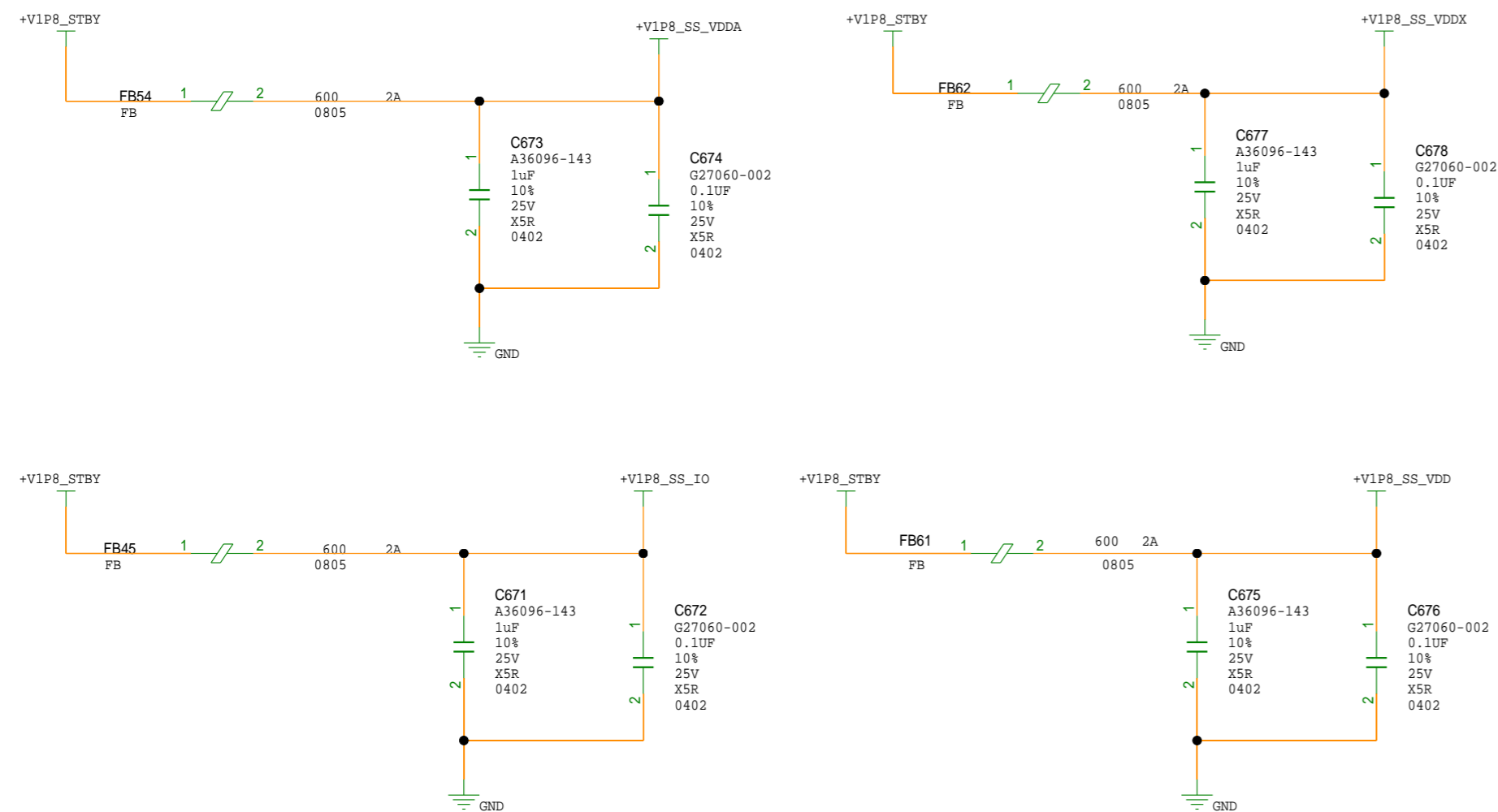
Note:  
1. On the next negative transition of CLK0 or CLK1.

Tue Oct 1 13:22:36 2024

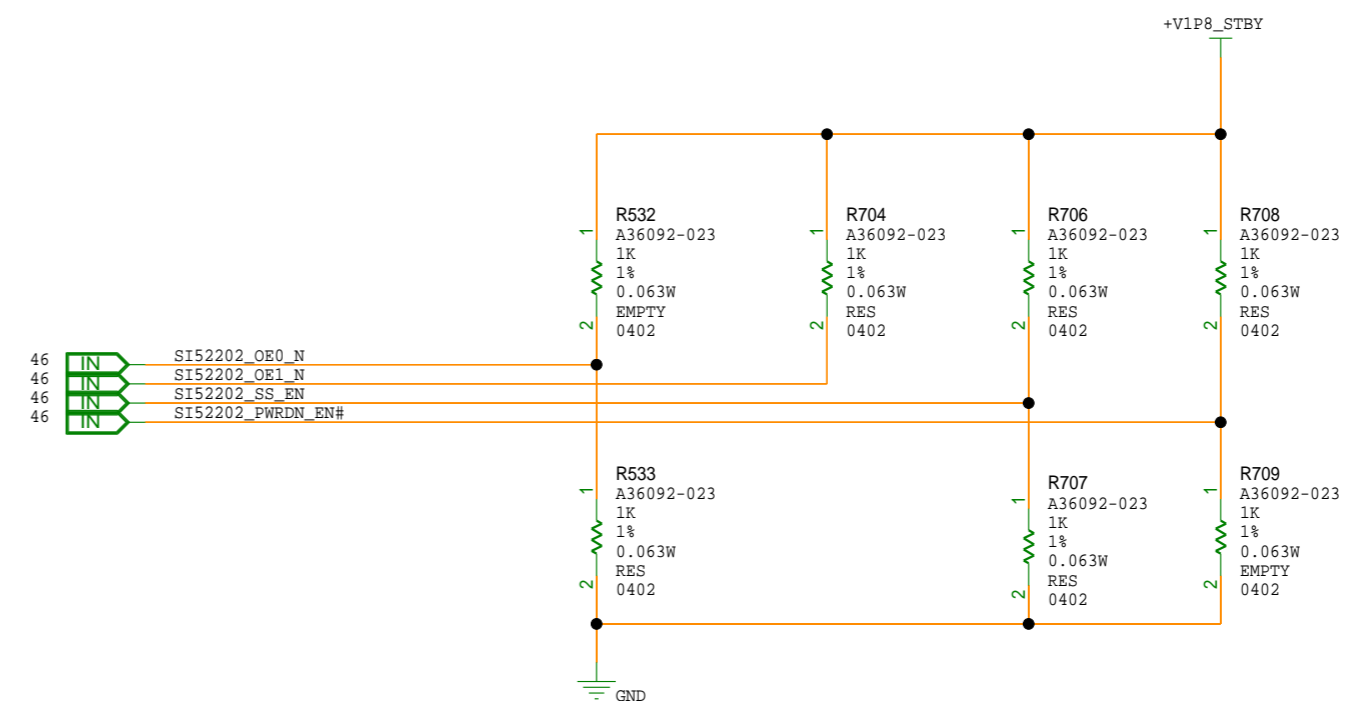
# PCIe 100MHz CLOCK SOURCE



## POWER SUPPLY DE-CAP



## SI52202 CONTROLS SETTING



Tue Oct 1 13:22:36 2024

# CLOCK-SI52202

DEPARTMENT



SIZE

CODE

DOCUMENT NUMBER

REV

C+

34649

150-330724-B1

2.0

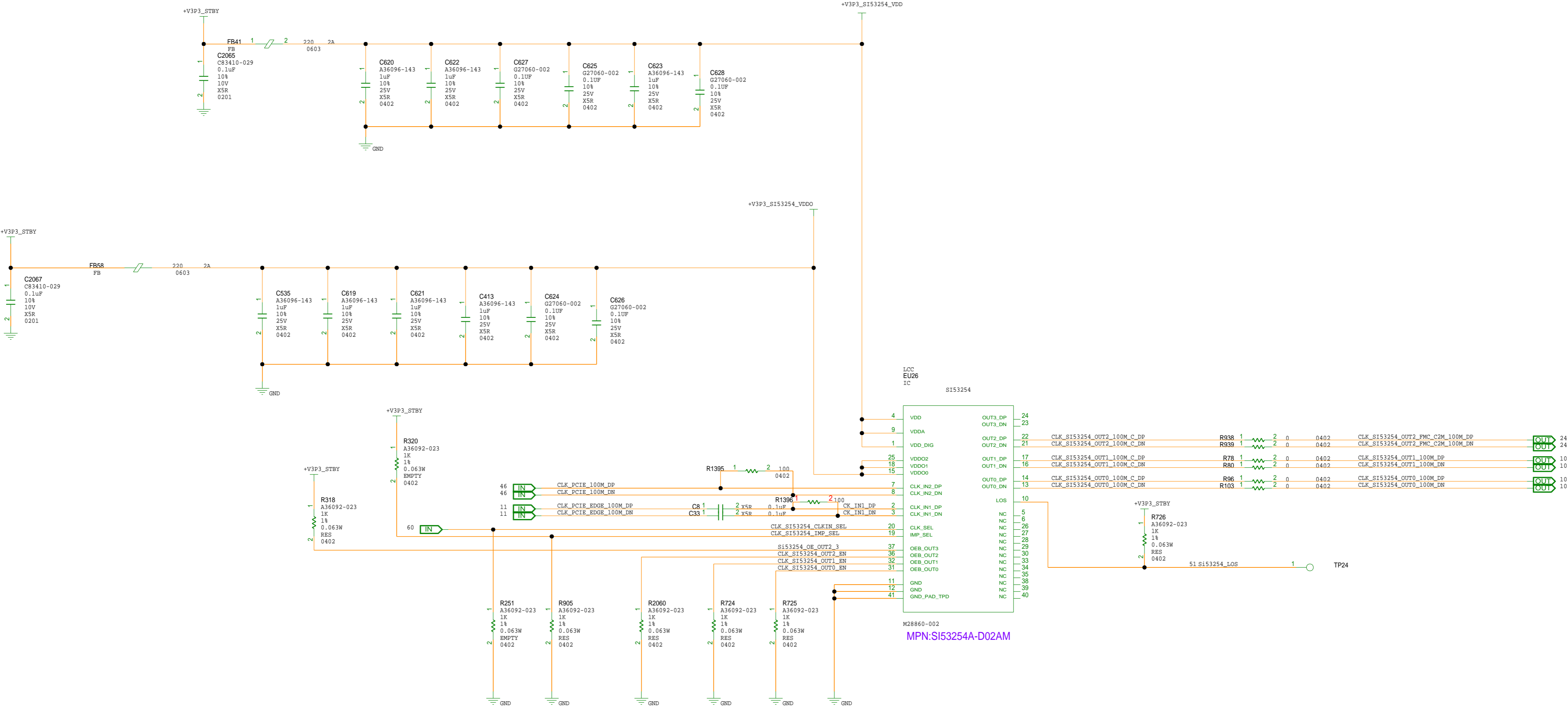
SCALE:

DO NOT SCALE DRAWING

SHEET

46 OF 74


# PCIE CLOCK BUFFER



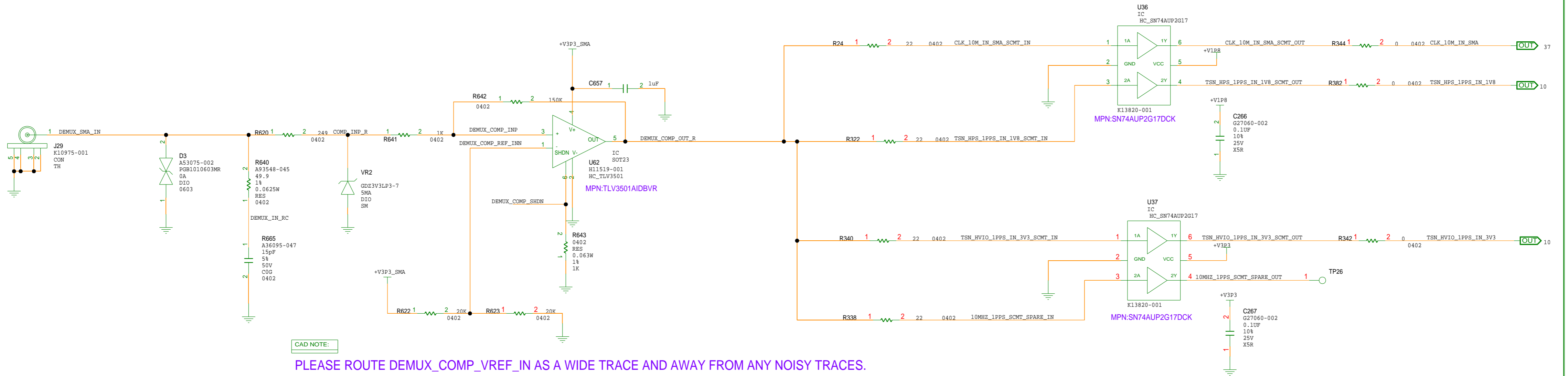
DESIGN NOTE:  
 CLKSEL=0 SELECTS CLK\_IN1  
 CLKSEL=1 SELECTS CLK\_IN2

Tue Oct 1 13:22:36 2024

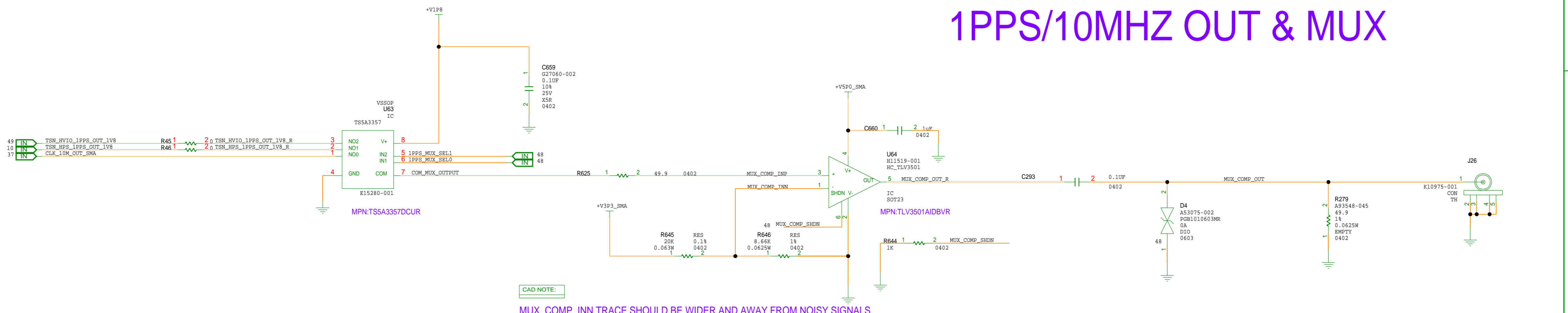
CLOCK\_MUX\_SI53254

|            |   |                      |       |                 |          |
|------------|---|----------------------|-------|-----------------|----------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV      |
|            |   | C+                   | 34649 | 150-330724-B1   | 2.0      |
| SCALE:     |   | DO NOT SCALE DRAWING |       | SHEET           | 47 OF 74 |

# 1PPS/10MHZ IN & DE-MUX



# 1PPS/10MHZ OUT & MUX



# MUX & DEMUX SEL SETTING

TSA5A3357 FUNCTIONAL TABLE

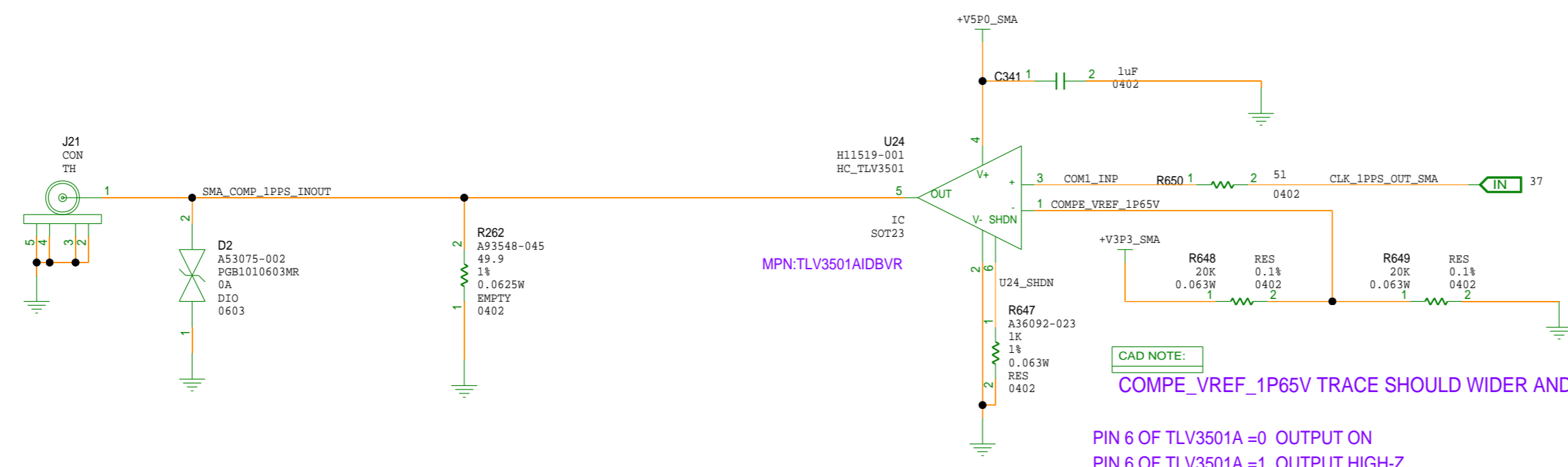
| IN1 | IN2 | COM TO NO0 | COM TO NO1 | COM TO NO2 |
|-----|-----|------------|------------|------------|
| L   | L   | OFF        | OFF        | OFF        |
| H   | L   | ON         | OFF        | OFF        |
| L   | H   | OFF        | ON         | OFF        |
| H   | H   | OFF        | OFF        | ON         |

Tue Oct 1 13:22:37 2024



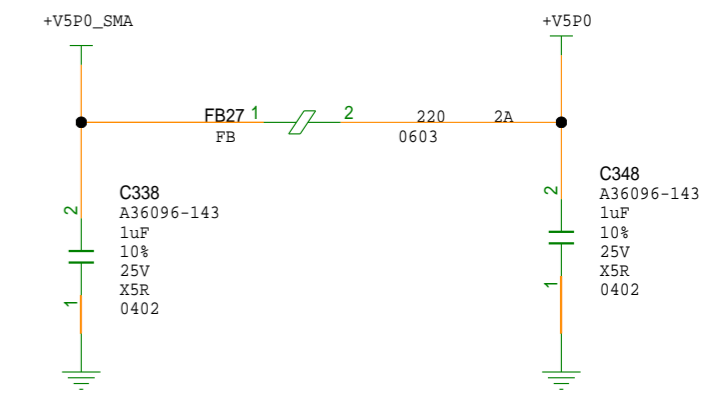
# 1PPS CLK OUT

VIN MIN 0-0.5V  
VIN MAX 0-5.5V

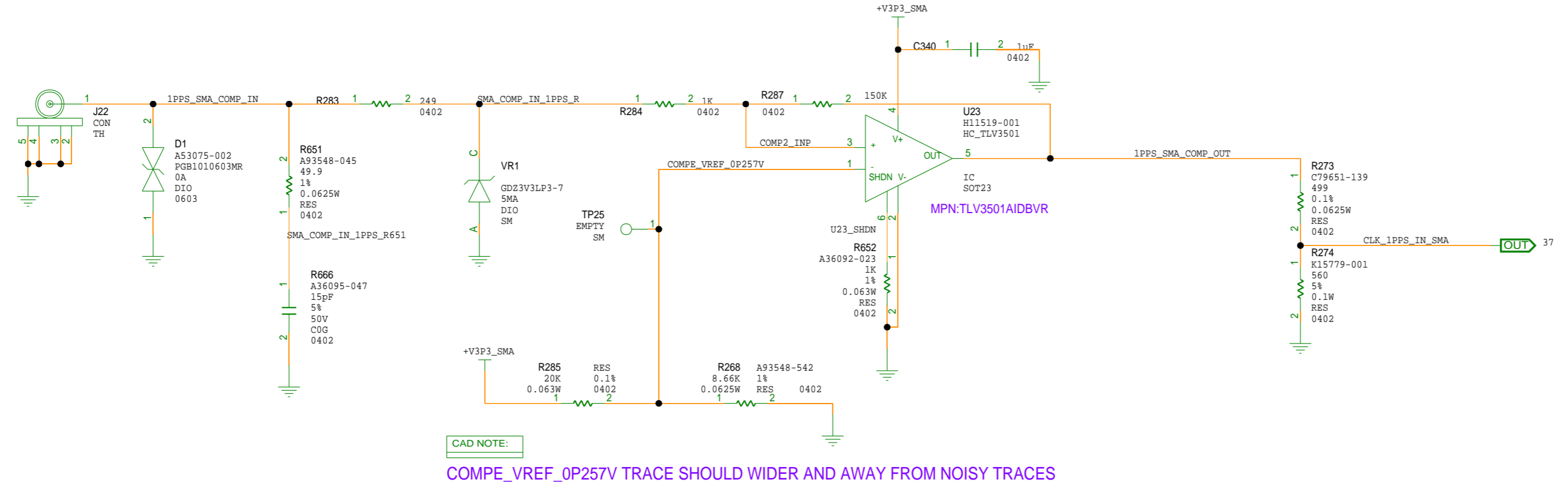


CAD NOTE:  
COMPE\_VREF\_1P65V TRACE SHOULD WIDER AND AWAY FROM NOISY TRACES

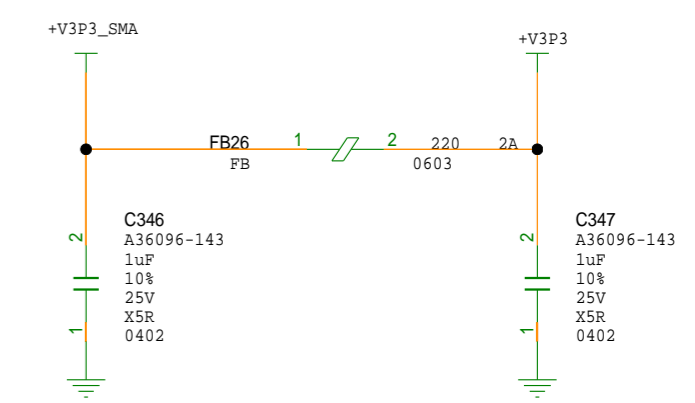
PIN 6 OF TLV3501A = 0 OUTPUT ON  
PIN 6 OF TLV3501A = 1 OUTPUT HIGH-Z



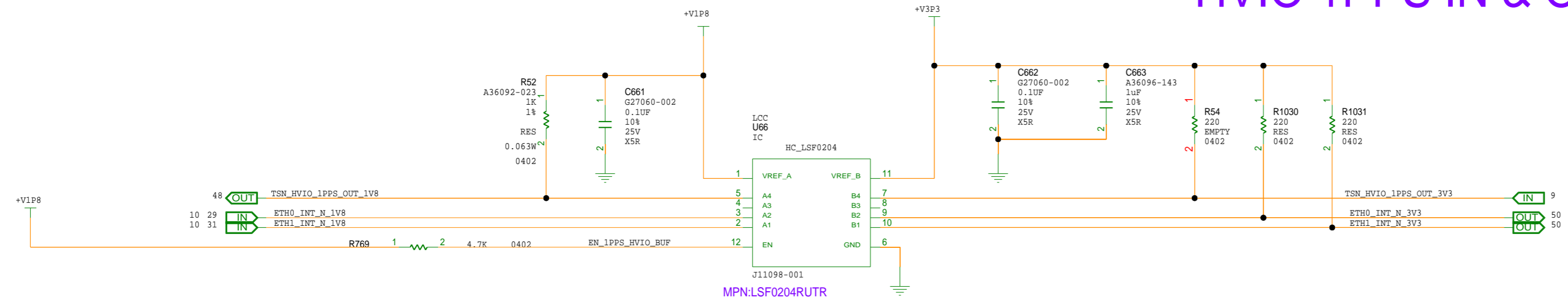
# 1PPS CLK IN



CAD NOTE:  
COMPE\_VREF\_0P257V TRACE SHOULD WIDER AND AWAY FROM NOISY TRACES



# HVIO 1PPS IN & OUT LVL SHIFTER

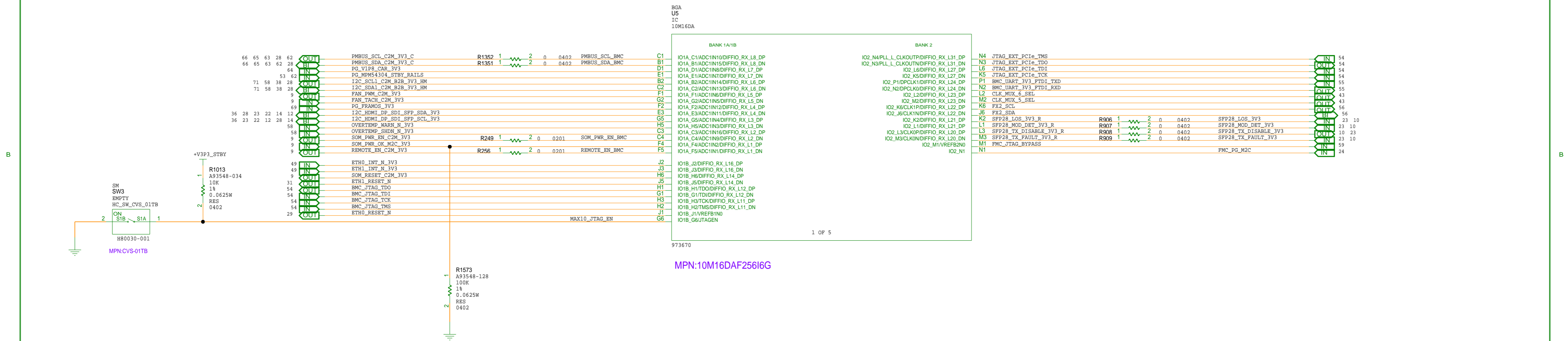


Tue Oct 1 13:22:37 2024

# CLOCK-1PPS INOUT

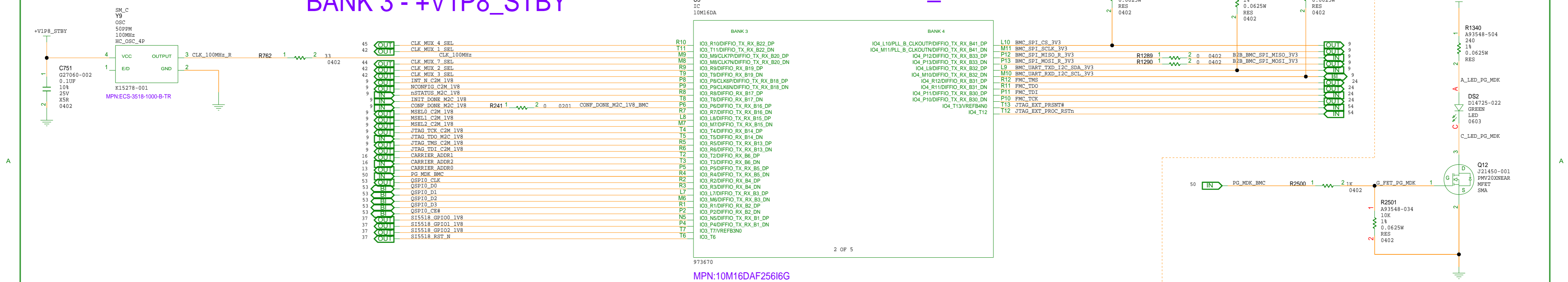
|            |                      |                      |       |                 |          |
|------------|----------------------|----------------------|-------|-----------------|----------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV      |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0      |
| SCALE:     |                      | DO NOT SCALE DRAWING |       | SHEET           | 49 OF 74 |

# BANK1A 1B AND 2 - +V3P3\_STBY



# BANK 3 - +V1P8\_STBY

# BANK 4 - +V3P3\_STBY



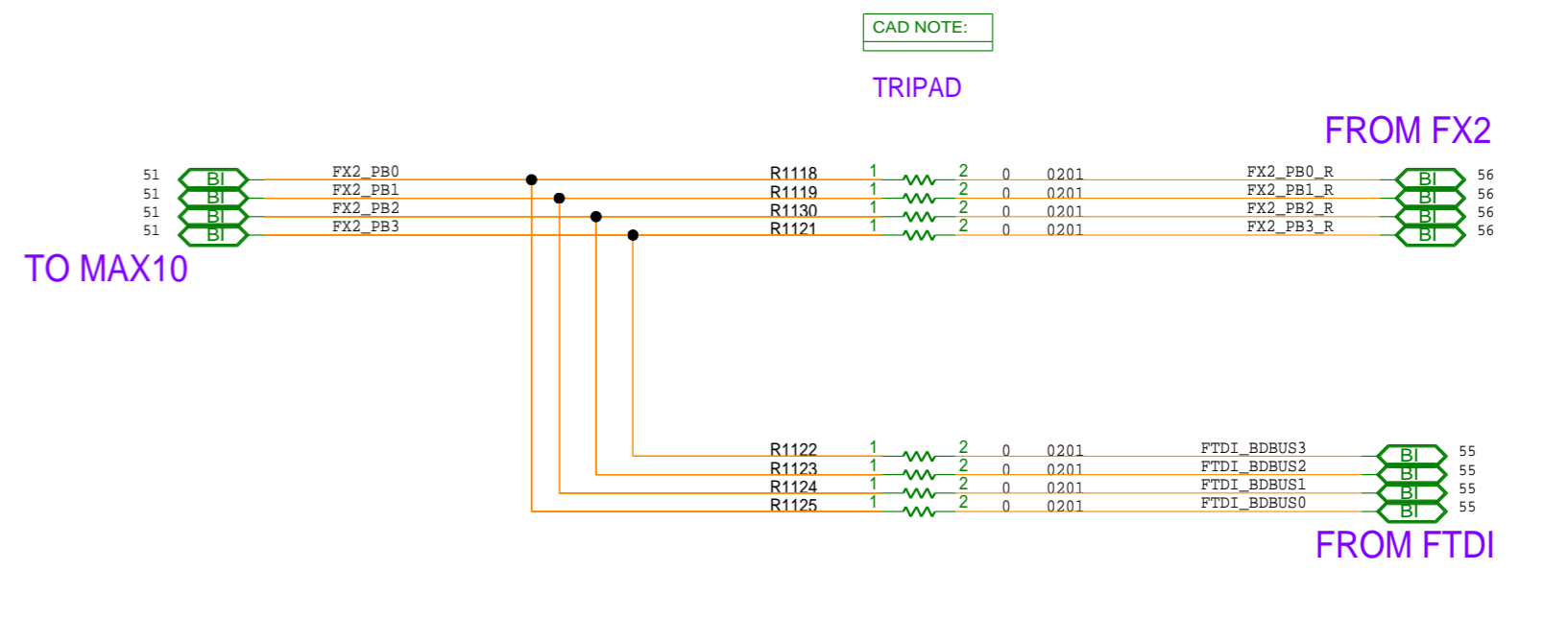
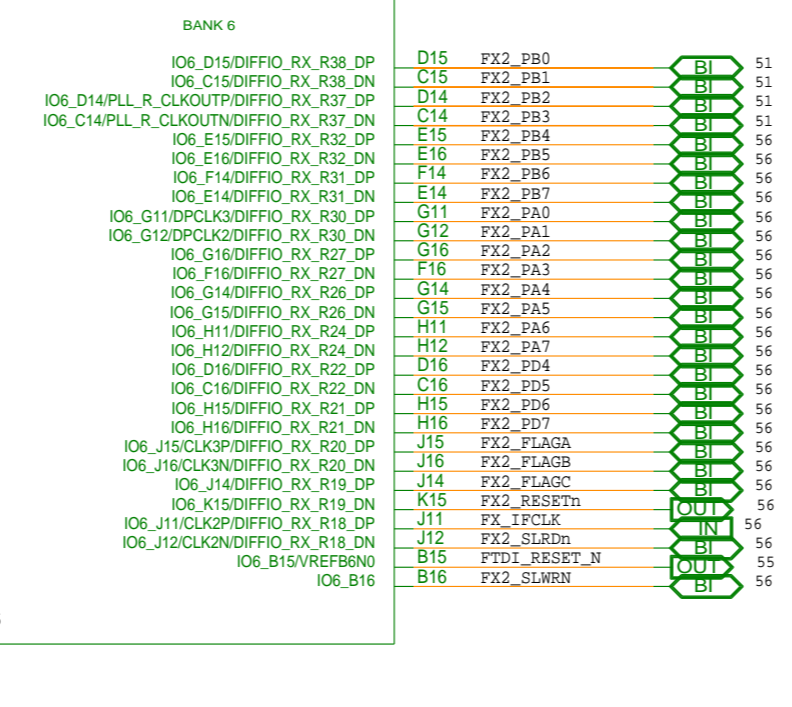
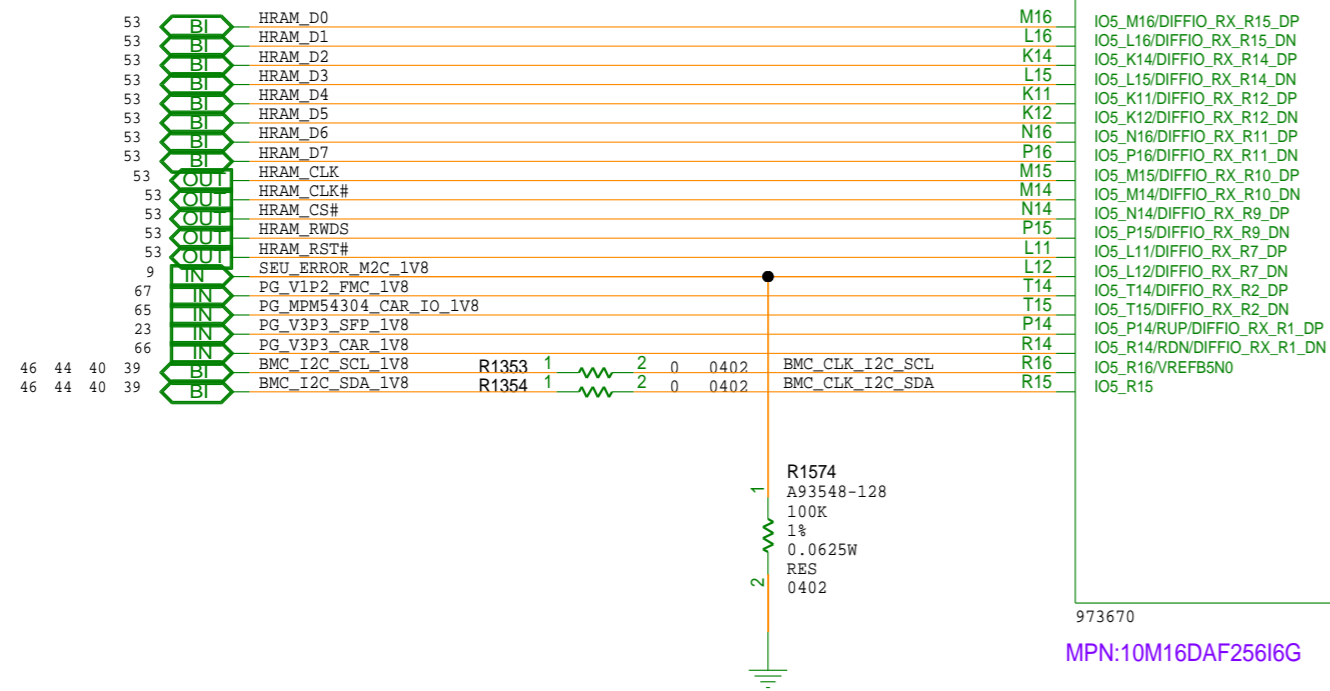
Tue Oct 1 13:22:37 2024

MAX10\_IO\_BANK\_1A\_1B\_2\_3\_4

|            |                            |                      |               |                                  |            |
|------------|----------------------------|----------------------|---------------|----------------------------------|------------|
| DEPARTMENT | altera<br>An Intel Company | SIZE<br>C+           | CODE<br>34649 | DOCUMENT NUMBER<br>150-330724-B1 | REV<br>2.0 |
| SCALE:     |                            | DO NOT SCALE DRAWING |               | SHEET                            | 51 OF 74   |

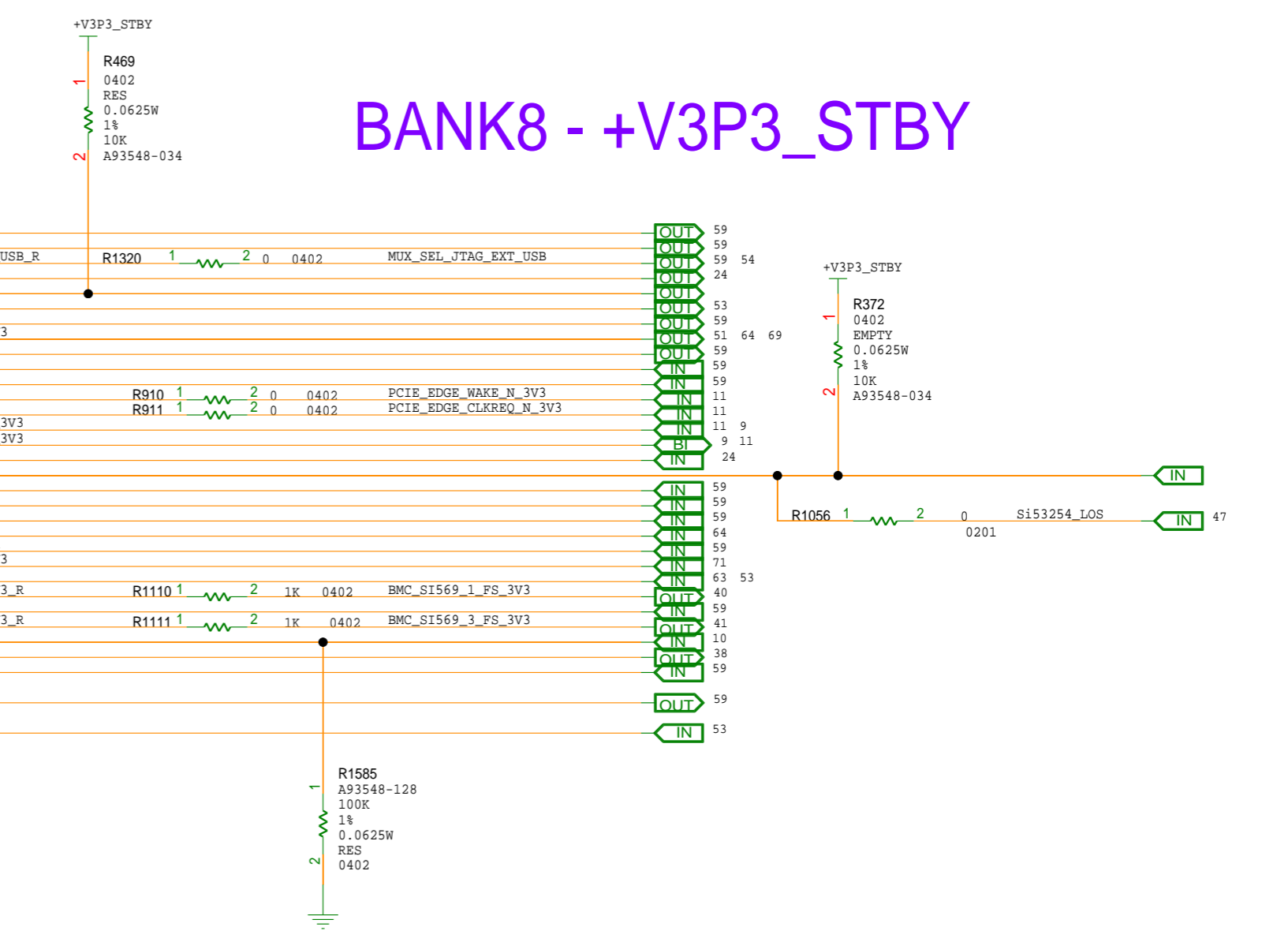
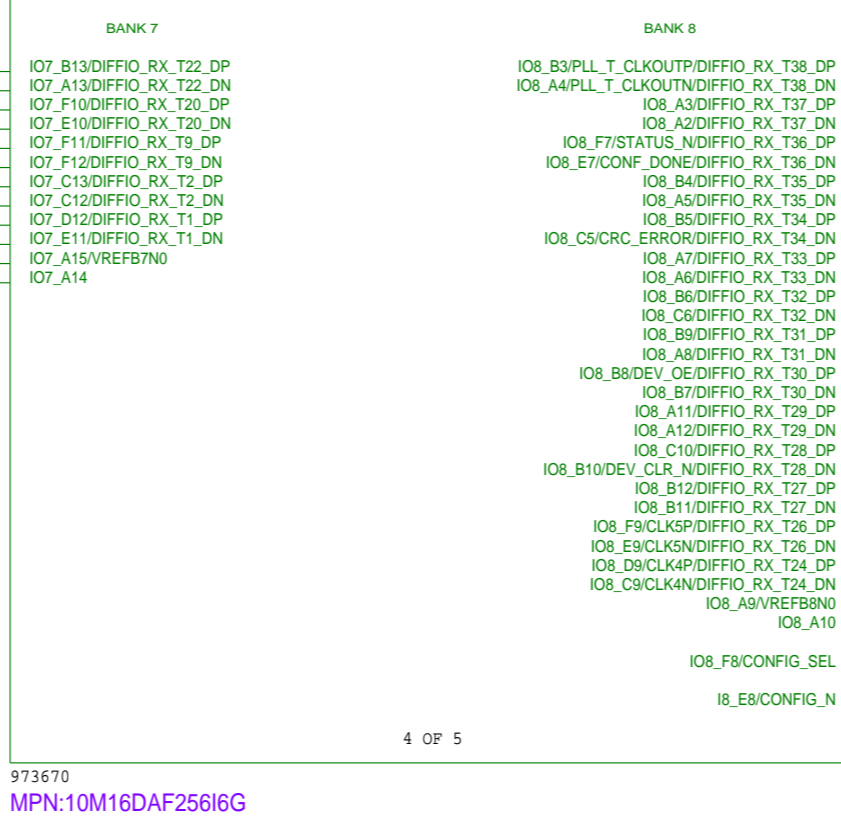
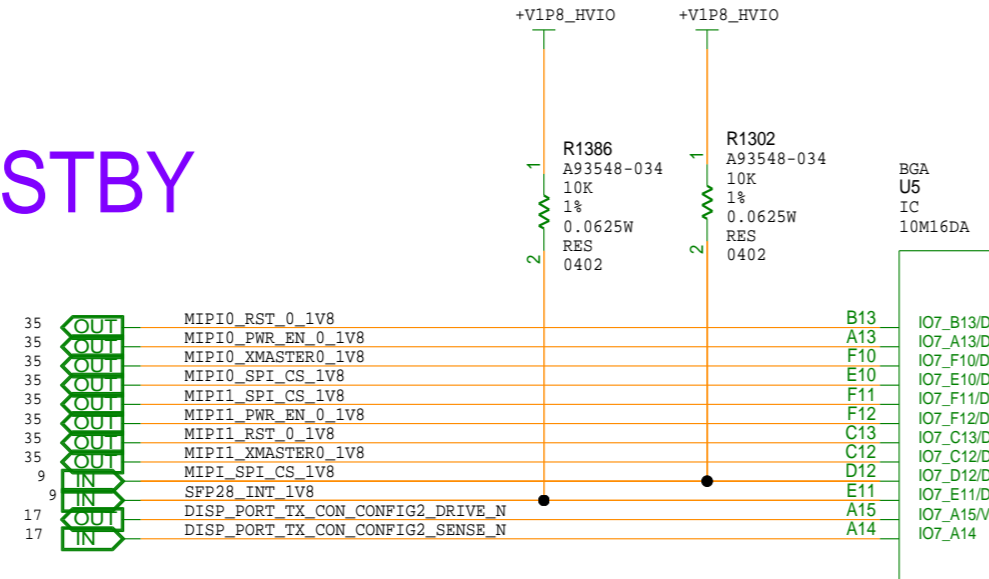
BANK 5 - +V1P8\_STBY

BANK 6 - +V3P3\_STBY

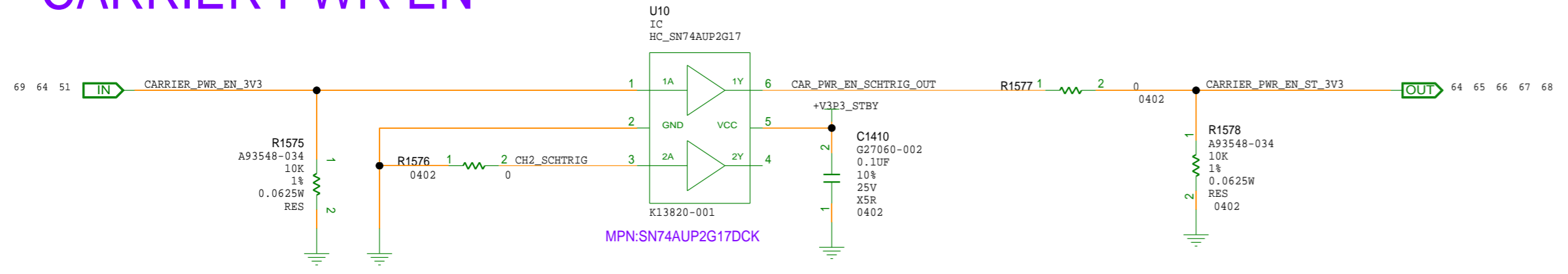


BANK 7 - +V1P8\_STBY

BANK 8 - +V3P3\_STBY

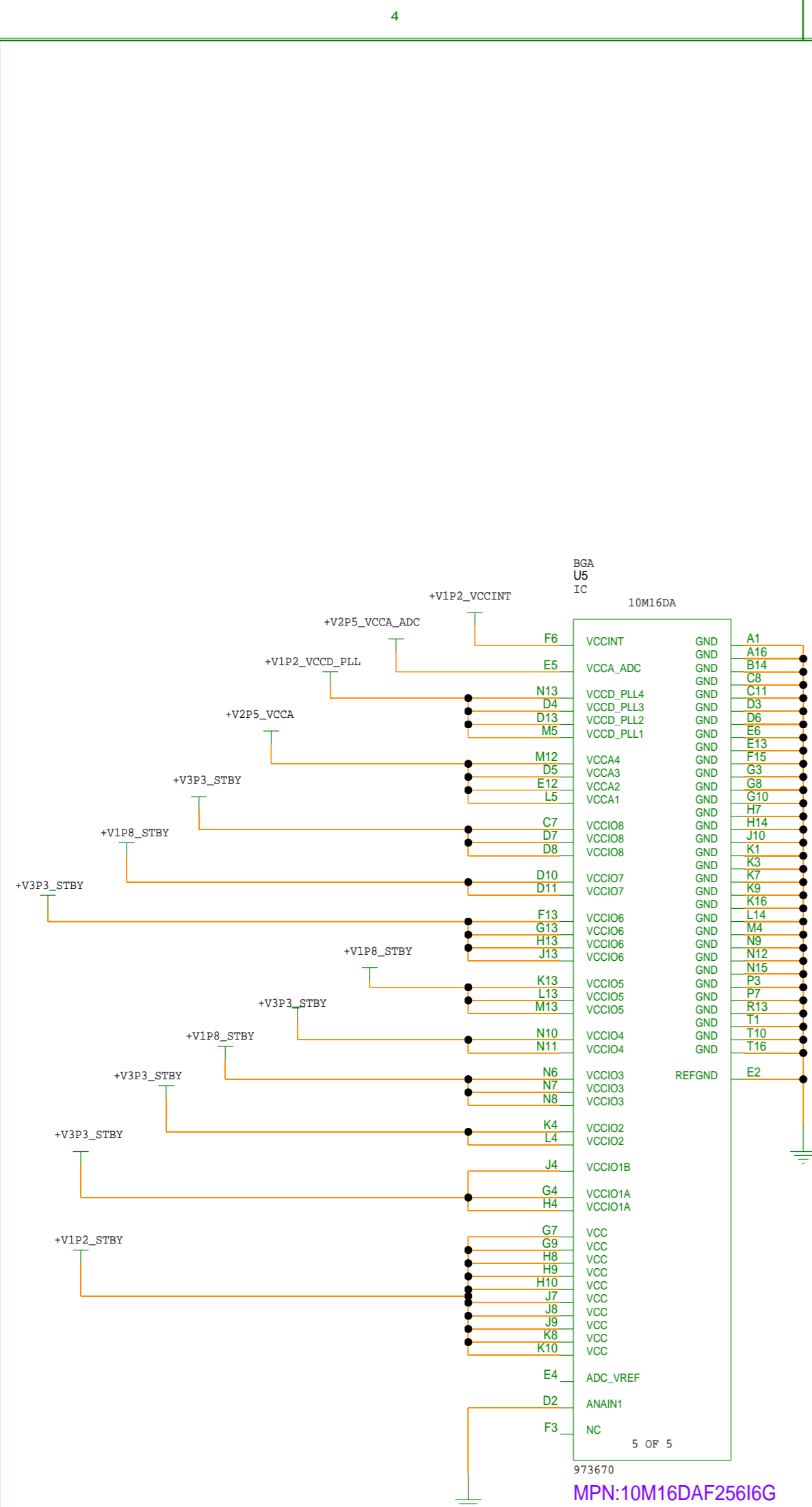


CARRIER PWR EN

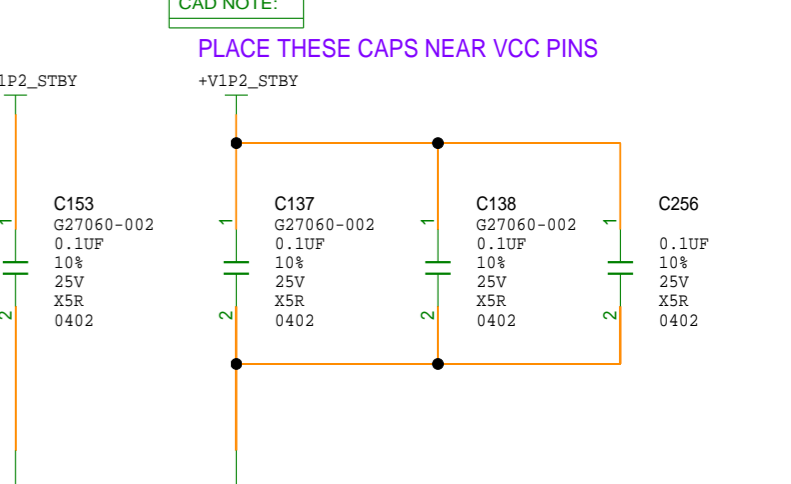
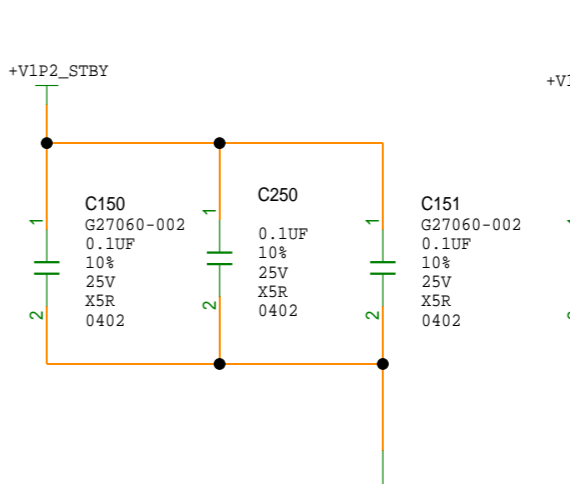
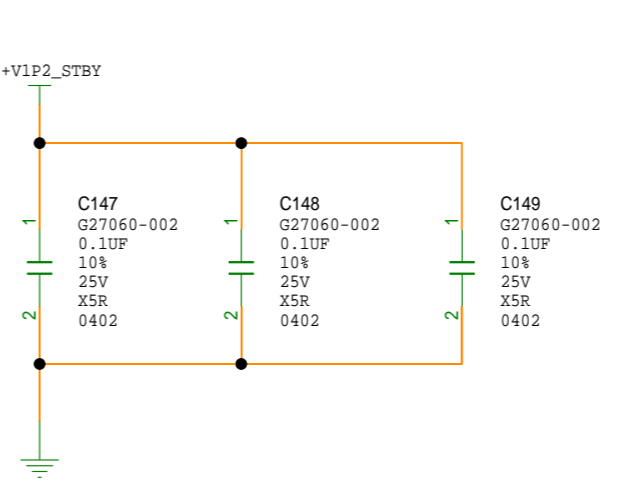
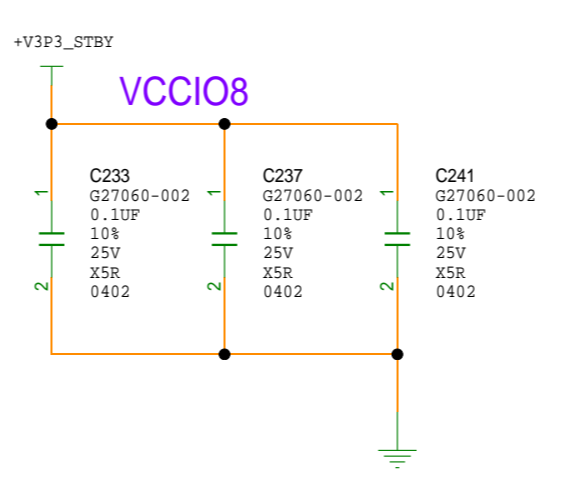
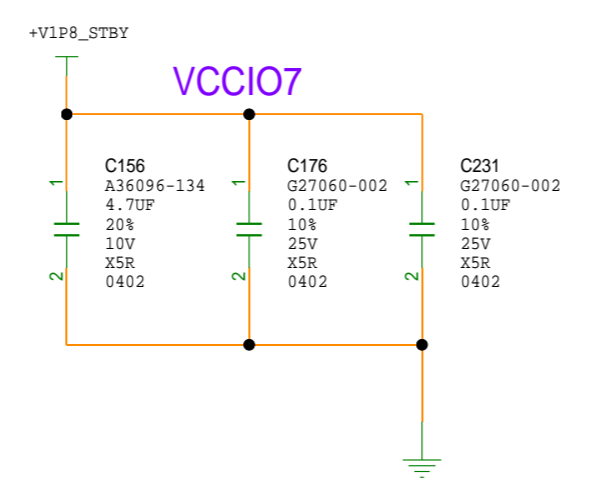


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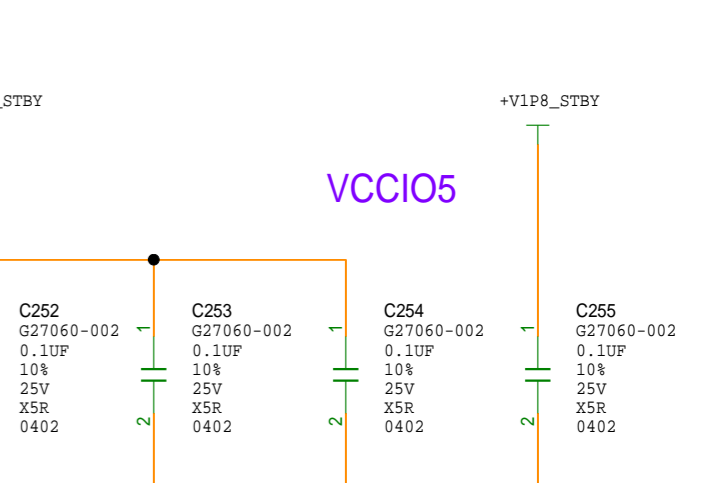
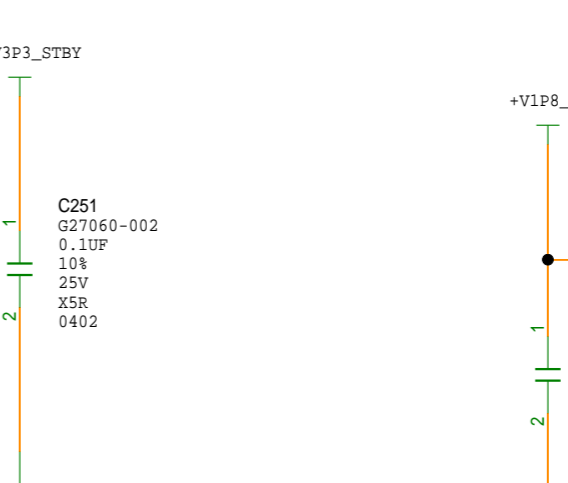
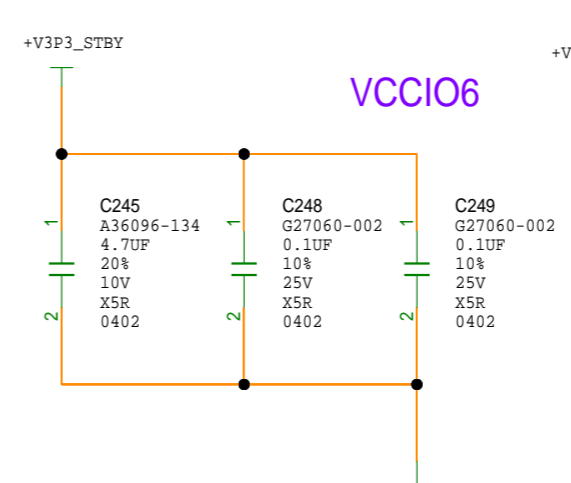
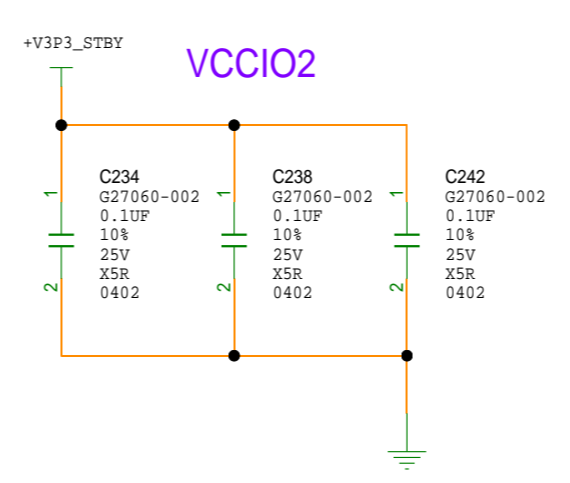
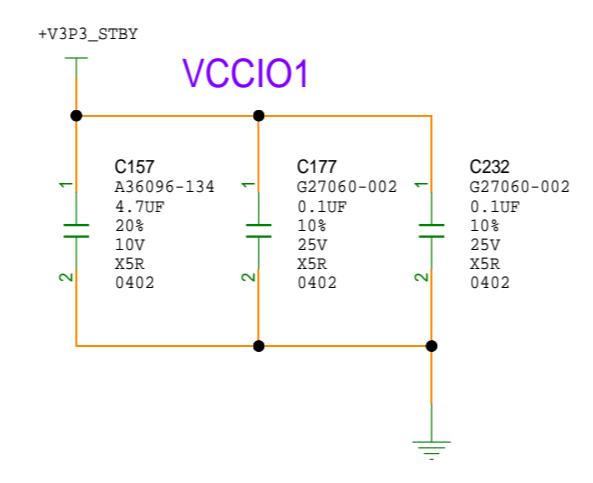
|            |        |                      |                 |                |
|------------|--------|----------------------|-----------------|----------------|
| DEPARTMENT | SIZE   | CODE                 | DOCUMENT NUMBER | REV            |
|            | C+     | 34649                | 150-330724-B1   | 2.0            |
|            | SCALE: | DO NOT SCALE DRAWING |                 | SHEET 52 OF 74 |



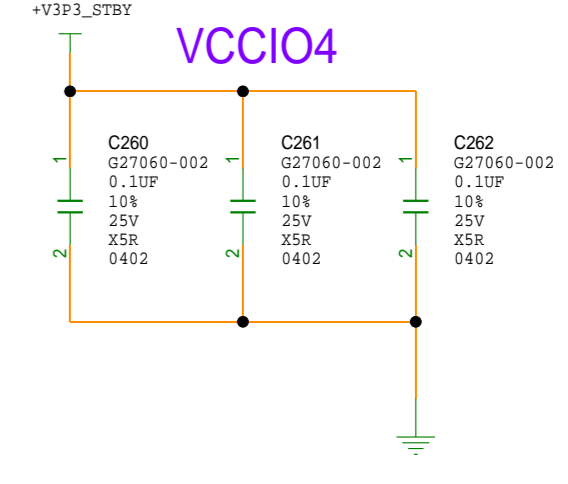
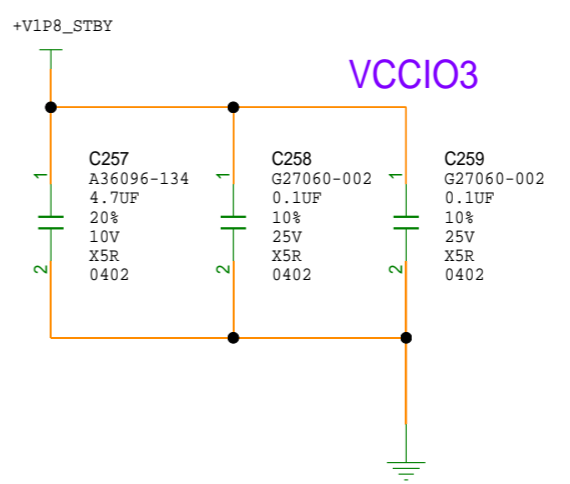
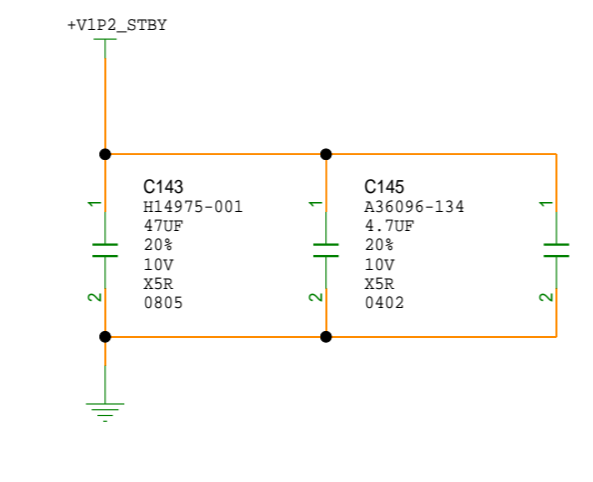
MPN:10M16DAF256I6G



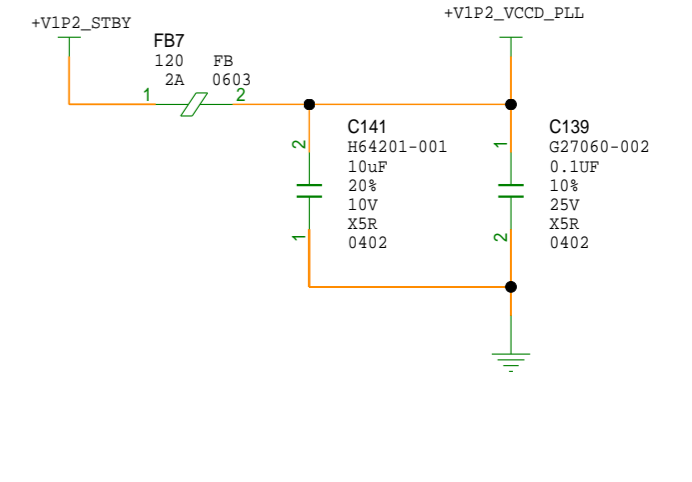
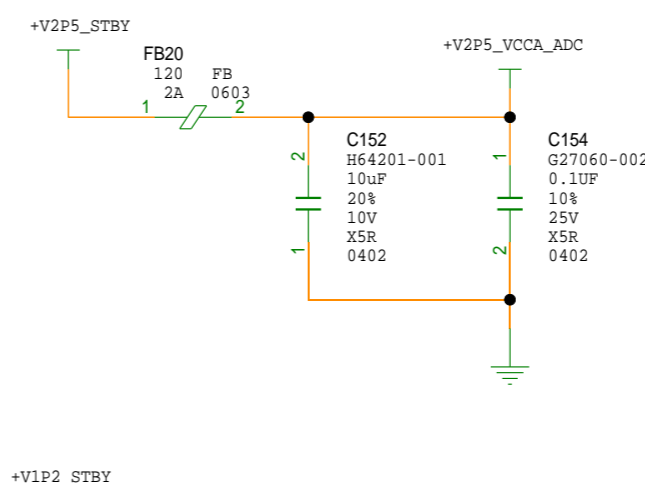
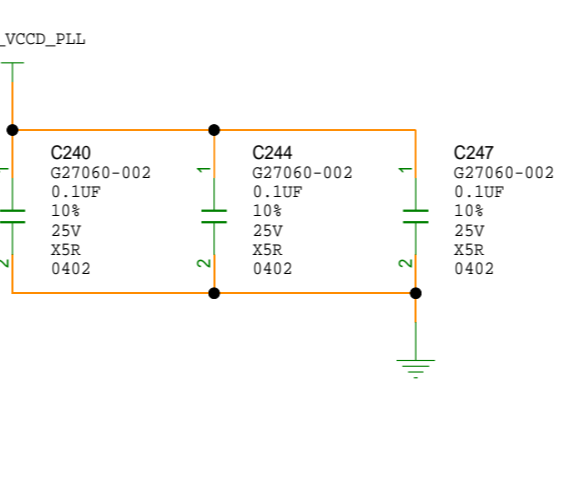
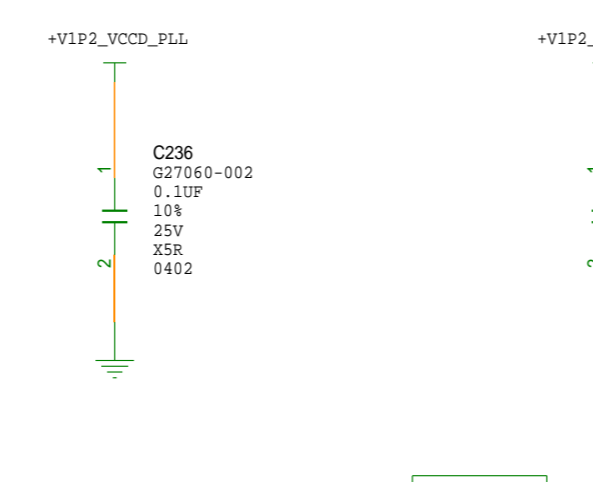
CAD NOTE:  
PLACE THESE CAPS NEAR VCC PINS



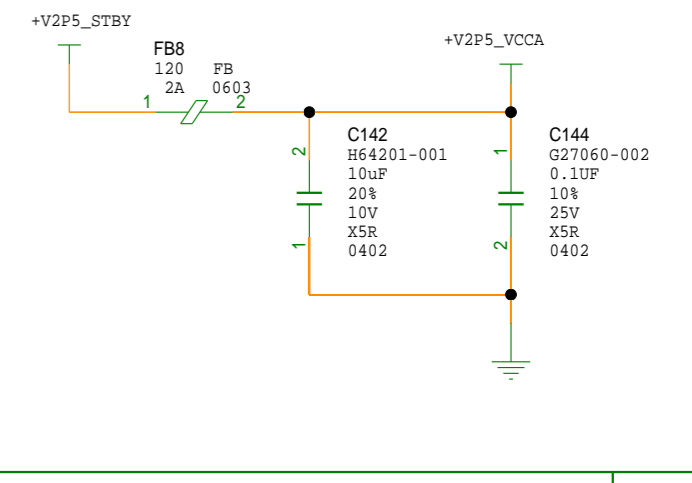
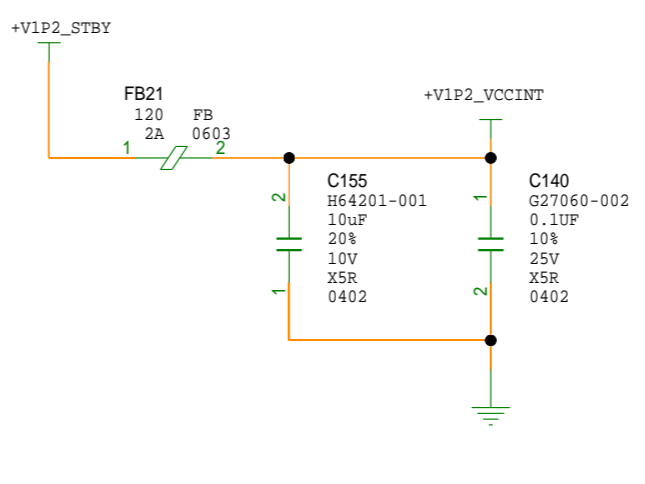
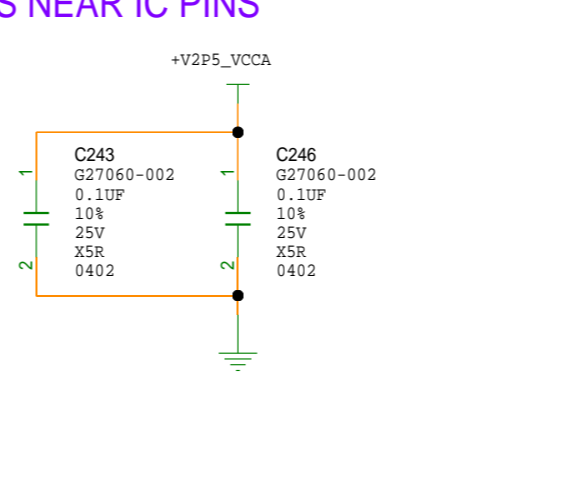
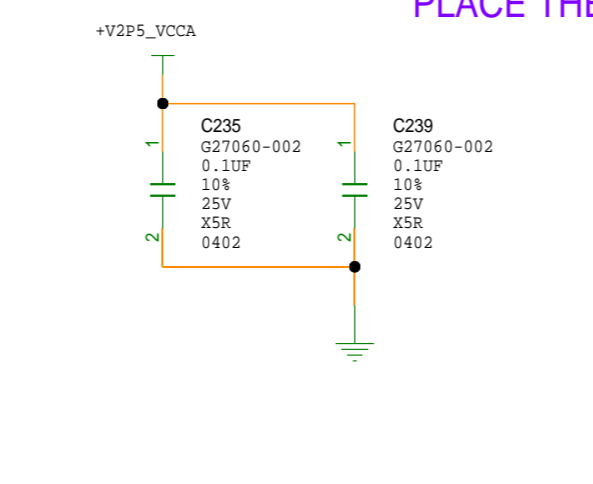
VCCIO5



CAD NOTE:  
PLACE THESE CAPS NEAR IC PINS



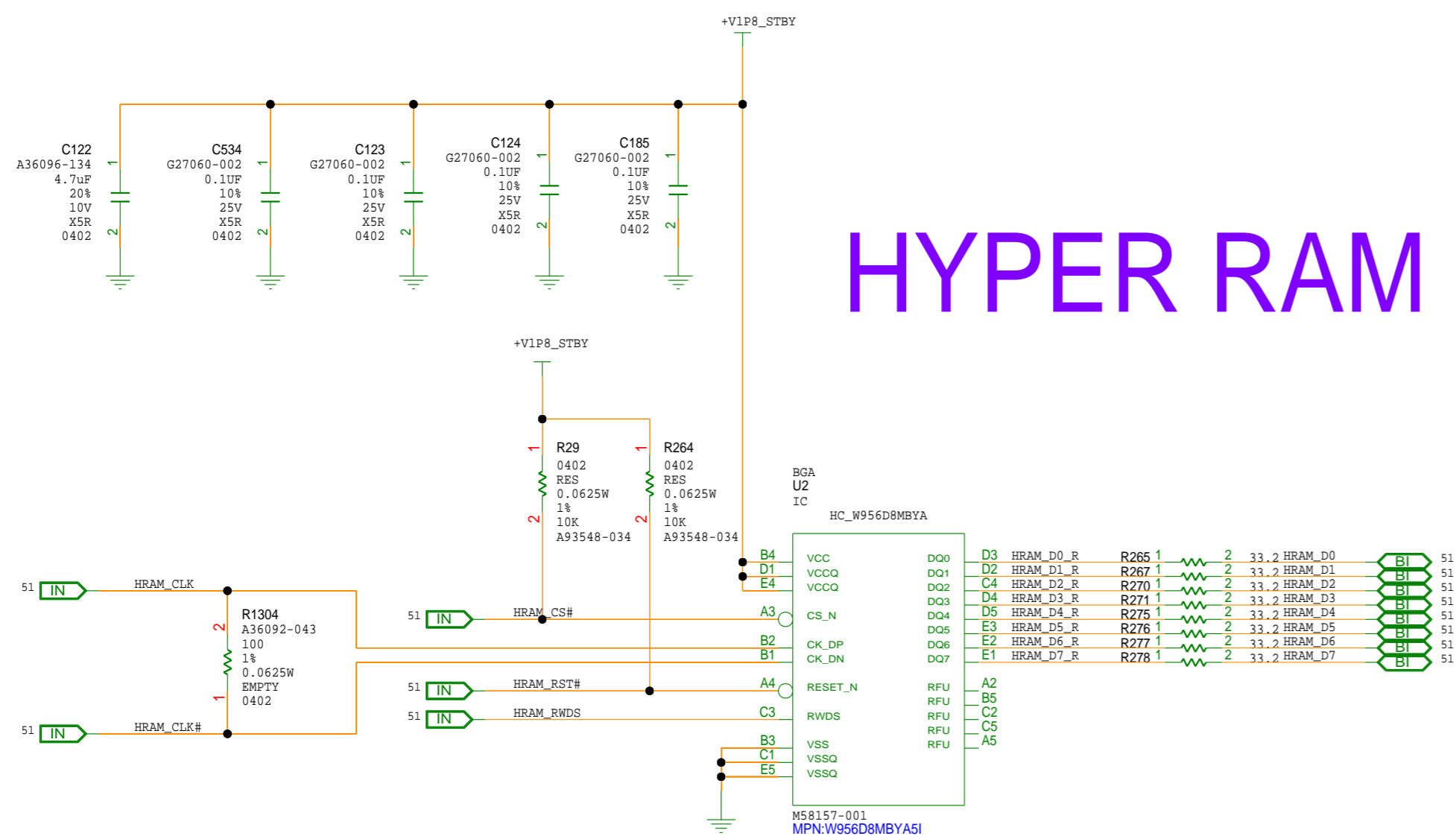
CAD NOTE:  
PLACE THESE CAPS NEAR IC PINS



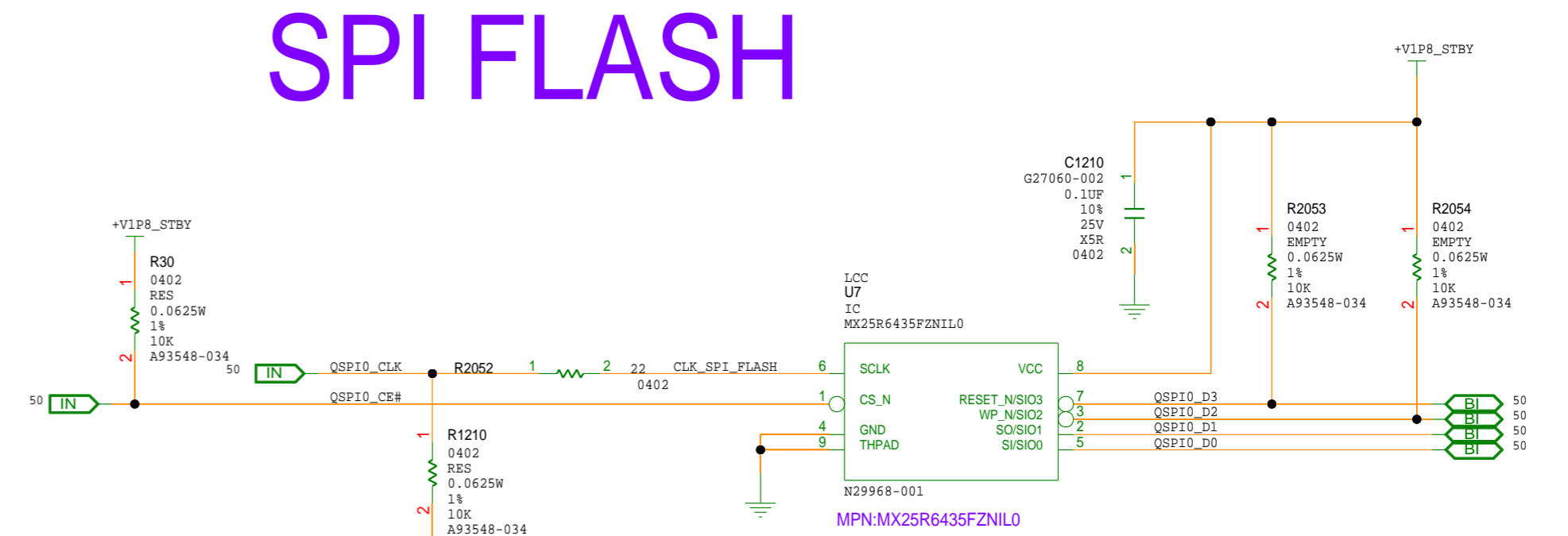
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# MAX10 - DECAPS

|            |                            |            |                      |                                  |                |
|------------|----------------------------|------------|----------------------|----------------------------------|----------------|
| DEPARTMENT | altera<br>An Intel Company | SIZE<br>C+ | CODE<br>34649        | DOCUMENT NUMBER<br>150-330724-B1 | REV<br>2.0     |
| SCALE:     |                            |            | DO NOT SCALE DRAWING |                                  | SHEET 53 OF 74 |

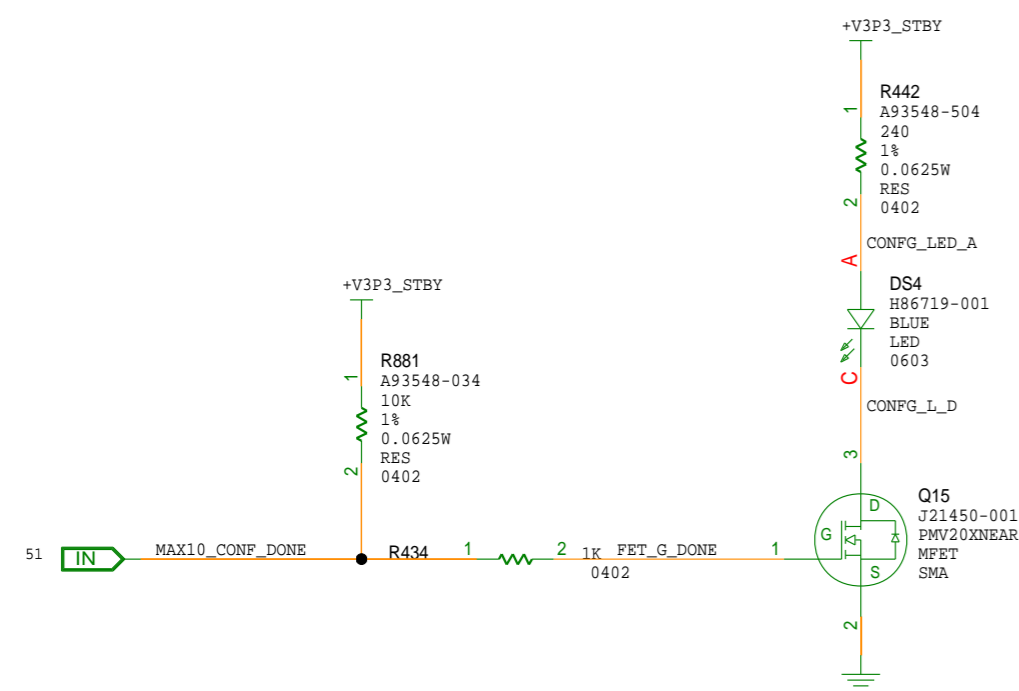


# HYPER RAM

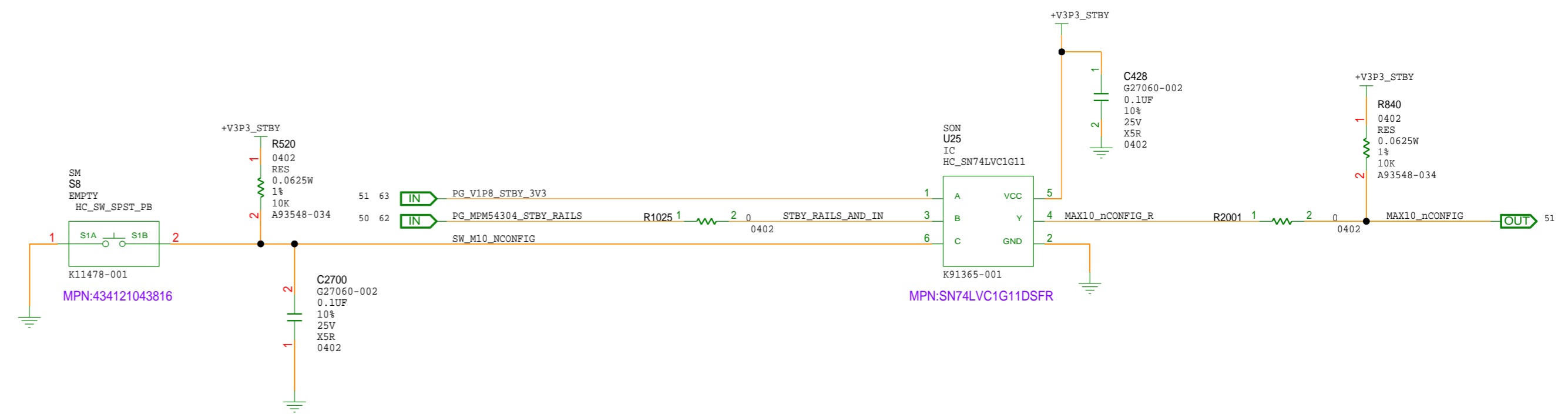


# SPI FLASH

# CONF DONE LED



# MAX10 - NCONFIG

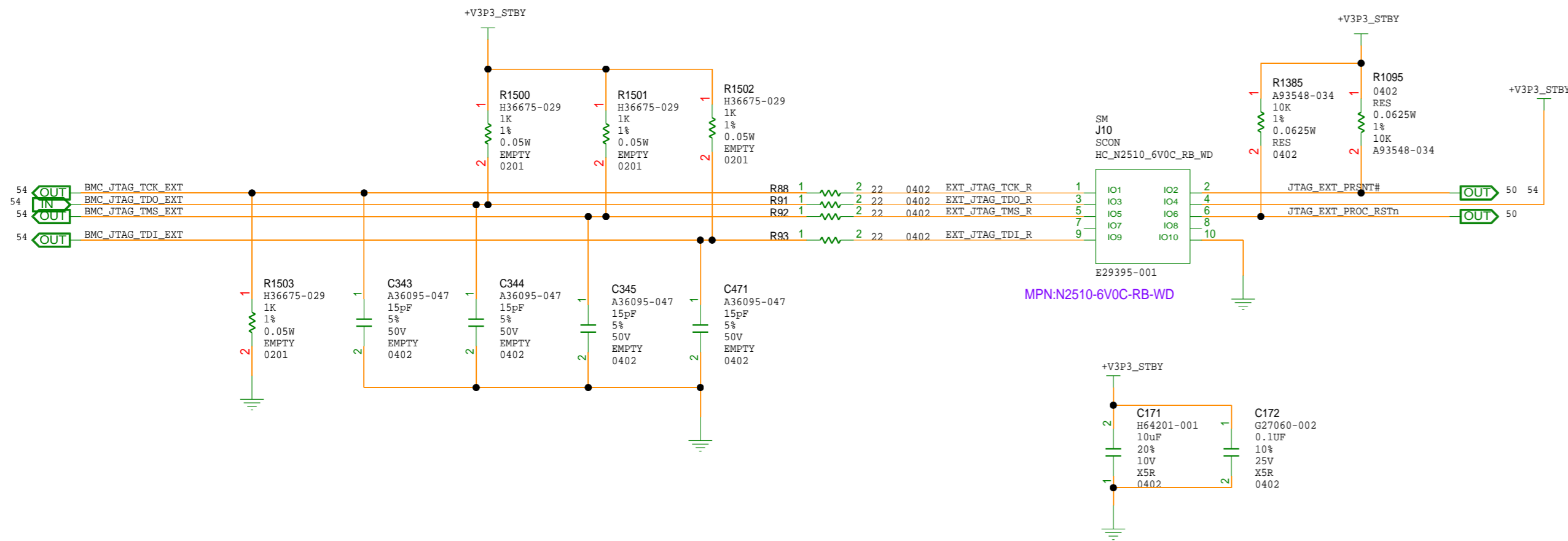


# MAX10 - CONFIG

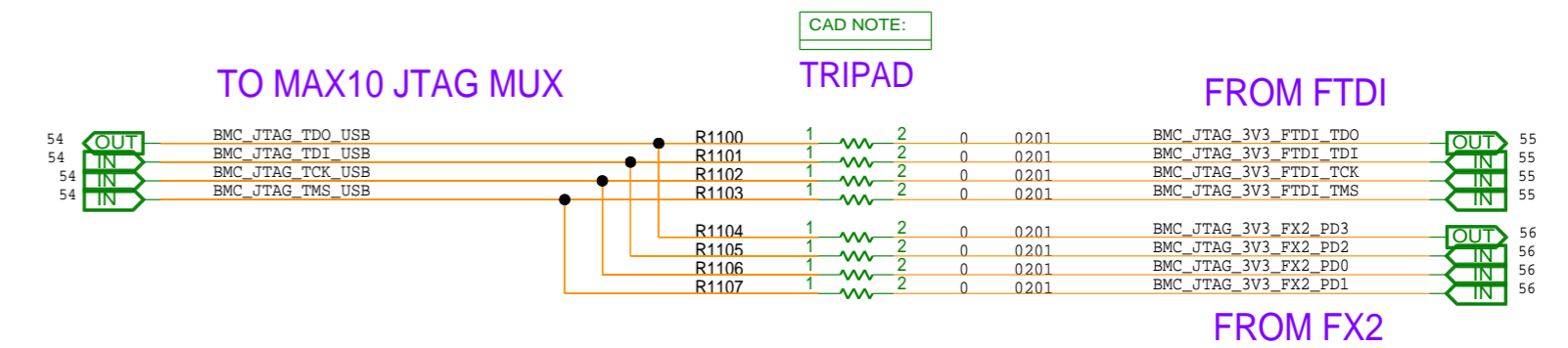
Tue Oct 1 13:22:38 2024

|            |                      |                      |       |                 |                |
|------------|----------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                      | DO NOT SCALE DRAWING |       |                 | SHEET 54 OF 74 |

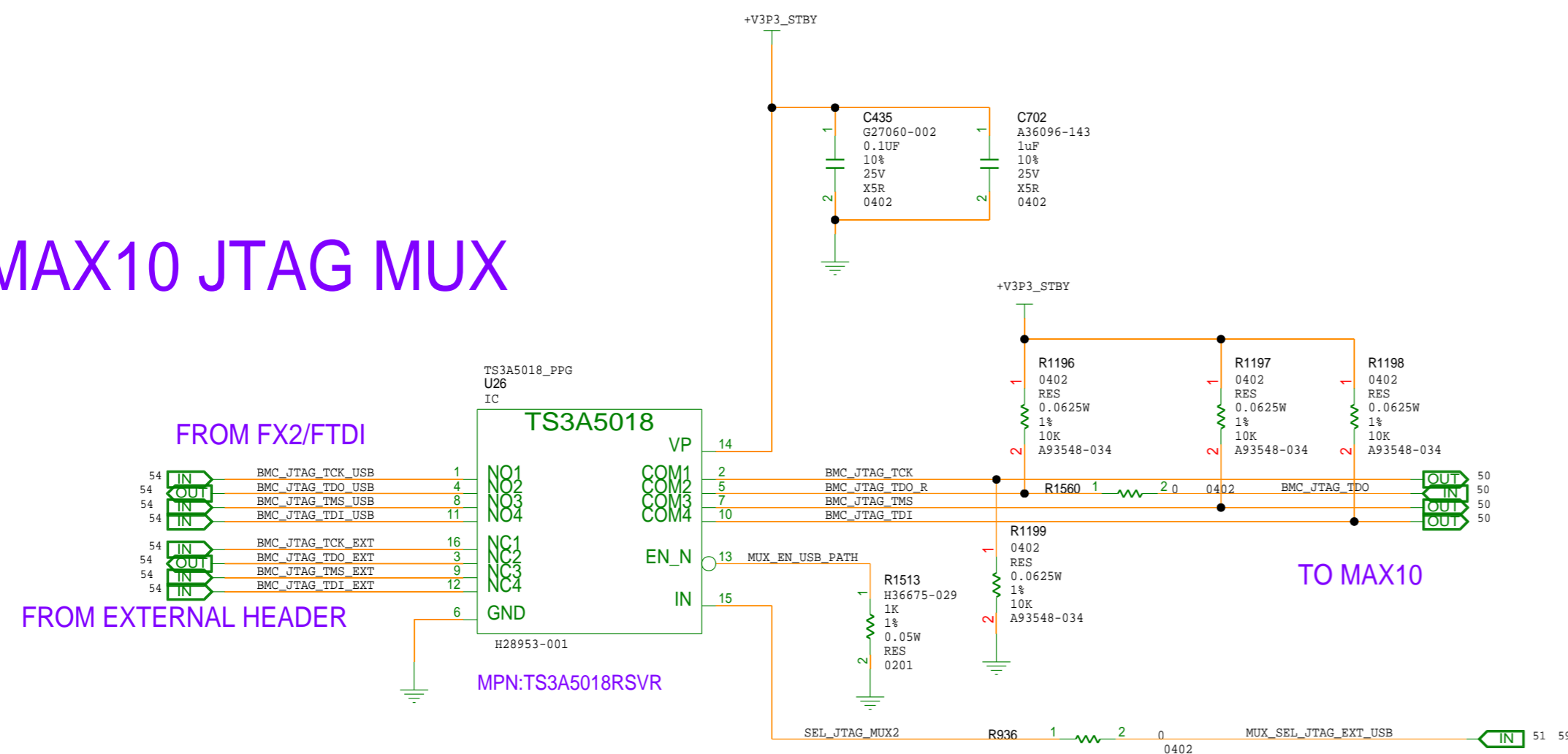
# MAX10 JTAG PROGRAMMING HEADER



# MAX10 JTAG USB PATH



# MAX10 JTAG MUX



# EXT/PCIe JTAG MUX

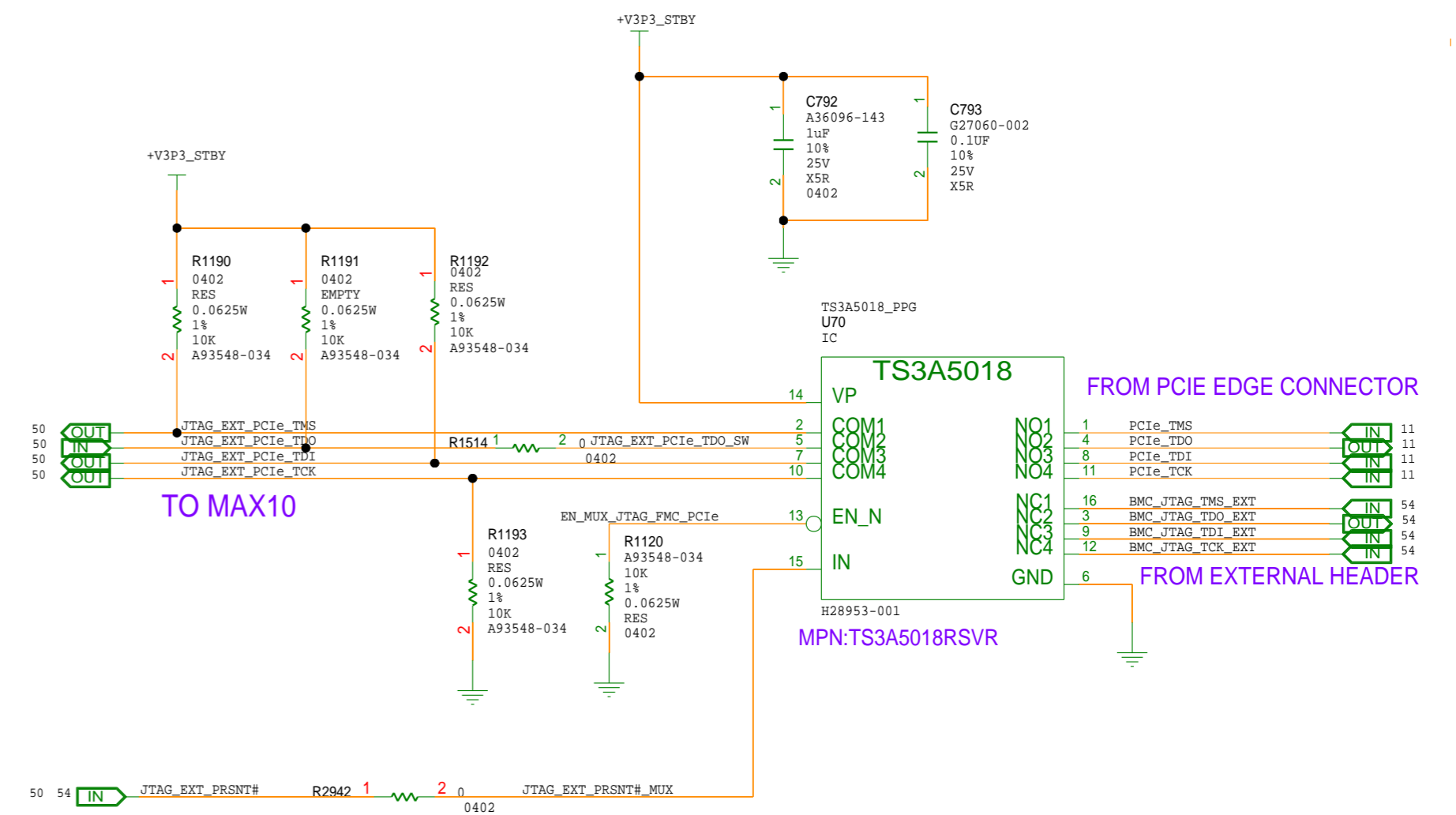


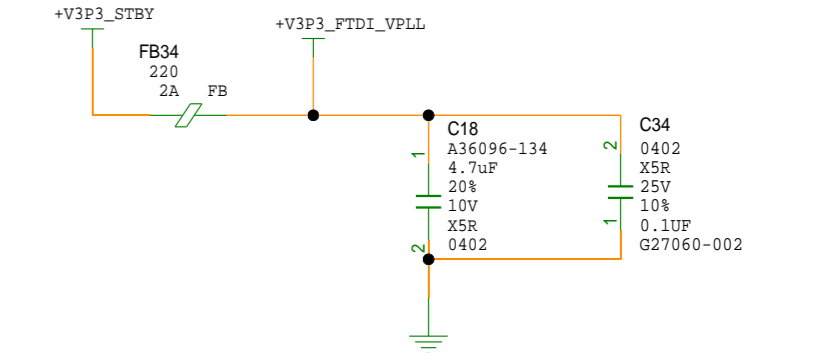
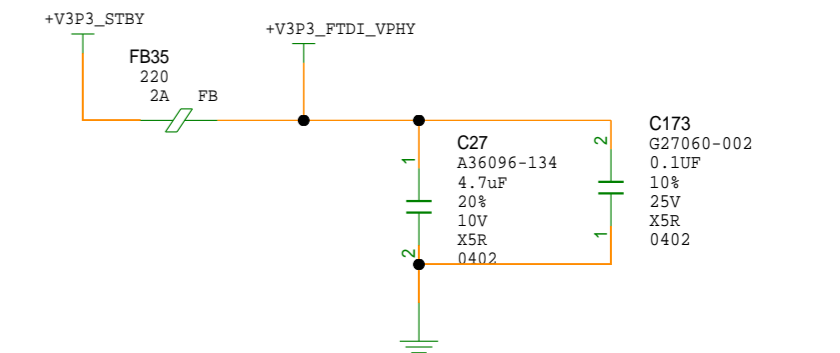
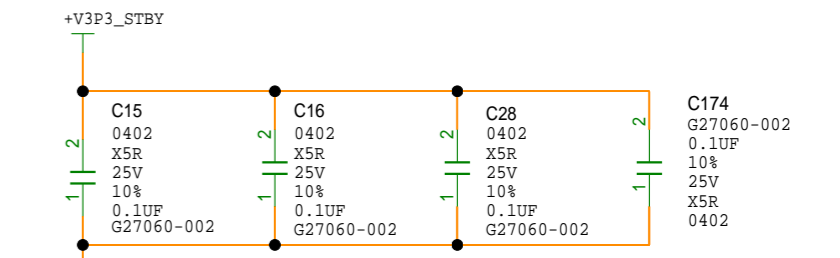
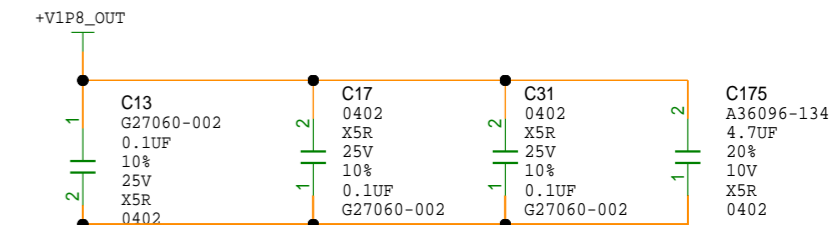
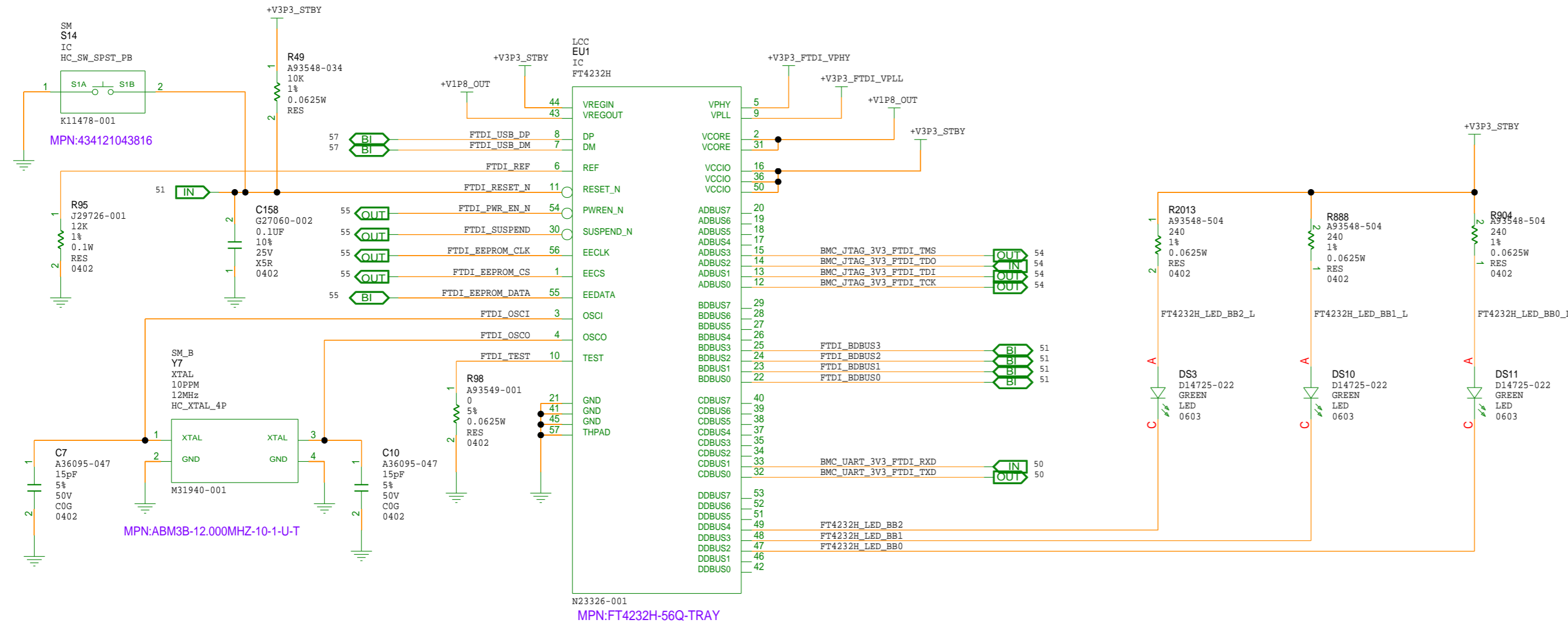
Table 1. Function Table

| EN | IN | NO TO COM, COM TO NO | NC TO COM, COM TO NC |
|----|----|----------------------|----------------------|
| L  | L  | OFF                  | ON                   |
| L  | H  | ON                   | OFF                  |
| H  | X  | OFF                  | OFF                  |

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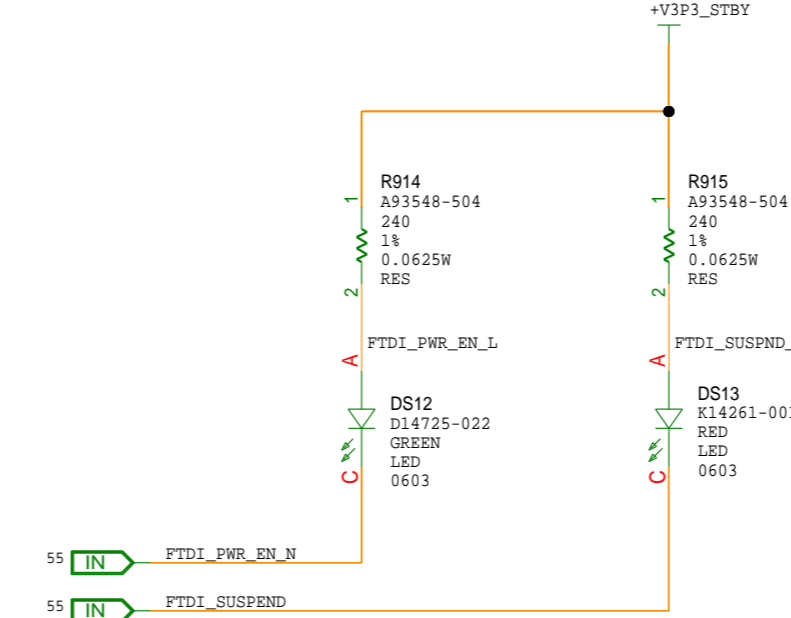
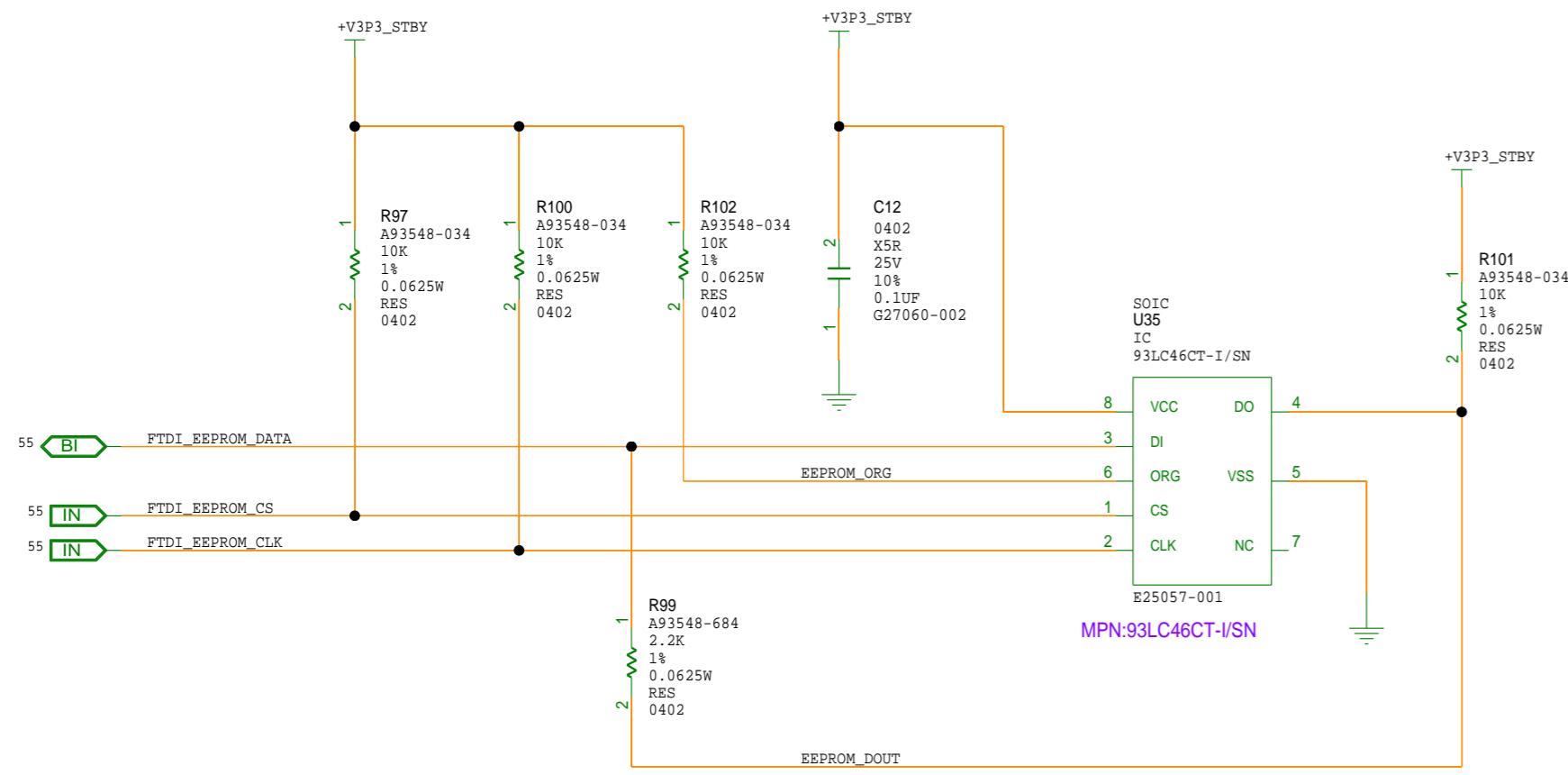
# FT4232H

# DECAP



# EEPROM

# LED



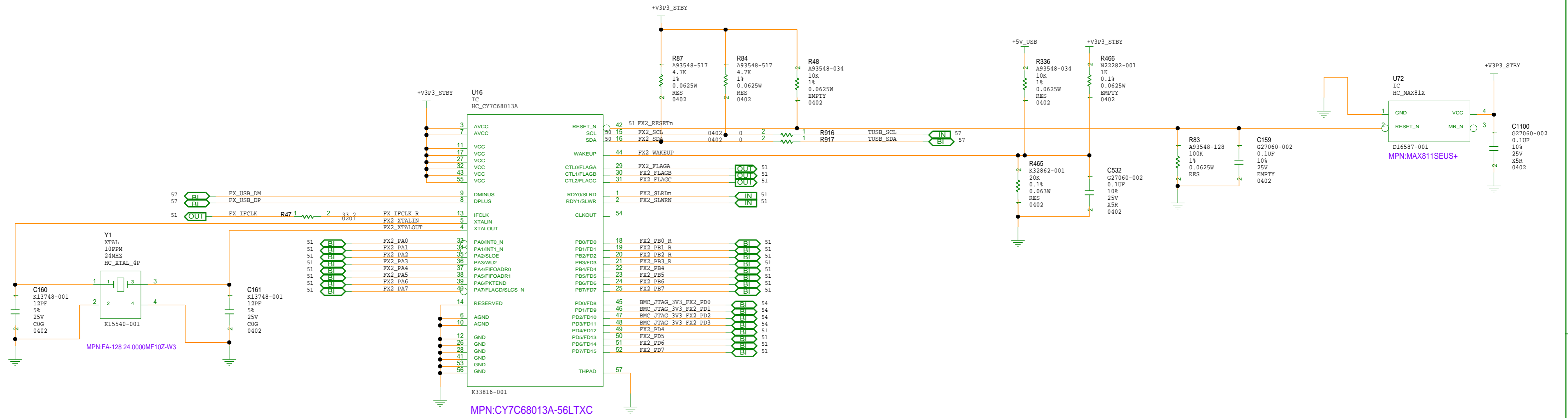
NOTE:  
 PWREN# = 0: NORMAL OPERATION.  
 PWREN# = 1: USB SUSPEND MODE OR DEVICE HAS NOT BEEN CONFIGURED.

NOTE:  
 SUSPEND# = 0: USB IS IN SUSPEND MODE

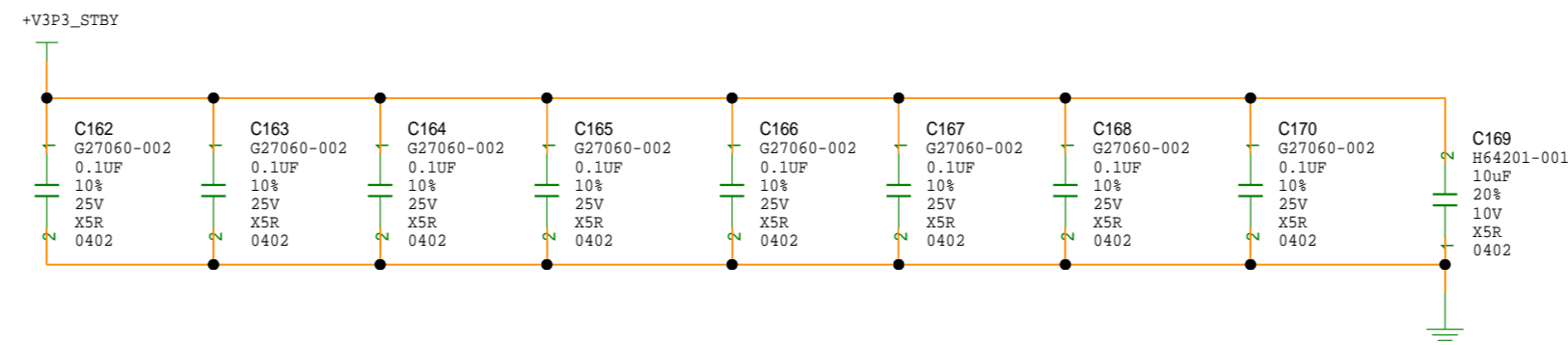
Tue Oct 1 13:22:38 2024

|            |   |                      |       |                 |          |
|------------|---|----------------------|-------|-----------------|----------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV      |
|            |   | C+                   | 34649 | 150-330724-B1   | 2.0      |
| SCALE:     |   | DO NOT SCALE DRAWING |       | SHEET           | 56 OF 74 |

# USB TO PARALLEL



# DECAP



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# USB TO PARALLEL

DEPARTMENT



SIZE  
C+

CODE  
34649

DOCUMENT NUMBER  
150-330724-B1

REV  
2.0

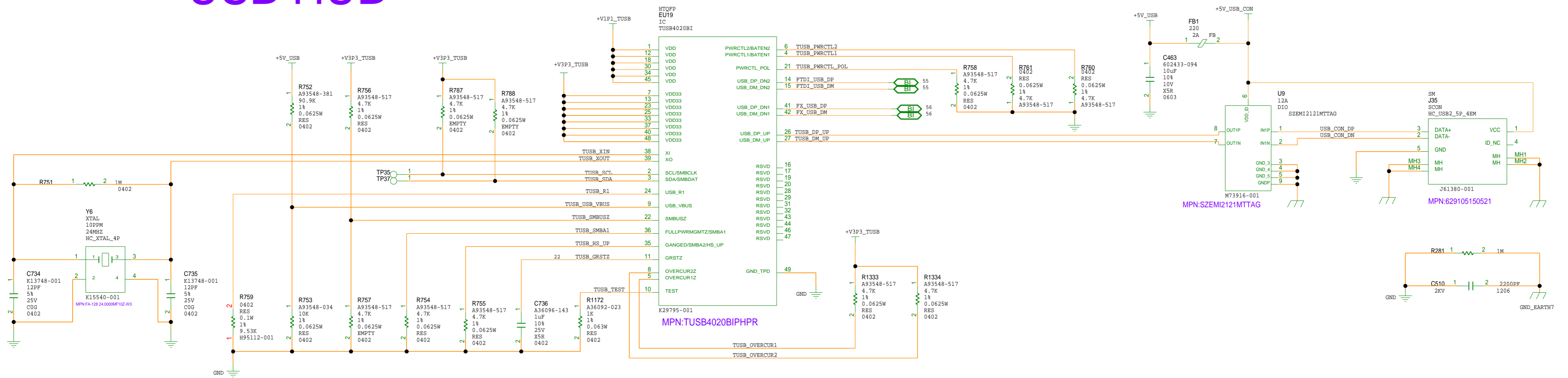
SCALE:

DO NOT SCALE DRAWING

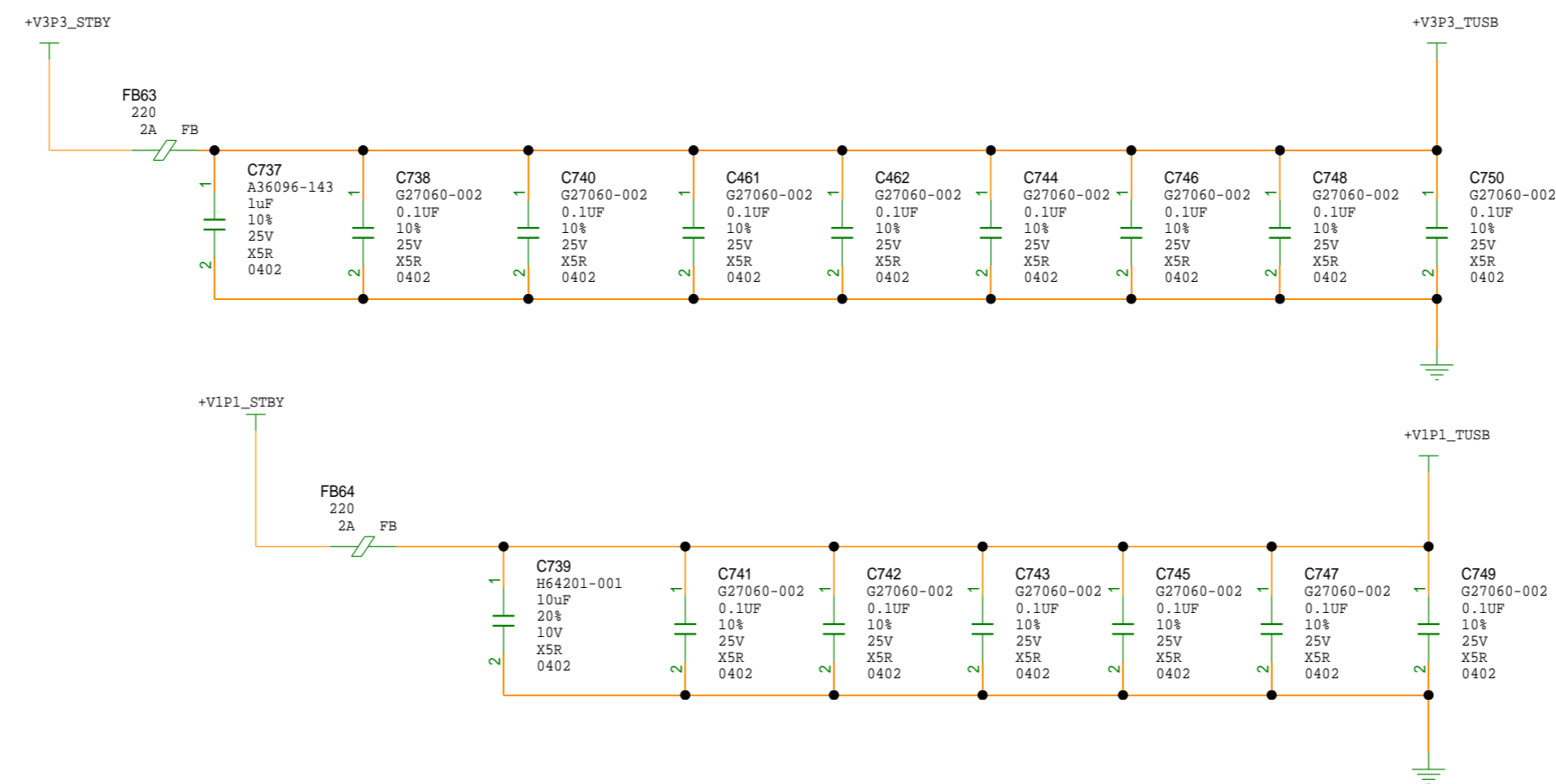
SHEET 57 OF 74



# USB HUB



# DECAP

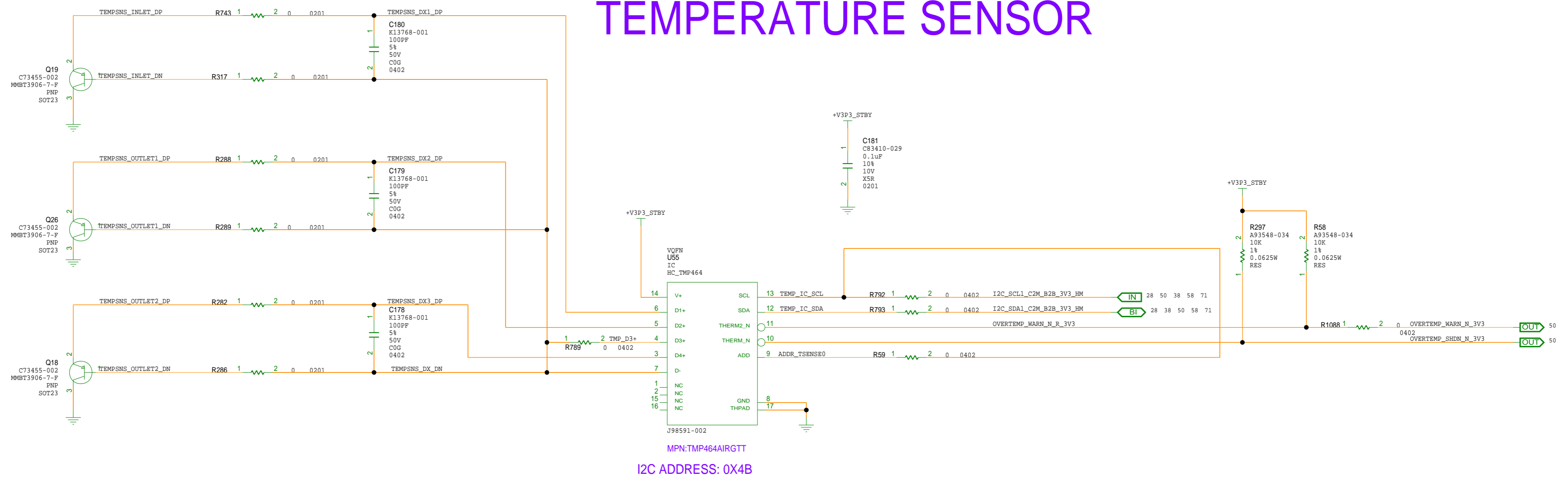


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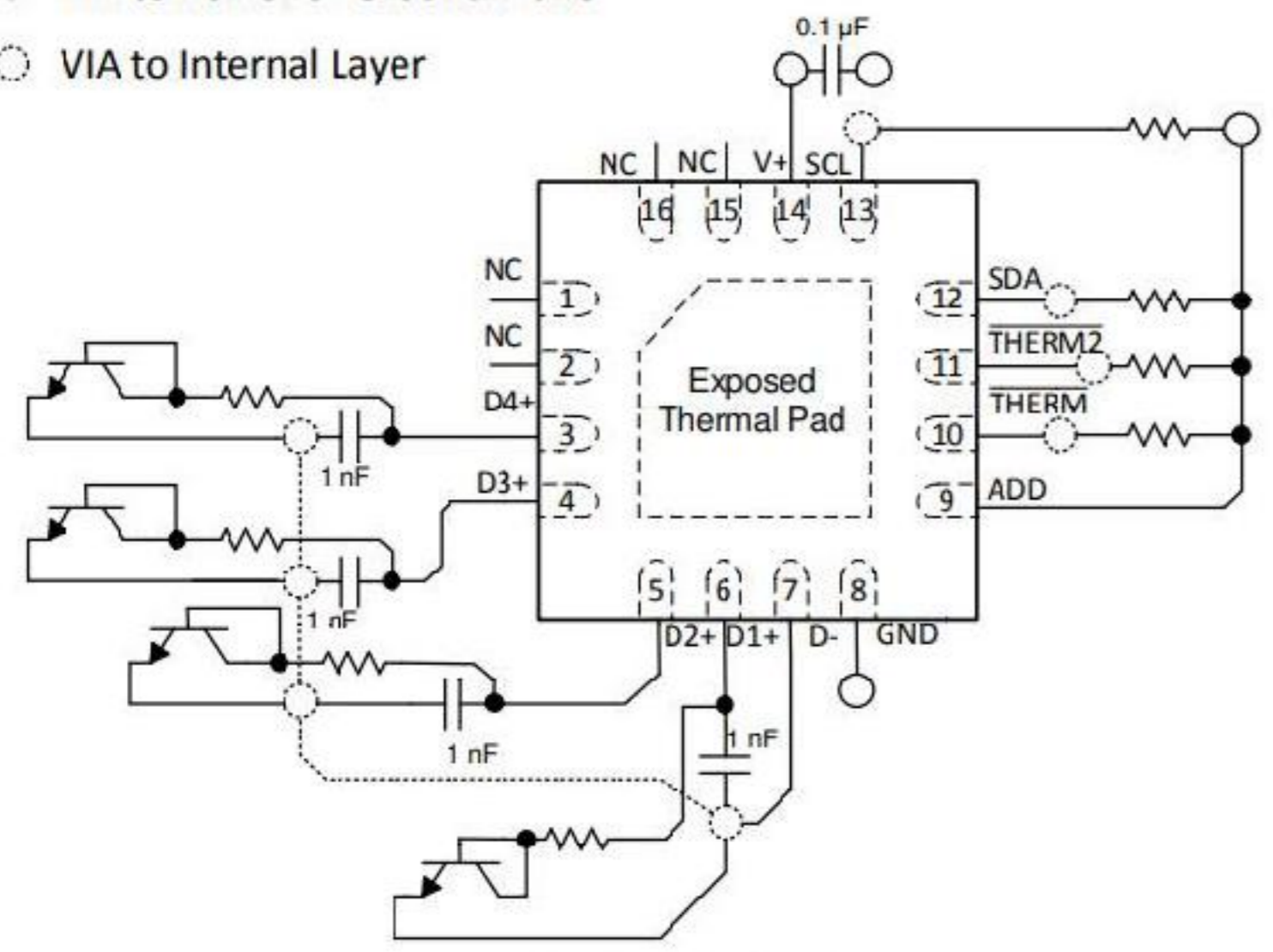
# USB HUB

|            |                      |                      |       |                 |                |
|------------|----------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                      | DO NOT SCALE DRAWING |       |                 | SHEET 58 OF 74 |

# TEMPERATURE SENSOR

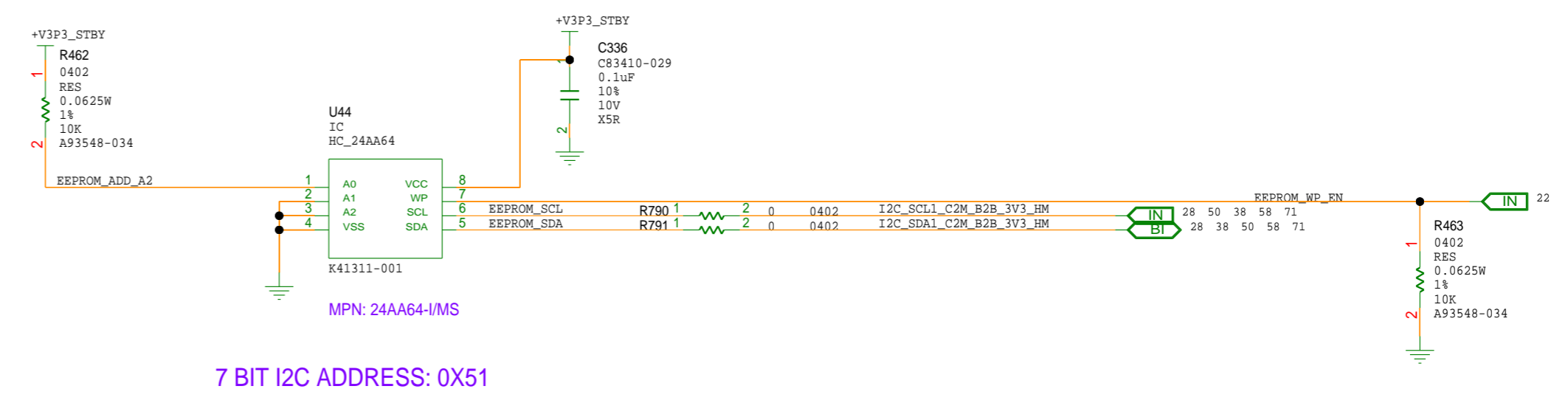


- VIA to Power or Ground Plane
- VIA to Internal Layer



TMP464 Layout Example

# EEPROM

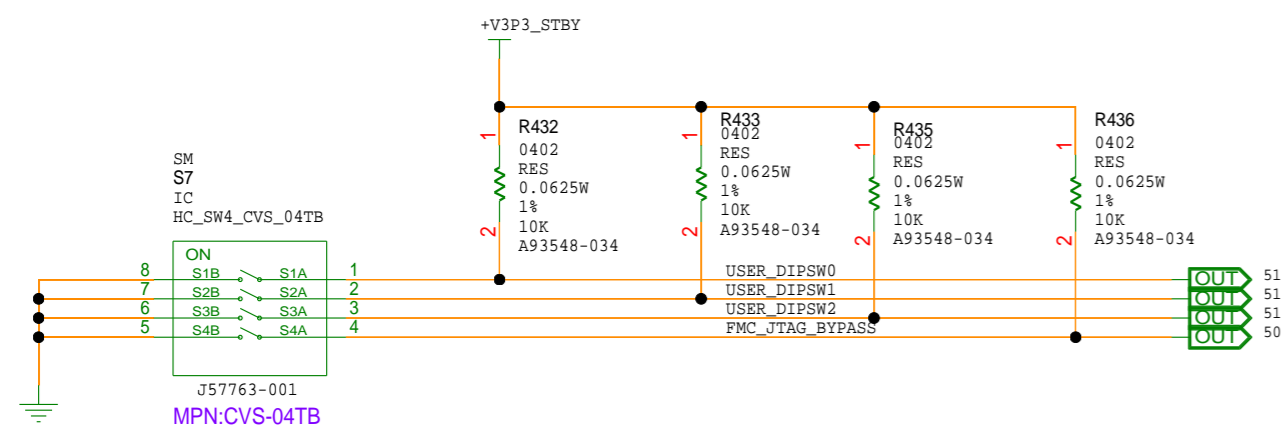


# TEMP SENSOR AND EEPROM

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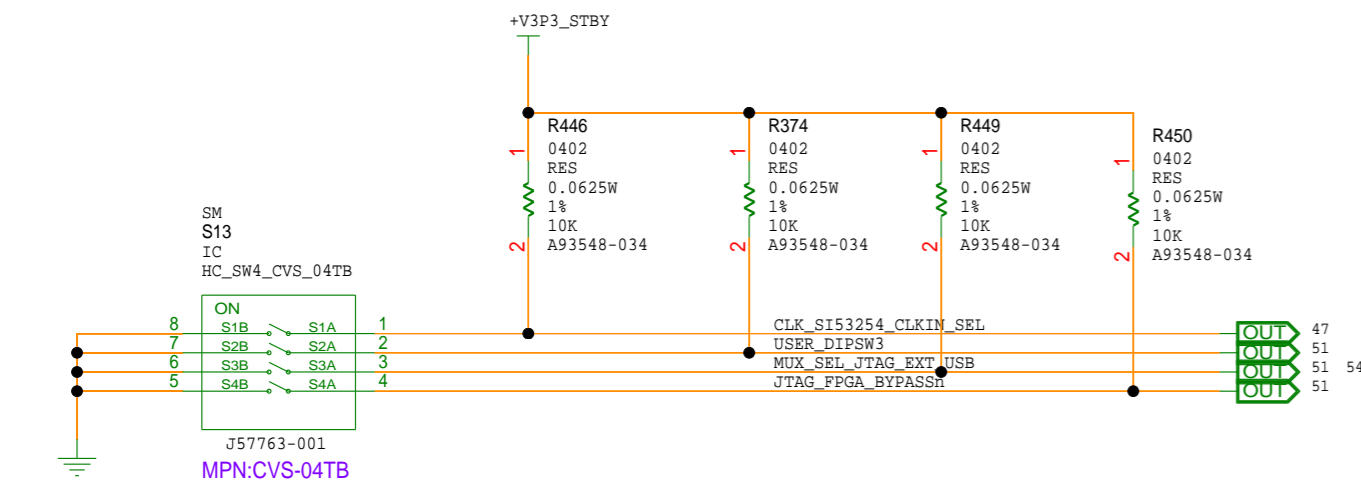
|            |                      |                      |       |                 |                |
|------------|----------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                      | DO NOT SCALE DRAWING |       |                 | SHEET 59 OF 74 |

# SPARE DIP SWITCH



## FMC JTAG MODE SELECT

S7.4: ON DISABLES FMC JTAG MODE  
S7.4: OFF ENABLES FMC JTAG MODE



## JTAG\_FPGA\_BYPASS

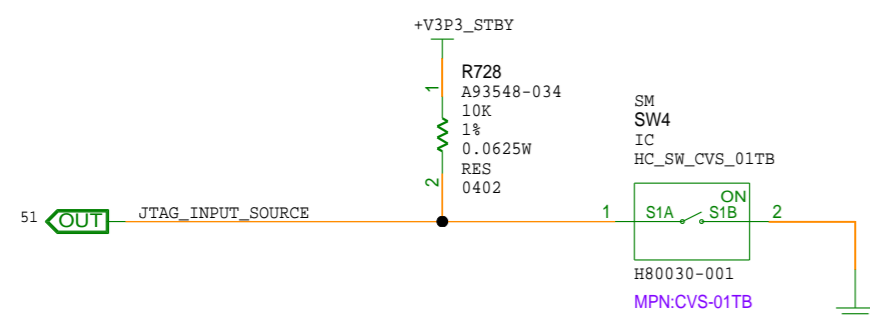
S13-4 ON(LOGIC LOW): FPGA BYPASSED

S13-4 OFF(LOGIC HIGH): FPGA SELECTED

## MUX\_SEL\_JTAG\_EXT\_USB

S13-3 ON(LOGIC LOW): EXT HEADER JTAG SELECTED

S13-3 OFF(LOGIC HIGH): USB JTAG SELECTED



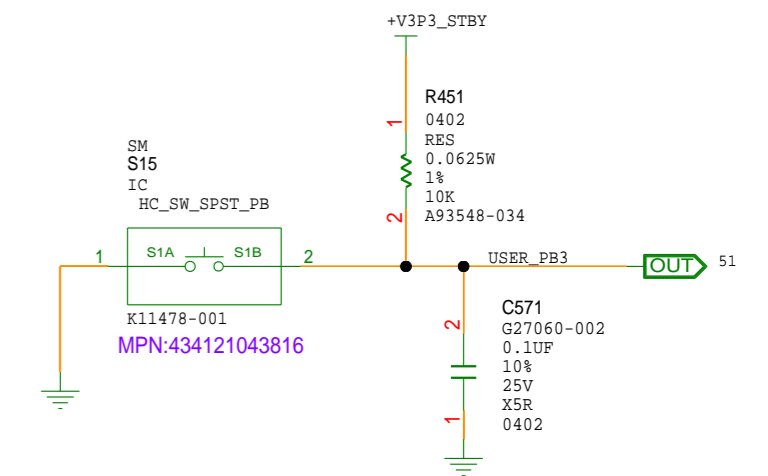
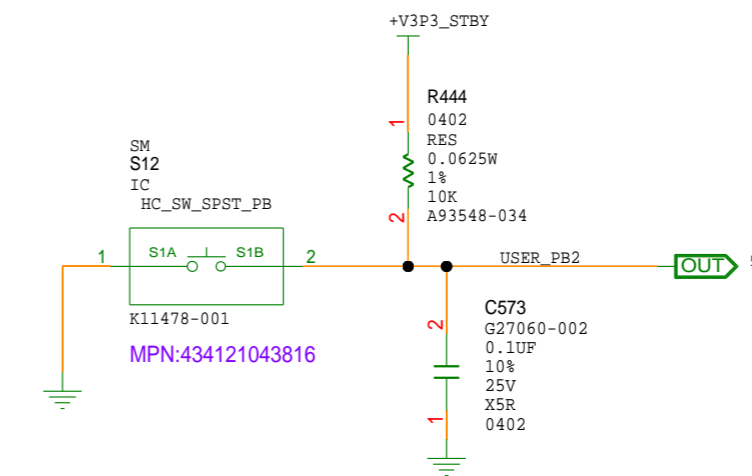
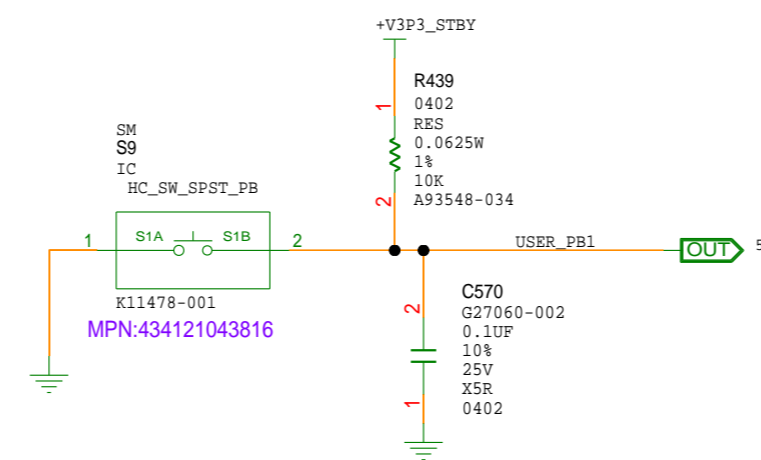
## JTAG MODE SELECT

SW4: ON ENABLES PCIE JTAG MODE

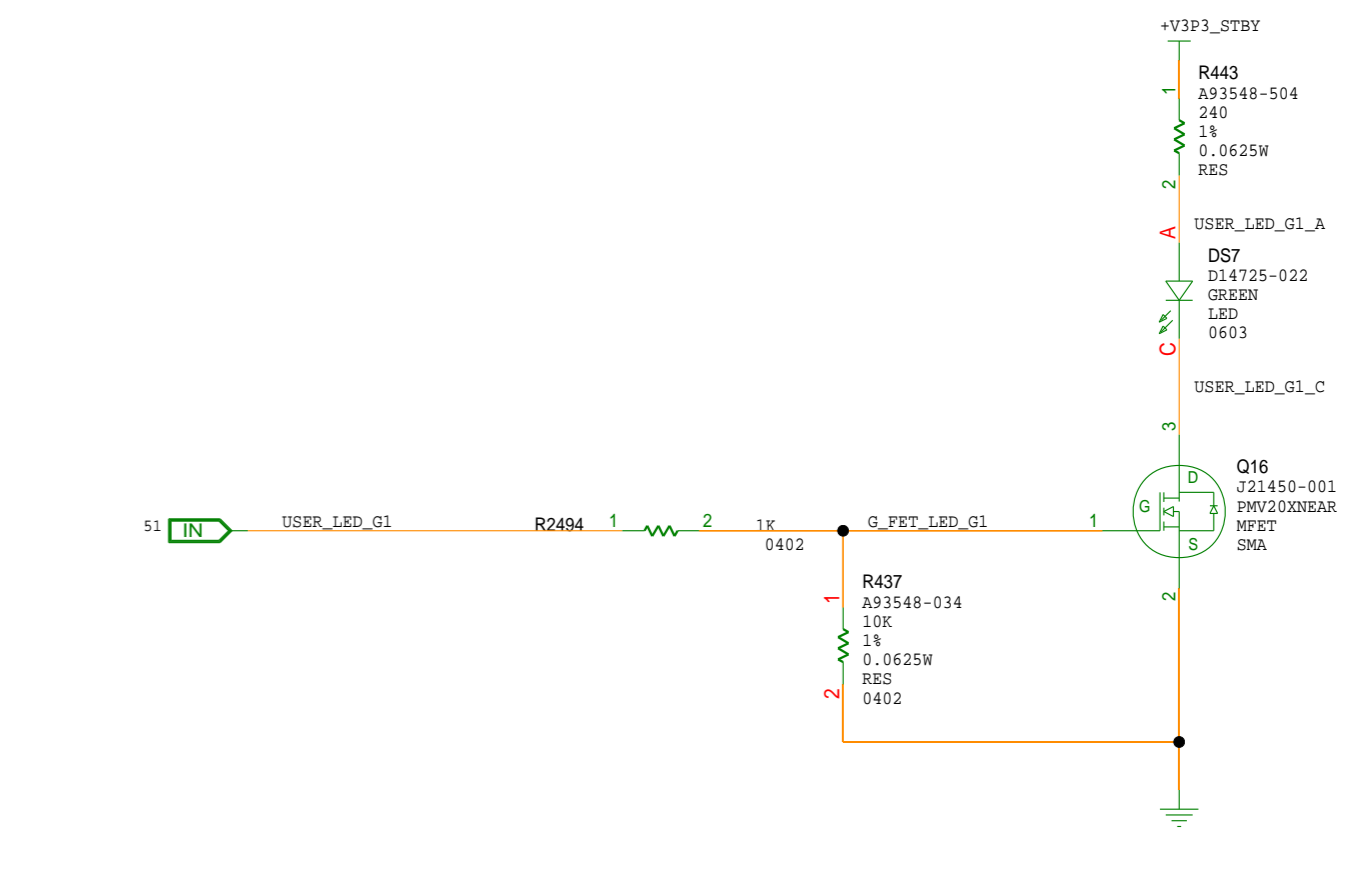
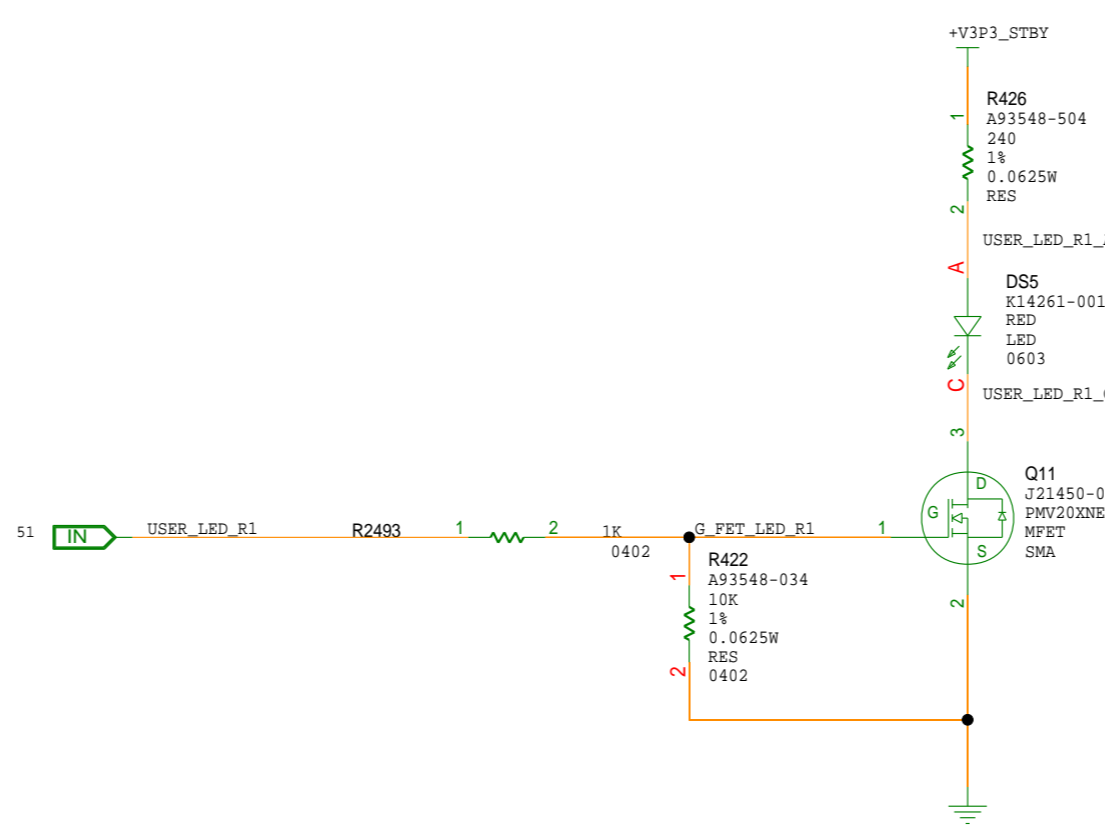
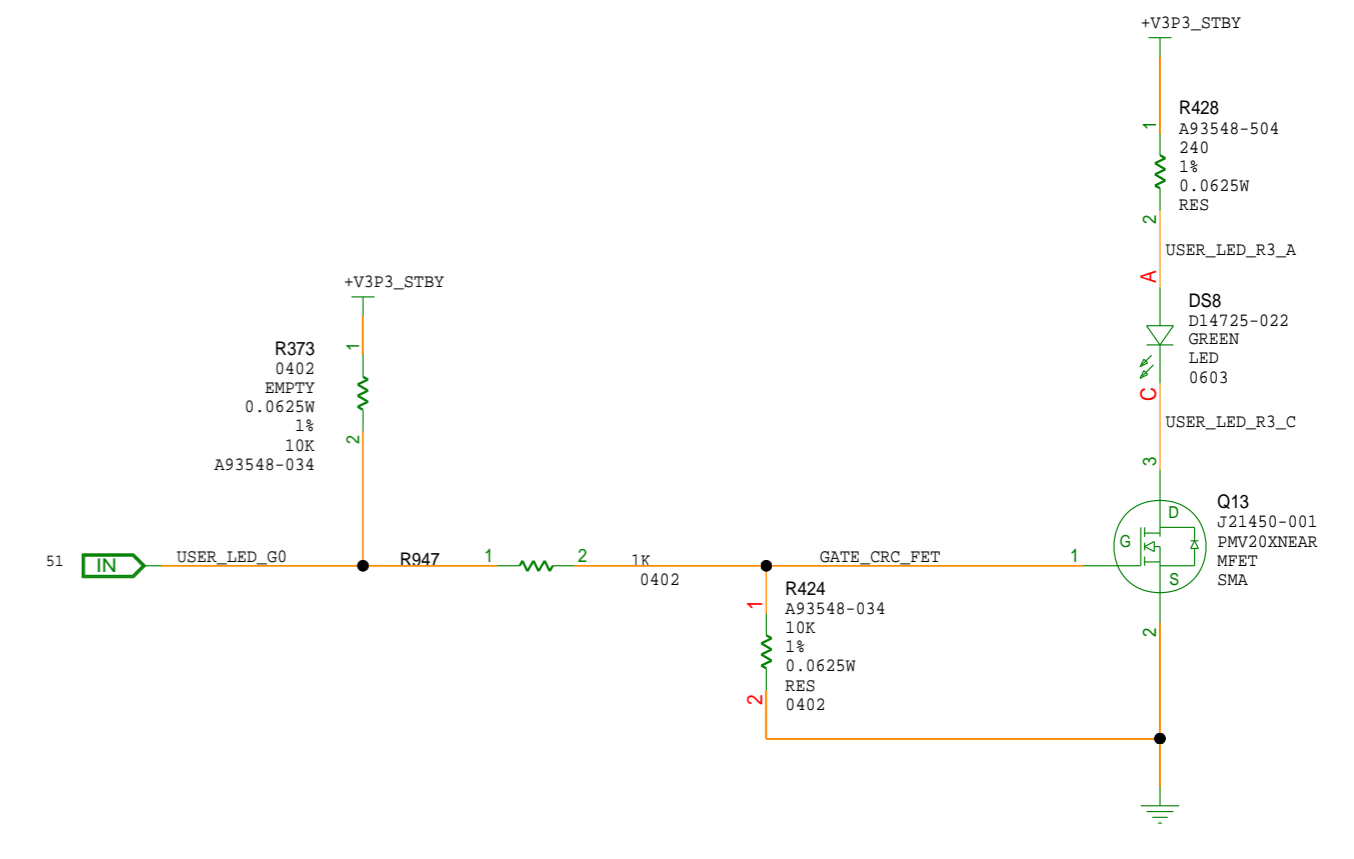
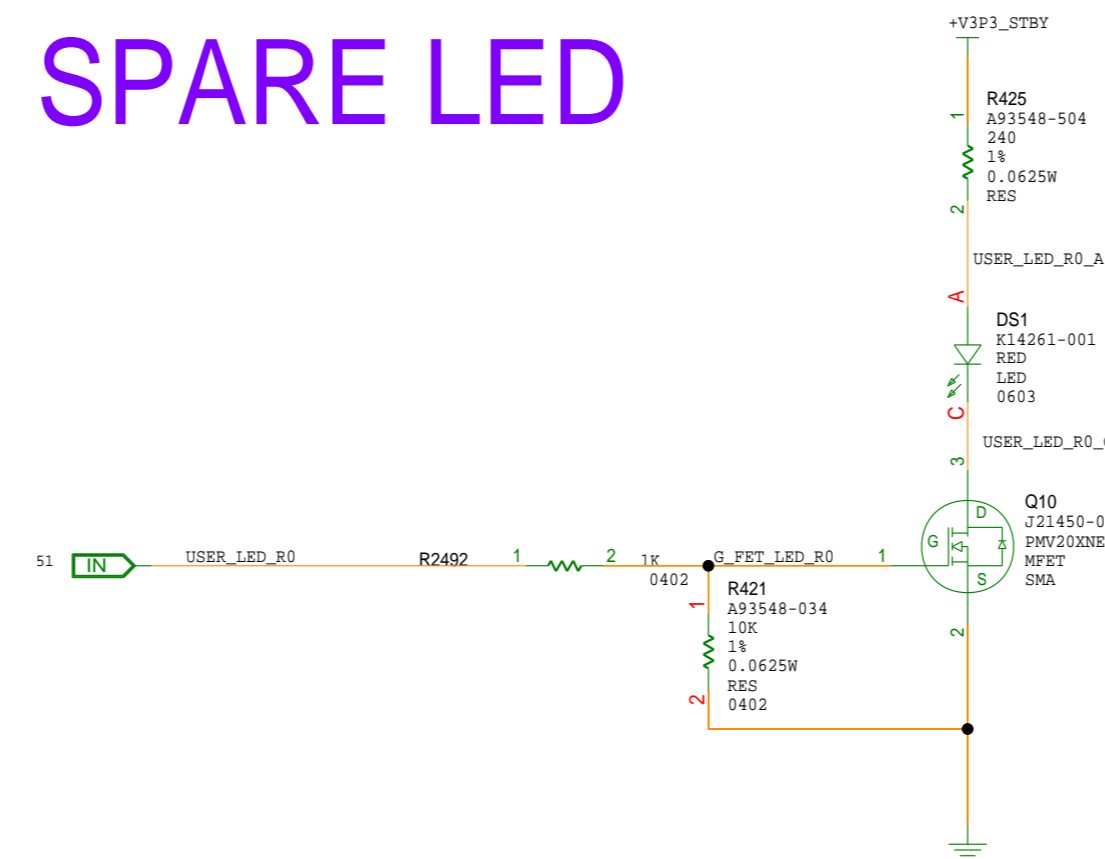
SW4: OFF ENABLES ON BOARD UBI1 MODE

# SPARE\_SWITCH\_LED

# SPARE PUSH BUTTON SWITCH



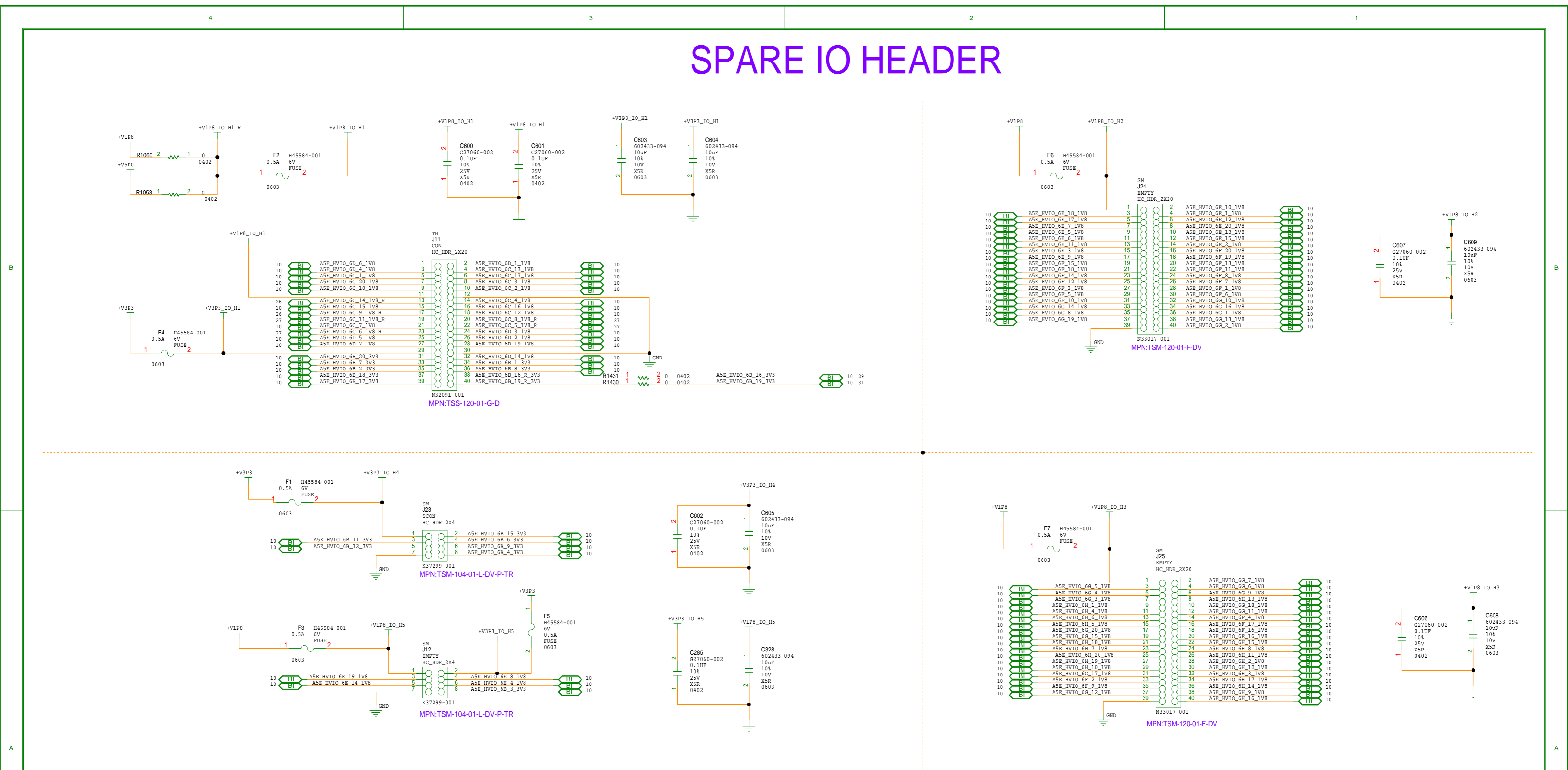
# SPARE LED



Tue Oct 1 13:22:39 2024

|            |                      |                      |       |                 |                |
|------------|----------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                      | DO NOT SCALE DRAWING |       |                 | SHEET 60 OF 74 |

# SPARE IO HEADER

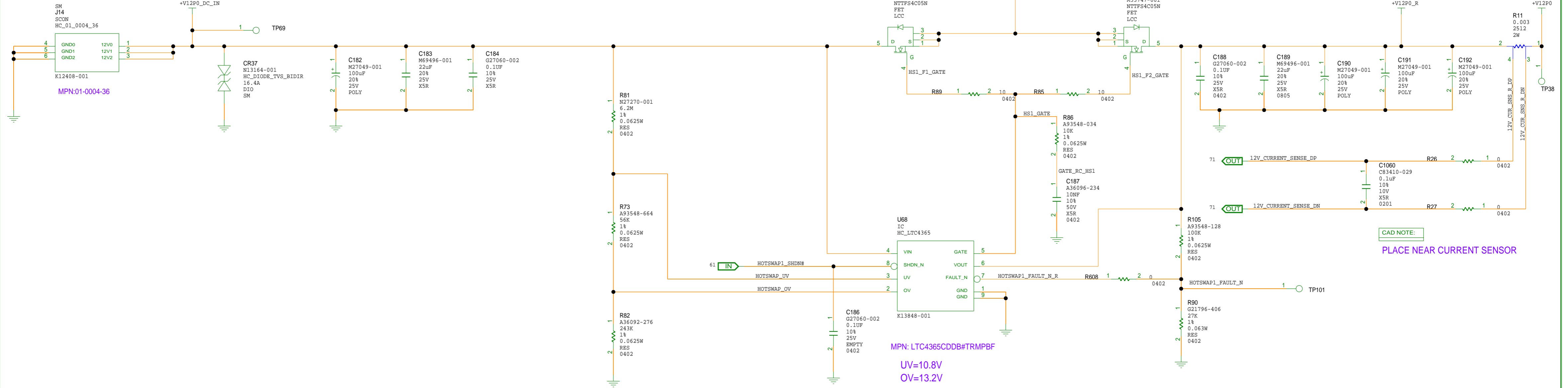


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# SPARE IO HEADER

|            |                      |                      |       |                 |                |
|------------|----------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                      | DO NOT SCALE DRAWING |       |                 | SHEET 61 OF 74 |

# 12V ATX CONN

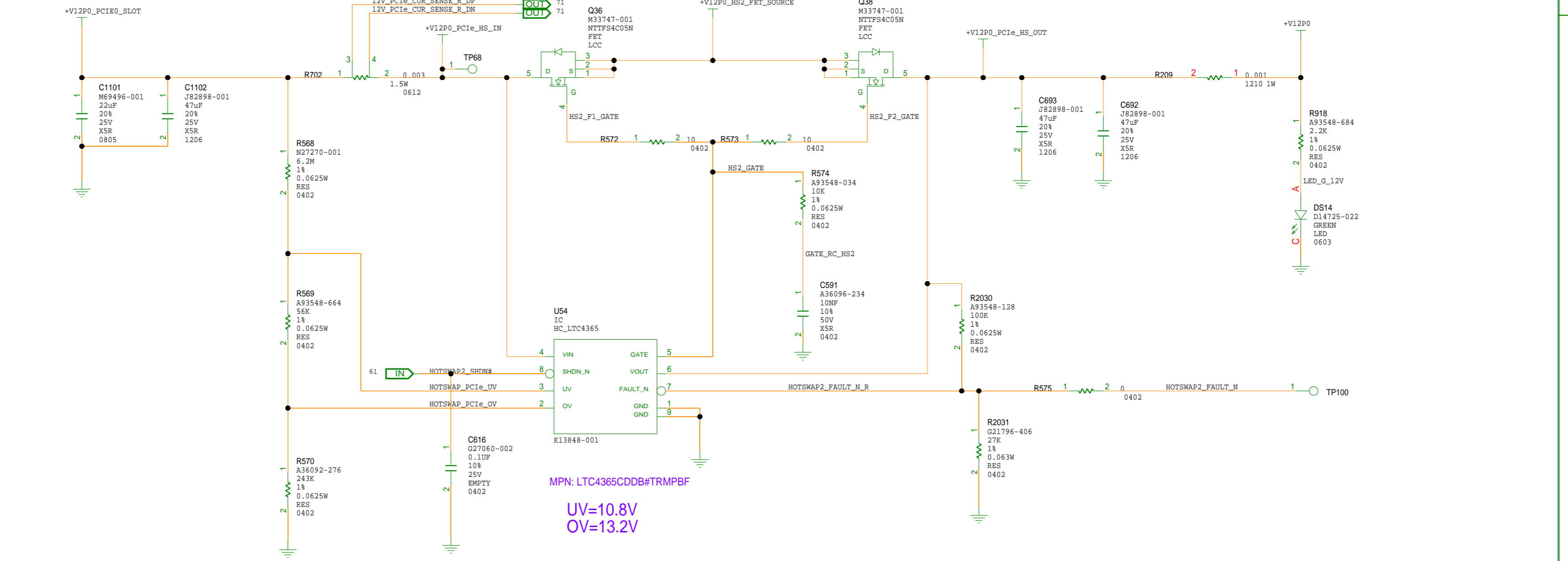


CAD NOTE: KEEP RES CLOSE TO FET AND STICH ENOUGH VIAS AT BOTH END TO CARRY 18A

CAD NOTE: PLACE NEAR CURRENT SENSOR

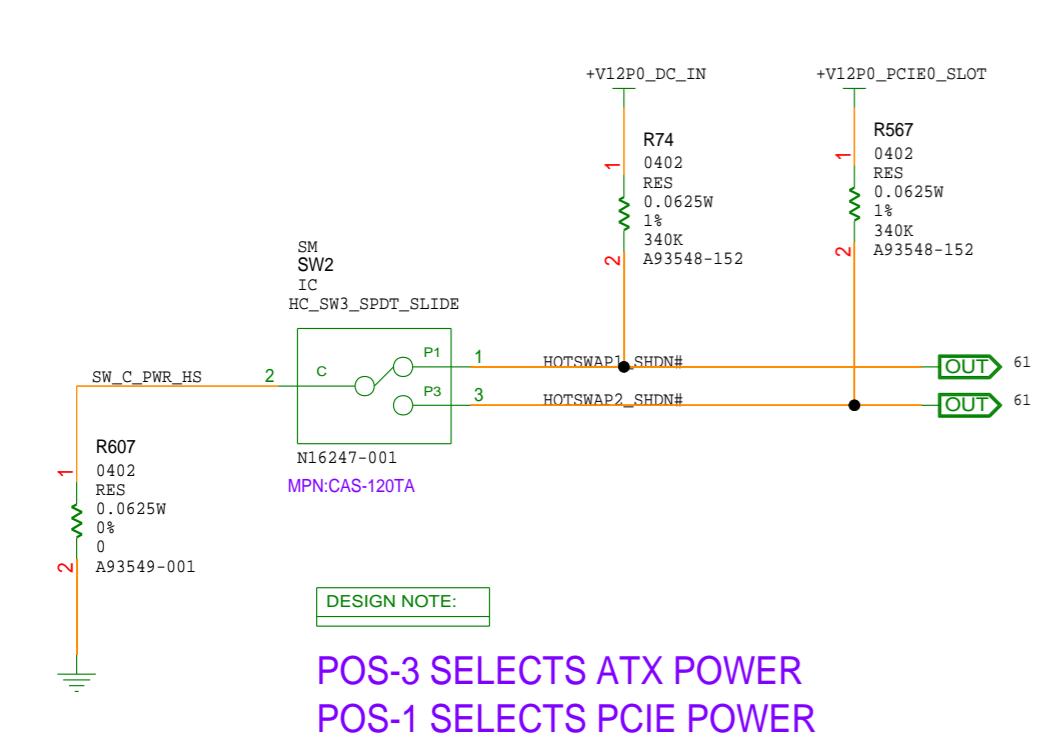
MPN: LTC4365CDDB#TRMPBF  
UV=10.8V  
OV=13.2V

# 12V - PCIE CONN



MPN: LTC4365CDDB#TRMPBF  
UV=10.8V  
OV=13.2V

# 12V POWER SEL SWITCH



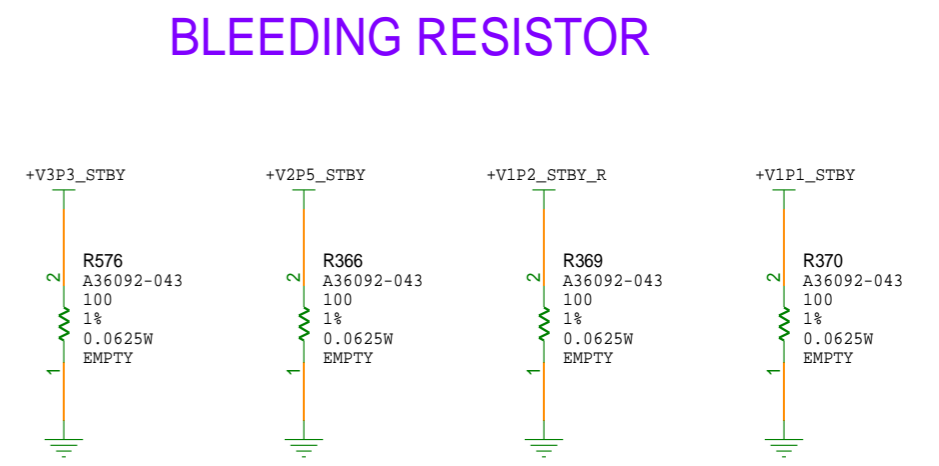
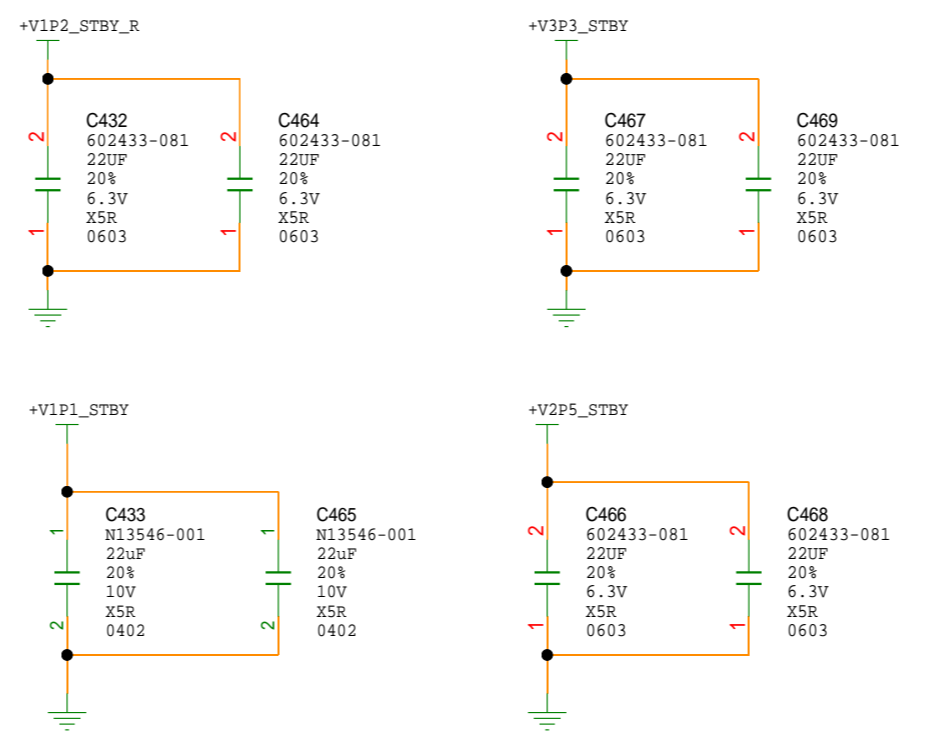
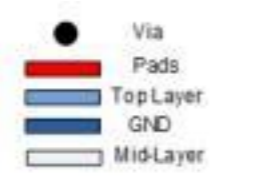
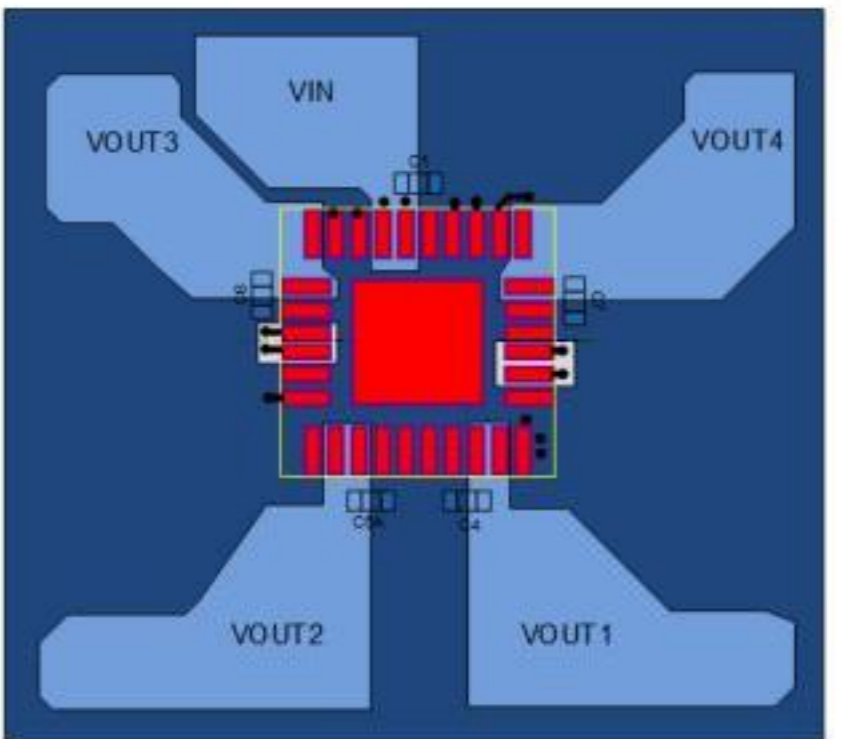
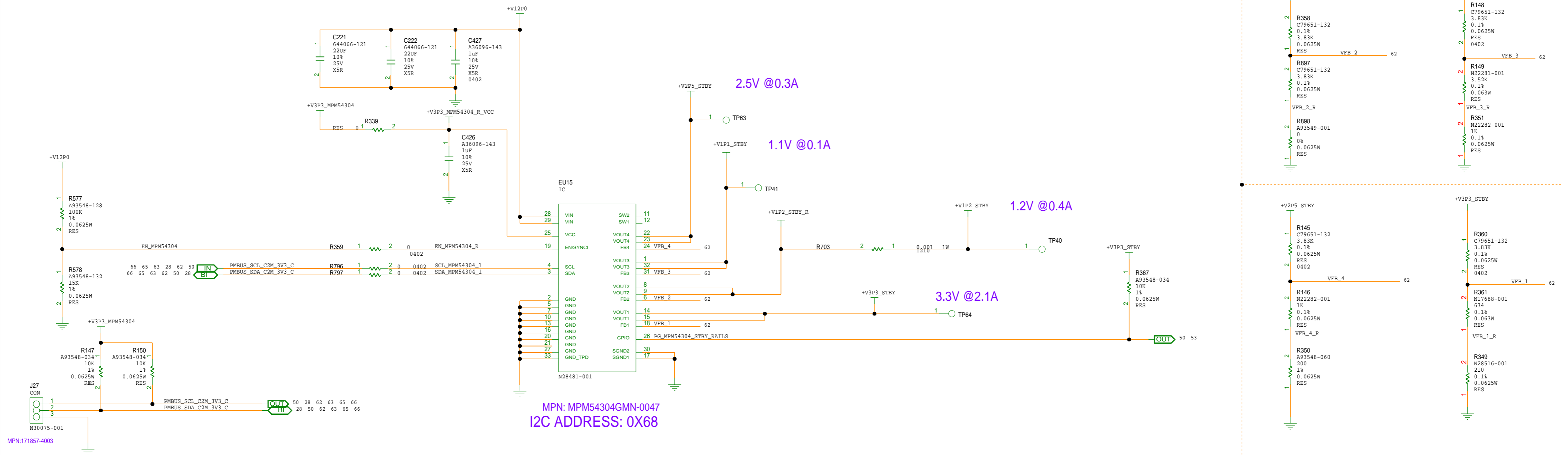
DESIGN NOTE:  
POS-3 SELECTS ATX POWER  
POS-1 SELECTS PCIE POWER

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# 12V POWER INPUT

|            |                      |                      |       |                 |                |
|------------|----------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                      | DO NOT SCALE DRAWING |       |                 | SHEET 62 OF 74 |

# +V1P1,+V1P2,+V2P5,+V3P3 - STBY



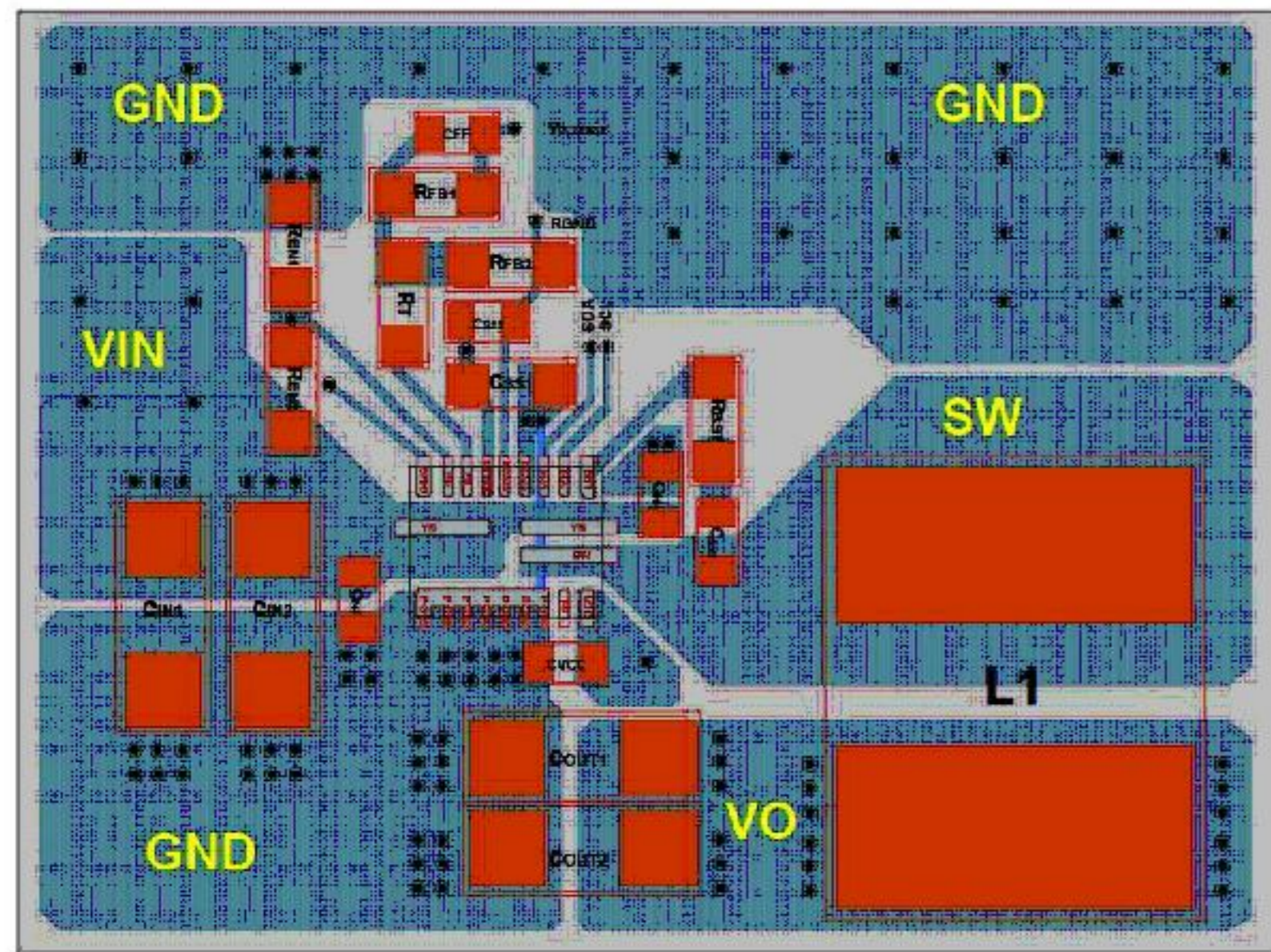
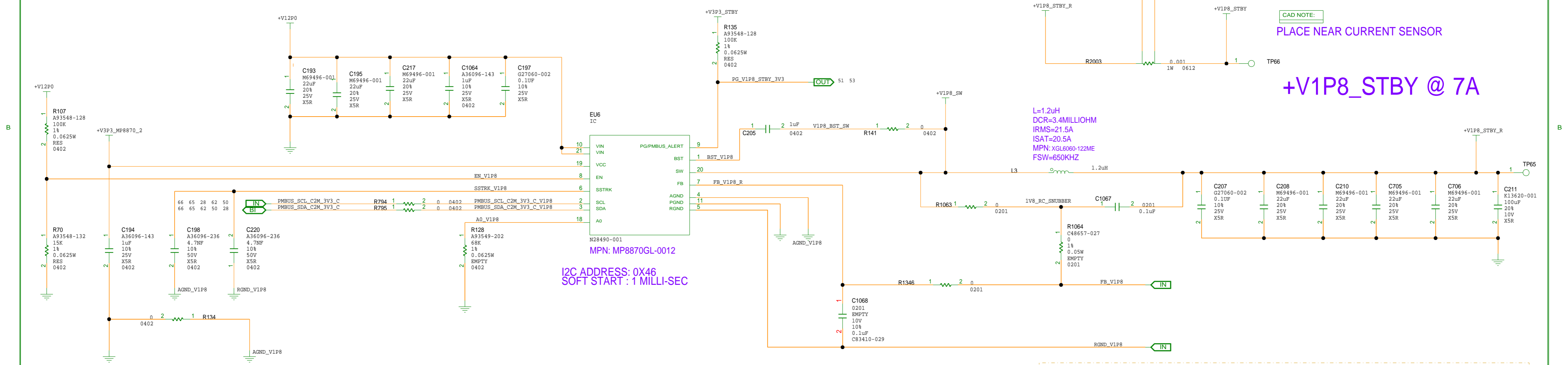
## BLEEDING RESISTOR

Tue Oct 1 13:22:40 2024

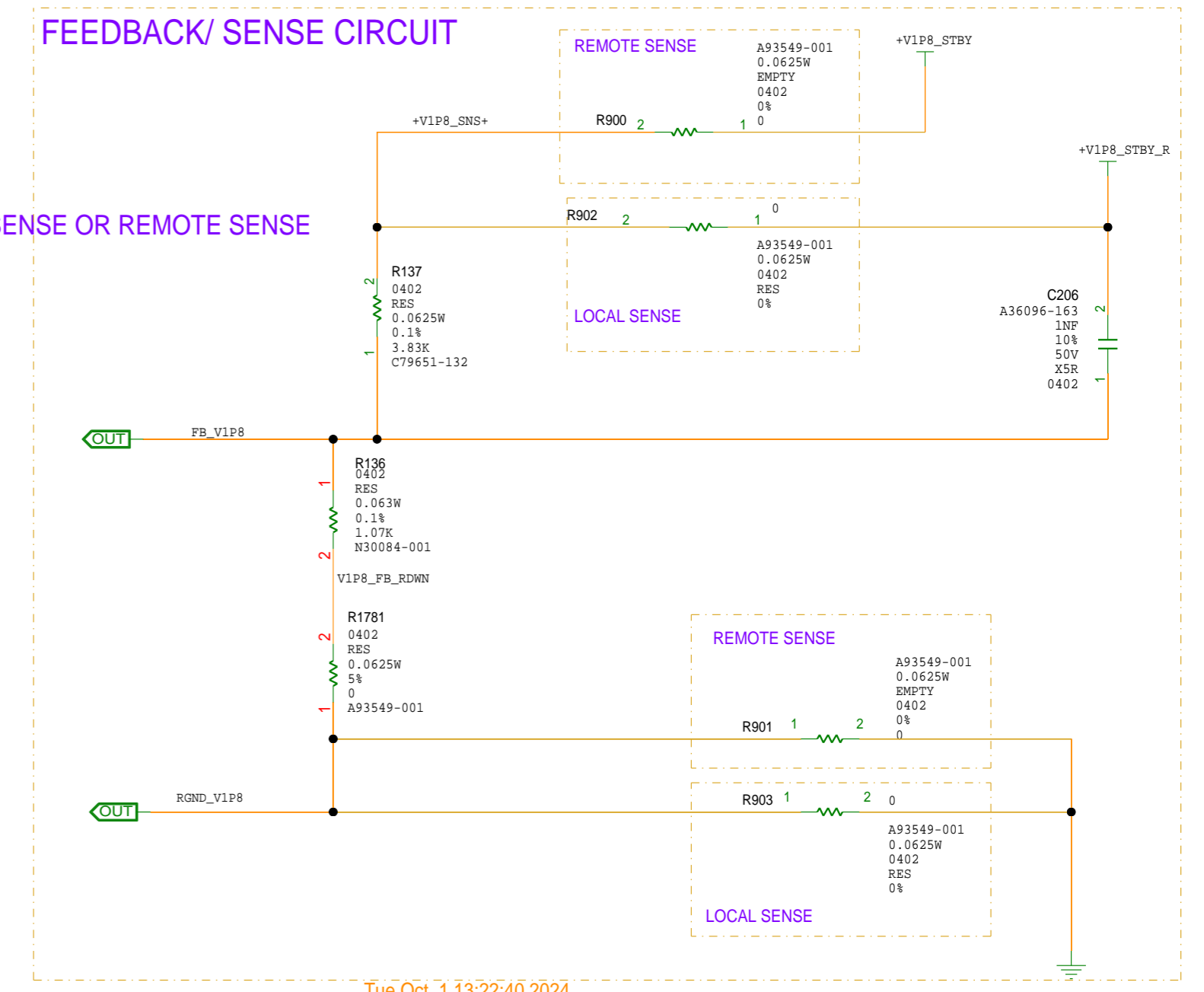
VR - +V1P1, +V1P2, +V2P5, +V3P3 - STBY

|            |                      |                      |       |                 |                |
|------------|----------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                      | DO NOT SCALE DRAWING |       |                 | SHEET 63 OF 74 |

# +V1P8 STBY



**CAD NOTE:**  
ROUTE THEM AS DIFFERENTIAL  
AVOID STUB WHEN USING LOCAL SENSE OR REMOTE SENSE

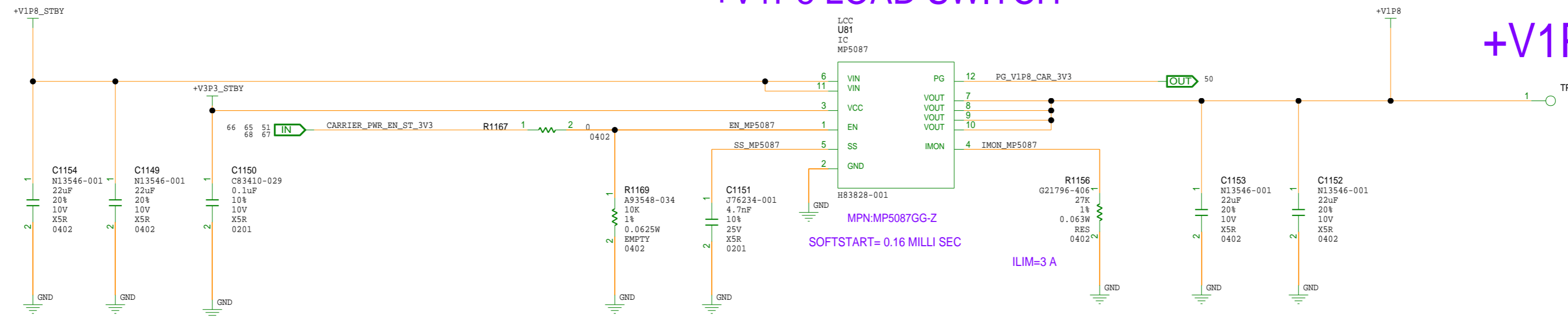


VR- +V1P8 - STBY

|            |                  |                      |       |                 |          |
|------------|------------------|----------------------|-------|-----------------|----------|
| DEPARTMENT | An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV      |
|            |                  | C+                   | 34649 | 150-330724-B1   | 2.0      |
| SCALE:     |                  | DO NOT SCALE DRAWING |       | SHEET           | 64 OF 74 |

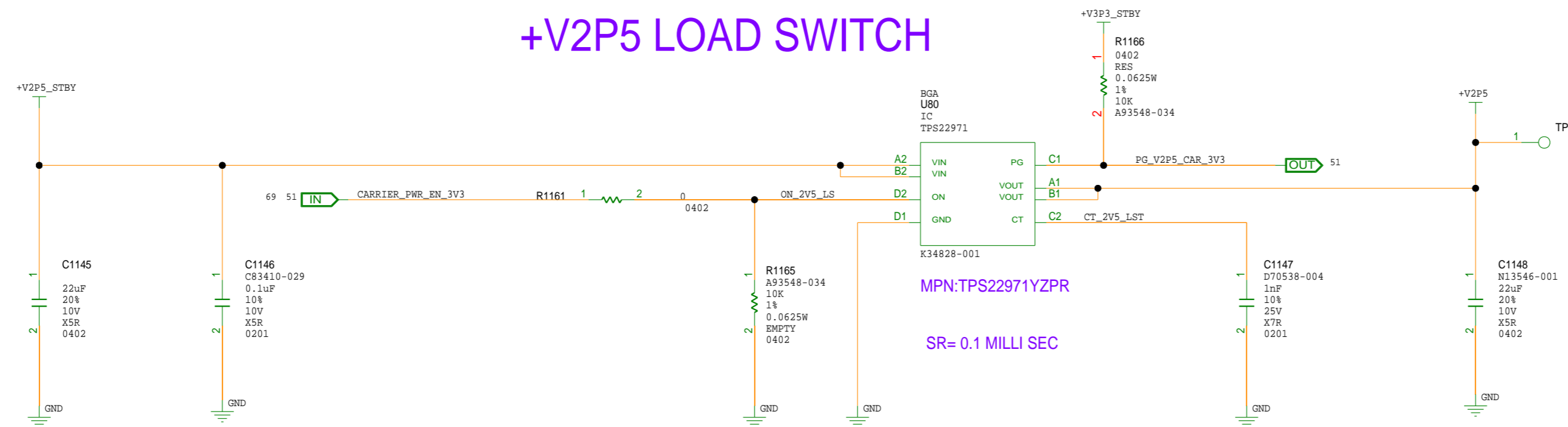
### +V1P8 LOAD SWITCH

### +V1P8 @ 2.2A



### +V2P5 LOAD SWITCH

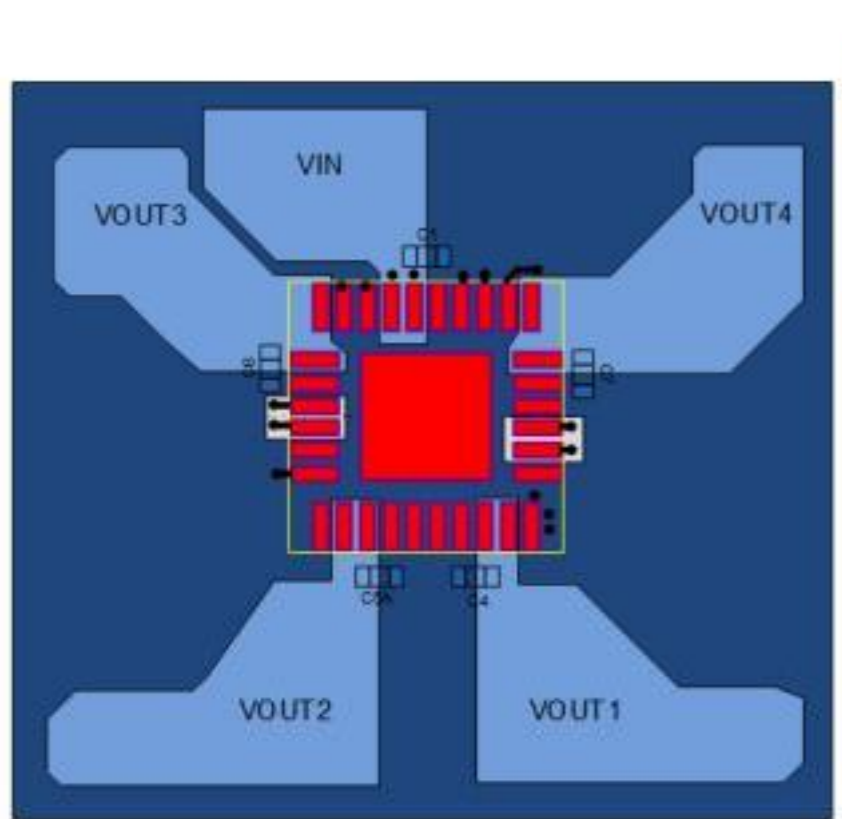
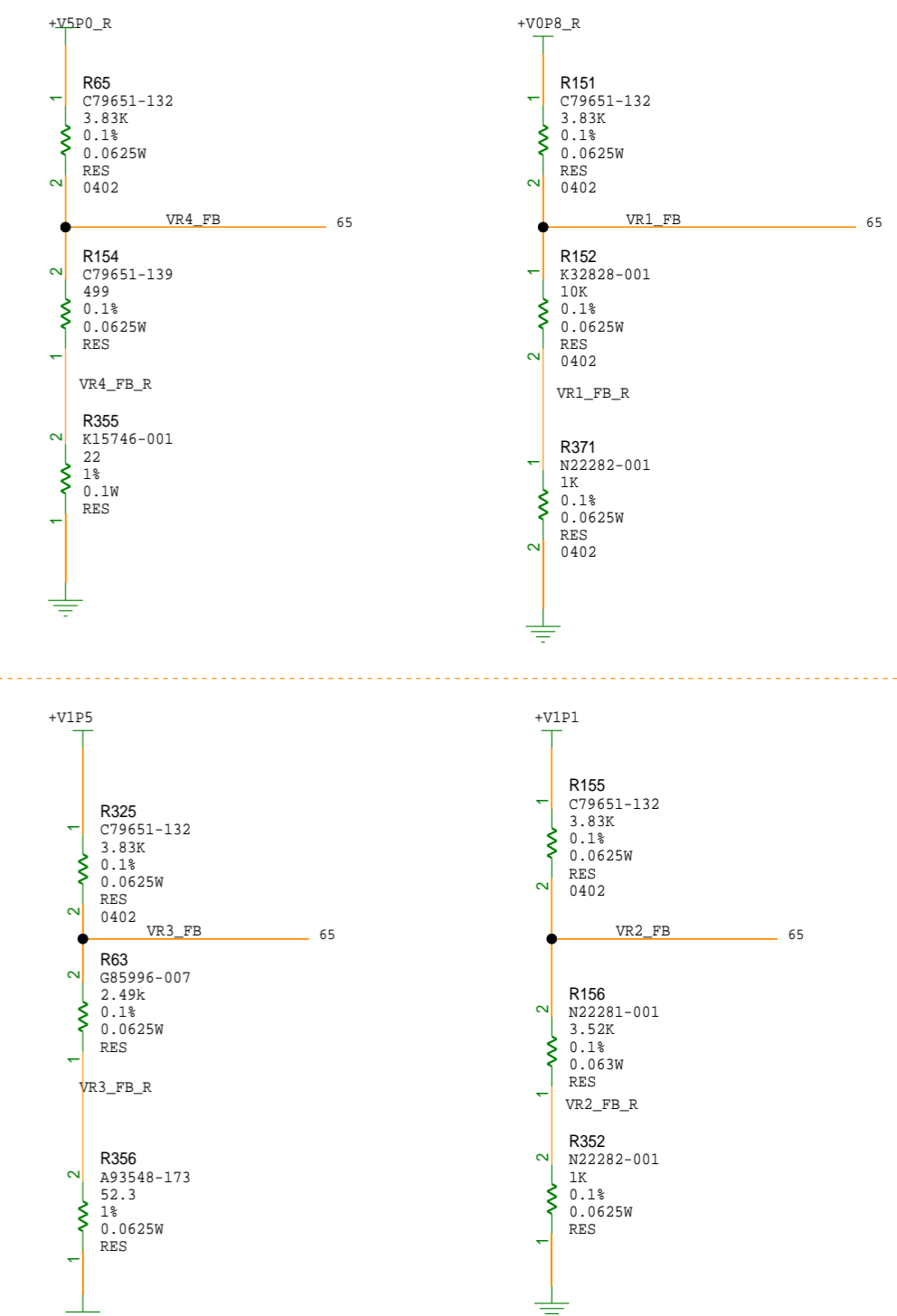
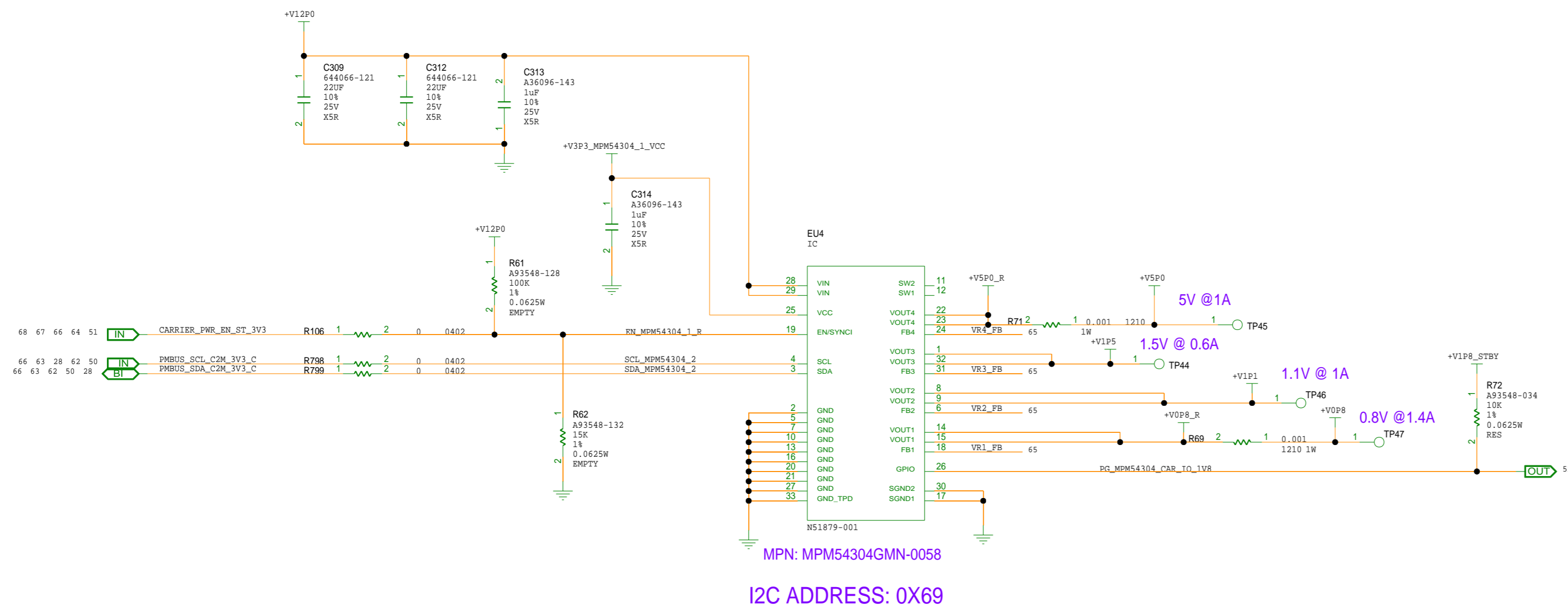
### +V2P5 @ 0.3A



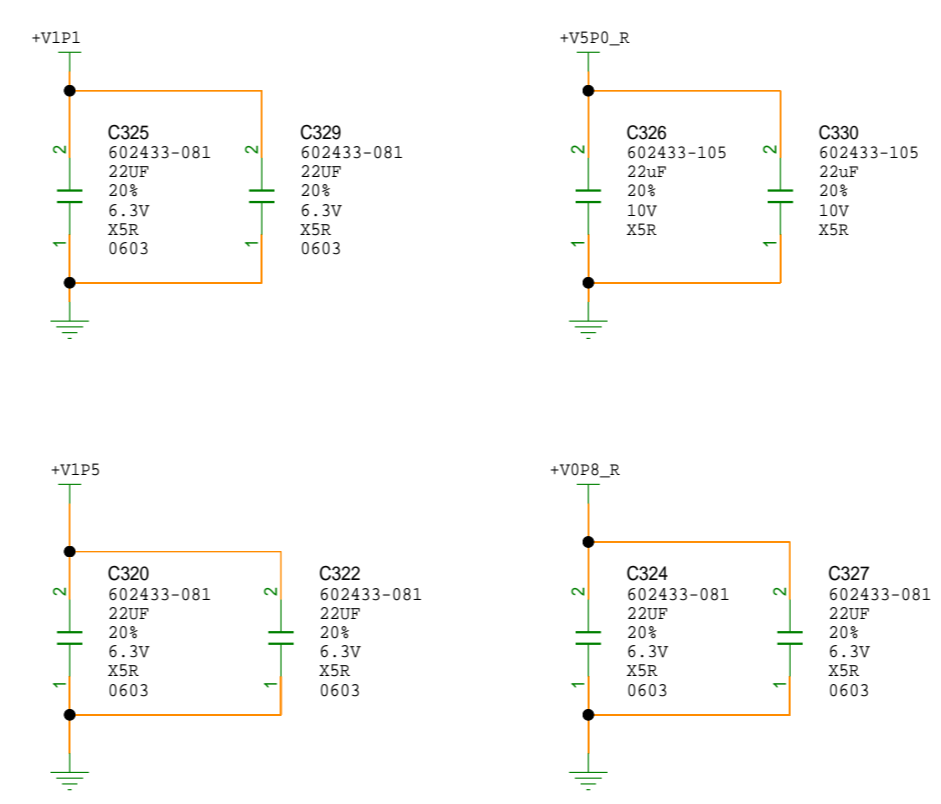
Tue Oct 1 13:22:41 2024



# +V0P8,+V1P1,+V1P5,+V5P0



● Via  
 ■ Pads  
 ■ Top Layer  
 ■ GND  
 ■ Mid-Layer



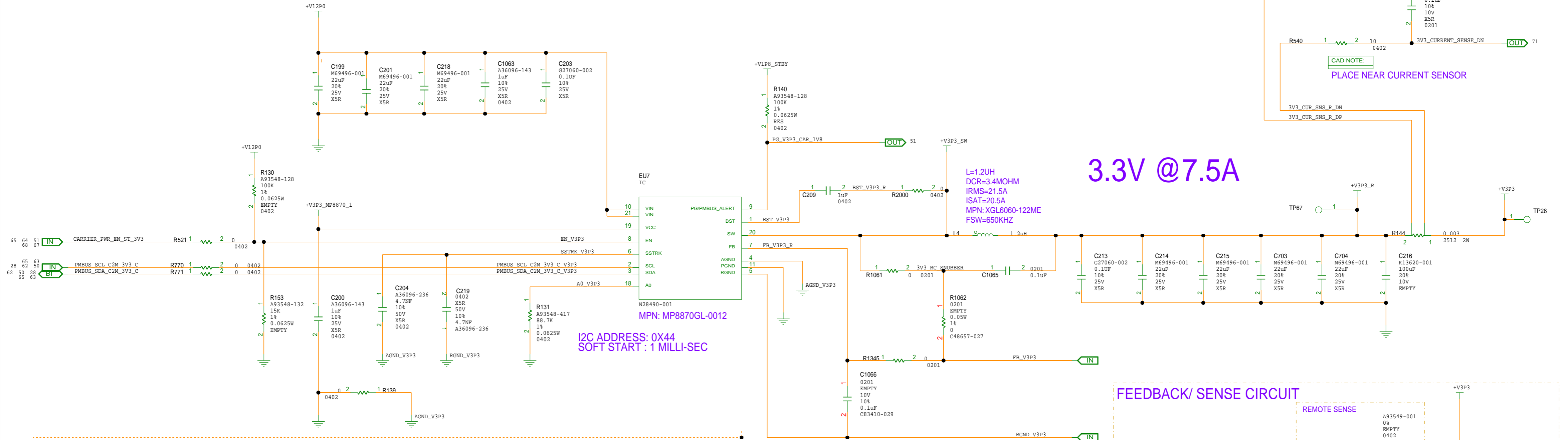
## BLEEDING RESISTOR

Tue Oct 1 13:22:41 2024

VR-+V0P8,+V1P1,+V1P5,+V5P0

|            |                      |                      |       |                 |                |
|------------|----------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                      | DO NOT SCALE DRAWING |       |                 | SHEET 66 OF 74 |

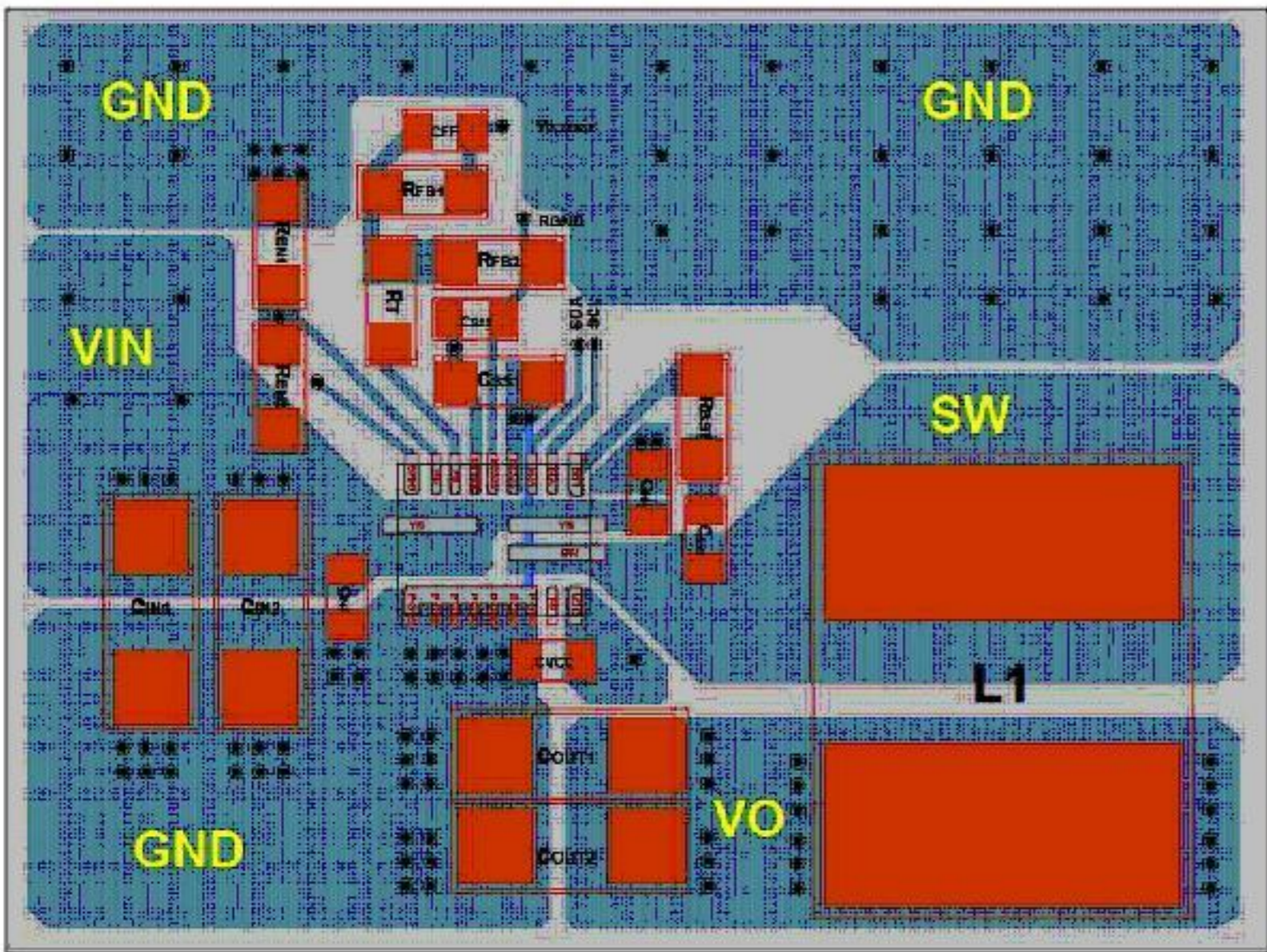
# +V3P3 RAIL



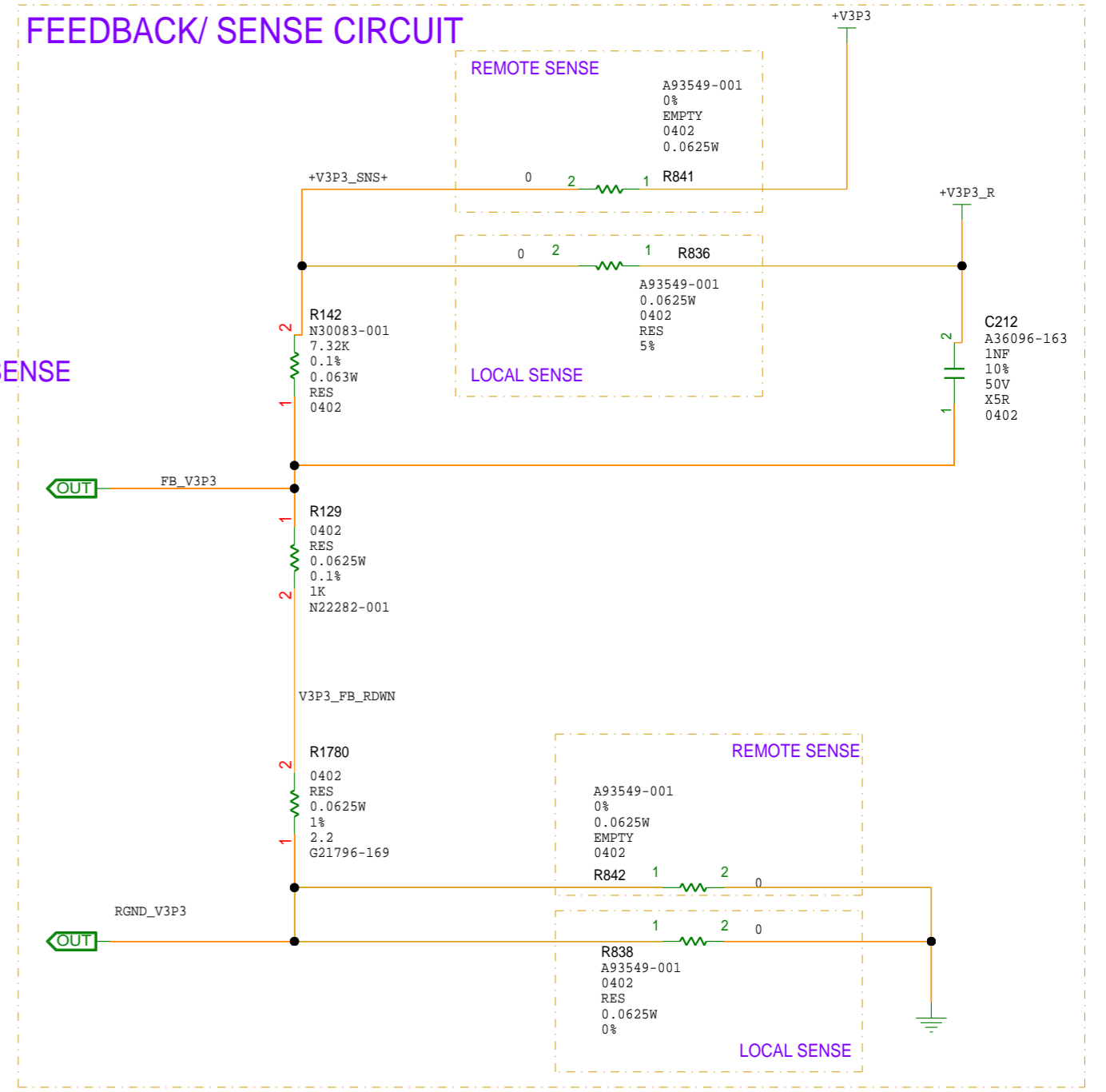
3.3V @ 7.5A

I2C ADDRESS: 0X44  
SOFT START : 1 MILLI-SEC

CAD NOTE:  
SENSE SIGNALS ROUTE AS DIFFERENTIAL  
AVOID STUB WHEN USING LOCAL SENSE OR REMOTE SENSE



- Top Layer
- Bottom Layer
- Inner Layer
- Vias

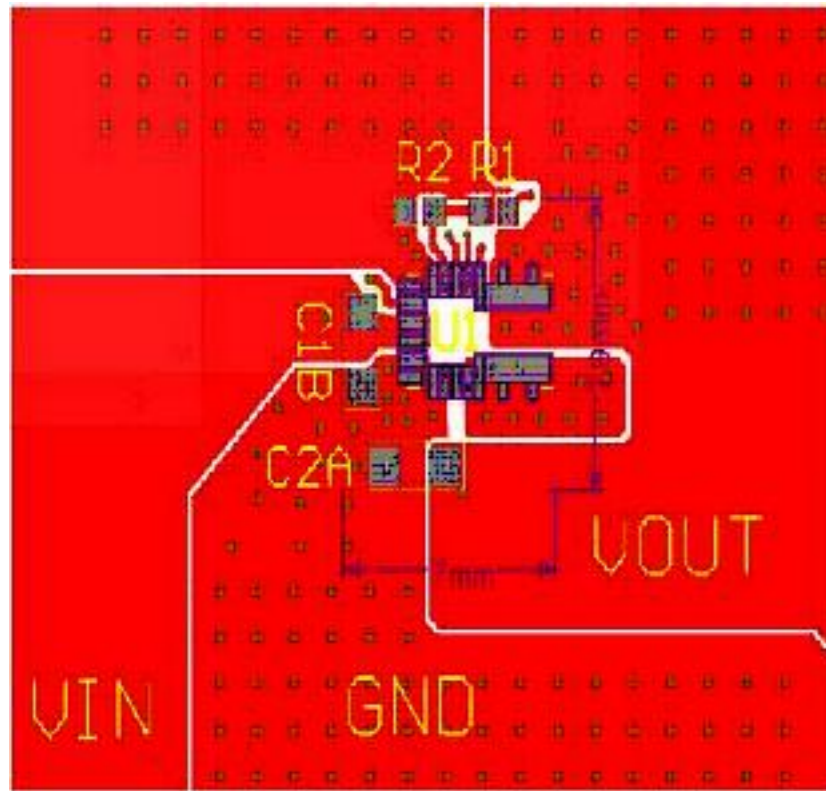
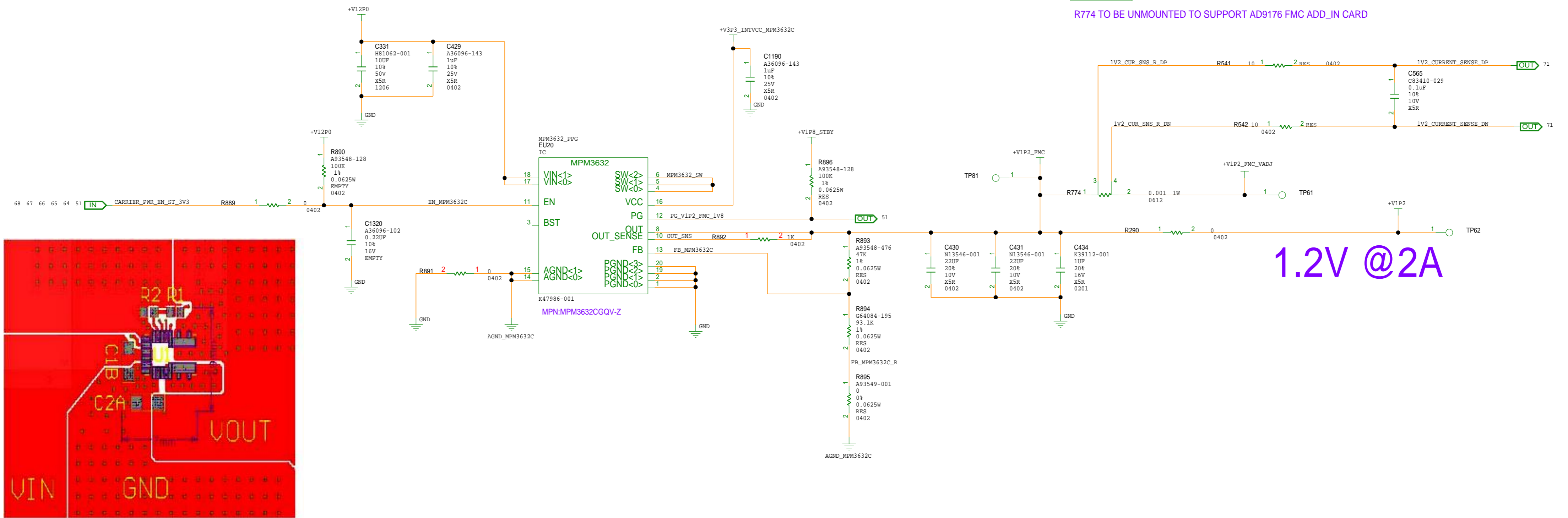


Tue Oct 1 13:22:41 2024

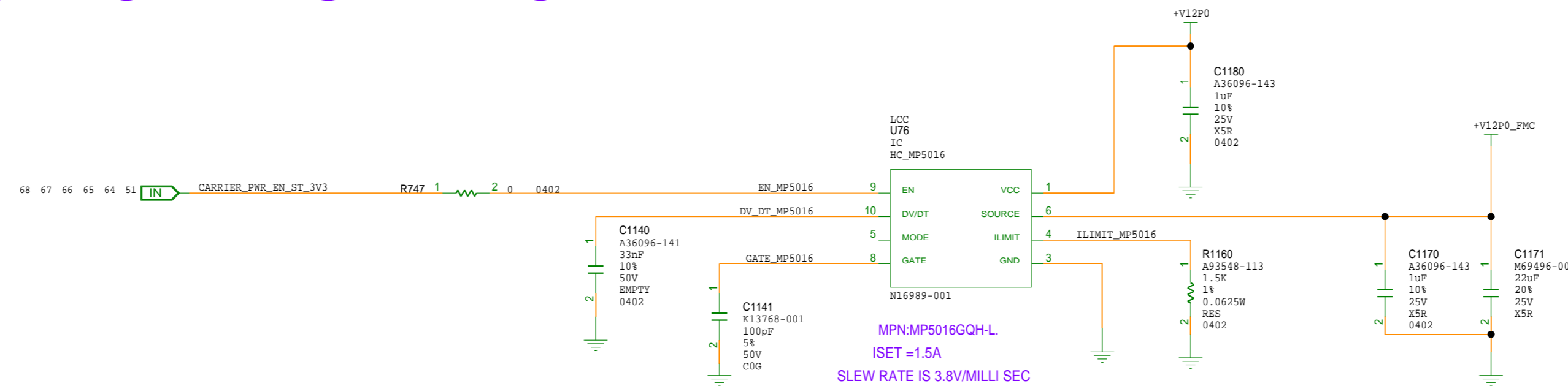
VR- +V3P3

|            |                                   |                      |       |                 |                |
|------------|-----------------------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <b>altera</b><br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                                   | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                                   | DO NOT SCALE DRAWING |       |                 | SHEET 67 OF 74 |

# +V1P2\_FMC



# +V12P0\_FMC LOAD SWITCH

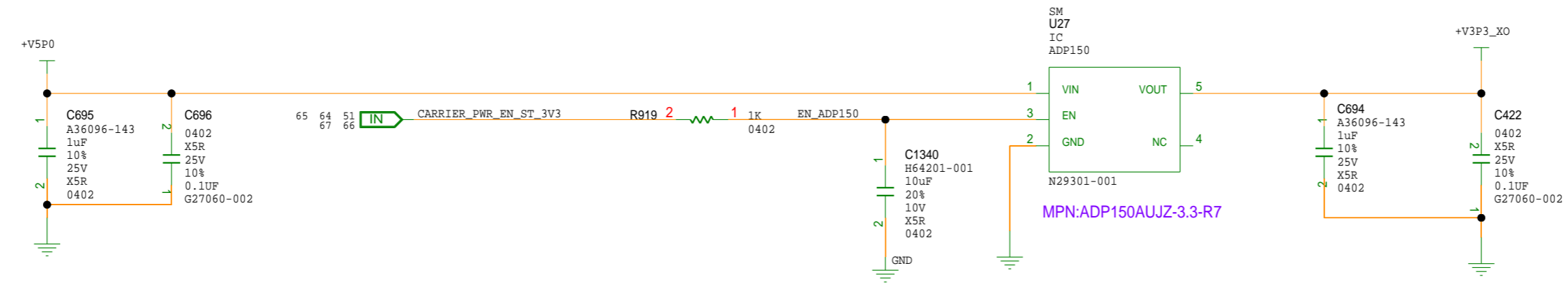


Tue Oct 1 13:22:41 2024

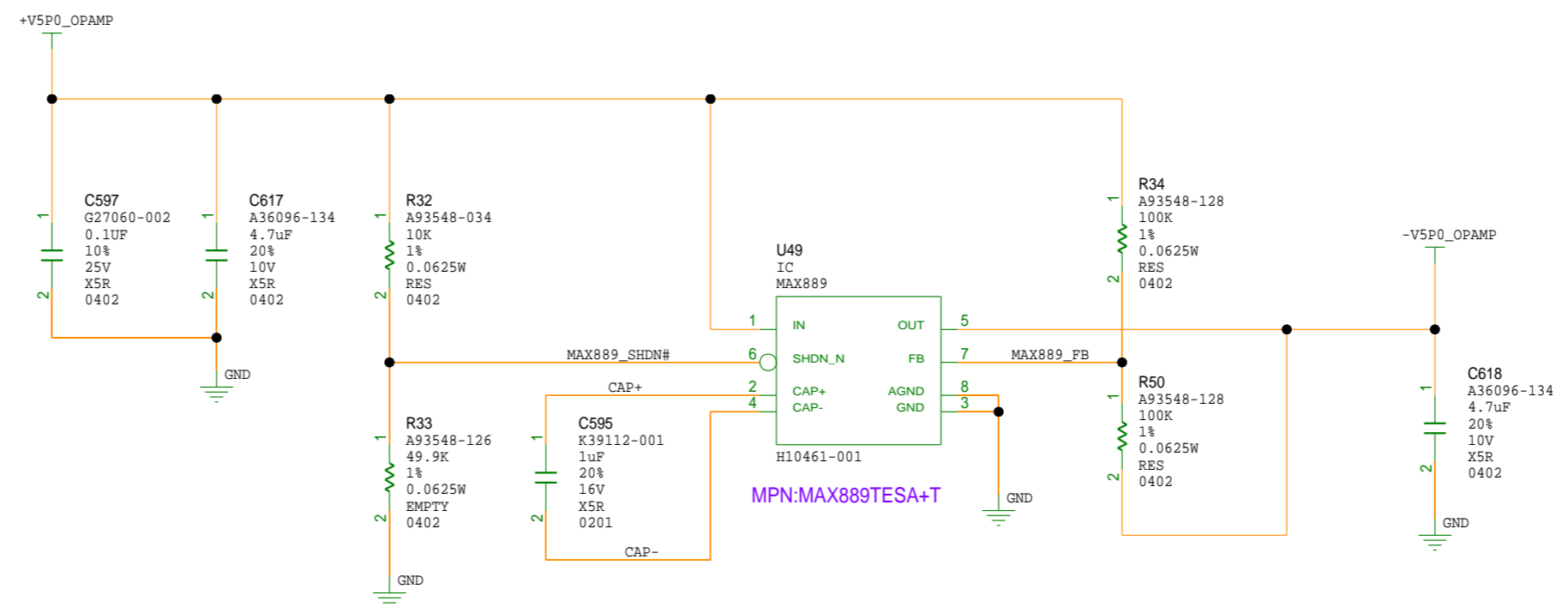
VR-+V1P2\_FMC, +V12P0\_FMC LS

|            |                      |                      |       |                 |                |
|------------|----------------------|----------------------|-------|-----------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV            |
|            |                      | C+                   | 34649 | 150-330724-B1   | 2.0            |
| SCALE:     |                      | DO NOT SCALE DRAWING |       |                 | SHEET 68 OF 74 |

# +V3P3\_XO - SI5518



# -V5P0 - TRI LEVEL SYNC



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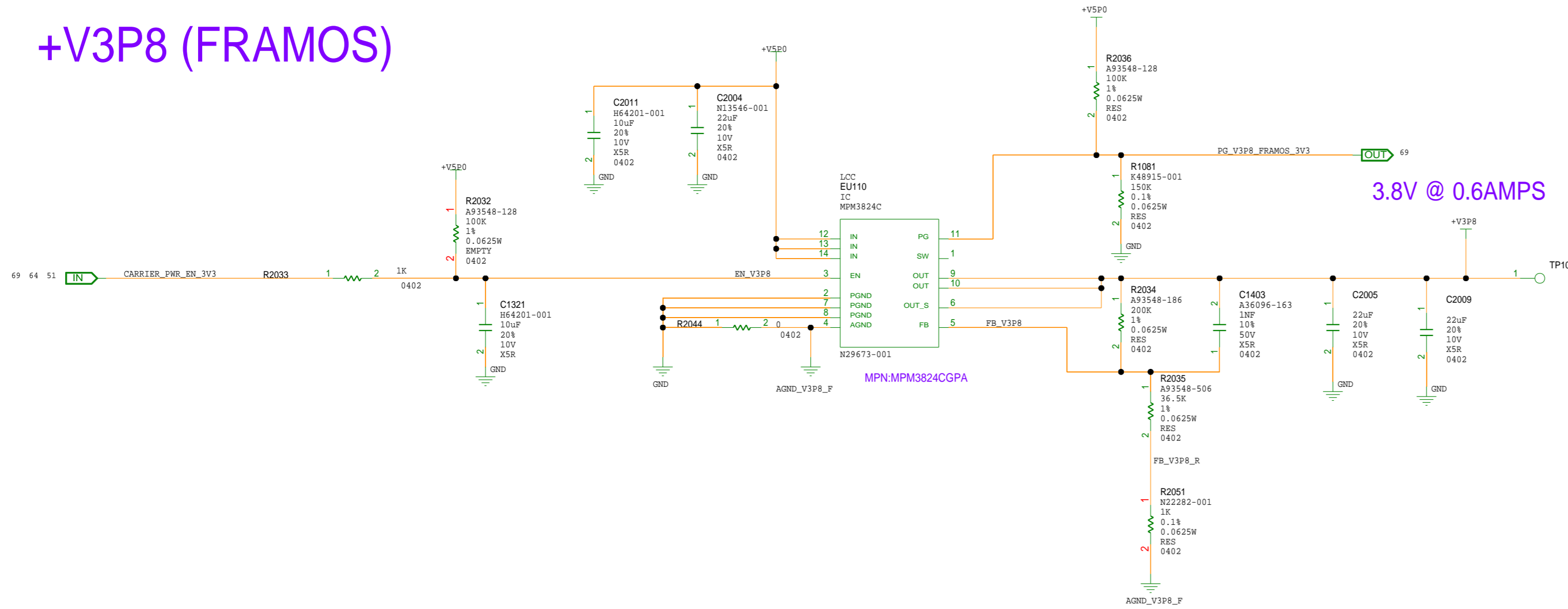
VR-+V3P3\_XO, -V5P0

DEPARTMENT

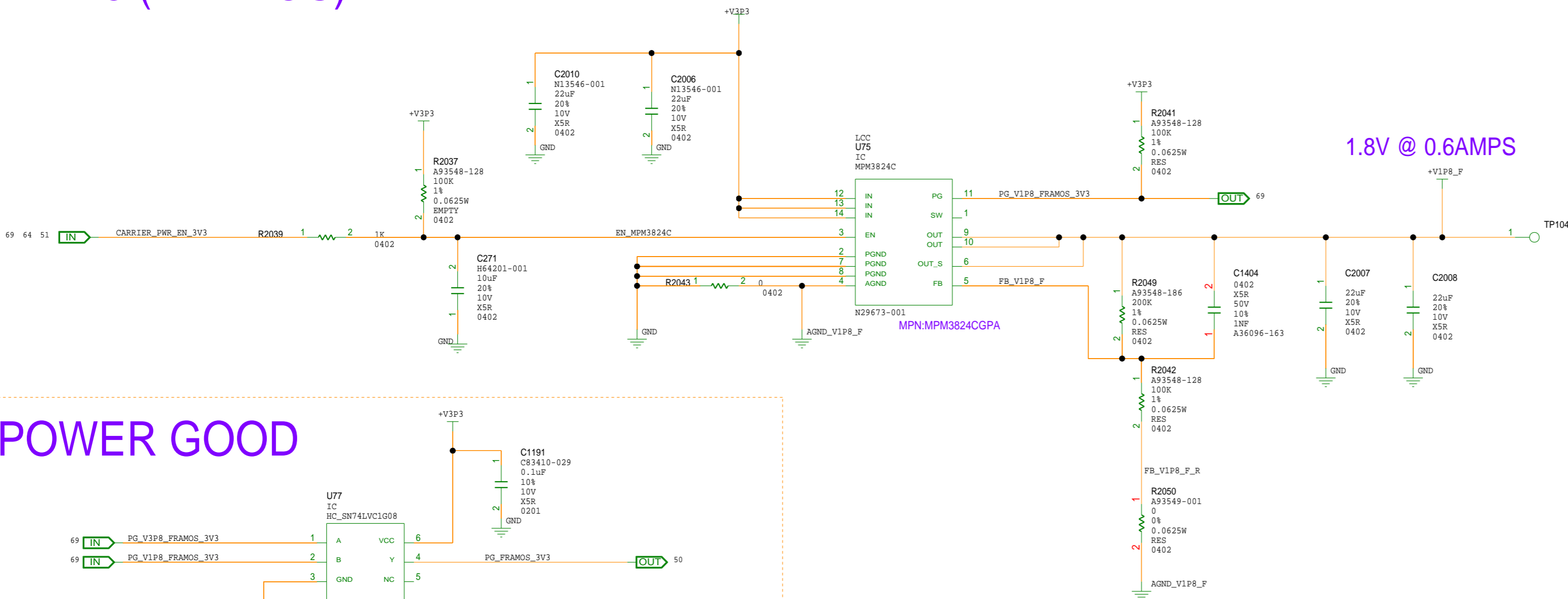


|            |               |                                  |                |
|------------|---------------|----------------------------------|----------------|
| SIZE<br>C+ | CODE<br>34649 | DOCUMENT NUMBER<br>150-330724-B1 | REV<br>2.0     |
| SCALE:     |               | DO NOT SCALE DRAWING             | SHEET 69 OF 74 |

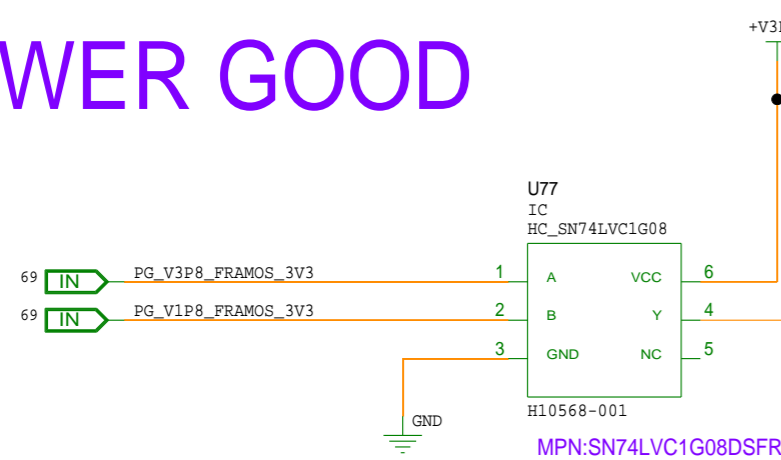
# +V3P8 (FRAMOS)



# +V1P8 (FRAMOS)



# POWER GOOD



## PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation, especially for the high switching frequency converter. A poorly optimized layout can result in poor line or load regulation or stability issues. For the best results, refer to Figure 3 and follow the guidelines below:

1. Place a 0805-sized ceramic input capacitor as close to the IC pins as possible.
2. Place a 0402-sized capacitor place at the bottom of the IC (optional).
3. Connect the two ends of the ceramic capacitor directly to IN and PGND.
4. Place the external feedback resistor next to FB.
5. Connect AGND and PGND at a single point.

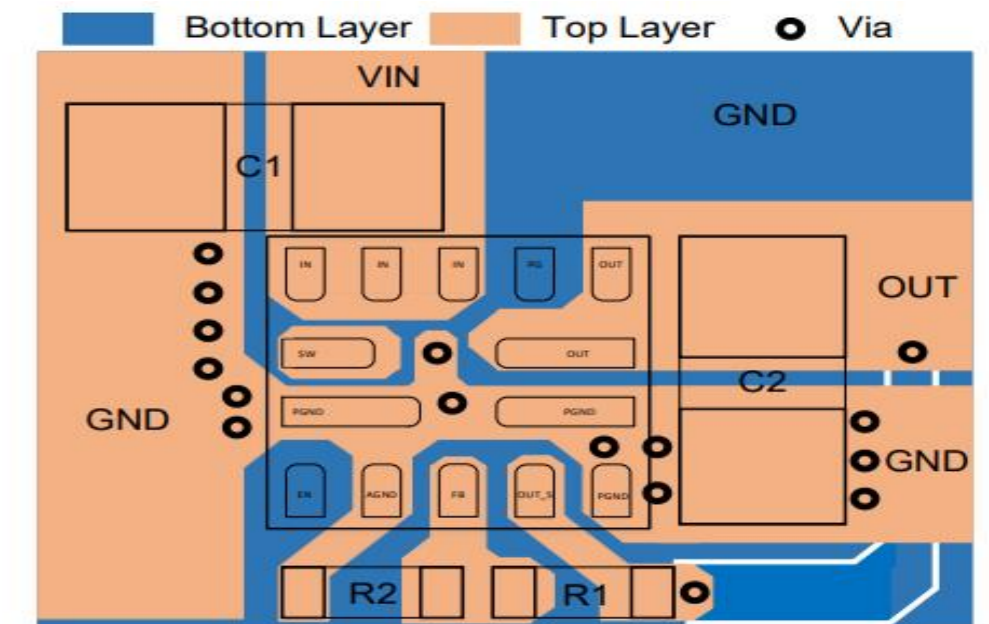



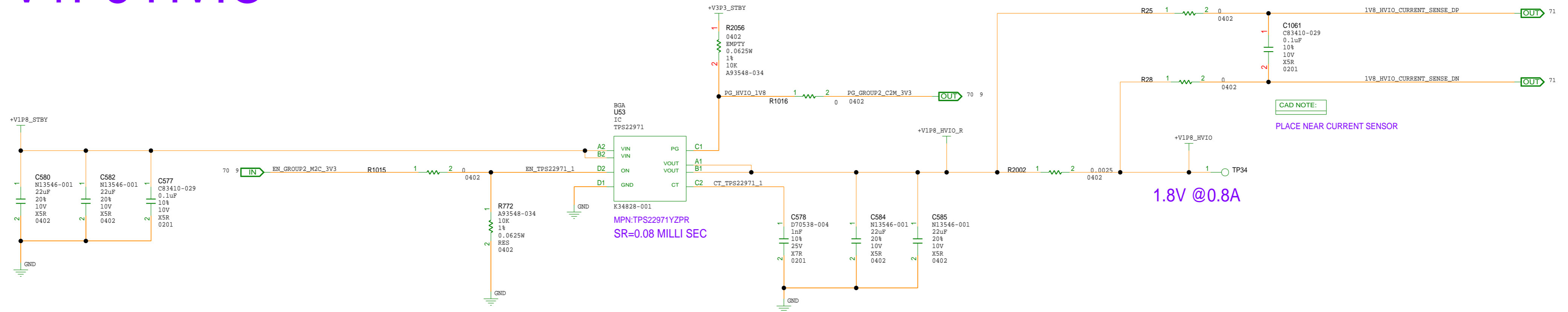
Figure 3: Recommended PCB Layout

VR - 3.8V, 1.8V FRAMOS

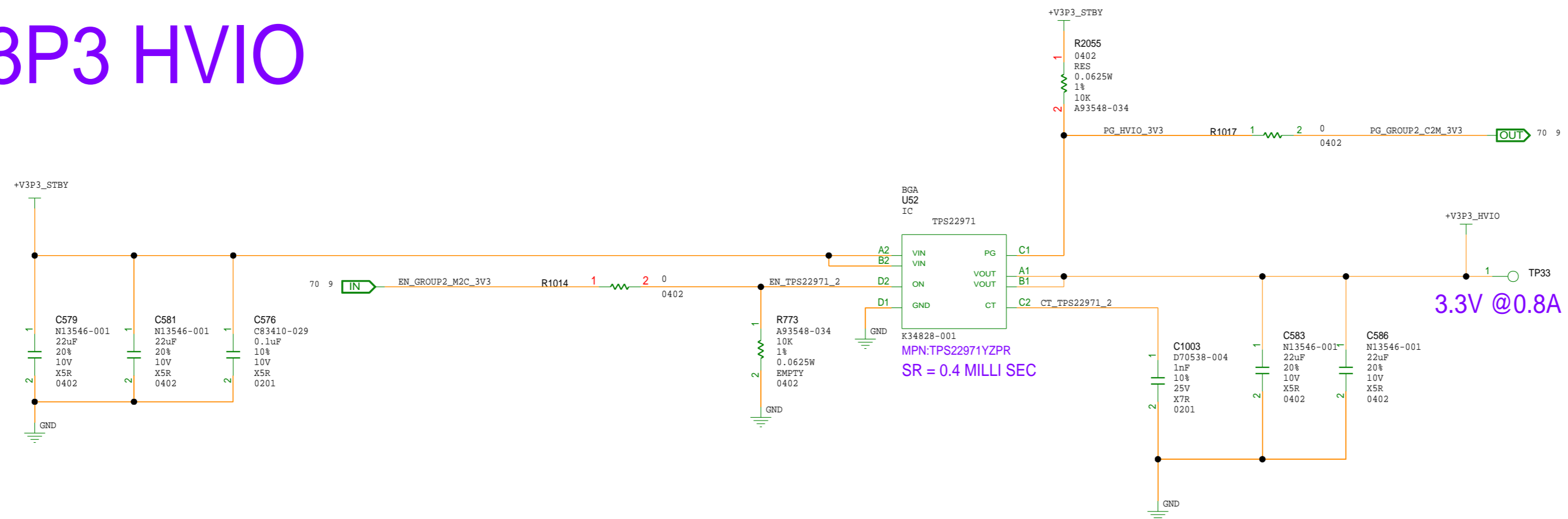
Tue Oct 1 13:22:42 2024

|            |   |      |       |                 |          |
|------------|---|------|-------|-----------------|----------|
| DEPARTMENT | <br>An Intel Company | SIZE | CODE  | DOCUMENT NUMBER | REV      |
|            |   | C+   | 34649 | 150-330724-B1   | 2.0      |
| SCALE:     | DO NOT SCALE DRAWING  |      |       | SHEET           | 70 OF 74 |

# +V1P8 HVIO




# +V3P3 HVIO

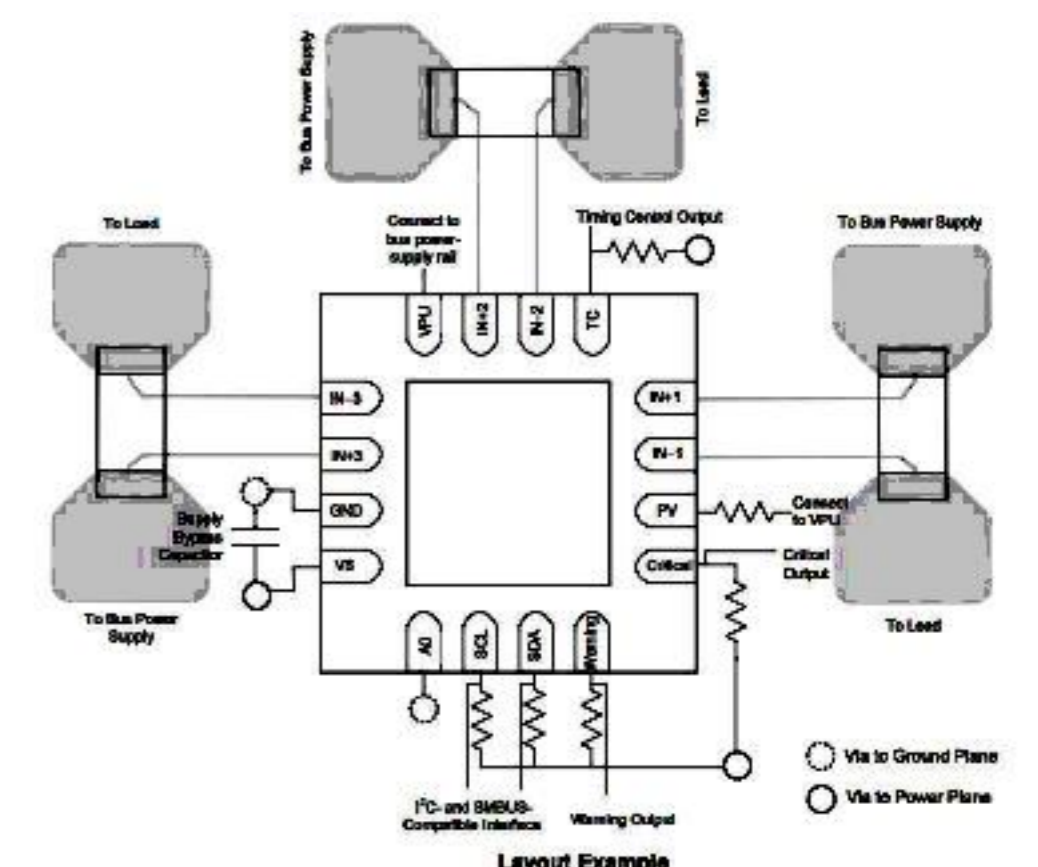
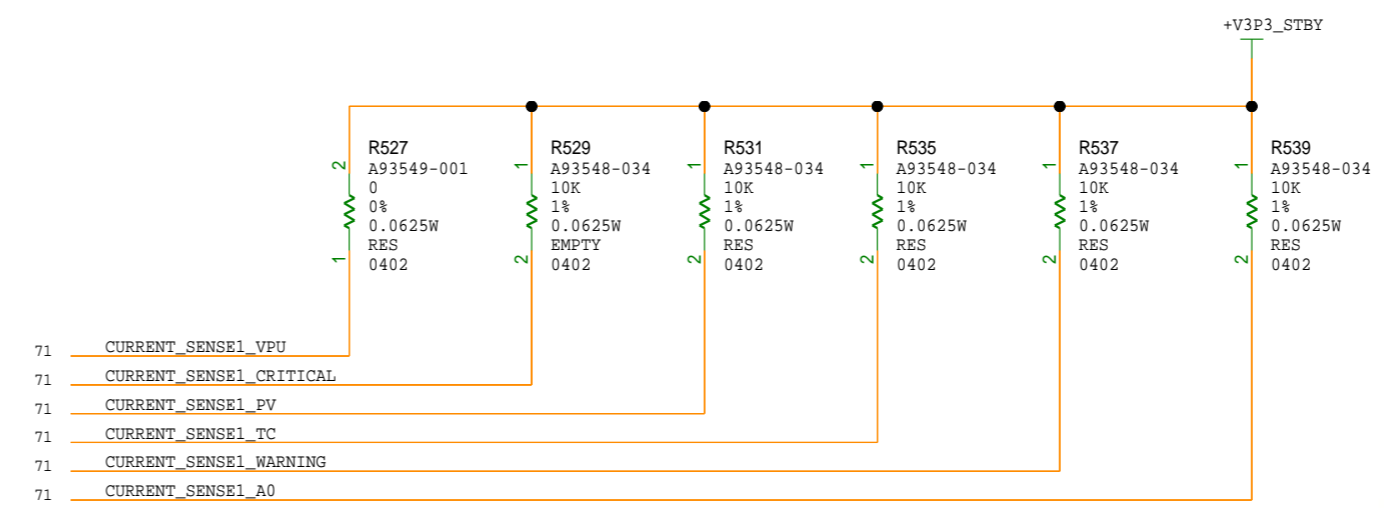
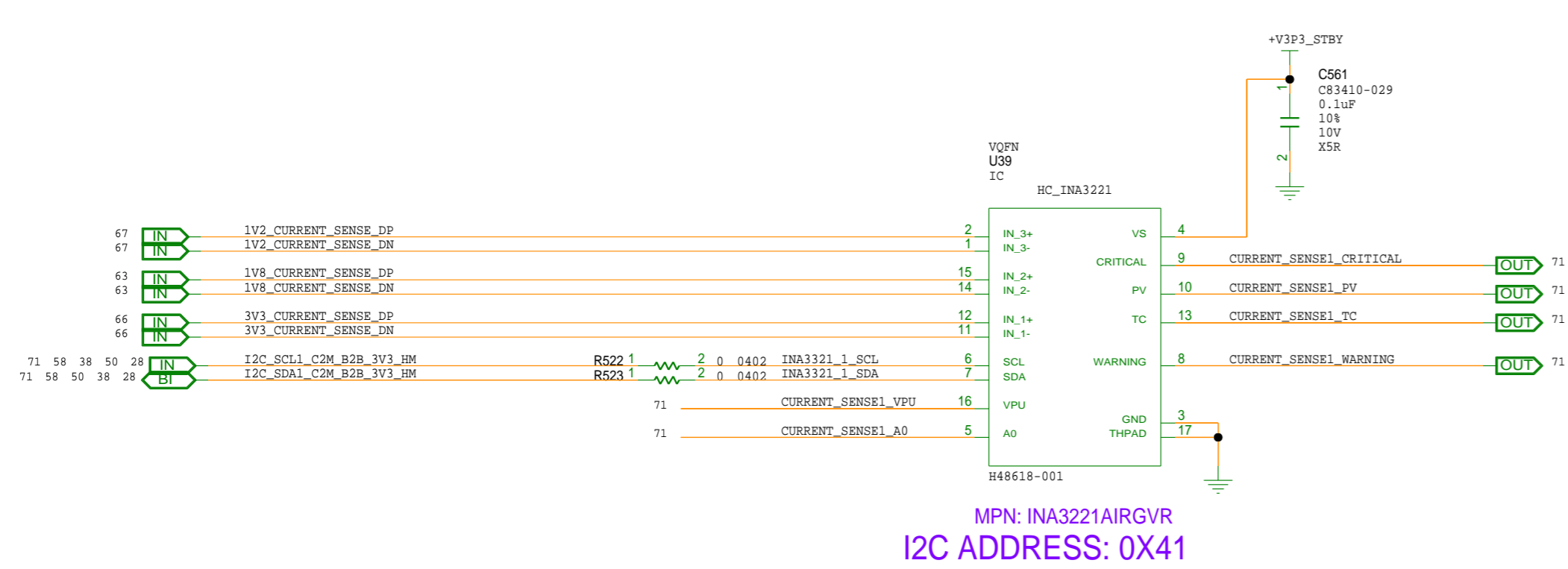


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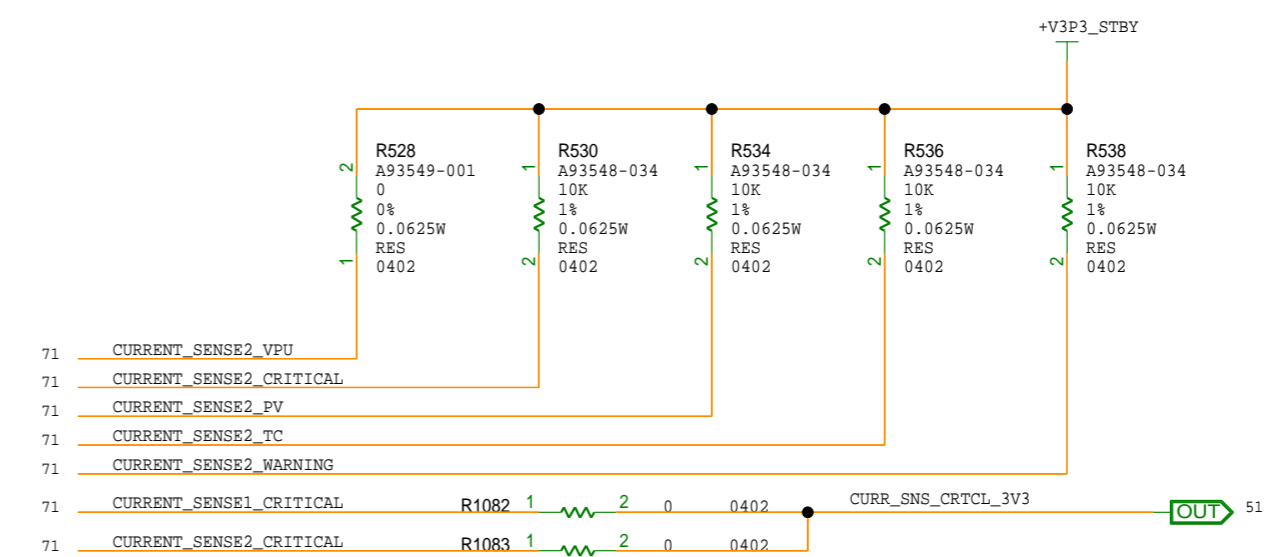
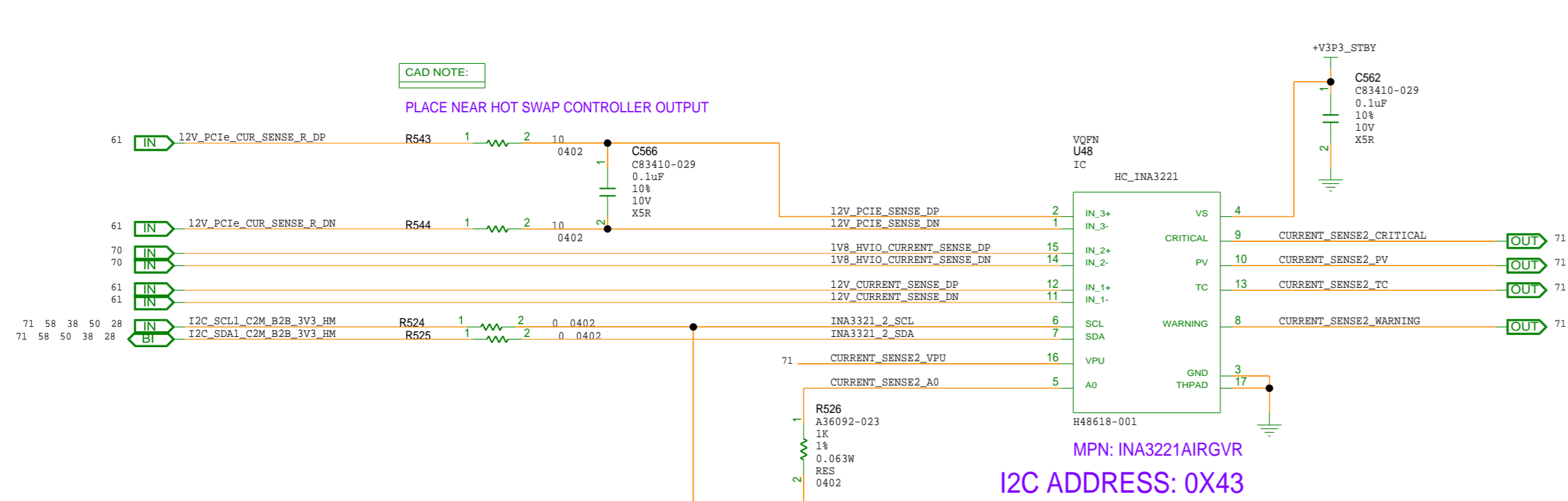
VR - +V1P8\_HVIO, +V3P3\_HVIO

|            |   |                      |       |                 |          |
|------------|---|----------------------|-------|-----------------|----------|
| DEPARTMENT | <br>An Intel Company | SIZE                 | CODE  | DOCUMENT NUMBER | REV      |
|            |   | C+                   | 34649 | 150-330724-B1   | 2.0      |
| SCALE:     |   | DO NOT SCALE DRAWING |       | SHEET           | 71 OF 74 |

# CURRENT SENSOR



# CURRENT SENSOR



# CURRENT SENSOR

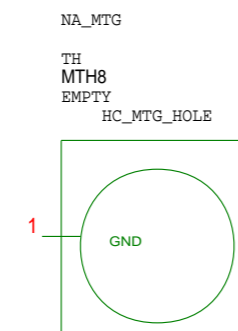
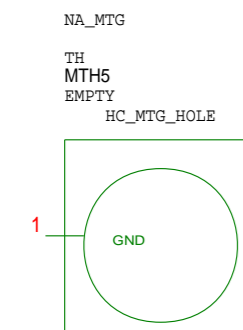
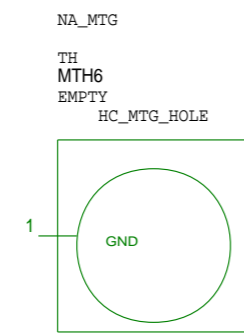
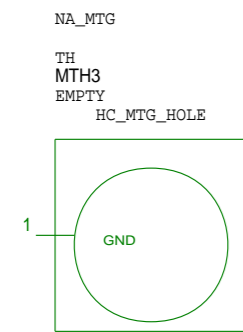
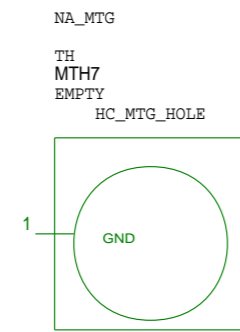
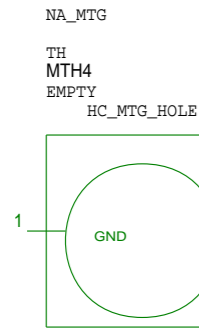
DEPARTMENT



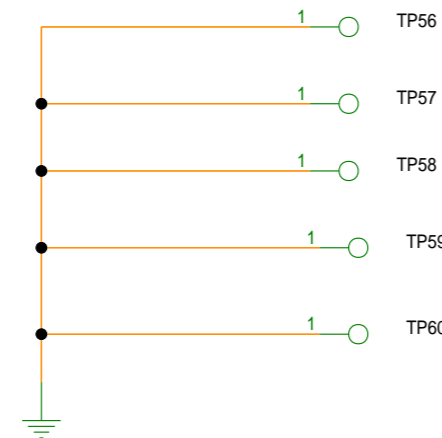
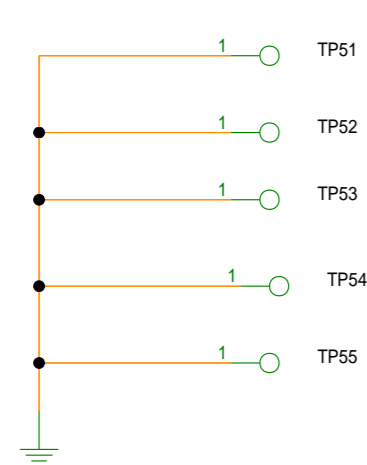
|        |                      |                 |                |
|--------|----------------------|-----------------|----------------|
| SIZE   | CODE                 | DOCUMENT NUMBER | REV            |
| C+     | 34649                | 150-330724-B1   | 2.0            |
| SCALE: | DO NOT SCALE DRAWING |                 | SHEET 72 OF 74 |

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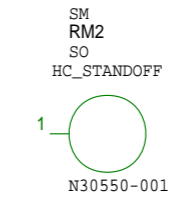
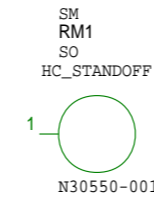
# CARRIER MOUNTING HOLES



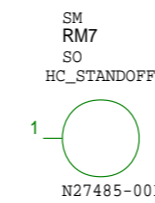
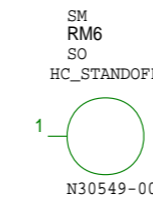
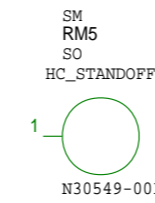
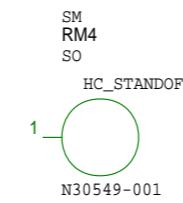
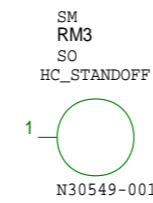
# GND TEST POINTS



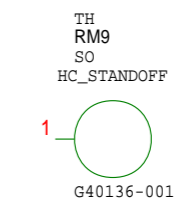
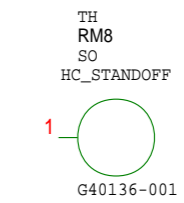
# ETHERNET PHY HEAT SINK MOUNTING HOLES



# SOM MOUNTING HOLES




# FRAMOS MOUNTING HOLES



# MOUNTING HOLES

Tue Oct 1 13:22:42 2024

|            |   |            |                      |                                  |                |
|------------|---|------------|----------------------|----------------------------------|----------------|
| DEPARTMENT | <br>An Intel Company | SIZE<br>C+ | CODE<br>34649        | DOCUMENT NUMBER<br>150-330724-B1 | REV<br>2.0     |
|            |   | SCALE:     | DO NOT SCALE DRAWING |                                  | SHEET 73 OF 74 |




# REVISION HISTORY

| S.NO | REV | DATE     | DESCRIPTION           |
|------|-----|----------|-----------------------|
| 1    | 1P0 | AUG-2023 | INITIAL RELEASE FAB-A |
| 2    | 2P0 | MAR-2024 | FAB-B RELEASE         |

# REVISION HISTORY

Tue Oct 1 11:18:02 2024

|            |   |                      |               |                                  |            |
|------------|---|----------------------|---------------|----------------------------------|------------|
| DEPARTMENT | <br>An Intel Company | SIZE<br>C+           | CODE<br>34649 | DOCUMENT NUMBER<br>150-330724-B1 | REV<br>2.0 |
| SCALE:     |   | DO NOT SCALE DRAWING |               | SHEET                            | 74 OF 74   |