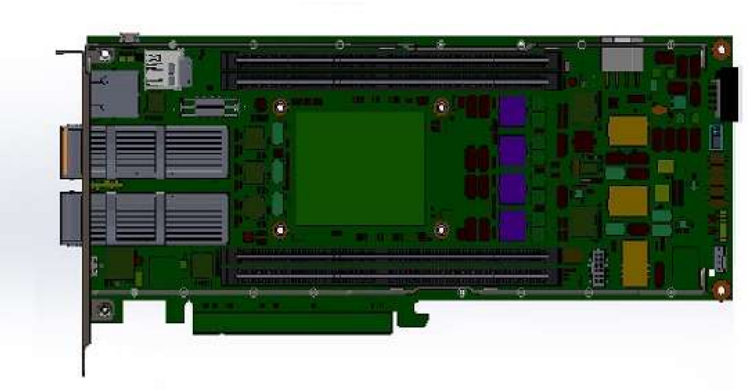
REV	DATE	PAGES	DESCRIPTION
A1	05/25/2022	All	Changed Enpirion power modules with ADI parts
B1	05/25/2022	All	IC LTM4668IY#PBF U66, U70 PGood 2,3,4 pins are made it NC & J22 modified as 2*2 connector
	12/04/2024	All	Altera branding related changes implemented

Board BOM : M75579-100
PCB P/N :100-0330692-B1



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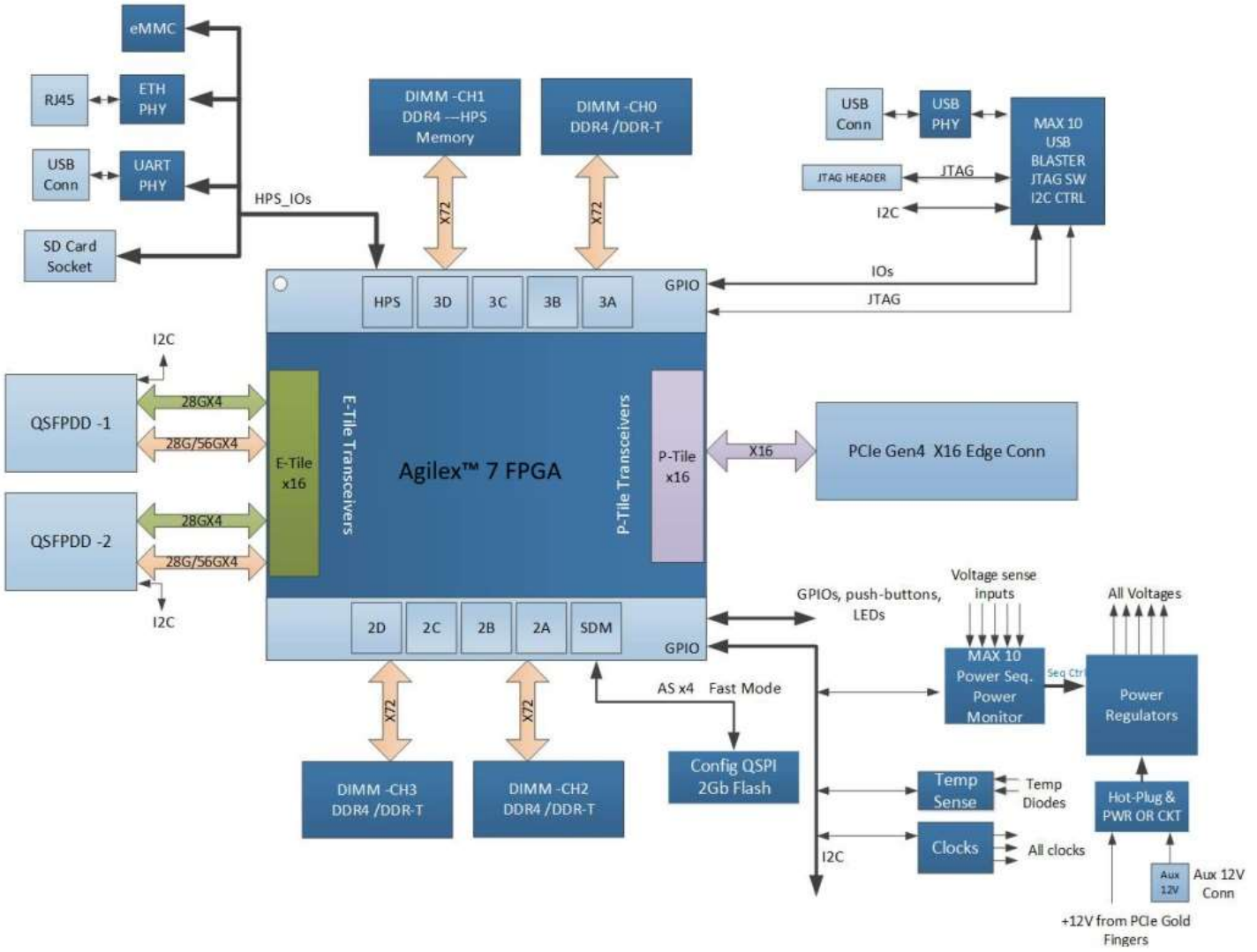
Title **Agilex™ 7 FPGA F-Series Development Kit (P-Tile and E-Tile)**

Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 1 of 67

System Block Diagram



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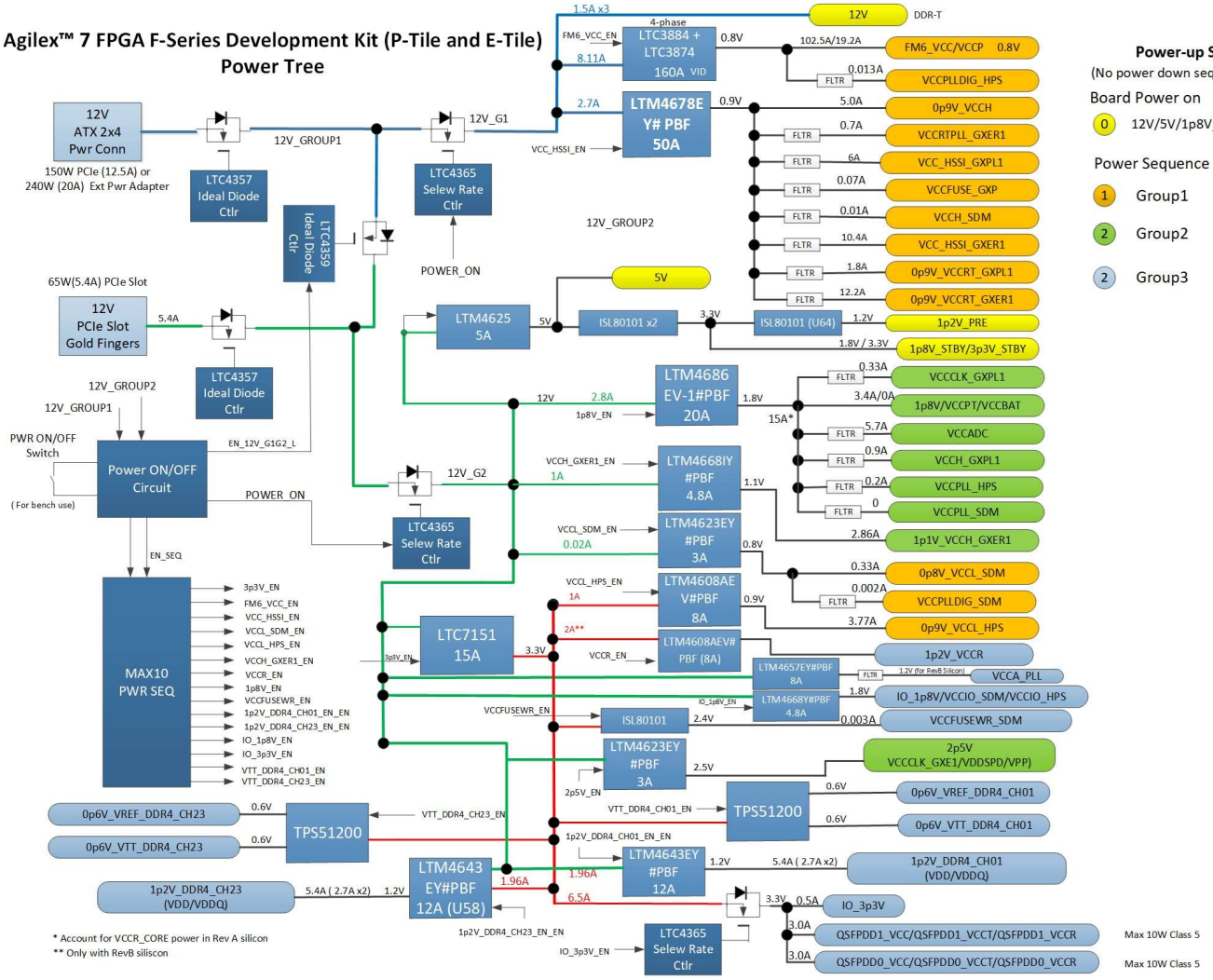
Size: B	Document Number: M75579-100(100-0330692-B1) Rev: C1
Date: Wednesday, December 04, 2024	Sheet 2 of 67

Agilex™ 7 FPGA F-Series Development Kit (P-Tile and E-Tile) Power Tree



* Account for VCCR_CORE power in Rev A silicon
** Only with RevB siliscon

Power-up Sequence:
(No power down sequence requirment)

Board Power on

0 12V/5V/1p8V_STBY/3p3V_STBY/1p2V_PRE

Power Sequence Start

1 Group1

2 Group2

2 Group3

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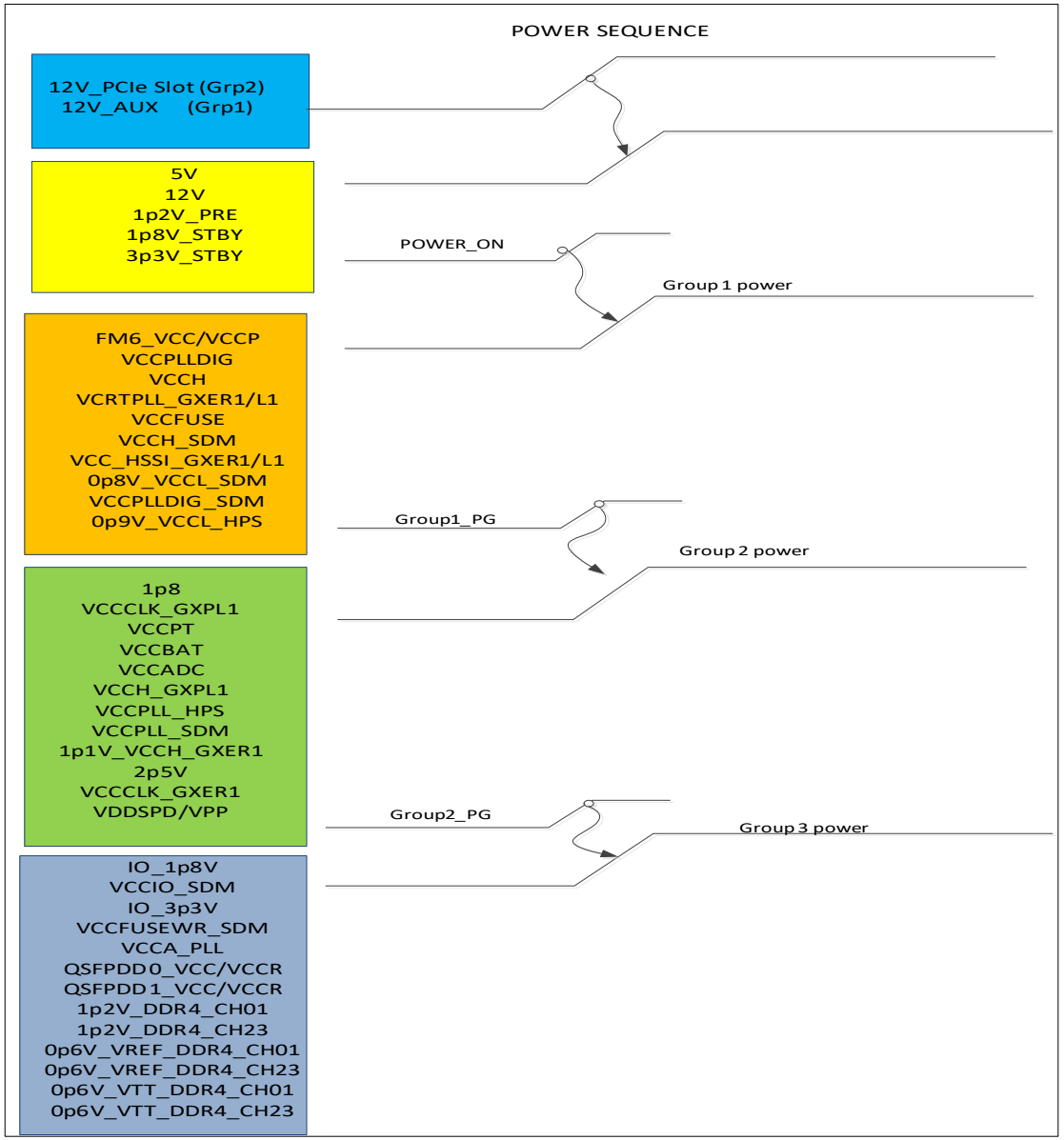
Size: D	Document Number: M75579-100(100-0330692-B1)	Rev: C1
Date: Wednesday, December 04, 2024	Sheet 3 of 67	

Power Sequence Timing



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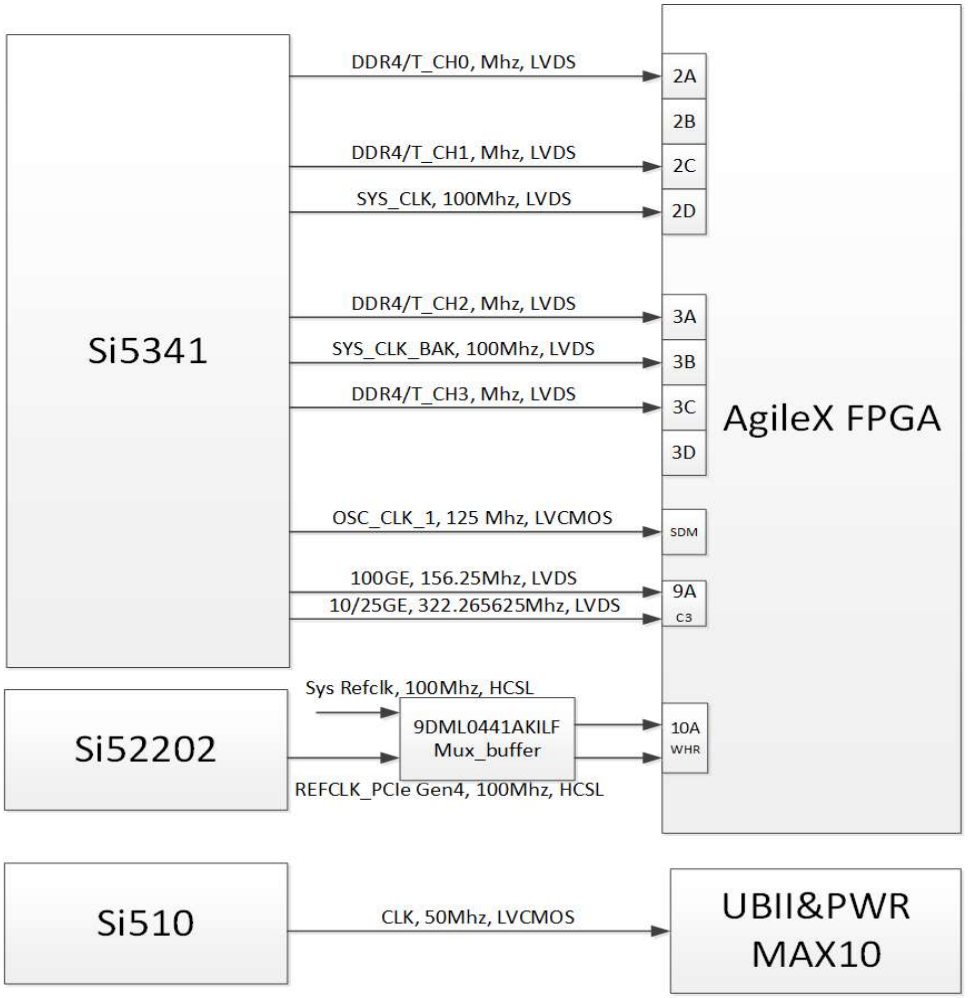
Size B	Document Number M75579-100(100-0330692-B1)	Rev C1
Date: Wednesday, December 04, 2024	Sheet 4 of 67	

Clock Tree



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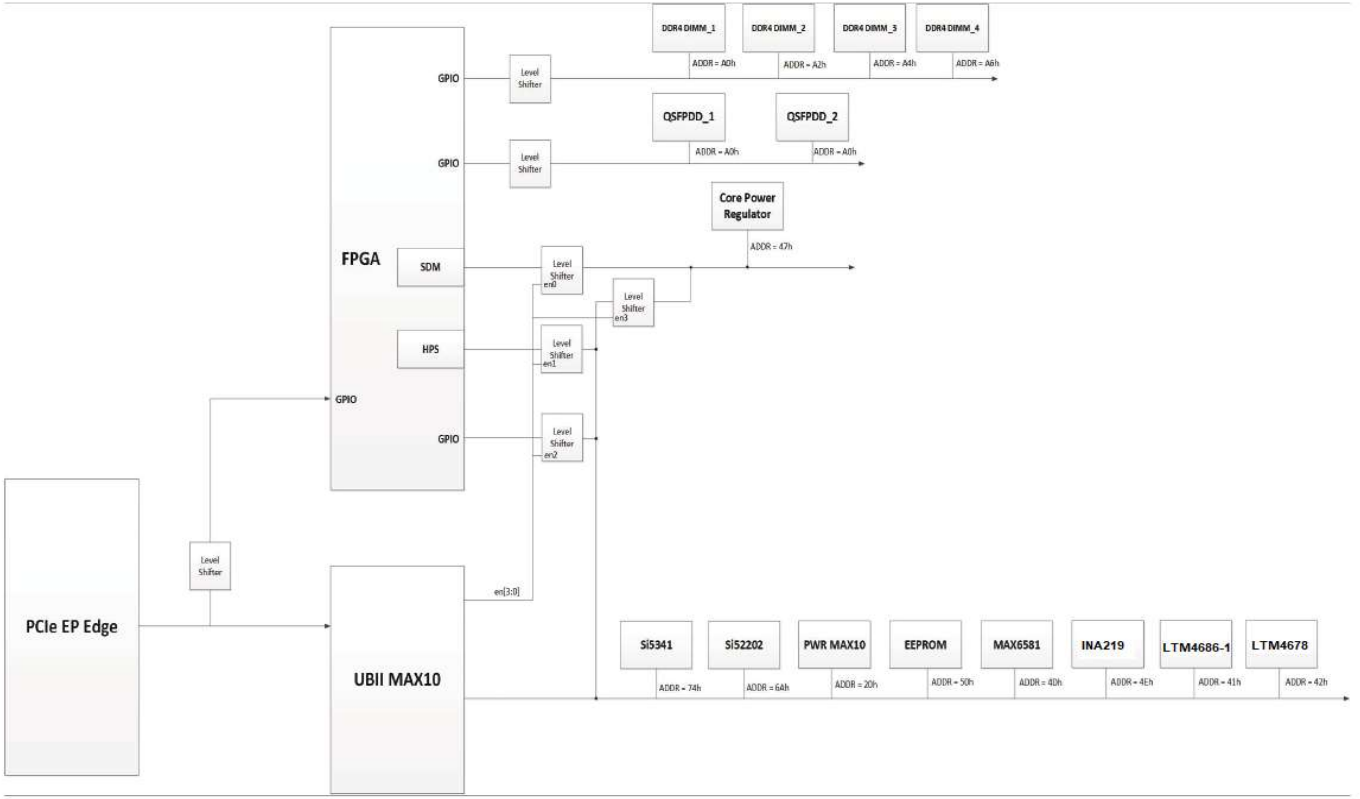
Size: B	Document Number: M75579-100(100-0330692-B1)	Rev: C1
Date: Wednesday, December 04, 2024	Sheet 5 of 67	

I2C Diagram



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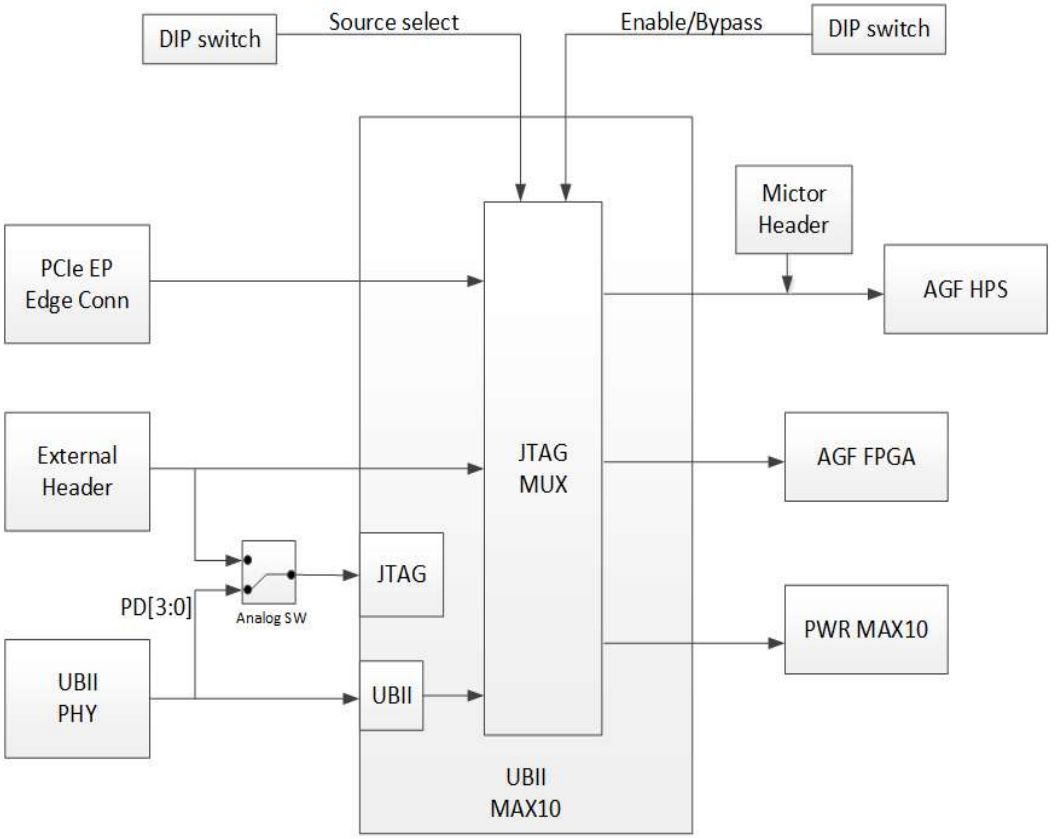
Size B	Document Number M75579-100(100-0330692-B1)		Rev C1
Date: Wednesday, December 04, 2024	Sheet 6 of 67		

JTAG Block Diagrram



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Date: Wednesday, December 04, 2024	Sheet 7 of 67	

DDR4/DDR-T DIMM Pin Map

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	12V	145	12V	38	DQ24	182	VSS	75	CLK0#	219	CLK1#	108	DQ40	252	VSS
2	VSS	146	VREFCA	39	VSS	183	DQ25	76	VDD	220	VDD	109	VSS	253	DQ41
3	DQ4	147	VSS	40	DQS12	184	VSS	77	VTT	221	VTT	110	DQS14	254	VSS
4	VSS	148	DQ5	41	DQS12#	185	DQS3#					111	DQS14#	255	DQS5#
5	DQ0	149	VSS	42	VSS	186	DQS3		KEY			112	VSS	256	DQS5
6	VSS	150	DQ1	43	DQ30	187	VSS					113	DQ46	257	VSS
7	DQS0	151	VSS	44	VSS	188	DQ31					114	VSS	258	DQ47
8	DQS0#	152	DQS0#	45	DQ26	189	VSS	78	EVENT	222	PARITY	115	DQ42	259	VSS
9	VSS	153	DQS0	46	VSS	190	DQ27	79	A0	223	VDD	116	VSS	260	DQ43
10	DQ6	154	VSS	47	CB4	191	VSS	80	VDD	224	BA1	117	DQ52	261	VSS
11	VSS	155	DQ7	48	VSS	192	CB5	81	BA0	225	A10	118	VSS	262	DQ53
12	DQ2	156	VSS	49	CB0	193	VSS	82	RAS#/A16	226	VDD	119	DQ48	263	VSS
13	VSS	157	DQ3	50	VSS	194	CB1	83	VDD	227	RFU	120	VSS	264	DQ49
14	DQ12	158	VSS	51	DQS17	195	VSS	84	CS0#	228	WE#/A14	121	DQS15	265	VSS
15	VSS	159	DQ13	52	DQS17#	196	DQS8#	85	VDD	229	VDD	122	DQS15#	266	DQS6#
16	DQ8	160	VSS	53	VSS	197	DQS8	86	CAS#/A15	230	SAVE#	123	VSS	267	DQS6
17	VSS	161	DQ9	54	CB6	198	VSS	87	ODT0	231	VDD	124	DQ54	268	VSS
18	DQS10	162	VSS	55	VSS	199	CB7	88	VDD	232	A13	125	VSS	269	DQ55
19	DQS10#	163	DQS1#	56	CB2	200	VSS	89	CS1#	233	VDD	126	DQ50	270	VSS
20	VSS	164	DQS1	57	VSS	201	CB3	90	VDD	234	A17	127	VSS	271	DQ51
21	DQ14	165	VSS	58	RESET#	202	VSS	91	ODT1	235	C2	128	DQ60	272	VSS
22	VSS	166	DQ15	59	VDD	203	CKE1	92	VDD	236	VDD	129	VSS	273	DQ61
23	DQ10	167	VSS	60	CKE0	204	VDD	93	C0	237	C1	130	DQ56	274	VSS
24	VSS	168	DQ11	61	VDD	205	RFU	94	VSS	238	SA2	131	VSS	275	DQ57
25	DQ20	169	VSS	62	ACT#	206	VDD	95	DQ36	239	VSS	132	DQS16	276	VSS
26	VSS	170	DQ21	63	BG0	207	BG1	96	VSS	240	DQ37	133	DQS16#	277	DQS7#
27	DQ16	171	VSS	64	VDD	208	ALERT#	97	DQ32	241	VSS	134	VSS	278	DQS7
28	VSS	172	DQ17	65	A12	209	VDD	98	VSS	242	DQ33	135	DQ62	279	VSS
29	DQS11	173	VSS	66	A9	210	A11	99	DQS13	243	VSS	136	VSS	280	DQ63
30	DQS11#	174	DQS2#	67	VDD	211	A7	100	DQS13#	244	DQS4#	137	DQ58	281	VSS
31	VSS	175	DQS2	68	A8	212	VDD	101	VSS	245	DQS4	138	VSS	282	DQ59
32	DQ22	176	VSS	69	A6	213	A5	102	DQ38	246	VSS	139	SA0	283	VSS
33	VSS	177	DQ23	70	VDD	214	A4	103	VSS	247	DQ39	140	SA1	284	VDDSPD
34	DQ18	178	VSS	71	A3	215	VDD	104	DQ34	248	VSS	141	SCL	285	SDA
35	VSS	179	DQ19	72	A1	216	A2	105	VSS	249	DQ35	142	VPP	286	VPP
36	DQ28	180	VSS	73	VDD	217	VDD	106	DQ44	250	VSS	143	VPP	287	VPP
37	VSS	181	DQ29	74	CLK0	218	CLK1	107	VSS	251	DQ45	144	RFU	288	VPP

DDR-T DIMM Pin Map is Identical to standard DDR4 DIMM Pin Map except the DDR-T protocol repurposes five of these pins:

CS1# (pin 89) : Grant, GNT# <0> Input

CKE1 (pin 203) : Request, REQ# <0> Output

ODT1 (pin 91) : Error, ERR# Output

CLK1 (pin 218):Early Read ID, ERID<0> Output

CLK1# (pin 219):Early Read ID, ERID<1> Output

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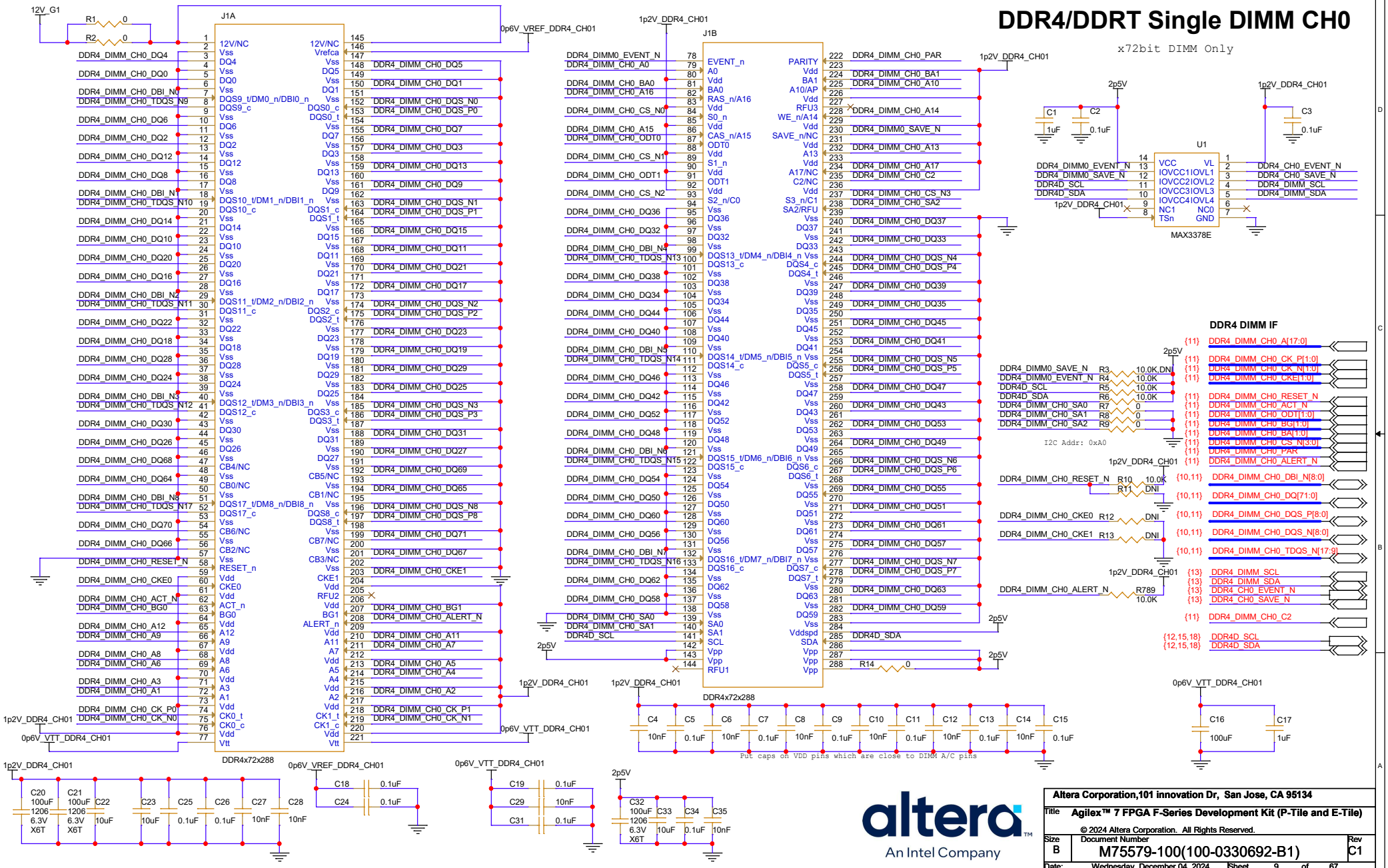
Size: B | Document Number: M75579-100(100-0330692-B1) | Rev: C1

Date: Wednesday, December 04, 2024 | Sheet 8 of 67

DDR4/DDRT Single DIMM CH0

x72bit DIMM Only



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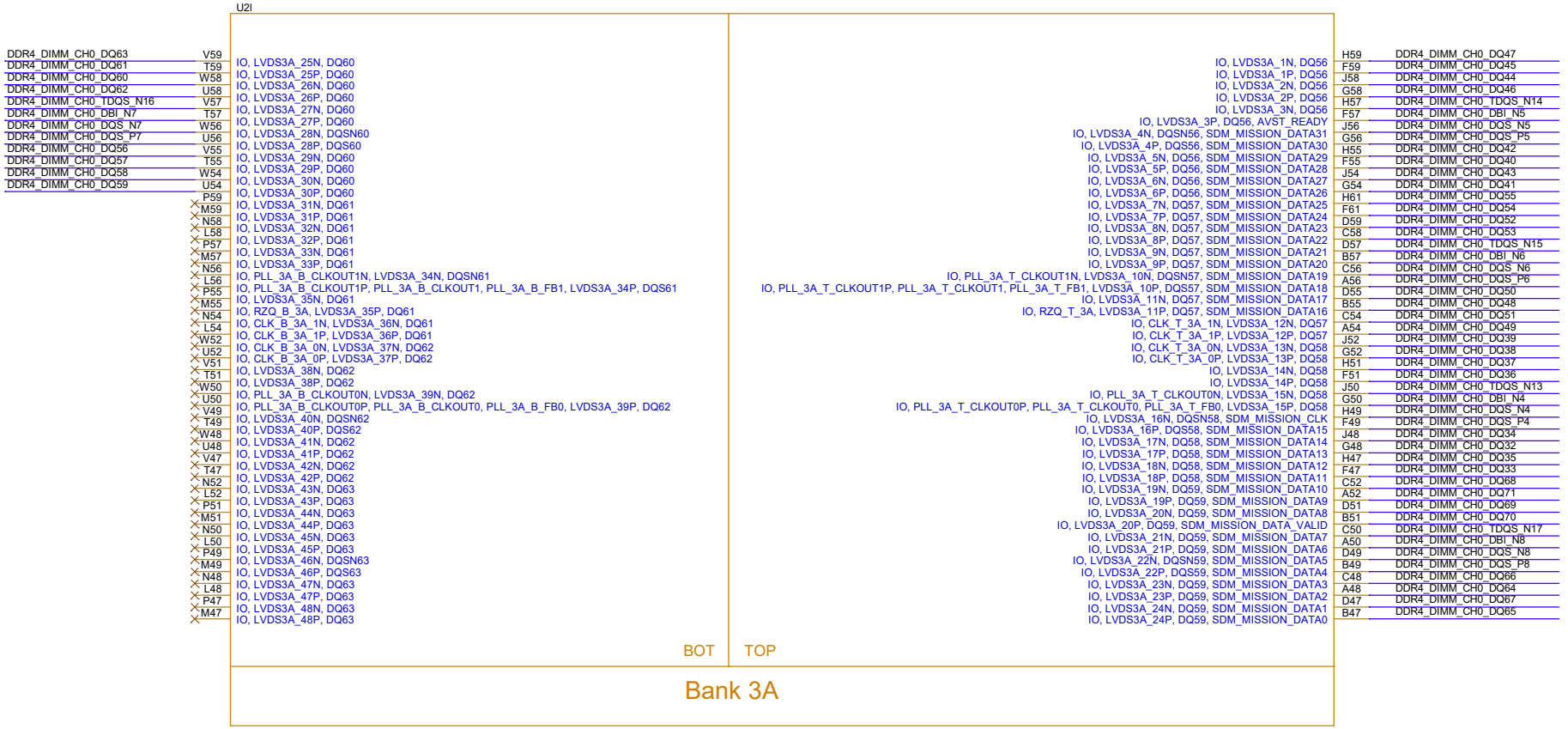
Date: Wednesday, December 04, 2024 Sheet 9 of 67

DDR4/T CH0 INTERFACE -- FPGA SIDE 3A



{9,11} DDR4_DIMM_CH0_DBI_N[8:0]
{9,11} DDR4_DIMM_CH0_DQ[71:0]
{9,11} DDR4_DIMM_CH0_DQS_P[8:0]
{9,11} DDR4_DIMM_CH0_DQS_N[8:0]
{9,11} DDR4_DIMM_CH0_TDQS_N[17:9]

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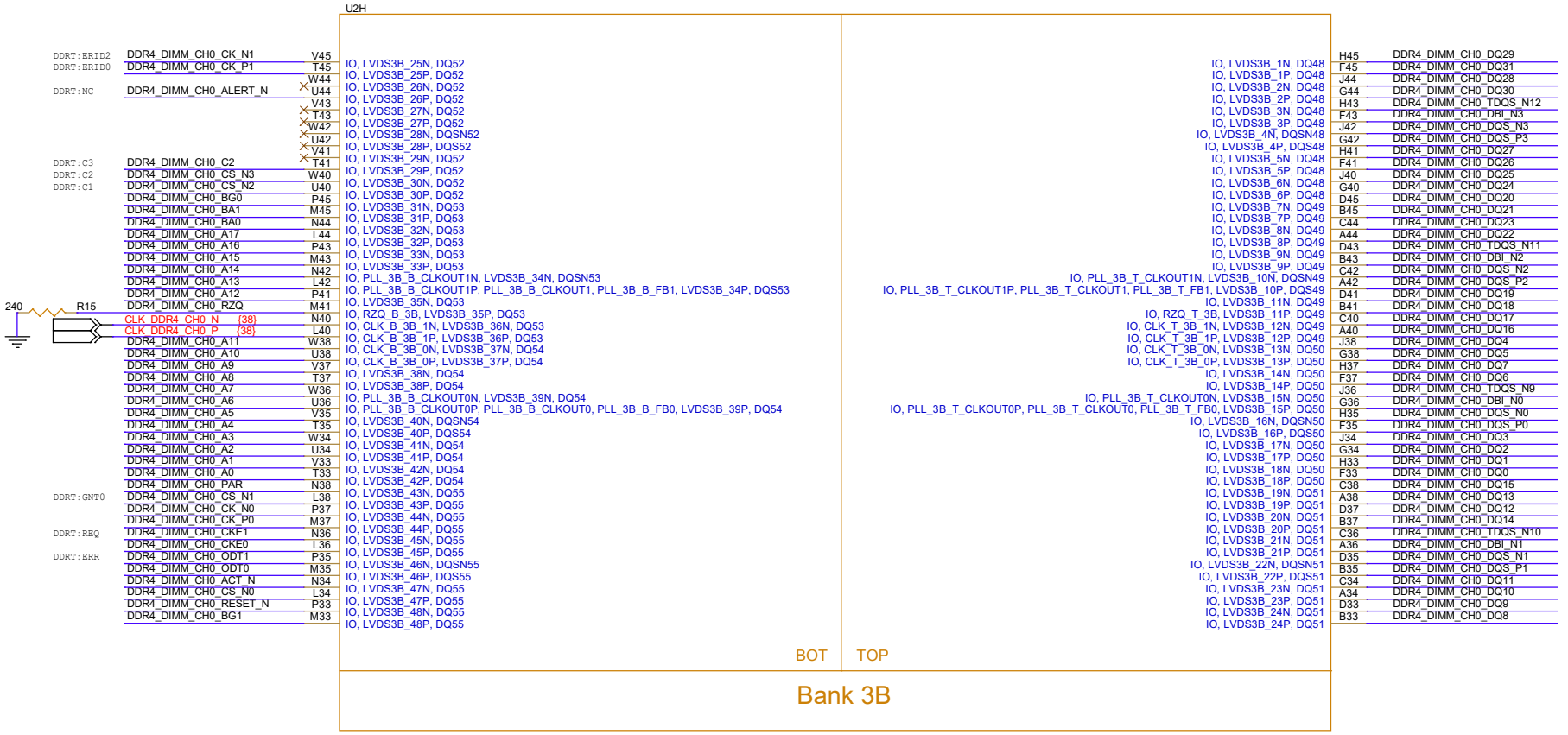
Date: Wednesday, December 04, 2024 Sheet 10 of 67

DDR4/T CH1 INTERFACE -- FPGA SIDE 3B



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Size	Document Number	Rev
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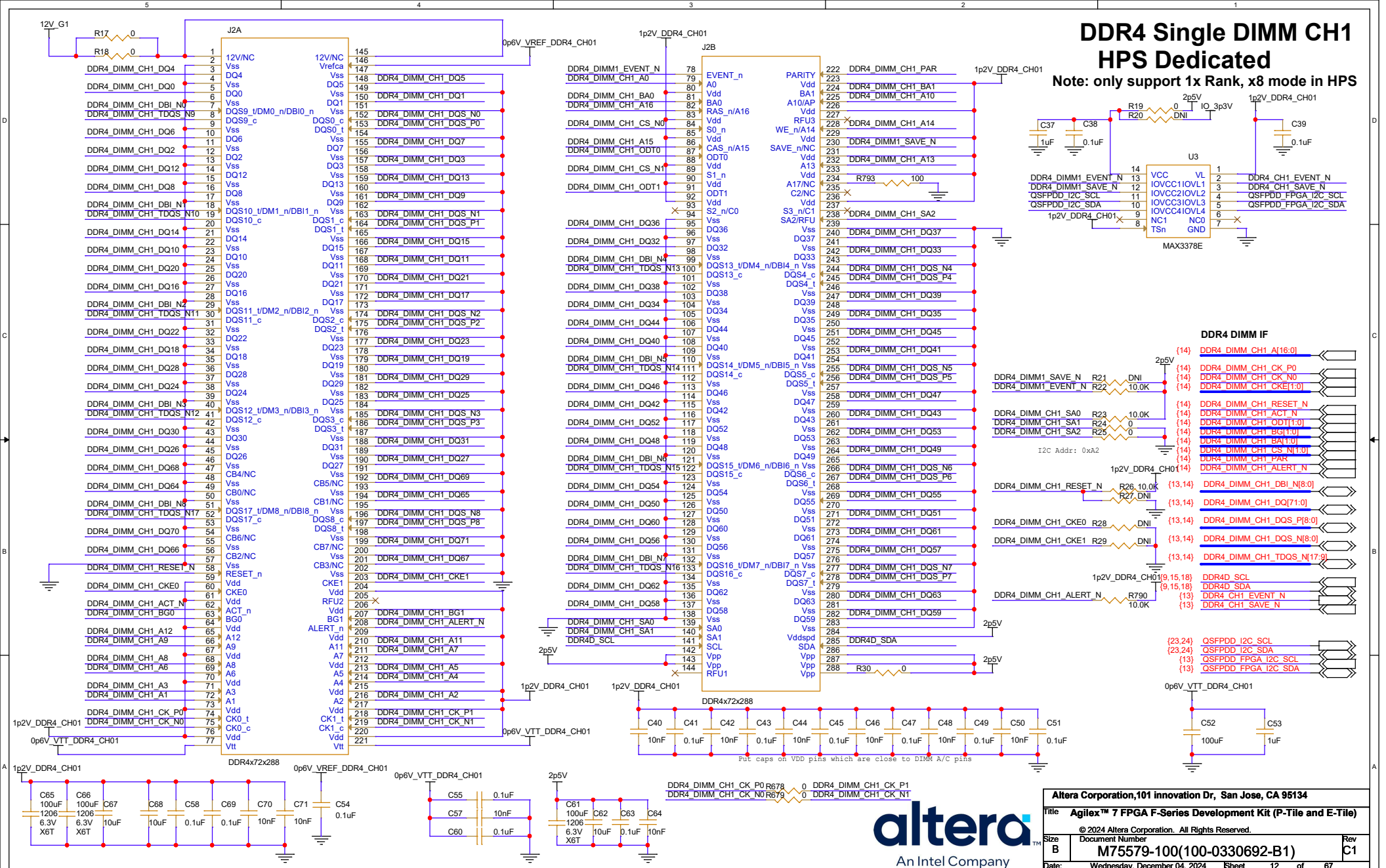
Date: Wednesday, December 04, 2024 Sheet 11 of 67

DDR4 Single DIMM CH1 HPS Dedicated

Note: only support 1x Rank, x8 mode in HPS



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Document Number	M75579-100(100-0330692-B1)
Rev	C1
Date:	Wednesday, December 04, 2024
Sheet	12 of 67

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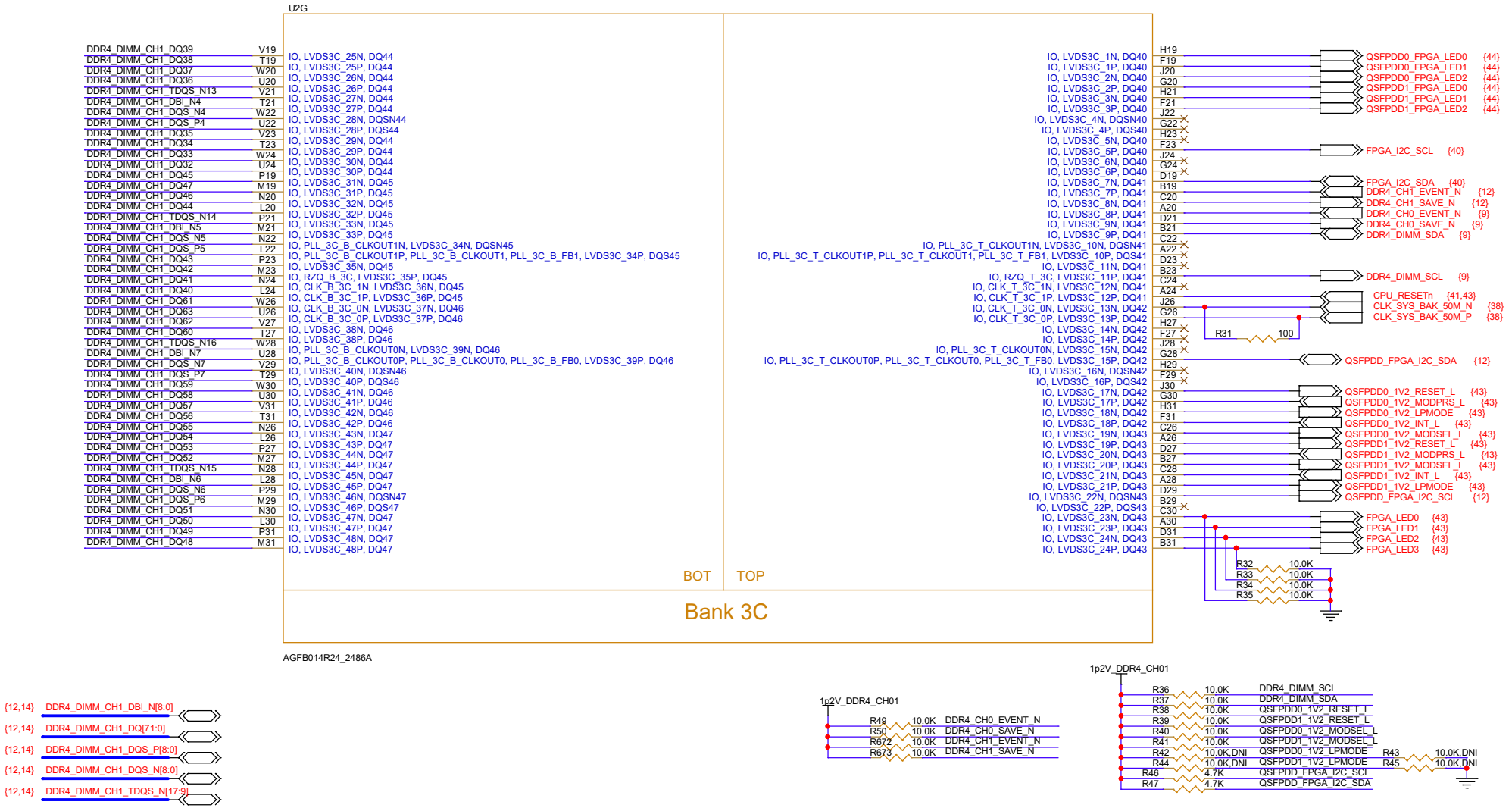
DDR4 DIMM CH1 Interface - FPGA Side 3C



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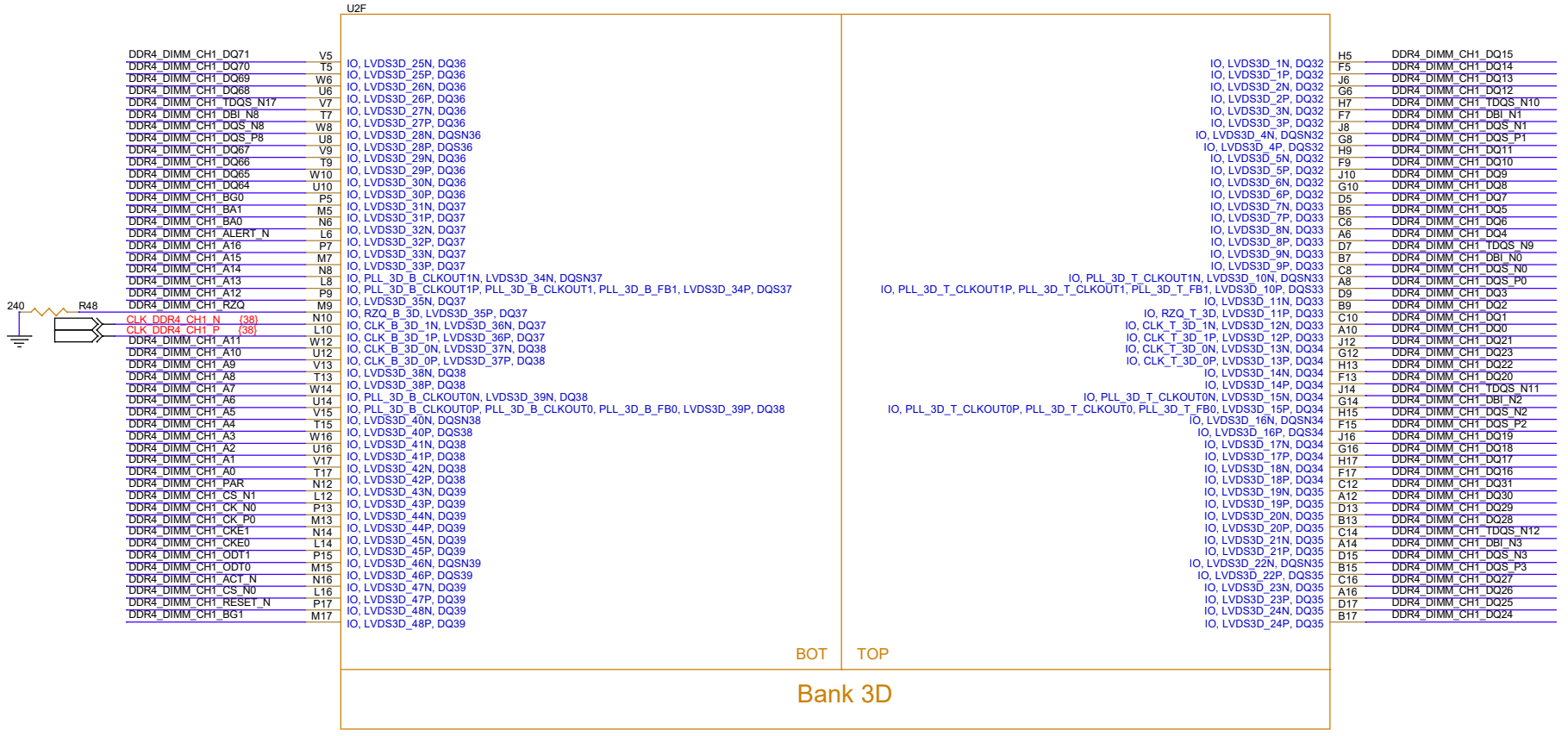
Date: Wednesday, December 04, 2024 Sheet 13 of 67

DDR4 CH1 Interface - FPGA Side 3D



{12} DDR4_DIMM_CH1_CK_P0
{12} DDR4_DIMM_CH1_CK_N0
{12} DDR4_DIMM_CH1_CKE[1:0]
{12} DDR4_DIMM_CH1_A[16:0]
{12} DDR4_DIMM_CH1_ODT[1:0]
{12} DDR4_DIMM_CH1_BG[1:0]
{12} DDR4_DIMM_CH1_BA[1:0]
{12} DDR4_DIMM_CH1_CS_N[1:0]
{12} DDR4_DIMM_CH1_RESET_N
{12} DDR4_DIMM_CH1_ACT_N
{12} DDR4_DIMM_CH1_PAR
{12} DDR4_DIMM_CH1_ALERT_N

{12,13} DDR4_DIMM_CH1_DBI_N[8:0]
{12,13} DDR4_DIMM_CH1_DQ[71:0]
{12,13} DDR4_DIMM_CH1_DQS_P[8:0]
{12,13} DDR4_DIMM_CH1_DQS_N[8:0]
{12,13} DDR4_DIMM_CH1_TDQS_N[17:9]

CLK_DDR4_CH1_P R53 DNI CLK_DDR4_CH1_N

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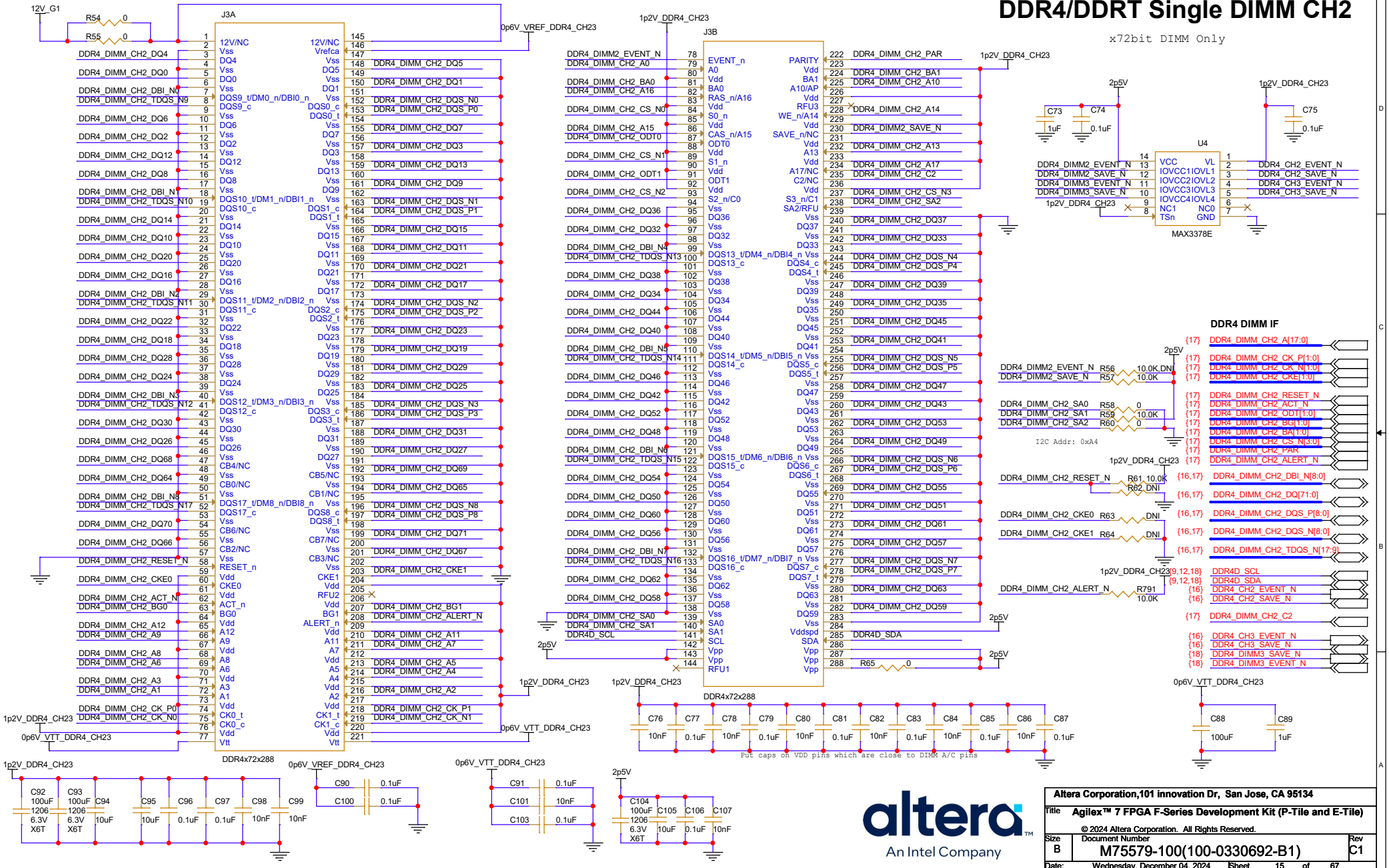
Document Number: M75579-100(100-0330692-B1)
Rev: C1
Date: Wednesday, December 04, 2024
Sheet 14 of 67

DDR4/DDRT Single DIMM CH2

x72bit DIMM Only



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Size: B | Document Number: M75579-100(100-0330692-B1) | Rev: C1

Date: Wednesday, December 04, 2024 | Sheet 15 of 67

DDR4/T CH2 INTERFACE -- FPGA SIDE 2A

{15,17} DDR4_DIMM_CH2_DBI_N[8:0]
{15,17} DDR4_DIMM_CH2_DQ[71:0]
{15,17} DDR4_DIMM_CH2_DQS_P[8:0]
{15,17} DDR4_DIMM_CH2_DQS_N[8:0]
{15,17} DDR4_DIMM_CH2_TDQS_N[17:9]

1p2V_DDR4_CH23

R674 10.0K DDR4_CH2_EVENT_N
R675 10.0K DDR4_CH2_SAVE_N
R676 10.0K DDR4_CH3_EVENT_N
R677 10.0K DDR4_CH3_SAVE_N

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Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 16 of 67

DDR4/T CH2 INTERFACE -- FPGA SIDE 2B

U2D

DDRT:ERID2	DDR4_DIMM_CH2_CK_N1	CF43	IO, LVDS2B_25N, DQ20	IO, LVDS2B_1N, DQ16	CT43	DDR4_DIMM_CH2_DQ39
DDRT:ERID0	DDR4_DIMM_CH2_CK_P1	CH43	IO, LVDS2B_25P, DQ20	IO, LVDS2B_1P, DQ16	CV43	DDR4_DIMM_CH2_DQ37
		CE42	IO, LVDS2B_26N, DQ20	IO, LVDS2B_2N, DQ16	CR42	DDR4_DIMM_CH2_DQ38
DDRT:NC	DDR4_DIMM_CH2_ALERT_N	CG42	IO, LVDS2B_26P, DQ20	IO, LVDS2B_2P, DQ16	CU42	DDR4_DIMM_CH2_DQ36
		CF41	IO, LVDS2B_27N, DQ20	IO, LVDS2B_3N, DQ16	CT41	DDR4_DIMM_CH2_TDQS_N13
		CH41	IO, LVDS2B_27P, DQ20	IO, LVDS2B_3P, DQ16	CV41	DDR4_DIMM_CH2_DBI_N4
		CE40	IO, LVDS2B_28N, DQSN20	IO, LVDS2B_4N, DQSN16	CR40	DDR4_DIMM_CH2_DQS_N4
		CG40	IO, LVDS2B_28P, DQS20	IO, LVDS2B_4P, DQS16	CU40	DDR4_DIMM_CH2_DQS_P4
		CF39	IO, LVDS2B_29N, DQ20	IO, LVDS2B_5N, DQ16	CT39	DDR4_DIMM_CH2_DQ32
DDRT:C3	DDR4_DIMM_CH2_C2	CH39	IO, LVDS2B_29P, DQ20	IO, LVDS2B_5P, DQ16	CV39	DDR4_DIMM_CH2_DQ33
DDRT:C2	DDR4_DIMM_CH2_CS_N3	CE38	IO, LVDS2B_30N, DQ20	IO, LVDS2B_6N, DQ16	CR38	DDR4_DIMM_CH2_DQ35
DDRT:C1	DDR4_DIMM_CH2_CS_N2	CG38	IO, LVDS2B_30P, DQ20	IO, LVDS2B_6P, DQ16	CU38	DDR4_DIMM_CH2_DQ34
	DDR4_DIMM_CH2_BG0	CK43	IO, LVDS2B_31N, DQ21	IO, LVDS2B_7N, DQ17	CY43	DDR4_DIMM_CH2_DQ47
	DDR4_DIMM_CH2_BA1	CM43	IO, LVDS2B_31P, DQ21	IO, LVDS2B_7P, DQ17	DB43	DDR4_DIMM_CH2_DQ45
	DDR4_DIMM_CH2_BA0	CL42	IO, LVDS2B_32N, DQ21	IO, LVDS2B_8N, DQ17	DA42	DDR4_DIMM_CH2_DQ46
	DDR4_DIMM_CH2_A17	CN42	IO, LVDS2B_32P, DQ21	IO, LVDS2B_8P, DQ17	DC42	DDR4_DIMM_CH2_DQ44
	DDR4_DIMM_CH2_A16	CK41	IO, LVDS2B_33N, DQ21	IO, LVDS2B_9N, DQ17	CY41	DDR4_DIMM_CH2_TDQS_N14
	DDR4_DIMM_CH2_A15	CM41	IO, LVDS2B_33P, DQ21	IO, LVDS2B_9P, DQ17	DB41	DDR4_DIMM_CH2_DBI_N5
	DDR4_DIMM_CH2_A14	CL40	IO, PLL_2B_B_CLKOUT1N, LVDS2B_34N, DQSN21	IO, PLL_2B_T_CLKOUT1N, LVDS2B_10N, DQSN17	DA40	DDR4_DIMM_CH2_DQS_N5
	DDR4_DIMM_CH2_A13	CN40	IO, PLL_2B_B_CLKOUT1P, PLL_2B_B_CLKOUT1, PLL_2B_B_FB1, LVDS2B_34P, DQS21	IO, PLL_2B_T_CLKOUT1P, PLL_2B_T_CLKOUT1, PLL_2B_T_FB1, LVDS2B_10P, DQS17	DC40	DDR4_DIMM_CH2_DQS_P5
	DDR4_DIMM_CH2_A12	CK39	IO, LVDS2B_35N, DQ21	IO, LVDS2B_11N, DQ17	CY39	DDR4_DIMM_CH2_DQ40
240 R66	DDR4_DIMM_CH2_RZQ	CM39	IO, RZQ_B_2B, LVDS2B_35P, DQ21	IO, RZQ_T_2B, LVDS2B_11P, DQ17	DB39	DDR4_DIMM_CH2_DQ41
	CLK_DDR4_CH2_N {38}	CL38	IO, CLK_B_2B_1N, LVDS2B_36N, DQ21	IO, CLK_T_2B_1N, LVDS2B_12N, DQ17	DA38	DDR4_DIMM_CH2_DQ43
	CLK_DDR4_CH2_P {38}	CN38	IO, CLK_B_2B_1P, LVDS2B_36P, DQ21	IO, CLK_T_2B_1P, LVDS2B_12P, DQ17	DC38	DDR4_DIMM_CH2_DQ42
	DDR4_DIMM_CH2_A11	CE36	IO, CLK_B_2B_0N, LVDS2B_37N, DQ22	IO, CLK_T_2B_0N, LVDS2B_13N, DQ18	CR36	DDR4_DIMM_CH2_DQ63
	DDR4_DIMM_CH2_A10	CG36	IO, CLK_B_2B_0P, LVDS2B_37P, DQ22	IO, CLK_T_2B_0P, LVDS2B_13P, DQ18	CU36	DDR4_DIMM_CH2_DQ61
	DDR4_DIMM_CH2_A9	CF35	IO, LVDS2B_38N, DQ22	IO, LVDS2B_14N, DQ18	CT35	DDR4_DIMM_CH2_DQ62
	DDR4_DIMM_CH2_A8	CH35	IO, LVDS2B_38P, DQ22	IO, LVDS2B_14P, DQ18	CV35	DDR4_DIMM_CH2_DQ60
	DDR4_DIMM_CH2_A7	CE34	IO, PLL_2B_B_CLKOUT0N, LVDS2B_39N, DQ22	IO, PLL_2B_T_CLKOUT0N, LVDS2B_15N, DQ18	CR34	DDR4_DIMM_CH2_TDQS_N16
	DDR4_DIMM_CH2_A6	CG34	IO, PLL_2B_B_CLKOUT0P, PLL_2B_B_CLKOUT0, PLL_2B_B_FB0, LVDS2B_39P, DQ22	IO, PLL_2B_T_CLKOUT0P, PLL_2B_T_CLKOUT0, PLL_2B_T_FB0, LVDS2B_15P, DQ18	CU34	DDR4_DIMM_CH2_DBI_N7
	DDR4_DIMM_CH2_A5	CF33	IO, LVDS2B_40N, DQSN22	IO, LVDS2B_16N, DQSN18	CT33	DDR4_DIMM_CH2_DQS_N7
	DDR4_DIMM_CH2_A4	CH33	IO, LVDS2B_40P, DQS22	IO, LVDS2B_16P, DQS18	CV33	DDR4_DIMM_CH2_DQS_P7
	DDR4_DIMM_CH2_A3	CE32	IO, LVDS2B_41N, DQ22	IO, LVDS2B_17N, DQ18	CR32	DDR4_DIMM_CH2_DQ56
	DDR4_DIMM_CH2_A2	CG32	IO, LVDS2B_41P, DQ22	IO, LVDS2B_17P, DQ18	CU32	DDR4_DIMM_CH2_DQ57
	DDR4_DIMM_CH2_A1	CF31	IO, LVDS2B_42N, DQ22	IO, LVDS2B_18N, DQ18	CT31	DDR4_DIMM_CH2_DQ59
	DDR4_DIMM_CH2_A0	CH31	IO, LVDS2B_42P, DQ22	IO, LVDS2B_18P, DQ18	CV31	DDR4_DIMM_CH2_DQ58
	DDR4_DIMM_CH2_PAR	CL36	IO, LVDS2B_43N, DQ23	IO, LVDS2B_19N, DQ19	DA36	DDR4_DIMM_CH2_DQ52
DDRT:GNT0	DDR4_DIMM_CH2_CS_N1	CN36	IO, LVDS2B_43P, DQ23	IO, LVDS2B_19P, DQ19	DC36	DDR4_DIMM_CH2_DQ53
	DDR4_DIMM_CH2_CK_N0	CK35	IO, LVDS2B_44N, DQ23	IO, LVDS2B_20N, DQ19	CY35	DDR4_DIMM_CH2_DQ55
	DDR4_DIMM_CH2_CK_P0	CM35	IO, LVDS2B_44P, DQ23	IO, LVDS2B_20P, DQ19	DB35	DDR4_DIMM_CH2_DQ54
DDRT:REQ	DDR4_DIMM_CH2_CKE1	CL34	IO, LVDS2B_45N, DQ23	IO, LVDS2B_21N, DQ19	DA34	DDR4_DIMM_CH2_TDQS_N15
	DDR4_DIMM_CH2_CKE0	CN34	IO, LVDS2B_45P, DQ23	IO, LVDS2B_21P, DQ19	DC34	DDR4_DIMM_CH2_DBI_N6
DDRT:ERR	DDR4_DIMM_CH2_ODT1	CK33	IO, LVDS2B_46N, DQSN23	IO, LVDS2B_22N, DQSN19	CY33	DDR4_DIMM_CH2_DQS_N6
	DDR4_DIMM_CH2_ODT0	CM33	IO, LVDS2B_46P, DQS23	IO, LVDS2B_22P, DQS19	DB33	DDR4_DIMM_CH2_DQS_P6
	DDR4_DIMM_CH2_ACT_N	CL32	IO, LVDS2B_47N, DQ23	IO, LVDS2B_23N, DQ19	DA32	DDR4_DIMM_CH2_DQ48
	DDR4_DIMM_CH2_CS_N0	CN32	IO, LVDS2B_47P, DQ23	IO, LVDS2B_23P, DQ19	DC32	DDR4_DIMM_CH2_DQ49
	DDR4_DIMM_CH2_RESET_N	CK31	IO, LVDS2B_48N, DQ23	IO, LVDS2B_24N, DQ19	CY31	DDR4_DIMM_CH2_DQ51
	DDR4_DIMM_CH2_BG1	CM31	IO, LVDS2B_48P, DQ23	IO, LVDS2B_24P, DQ19	DB31	DDR4_DIMM_CH2_DQ50

BOT TOP

Bank 2B

AGFB014R24_2486A

{15} DDR4_DIMM_CH2_CK_P[1:0]
{15} DDR4_DIMM_CH2_CK_N[1:0]
{15} DDR4_DIMM_CH2_CKE[1:0]
{15} DDR4_DIMM_CH2_A[17:0]
{15} DDR4_DIMM_CH2_ODT[1:0]
{15} DDR4_DIMM_CH2_BG[1:0]
{15} DDR4_DIMM_CH2_BA[1:0]
{15} DDR4_DIMM_CH2_CS_N[3:0]
{15} DDR4_DIMM_CH2_RESET_N
{15} DDR4_DIMM_CH2_ACT_N
{15} DDR4_DIMM_CH2_PAR
{15} DDR4_DIMM_CH2_ALERT_N
{15} DDR4_DIMM_CH2_C2

{15,16} DDR4_DIMM_CH2_DBI_N[8:0]
{15,16} DDR4_DIMM_CH2_DQ[71:0]
{15,16} DDR4_DIMM_CH2_DQS_P[8:0]
{15,16} DDR4_DIMM_CH2_DQS_N[8:0]
{15,16} DDR4_DIMM_CH2_TDQS_N[17:9]

CLK_DDR4_CH2_P R67 DNI CLK_DDR4_CH2_N

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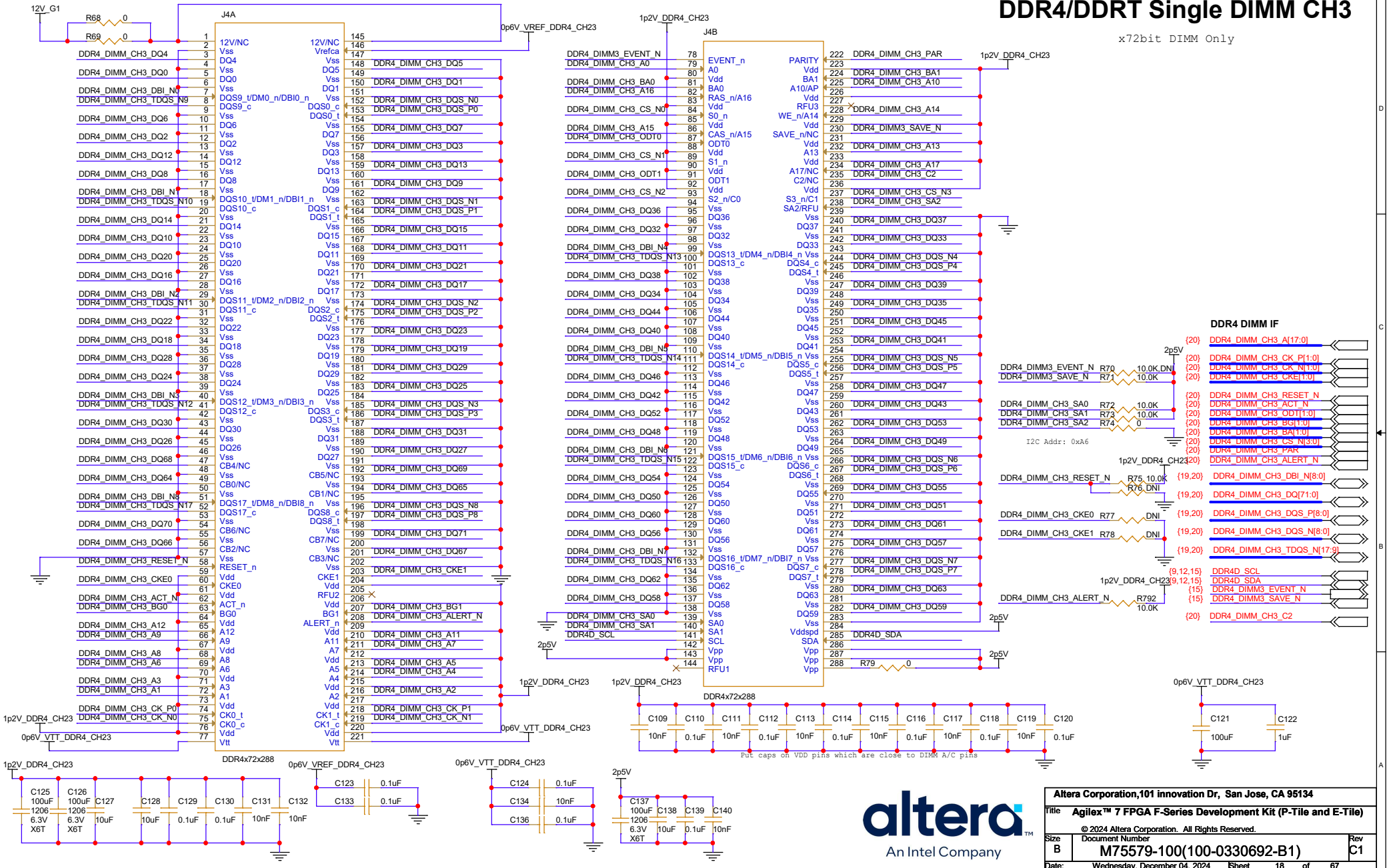
Title: Agilex™ 7 FPGA F-Series Development Kit (P-Tile and E-Tile)

Size: B | Document Number: M75579-100(100-0330692-B1) | Rev: C1

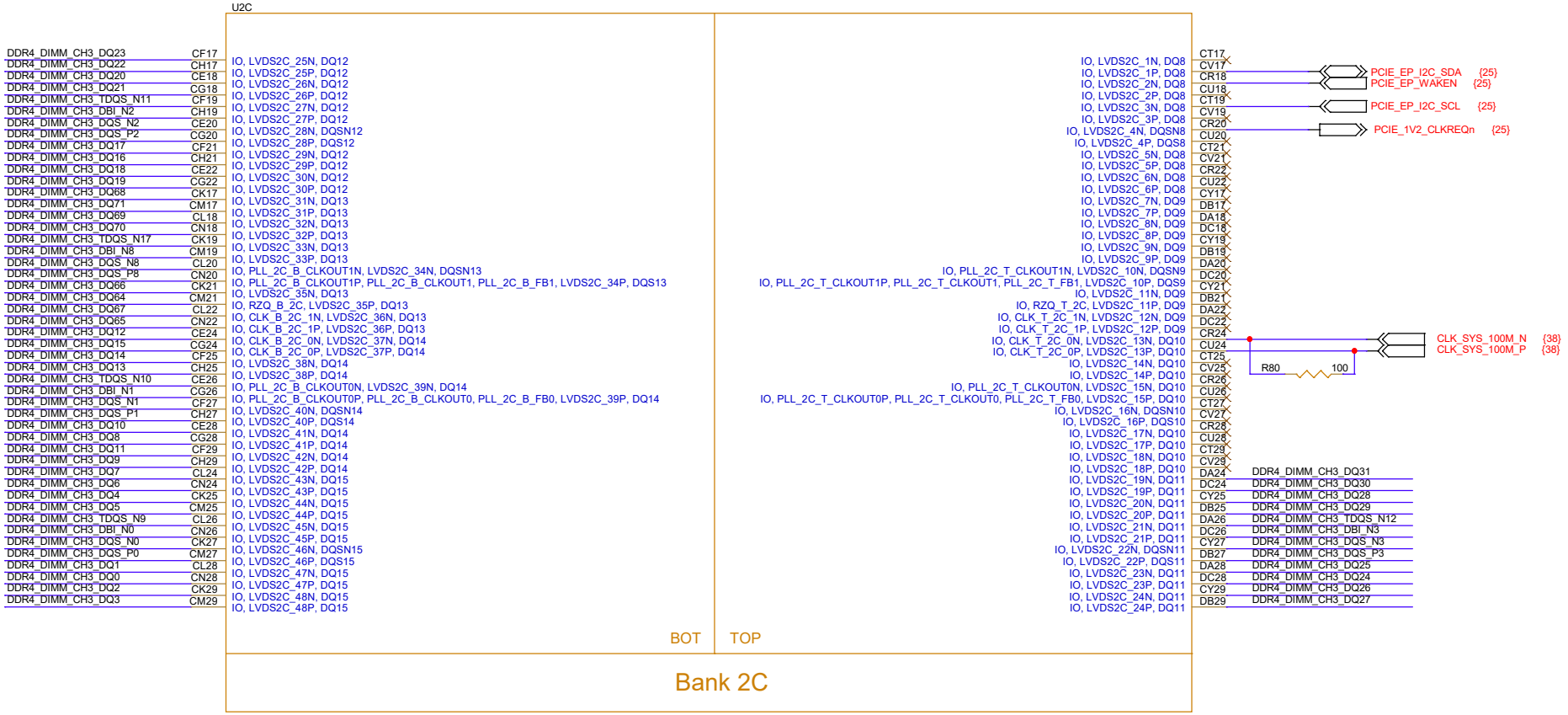
Date: Wednesday, December 04, 2024 | Sheet 17 of 67

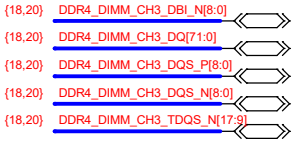
DDR4/DDRT Single DIMM CH3

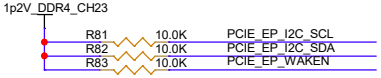
x72bit DIMM Only



DDR4/T CH3 INTERFACE -- FPGA SIDE 2C







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Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 19 of 67

DDR4/T CH3 INTERFACE -- FPGA SIDE 2D

U2B

DDR4_DIMM_CH3_DQ63	CF3	IO, LVDS2D_25N, DQ4
DDR4_DIMM_CH3_DQ62	CH3	IO, LVDS2D_25P, DQ4
DDR4_DIMM_CH3_DQ60	CE4	IO, LVDS2D_26N, DQ4
DDR4_DIMM_CH3_DQ61	CG4	IO, LVDS2D_26P, DQ4
DDR4_DIMM_CH3_TDQS_N16	CF5	IO, LVDS2D_27N, DQ4
DDR4_DIMM_CH3_DBI_N7	CH5	IO, LVDS2D_27P, DQ4
DDR4_DIMM_CH3_DQS_N7	CE6	IO, LVDS2D_28N, DQSN4
DDR4_DIMM_CH3_DQS_P7	CG6	IO, LVDS2D_28P, DQS4
DDR4_DIMM_CH3_DQ57	CF7	IO, LVDS2D_29N, DQ4
DDR4_DIMM_CH3_DQ56	CH7	IO, LVDS2D_29P, DQ4
DDR4_DIMM_CH3_DQ58	CE8	IO, LVDS2D_30N, DQ4
DDR4_DIMM_CH3_DQ59	CG8	IO, LVDS2D_30P, DQ4
DDR4_DIMM_CH3_DQ52	CK3	IO, LVDS2D_31N, DQ5
DDR4_DIMM_CH3_DQ55	CM3	IO, LVDS2D_31P, DQ5
DDR4_DIMM_CH3_DQ54	CL4	IO, LVDS2D_32N, DQ5
DDR4_DIMM_CH3_DQ53	CN4	IO, LVDS2D_32P, DQ5
DDR4_DIMM_CH3_TDQS_N15	CK5	IO, LVDS2D_33N, DQ5
DDR4_DIMM_CH3_DBI_N6	CM5	IO, LVDS2D_33P, DQ5
DDR4_DIMM_CH3_DQS_N6	CL6	IO, PLL_2D_B_CLKOUT1N, LVDS2D_34N, DQSN5
DDR4_DIMM_CH3_DQS_P6	CN6	IO, PLL_2D_B_CLKOUT1P, PLL_2D_B_CLKOUT1, PLL_2D_B_FB1, LVDS2D_34P, DQS5
DDR4_DIMM_CH3_DQ50	CK7	IO, LVDS2D_35N, DQ5
DDR4_DIMM_CH3_DQ48	CM7	IO, RZQ_B_2D, LVDS2D_35P, DQ5
DDR4_DIMM_CH3_DQ51	CL8	IO, CLK_B_2D_1N, LVDS2D_36N, DQ5
DDR4_DIMM_CH3_DQ49	CN8	IO, CLK_B_2D_1P, LVDS2D_36P, DQ5
DDR4_DIMM_CH3_DQ44	CE10	IO, CLK_B_2D_0N, LVDS2D_37N, DQ6
DDR4_DIMM_CH3_DQ47	CG10	IO, CLK_B_2D_0P, LVDS2D_37P, DQ6
DDR4_DIMM_CH3_DQ46	CF11	IO, LVDS2D_38N, DQ6
DDR4_DIMM_CH3_DQ45	CH11	IO, LVDS2D_38P, DQ6
DDR4_DIMM_CH3_TDQS_N14	CE12	IO, PLL_2D_B_CLKOUT0N, LVDS2D_39N, DQ6
DDR4_DIMM_CH3_DBI_N5	CG12	IO, PLL_2D_B_CLKOUT0P, PLL_2D_B_CLKOUT0, PLL_2D_B_FB0, LVDS2D_39P, DQ6
DDR4_DIMM_CH3_DQS_N5	CF13	IO, LVDS2D_40N, DQSN6
DDR4_DIMM_CH3_DQS_P5	CH13	IO, LVDS2D_40P, DQS6
DDR4_DIMM_CH3_DQ42	CE14	IO, LVDS2D_41N, DQ6
DDR4_DIMM_CH3_DQ40	CG14	IO, LVDS2D_41P, DQ6
DDR4_DIMM_CH3_DQ43	CF15	IO, LVDS2D_42N, DQ6
DDR4_DIMM_CH3_DQ41	CH15	IO, LVDS2D_42P, DQ6
DDR4_DIMM_CH3_DQ39	CL10	IO, LVDS2D_43N, DQ7
DDR4_DIMM_CH3_DQ38	CN10	IO, LVDS2D_43P, DQ7
DDR4_DIMM_CH3_DQ36	CK11	IO, LVDS2D_44N, DQ7
DDR4_DIMM_CH3_DQ37	CM11	IO, LVDS2D_44P, DQ7
DDR4_DIMM_CH3_TDQS_N13	CL12	IO, LVDS2D_45N, DQ7
DDR4_DIMM_CH3_DBI_N4	CN12	IO, LVDS2D_45P, DQ7
DDR4_DIMM_CH3_DQS_N4	CK13	IO, LVDS2D_46N, DQSN7
DDR4_DIMM_CH3_DQS_P4	CM13	IO, LVDS2D_46P, DQS7
DDR4_DIMM_CH3_DQ33	CL14	IO, LVDS2D_47N, DQ7
DDR4_DIMM_CH3_DQ32	CN14	IO, LVDS2D_47P, DQ7
DDR4_DIMM_CH3_DQ34	CK15	IO, LVDS2D_48N, DQ7
DDR4_DIMM_CH3_DQ35	CM15	IO, LVDS2D_48P, DQ7

BOT

		IO, LVDS2D_1N, DQ0
		IO, LVDS2D_1P, DQ0
		IO, LVDS2D_2N, DQ0
		IO, LVDS2D_2P, DQ0
		IO, LVDS2D_3N, DQ0
		IO, LVDS2D_3P, DQ0
		IO, LVDS2D_4N, DQSN0
		IO, LVDS2D_4P, DQS0
		IO, LVDS2D_5N, DQ0
		IO, LVDS2D_5P, DQ0
		IO, LVDS2D_6N, DQ0
		IO, LVDS2D_6P, DQ0
		IO, LVDS2D_7N, DQ1
		IO, LVDS2D_7P, DQ1
		IO, LVDS2D_8N, DQ1
		IO, LVDS2D_8P, DQ1
		IO, LVDS2D_9N, DQ1
		IO, LVDS2D_9P, DQ1
		IO, PLL_2D_T_CLKOUT1N, LVDS2D_10N, DQSN1
		IO, PLL_2D_T_CLKOUT1P, PLL_2D_T_CLKOUT1, PLL_2D_T_FB1, LVDS2D_10P, DQS1
		IO, LVDS2D_11N, DQ1
		IO, RZQ_T_2D, LVDS2D_11P, DQ1
		IO, CLK_T_2D_1N, LVDS2D_12N, DQ1
		IO, CLK_T_2D_1P, LVDS2D_12P, DQ1
		IO, CLK_T_2D_0N, LVDS2D_13N, DQ2
		IO, CLK_T_2D_0P, LVDS2D_13P, DQ2
		IO, LVDS2D_14N, DQ2
		IO, LVDS2D_14P, DQ2
		IO, PLL_2D_T_CLKOUT0N, LVDS2D_15N, DQ2
		IO, PLL_2D_T_CLKOUT0P, PLL_2D_T_CLKOUT0, PLL_2D_T_FB0, LVDS2D_15P, DQ2
		IO, LVDS2D_16N, DQSN2
		IO, LVDS2D_16P, DQS2
		IO, LVDS2D_17N, DQ2
		IO, LVDS2D_17P, DQ2
		IO, LVDS2D_18N, DQ2
		IO, LVDS2D_18P, DQ2
		IO, LVDS2D_19N, DQ3
		IO, LVDS2D_19P, DQ3
		IO, LVDS2D_20N, DQ3
		IO, LVDS2D_20P, DQ3
		IO, LVDS2D_21N, DQ3
		IO, LVDS2D_21P, DQ3
		IO, LVDS2D_22N, DQSN3
		IO, LVDS2D_22P, DQS3
		IO, LVDS2D_23N, DQ3
		IO, LVDS2D_23P, DQ3
		IO, LVDS2D_24N, DQ3
		IO, LVDS2D_24P, DQ3

TOP

CT3	DDR4_DIMM_CH3_CK_N1	DDRT:ERID2
CV3	DDR4_DIMM_CH3_CK_P1	DDRT:ERID0
CR4		
CU4	DDR4_DIMM_CH3_ALERT_N	DDRT:NC
CT5		
CV5		
CR6		
CU6		
CT7		
CV7	DDR4_DIMM_CH3_C2	DDRT:C3
CR8	DDR4_DIMM_CH3_CS_N3	DDRT:C2
CU8	DDR4_DIMM_CH3_CS_N2	DDRT:C1
CT1	DDR4_DIMM_CH3_BG0	
CV1	DDR4_DIMM_CH3_BA1	
CY3	DDR4_DIMM_CH3_BA0	
DA4	DDR4_DIMM_CH3_A17	
CY5	DDR4_DIMM_CH3_A16	
DB5	DDR4_DIMM_CH3_A15	
DA6	DDR4_DIMM_CH3_A14	
DC6	DDR4_DIMM_CH3_A13	
CY7	DDR4_DIMM_CH3_A12	
DB7	DDR4_DIMM_CH3_RZQ	
DA8 (38)	CLK_DDR4_CH3_N	
DC8 (38)	CLK_DDR4_CH3_P	
CR10	DDR4_DIMM_CH3_A11	
CU10	DDR4_DIMM_CH3_A10	
CT11	DDR4_DIMM_CH3_A9	
CV11	DDR4_DIMM_CH3_A8	
CR12	DDR4_DIMM_CH3_A7	
CU12	DDR4_DIMM_CH3_A6	
CT13	DDR4_DIMM_CH3_A5	
CV13	DDR4_DIMM_CH3_A4	
CR14	DDR4_DIMM_CH3_A3	
CU14	DDR4_DIMM_CH3_A2	
CT15	DDR4_DIMM_CH3_A1	
CV15	DDR4_DIMM_CH3_A0	
DA10	DDR4_DIMM_CH3_PAR	
DC10	DDR4_DIMM_CH3_CS_N1	DDRT:GNT0
CY11	DDR4_DIMM_CH3_CK_N0	
DB11	DDR4_DIMM_CH3_CK_P0	
DA12	DDR4_DIMM_CH3_CKE1	DDRT:REQ
DC12	DDR4_DIMM_CH3_CKE0	
CY13	DDR4_DIMM_CH3_ODT1	DDRT:ERR
DB13	DDR4_DIMM_CH3_ODT0	
DA14	DDR4_DIMM_CH3_ACT_N	
DC14	DDR4_DIMM_CH3_CS_N0	
CY15	DDR4_DIMM_CH3_RESET_N	
DB15	DDR4_DIMM_CH3_BG1	

240 R84

Bank 2D

AGFB014R24_2486A

{18} DDR4_DIMM_CH3_CK_P[1:0]
{18} DDR4_DIMM_CH3_CK_N[1:0]
{18} DDR4_DIMM_CH3_CKE[1:0]
{18} DDR4_DIMM_CH3_A[17:0]
{18} DDR4_DIMM_CH3_ODT[1:0]
{18} DDR4_DIMM_CH3_BG[1:0]
{18} DDR4_DIMM_CH3_BA[1:0]
{18} DDR4_DIMM_CH3_CS_N[3:0]
{18} DDR4_DIMM_CH3_RESET_N
{18} DDR4_DIMM_CH3_ACT_N
{18} DDR4_DIMM_CH3_PAR
{18} DDR4_DIMM_CH3_ALERT_N
{18} DDR4_DIMM_CH3_C2

{18,19} DDR4_DIMM_CH3_DBI_N[8:0]
{18,19} DDR4_DIMM_CH3_DQ[71:0]
{18,19} DDR4_DIMM_CH3_DQS_P[8:0]
{18,19} DDR4_DIMM_CH3_DQS_N[8:0]
{18,19} DDR4_DIMM_CH3_TDQS_N[17:9]

CLK_DDR4_CH3_P R85 DNI CLK_DDR4_CH3_N

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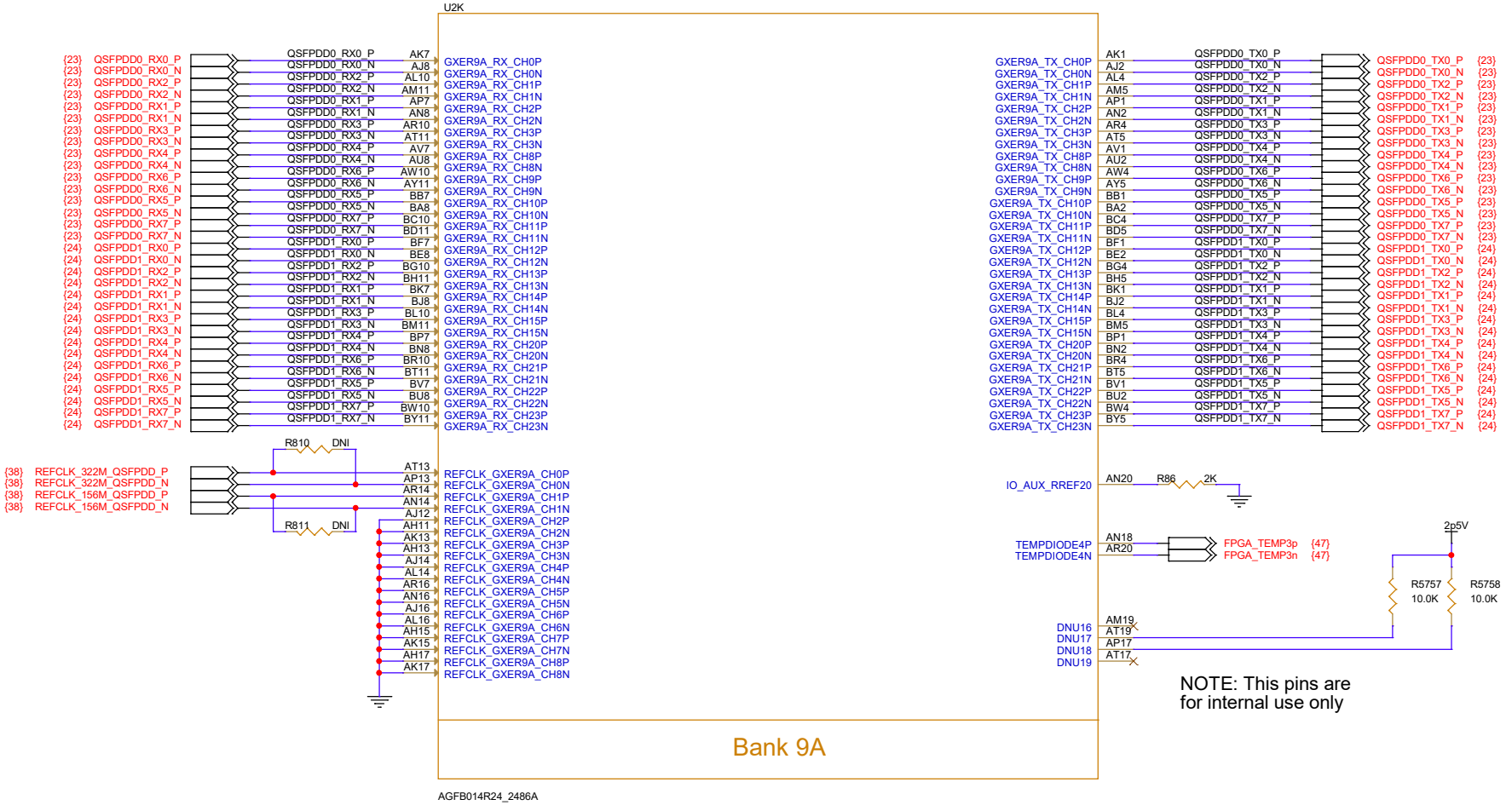
Title: Agilex™ 7 FPGA F-Series Development Kit (P-Tile and E-Tile)

Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 20 of 67

E-TILE BANK 9A



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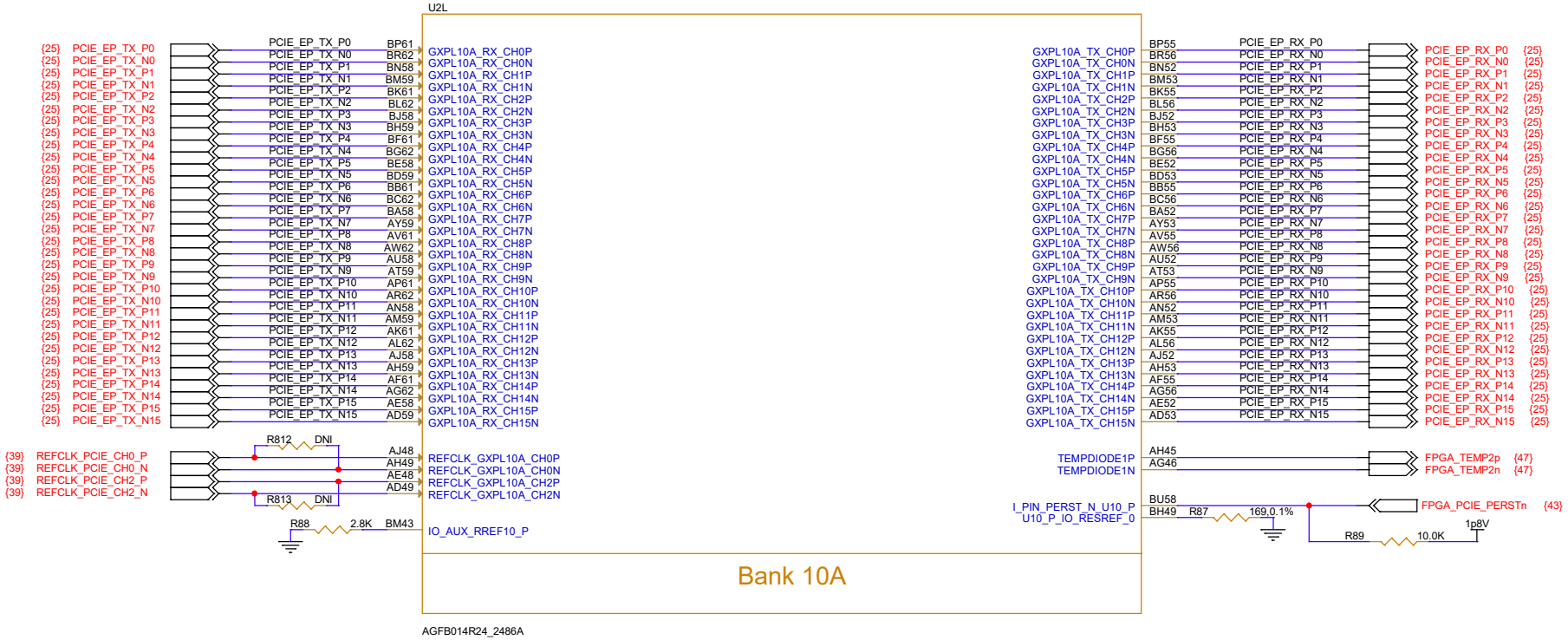
Title: Agilex™ 7 FPGA F-Series Development Kit (P-Tile and E-Tile)

Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 21 of 67

P-TILE BANK 10A



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Title: Agilex™ 7 FPGA F-Series Development Kit (P-Tile and E-Tile)		
Size: B	Document Number: M75579-100(100-0330692-B1)	Rev: C1
Date: Wednesday, December 04, 2024	Sheet 22 of 67	

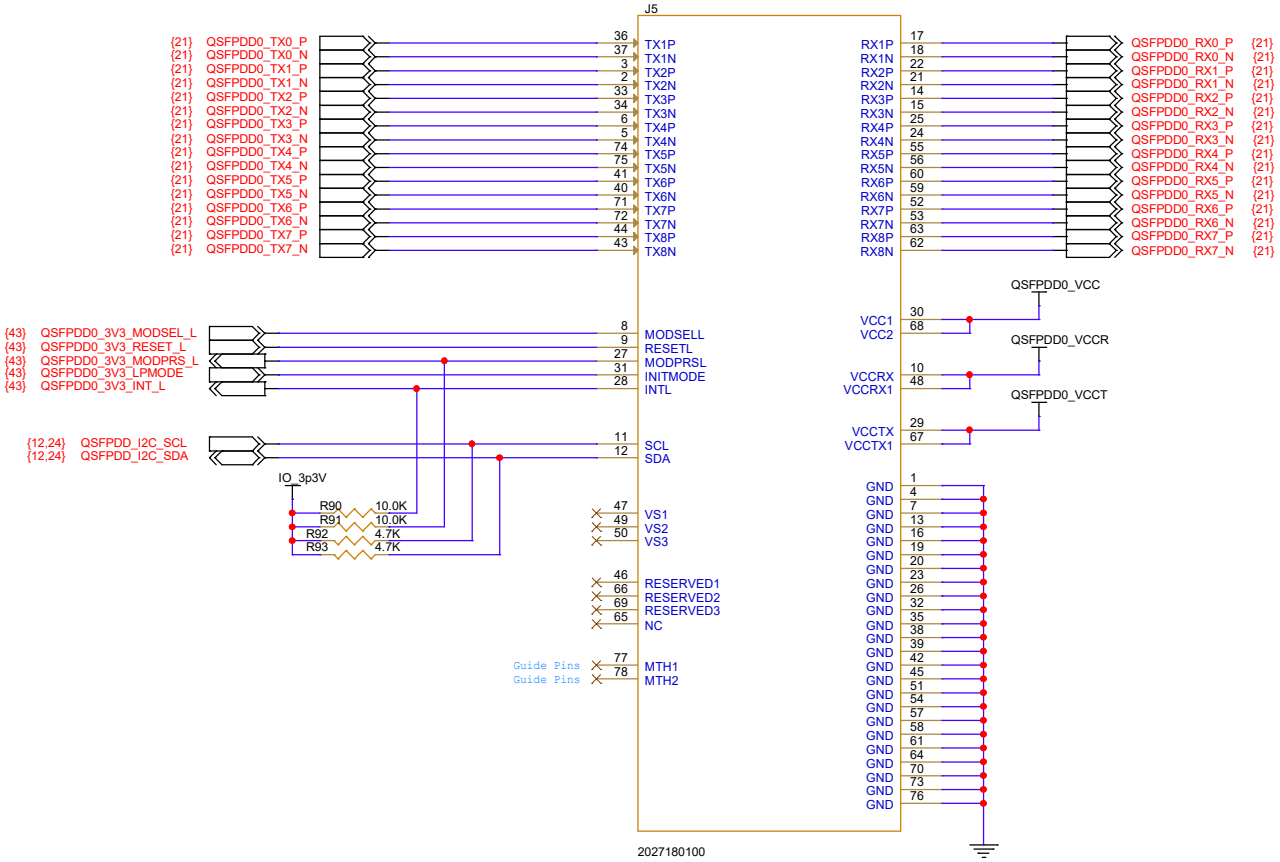
QSFPDD0

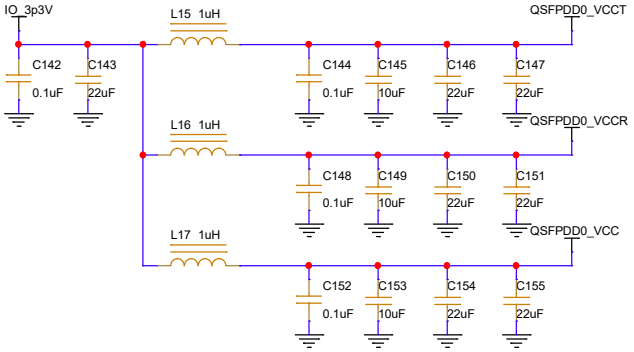
NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

NOTE 2: zQSFP 100-ohm termination is implemented via the FPGA on-chip termination.

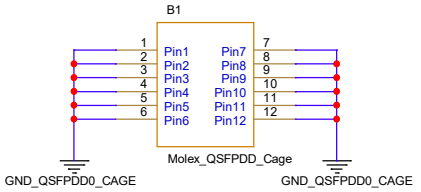
NOTE 3: DC blocking capacitors are in the module for RX and TX.

NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.

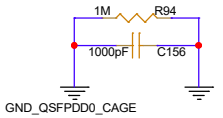




Place close to QSFPDD Connector



MOLEX MPN 2031431355



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Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 23 of 67

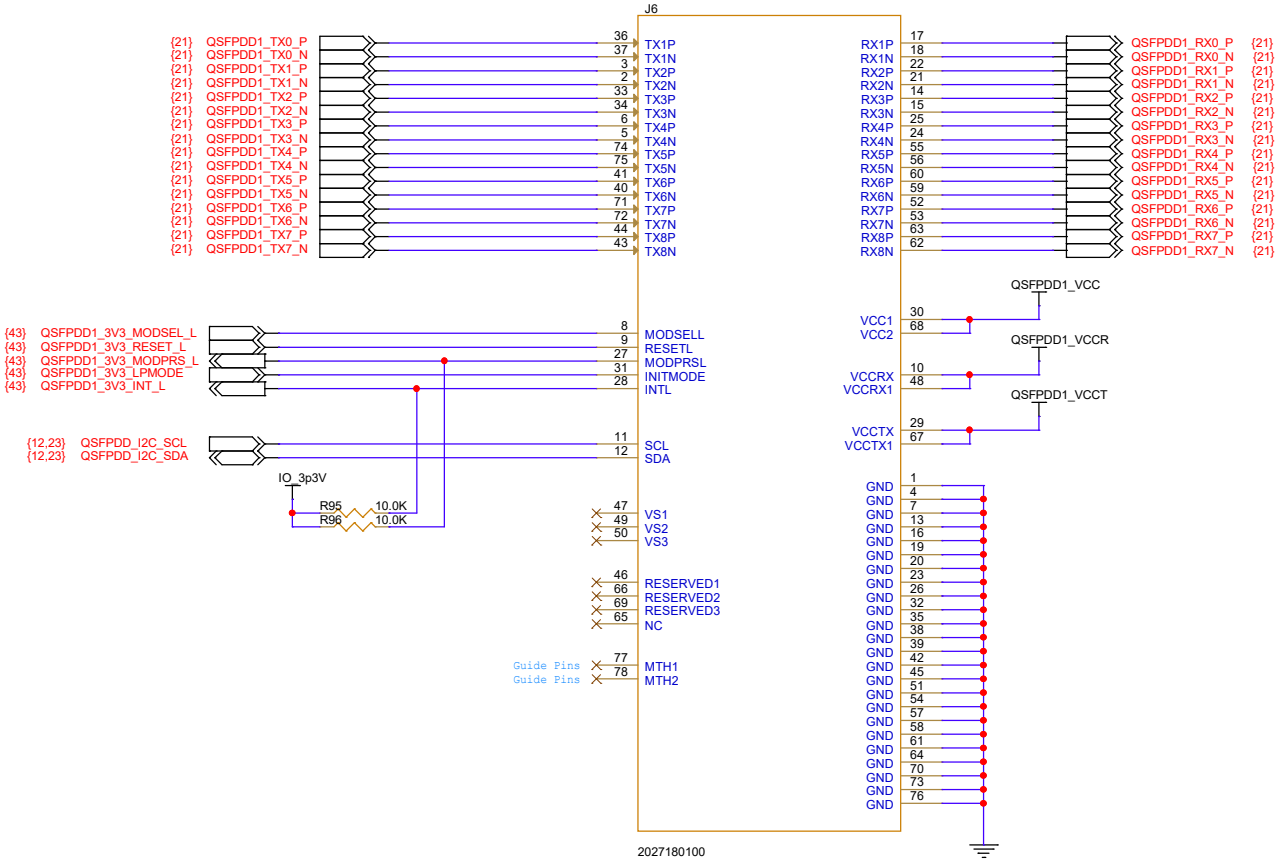
QSFPDD1

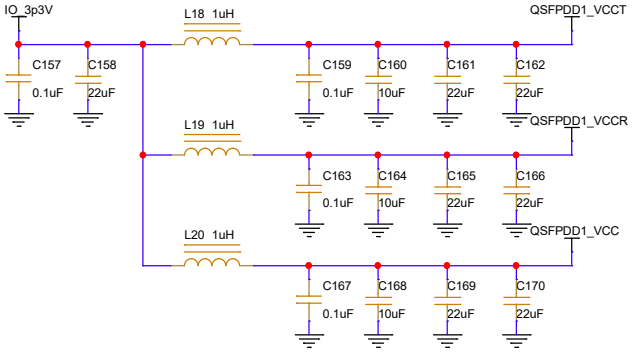
NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

NOTE 2: zQSFP 100-ohm termination is implemented via the FPGA on-chip termination.

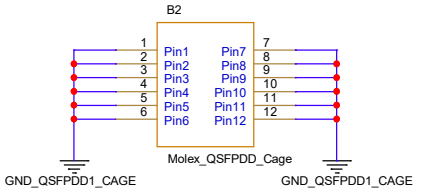
NOTE 3: DC blocking capacitors are in the module for RX and TX.

NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.

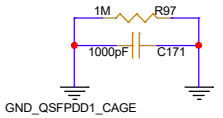




Place close to QSFPDD Connector



MOLEX MPN 2031431355



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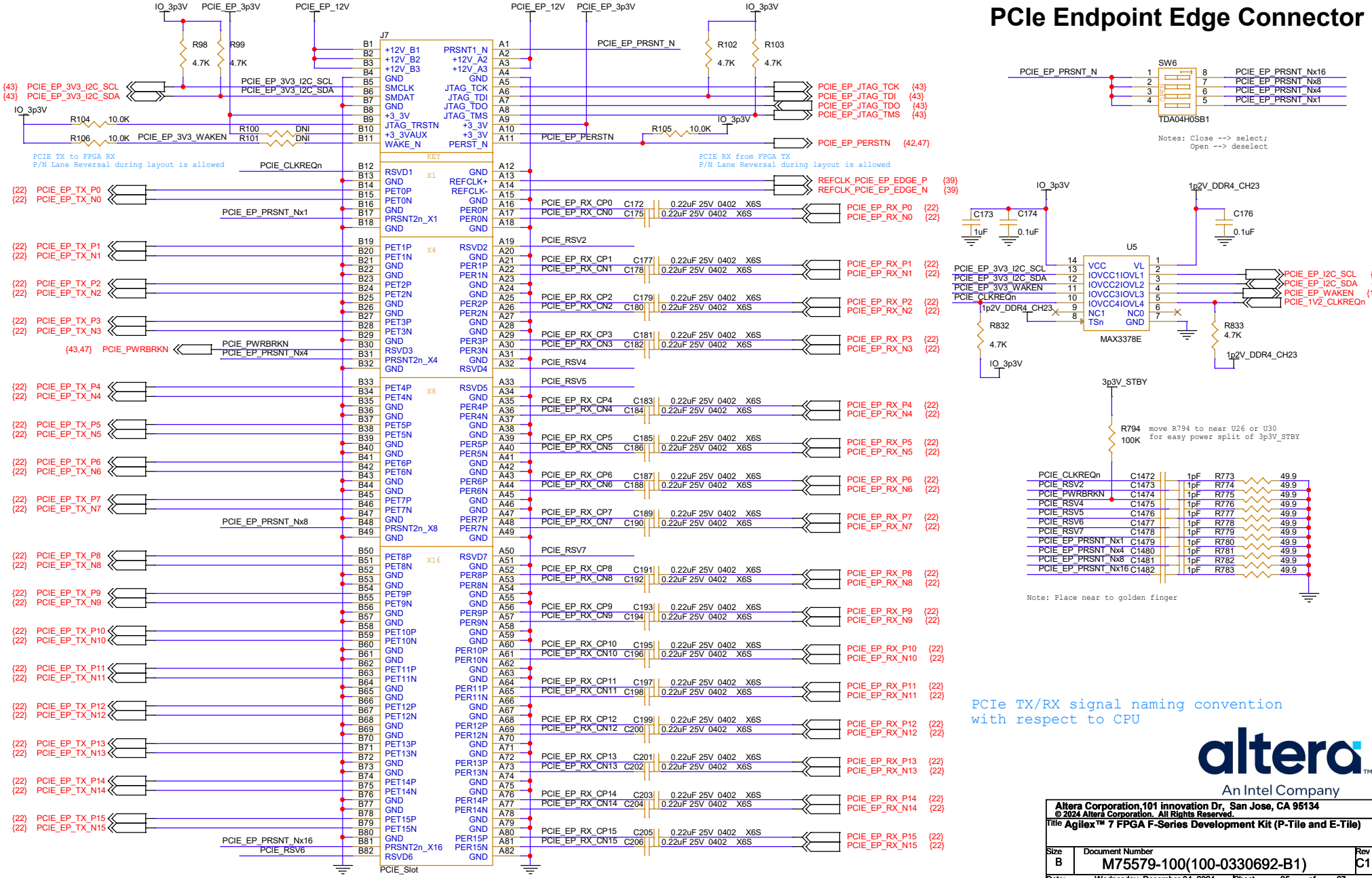
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 24 of 67

PCIe Endpoint Edge Connector



PCIe TX/RX signal naming convention
with respect to CPU

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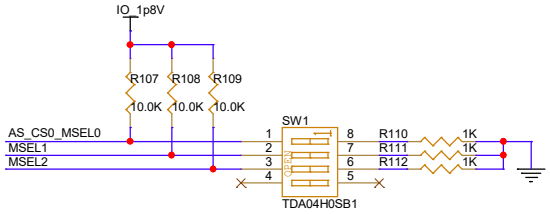
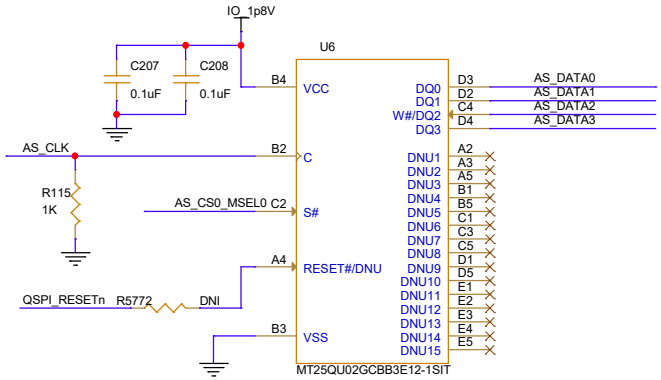
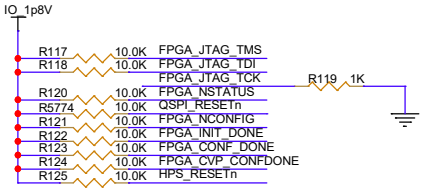
Date: Wednesday, December 04, 2024 Sheet 25 of 67

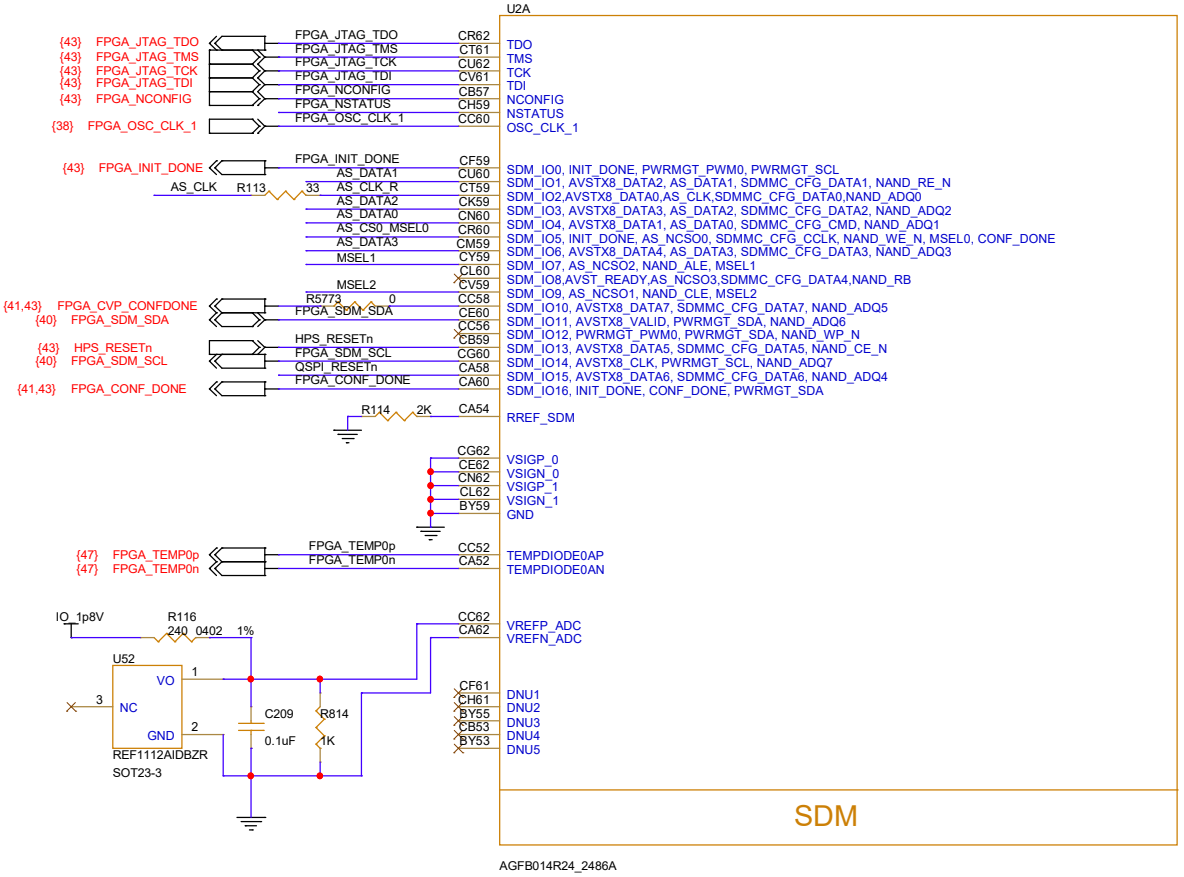
SDM & Configuration



Config Mode	MSEL2	MSEL1	MSEL0
AS_FAST	0	0	1
AS_NORMAL	0	1	1







AGFB014R24_2486A

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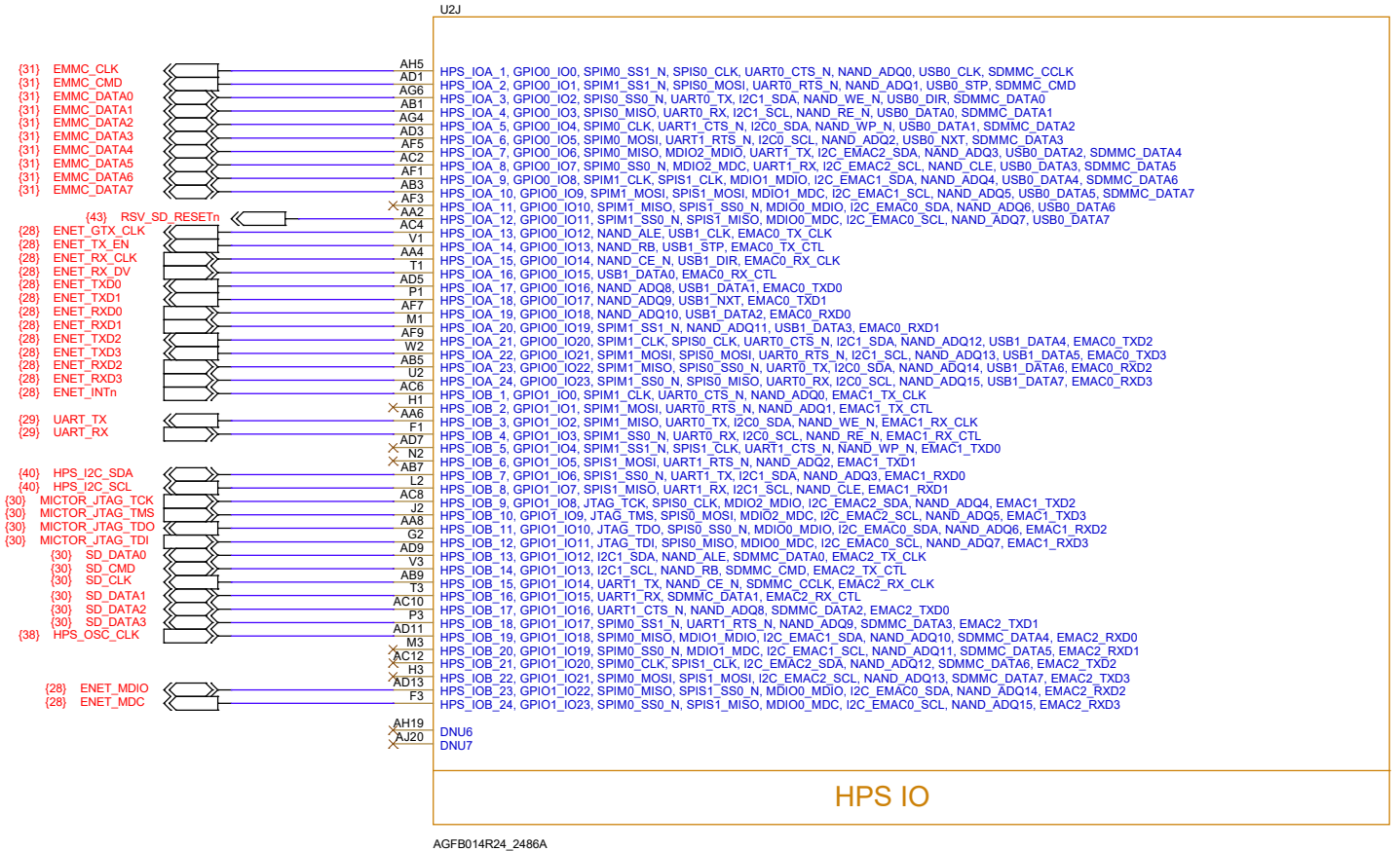
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 26 of 67

Bank HPS



AGFB014R24_2486A

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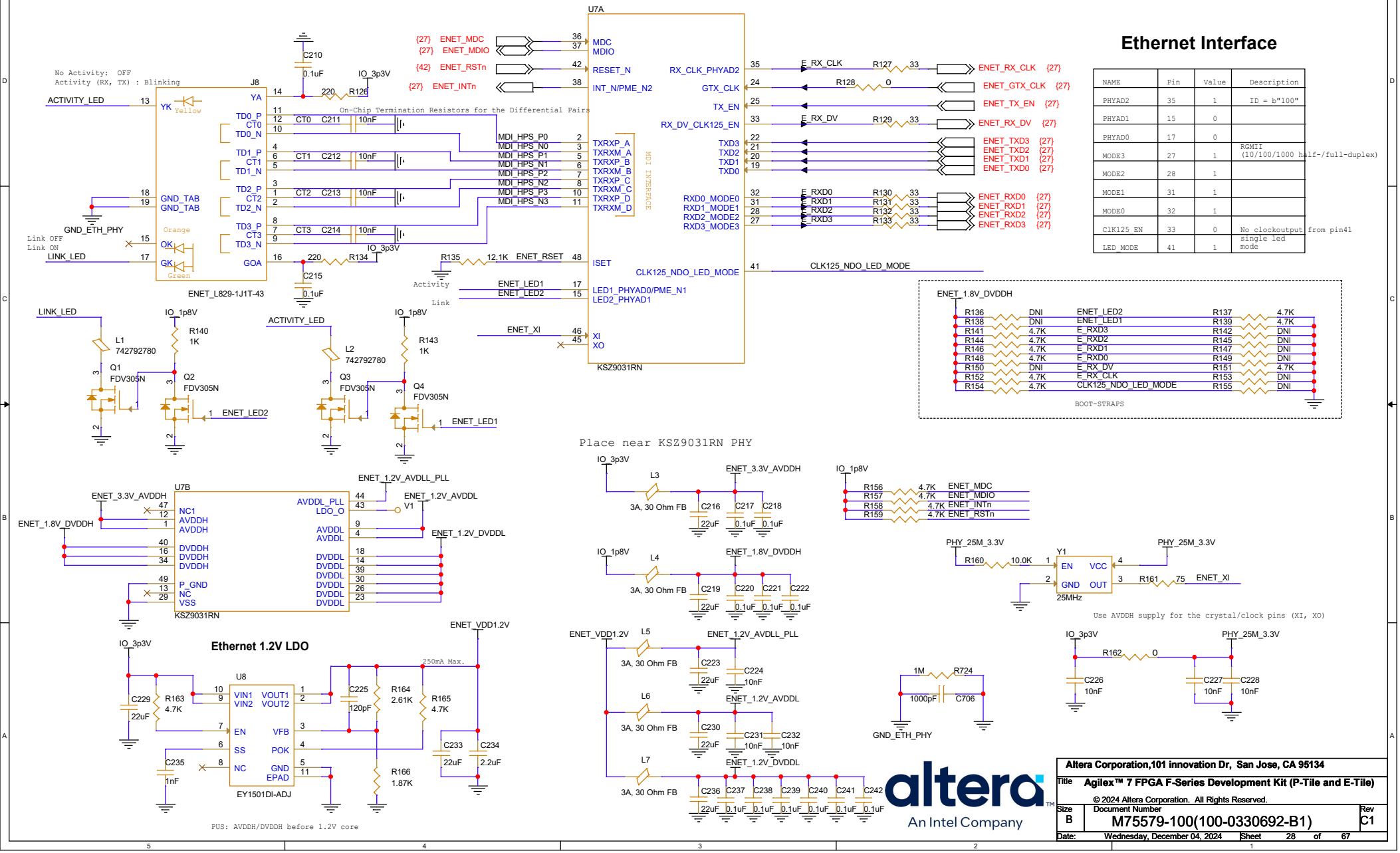
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 27 of 67

10/100/1000 Ethernet - HPS



Ethernet Interface

NAME	Pin	Value	Description
PHYAD2	35	1	ID = b"100"
PHYAD1	15	0	
PHYAD0	17	0	
MODE3	27	1	RGMII (10/100/1000 half-/full-duplex)
MODE2	28	1	
MODE1	31	1	
MODE0	32	1	
CLK125_EN	33	0	No clockoutput from pin41
LED_MODE	41	1	single led mode

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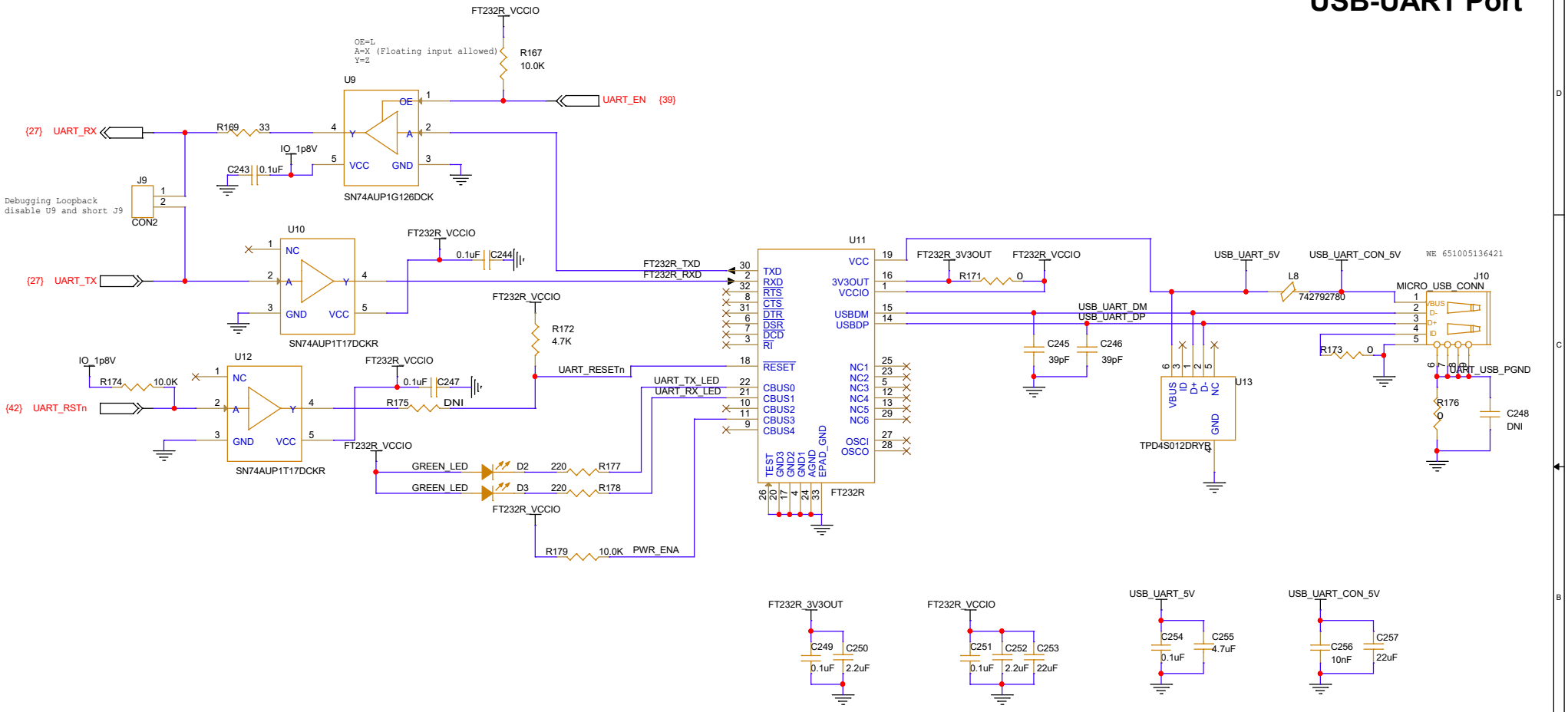
Size: B | Document Number: M75579-100(100-0330692-B1) | Rev: C1

Date: Wednesday, December 04, 2024 | Sheet 28 of 67

USB-UART Port



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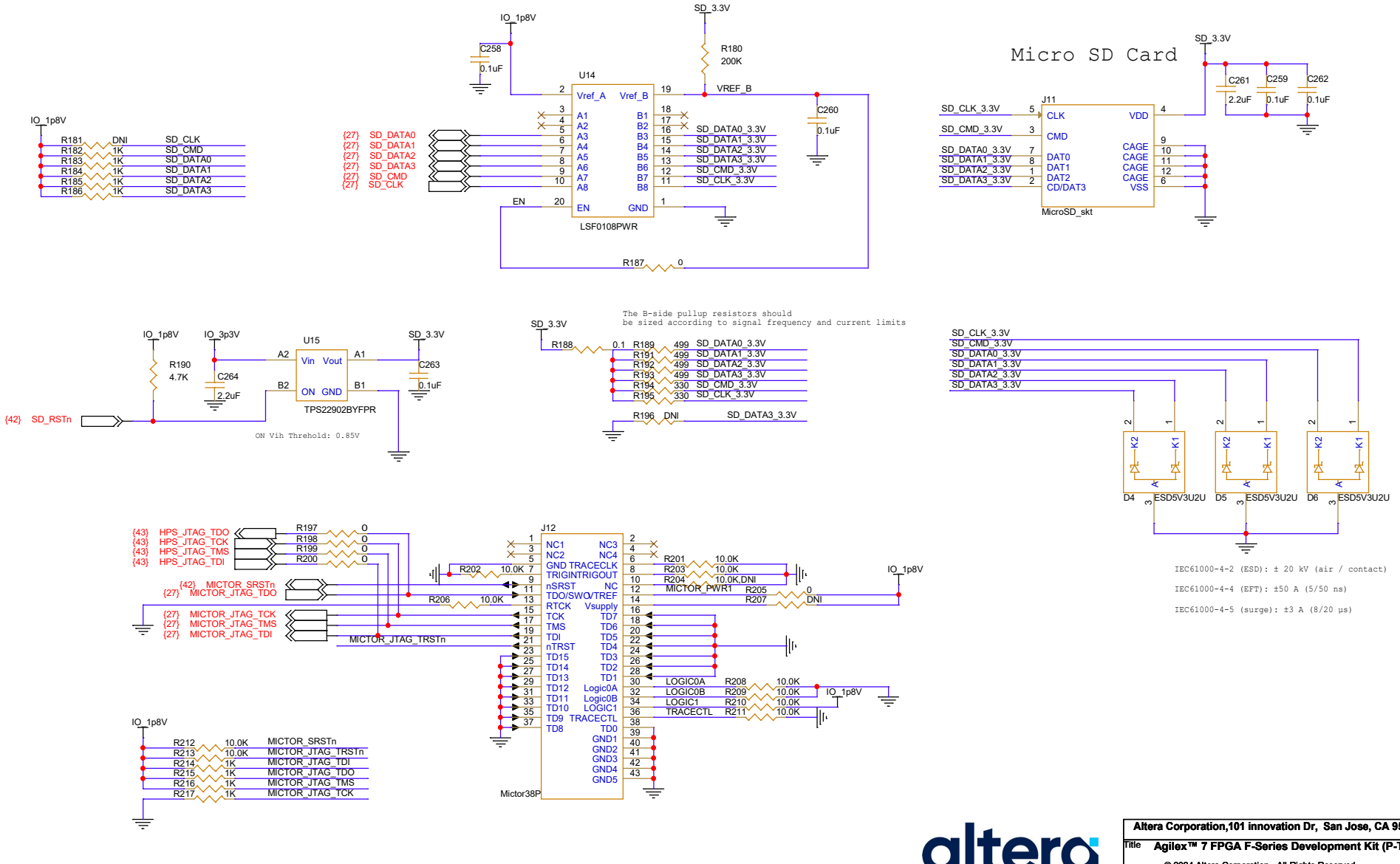
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 29 of 67

MicroSD Card



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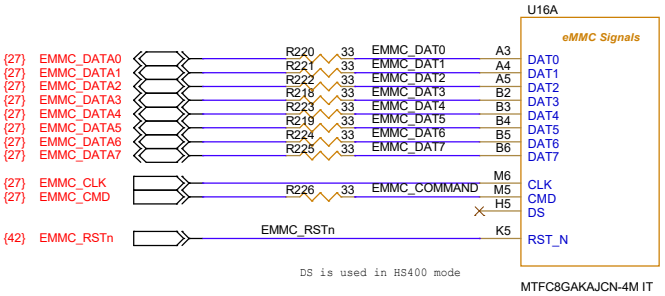
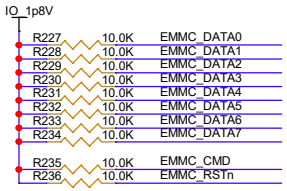
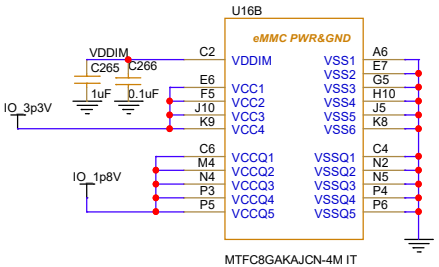
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

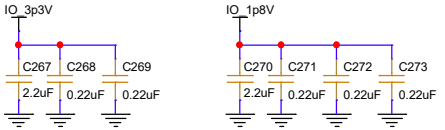
Date: Wednesday, December 04, 2024 Sheet 30 of 67

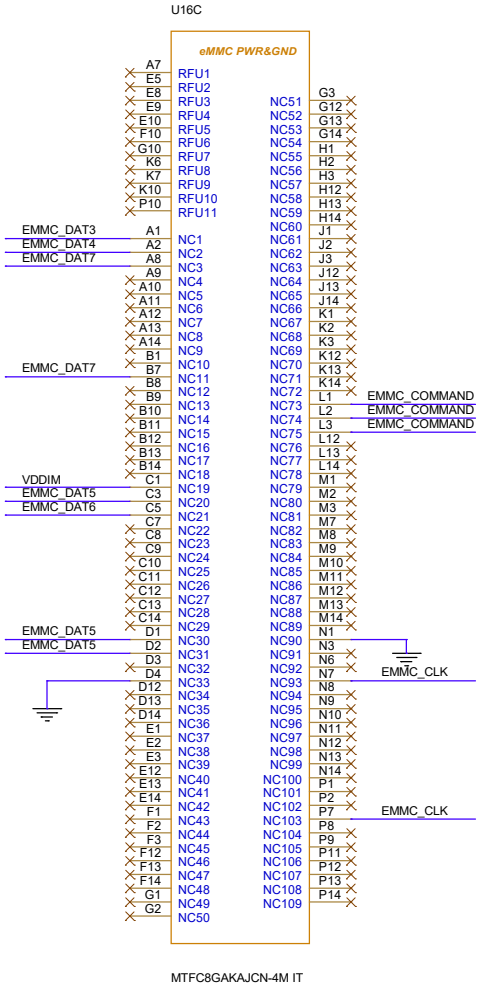
eMMC











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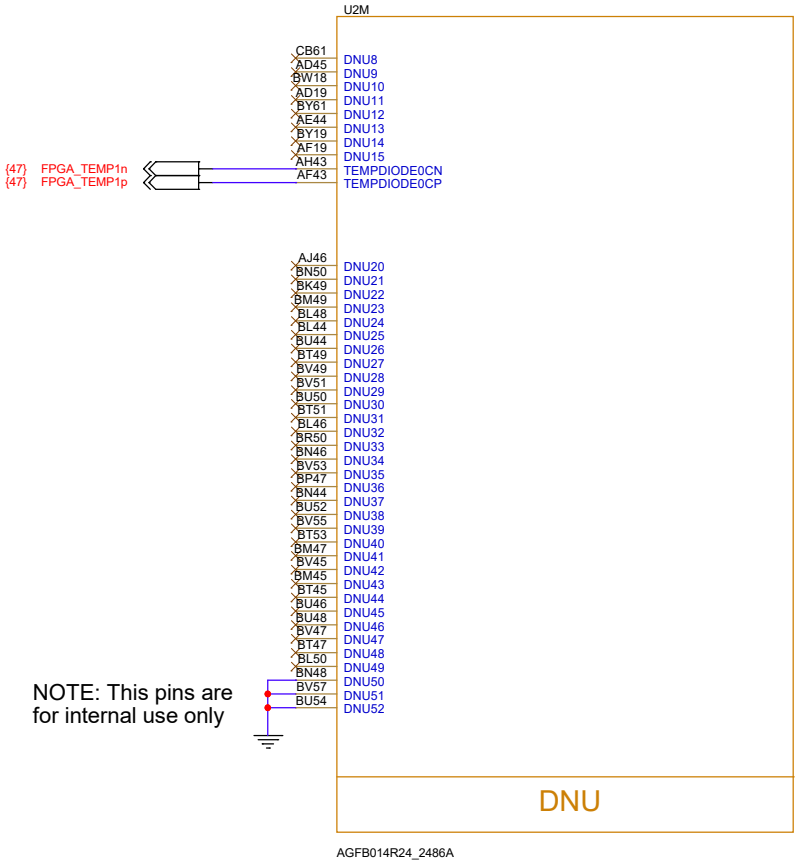
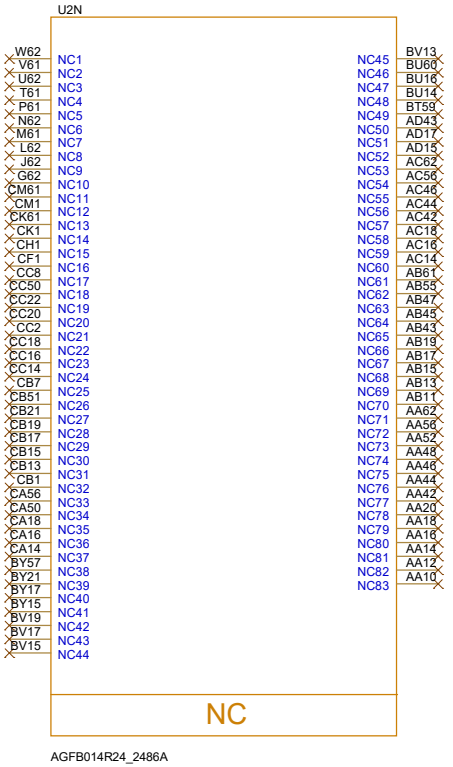
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 31 of 67

Bank NC/DNU





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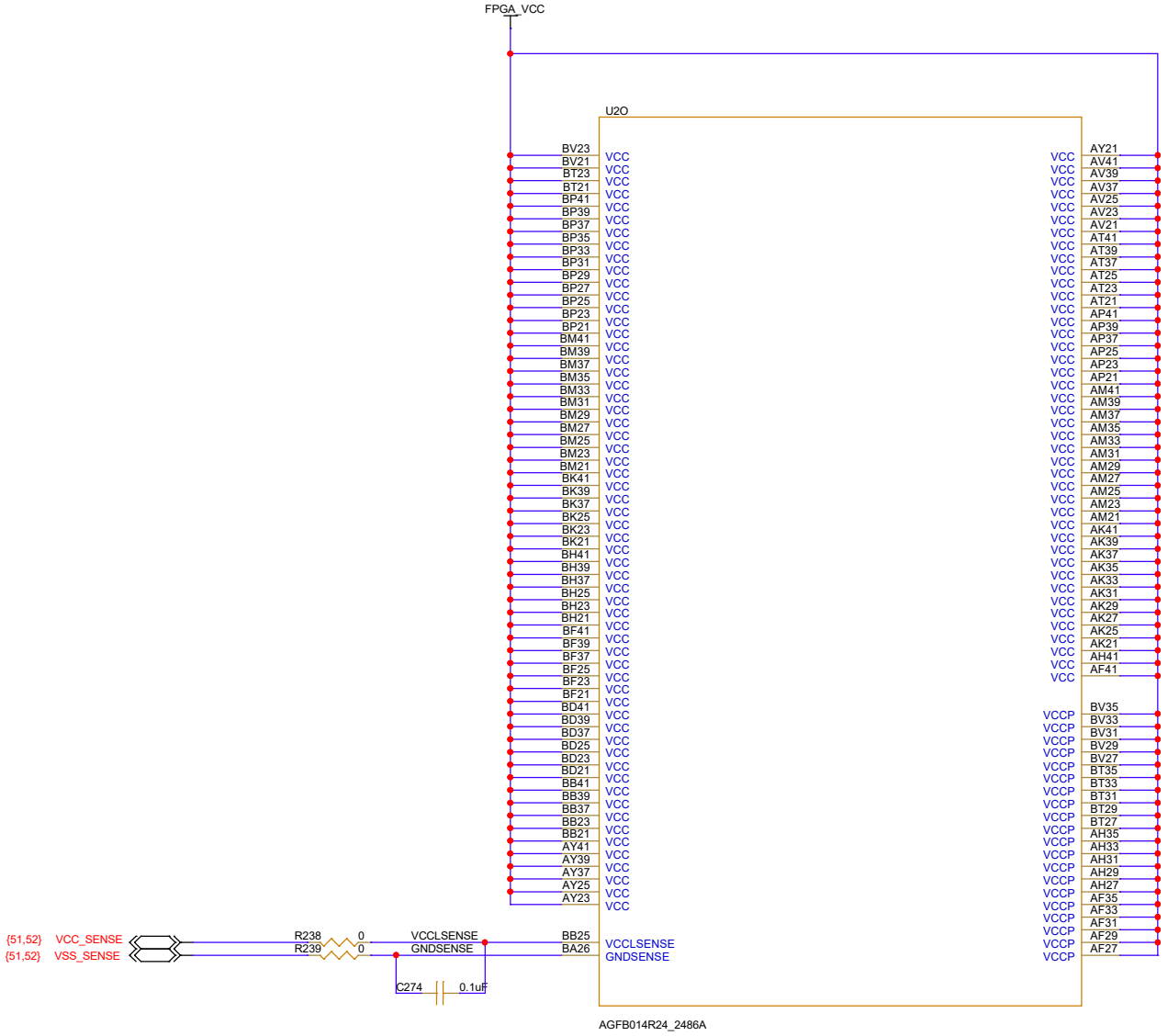
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 32 of 67

FPGA Power 1



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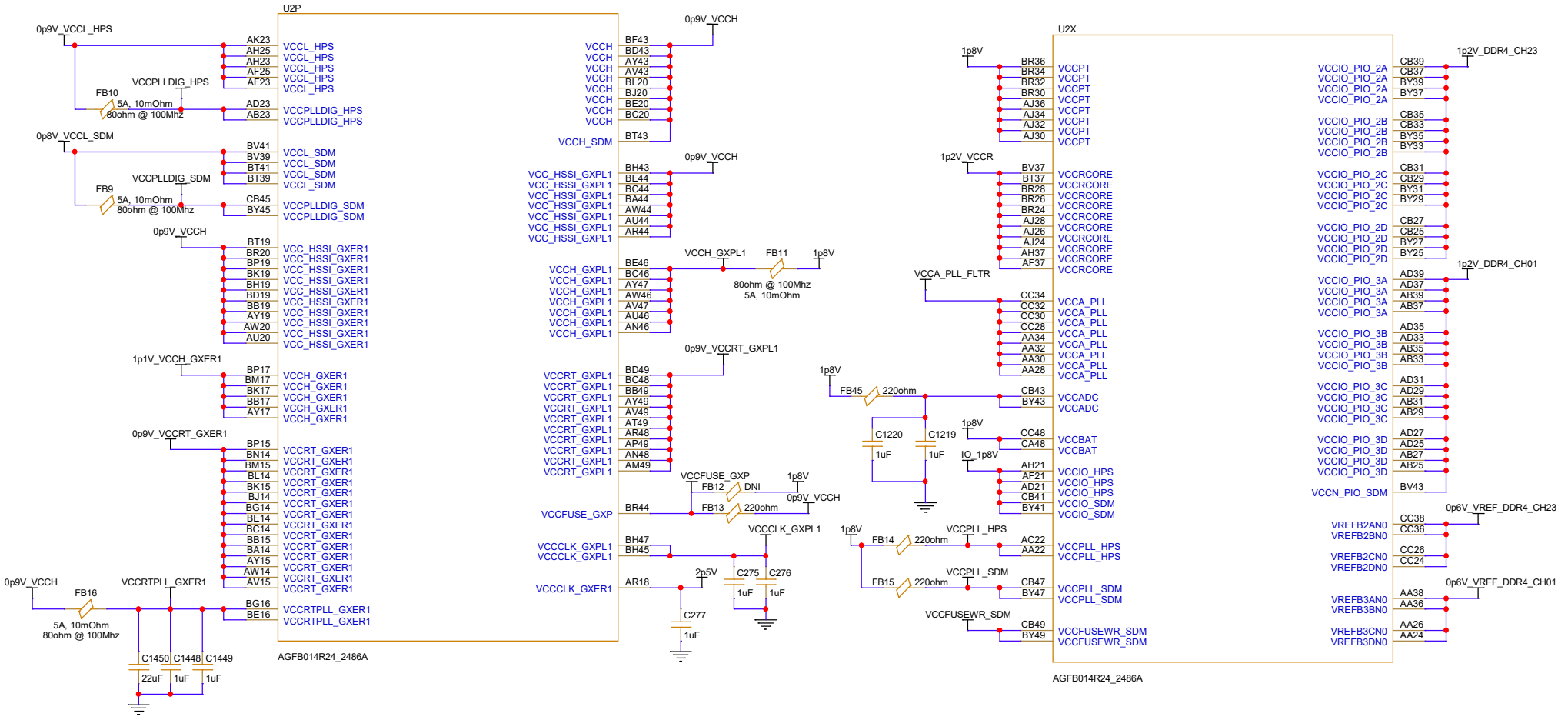
Size: B	Document Number: M75579-100(100-0330692-B1)	Rev: C1
Date: Wednesday, December 04, 2024	Sheet 33 of 67	

FPGA Power 2



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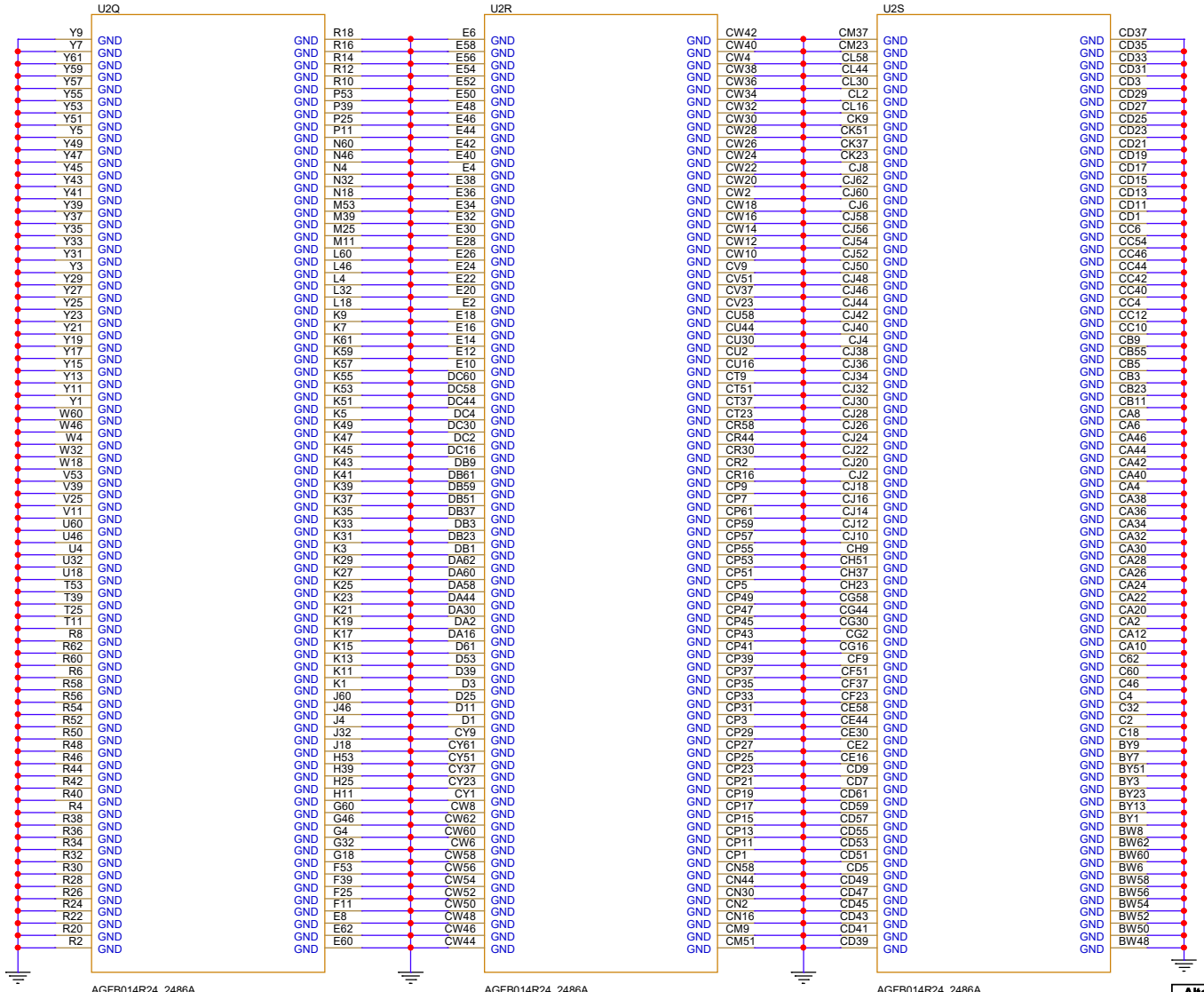
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 34 of 67

FPGA GND 1



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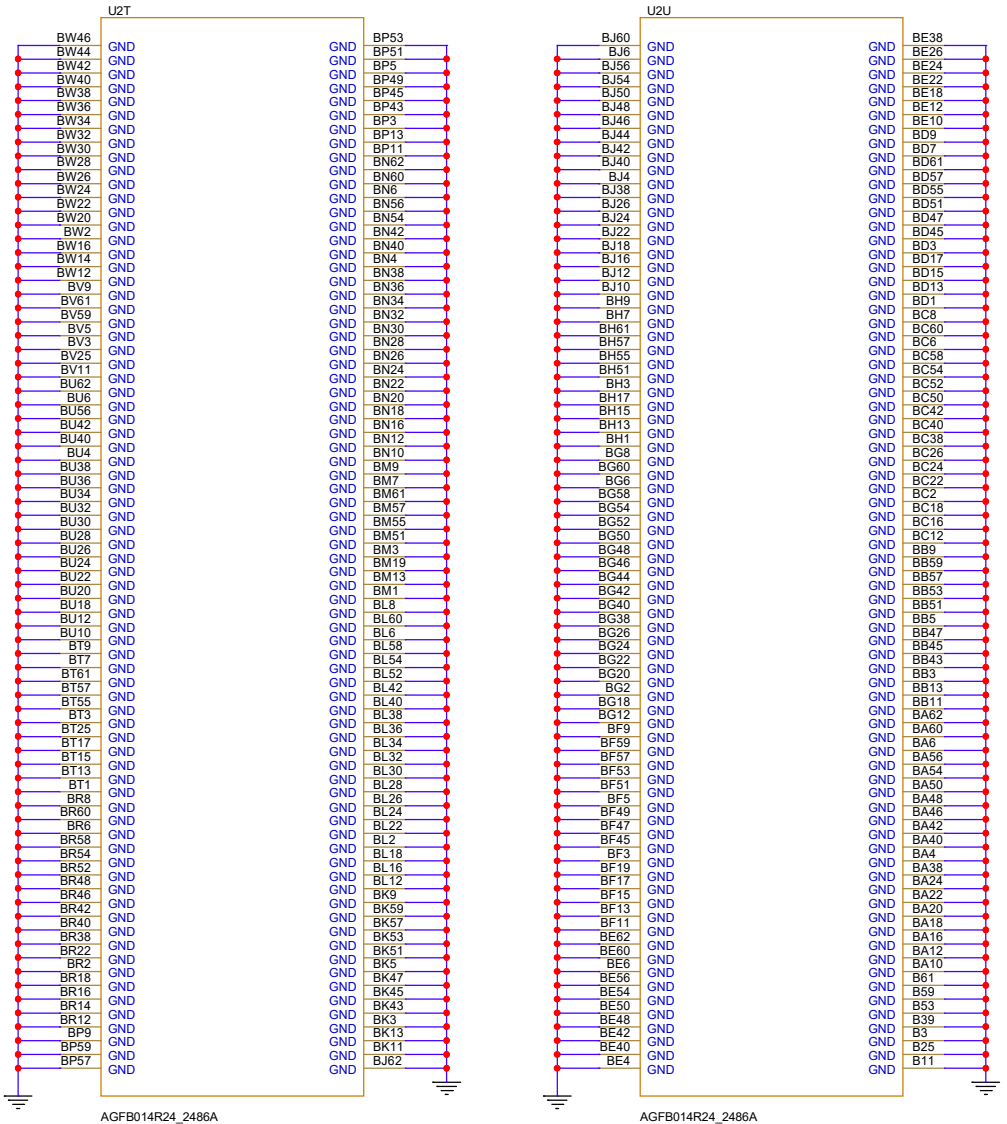
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 35 of 67

FPGA GND 2



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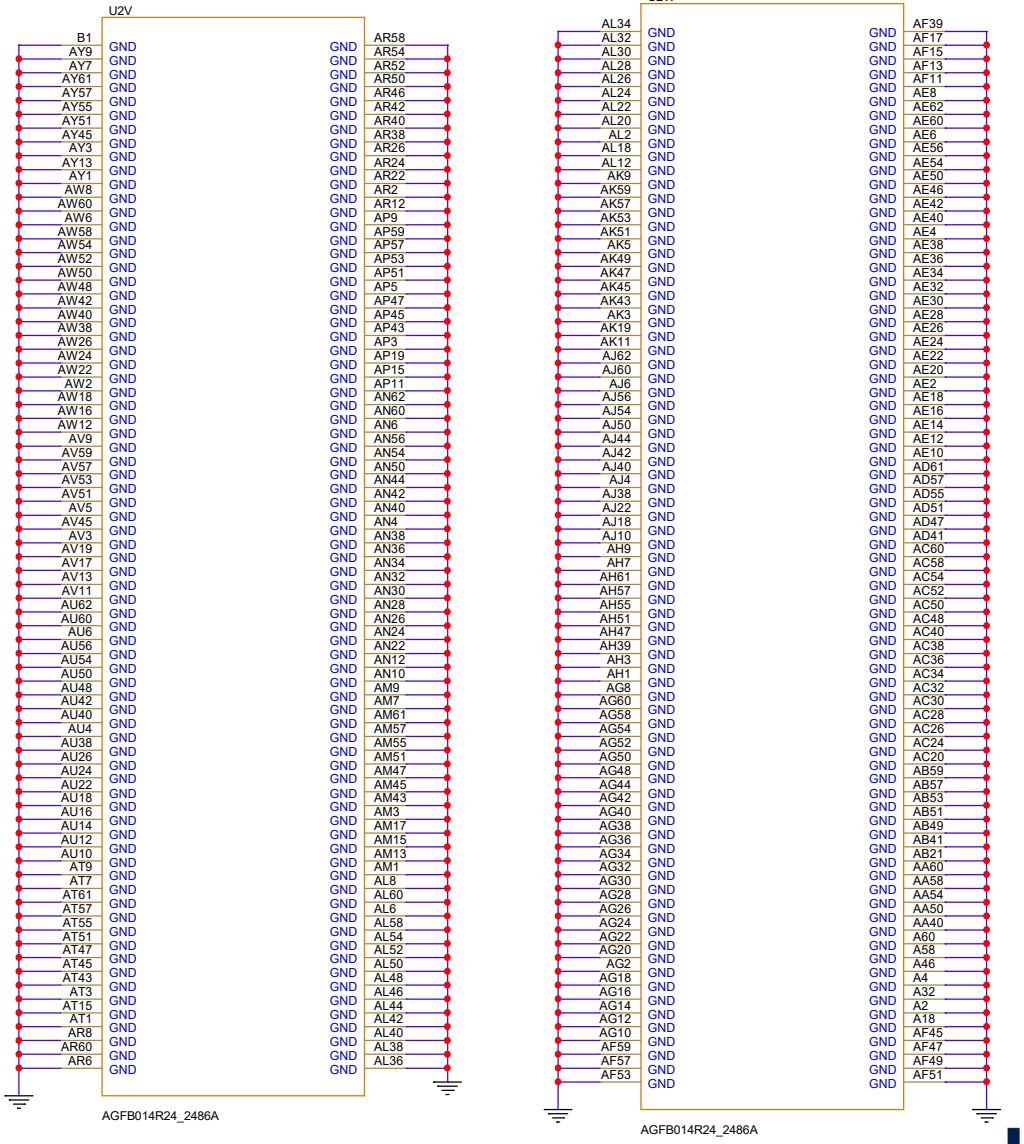
Size: B	Document Number: M75579-100(100-0330692-B1)	Rev: C1
Date: Wednesday, December 04, 2024	Sheet 36 of 67	

FPGA GND 3



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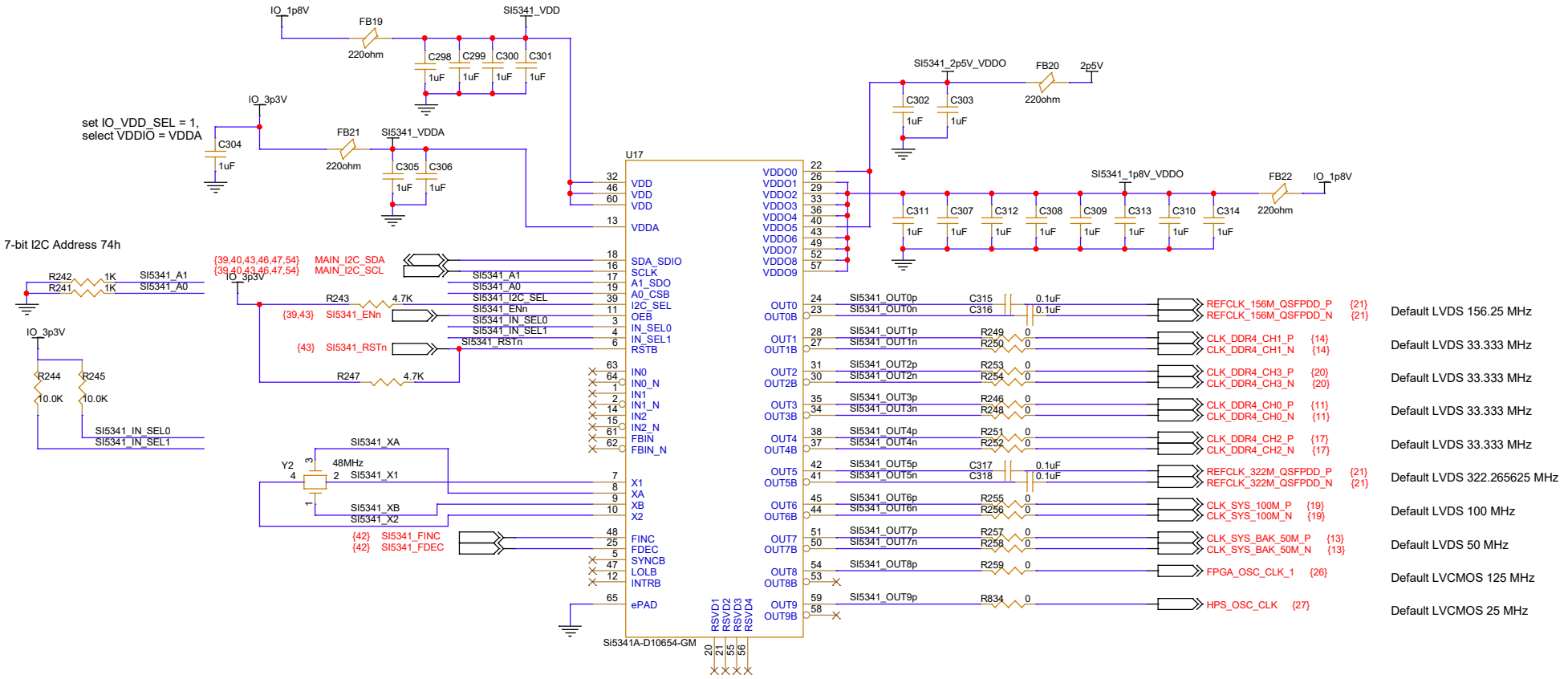
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 37 of 67

Clock 1



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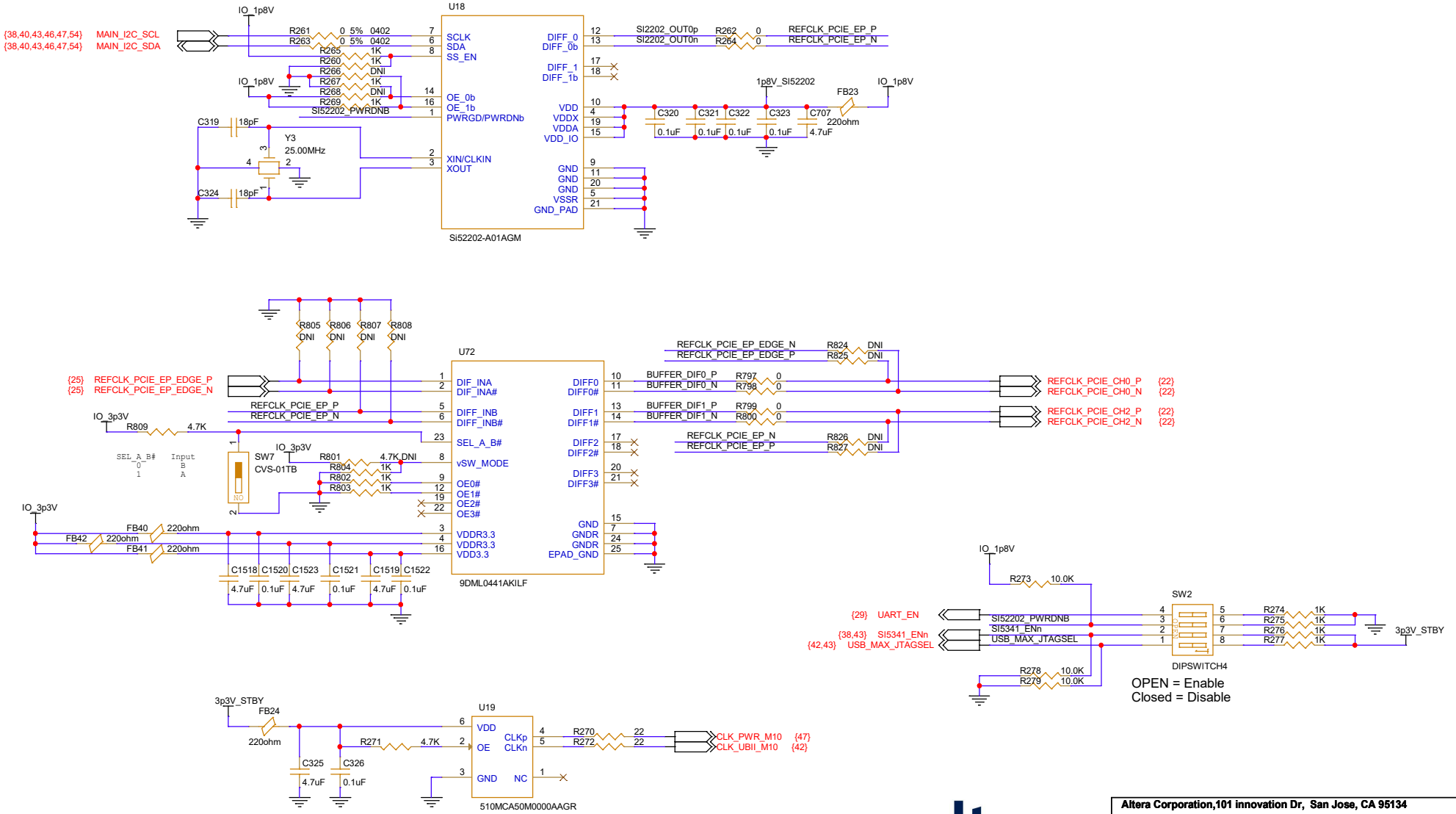
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 38 of 67

Clock 2



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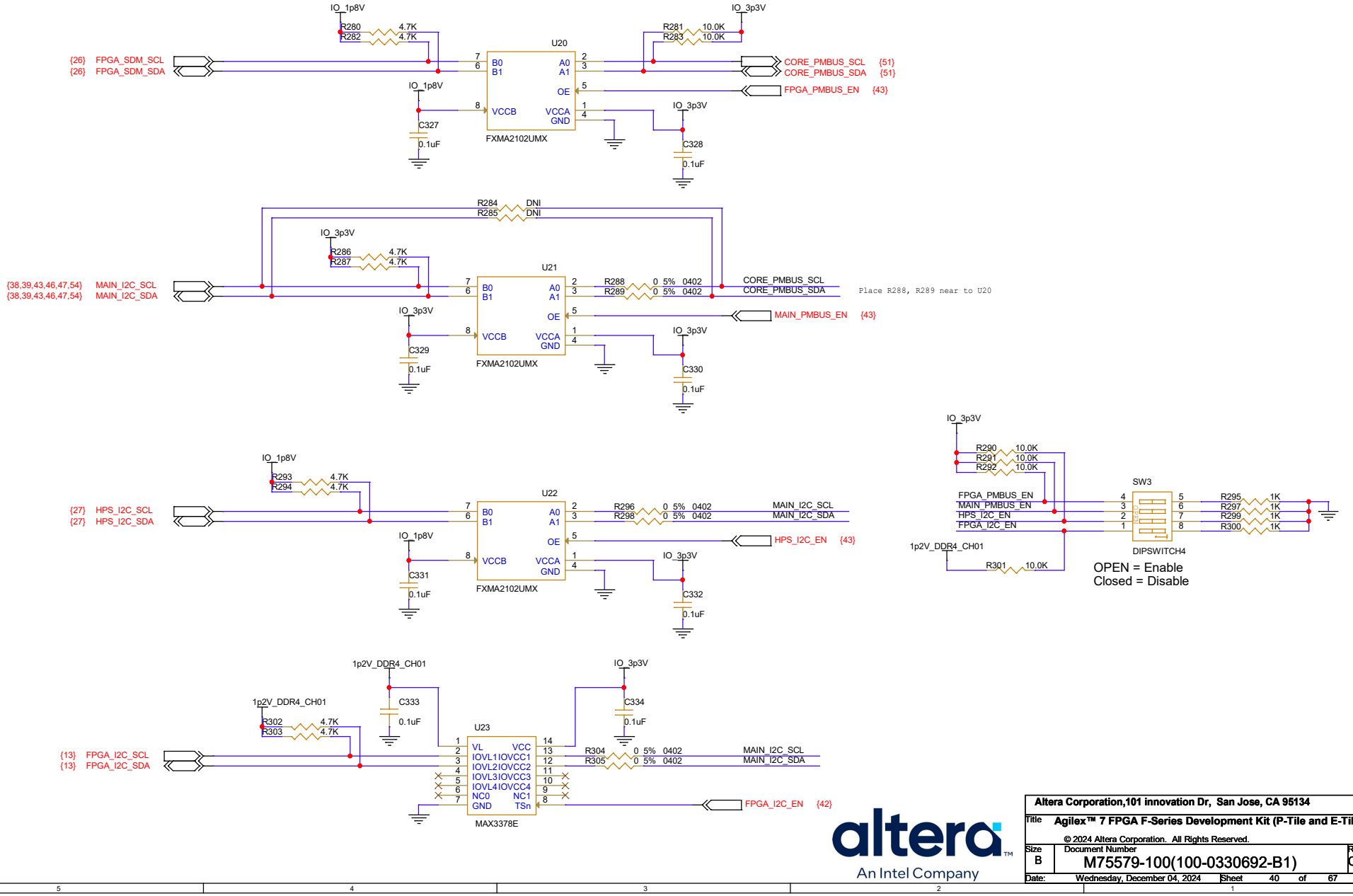
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 39 of 67

I2C And PMBUS



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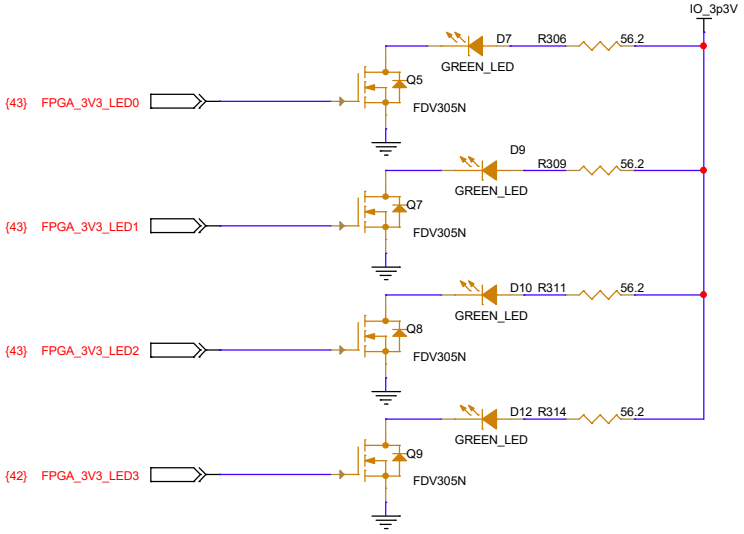
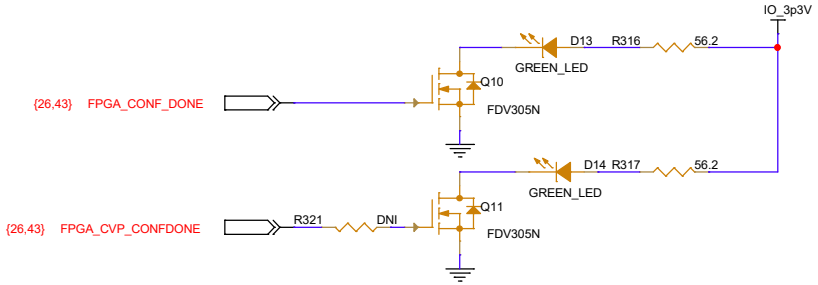
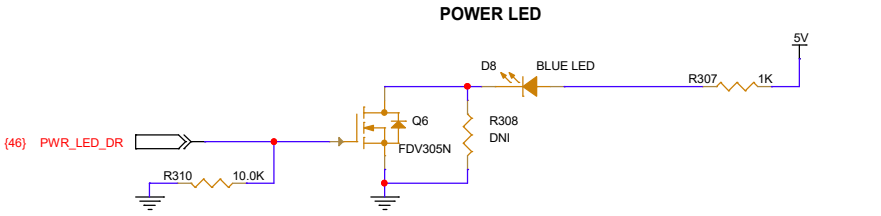
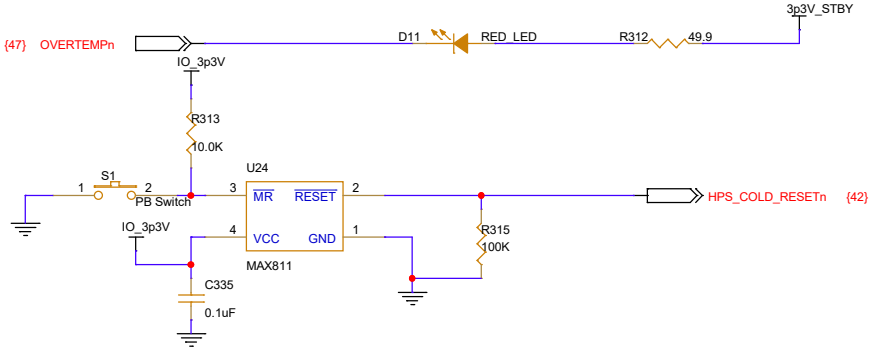
Title	Agilex™ 7 FPGA F-Series Development Kit (P-Tile and E-Tile)	
Size B	Document Number M75579-100(100-0330692-B1)	Rev C1
Date: Wednesday, December 04, 2024	Sheet 40 of 67	

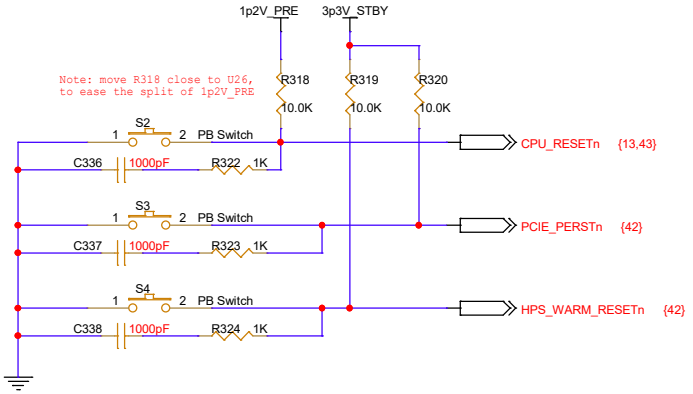
LEDs And PushButtons

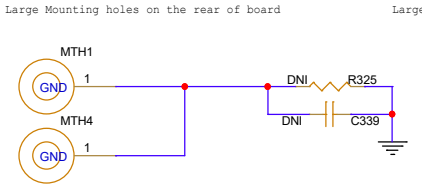


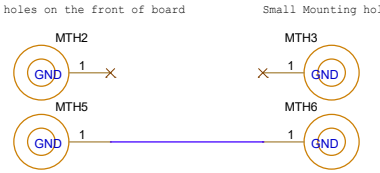












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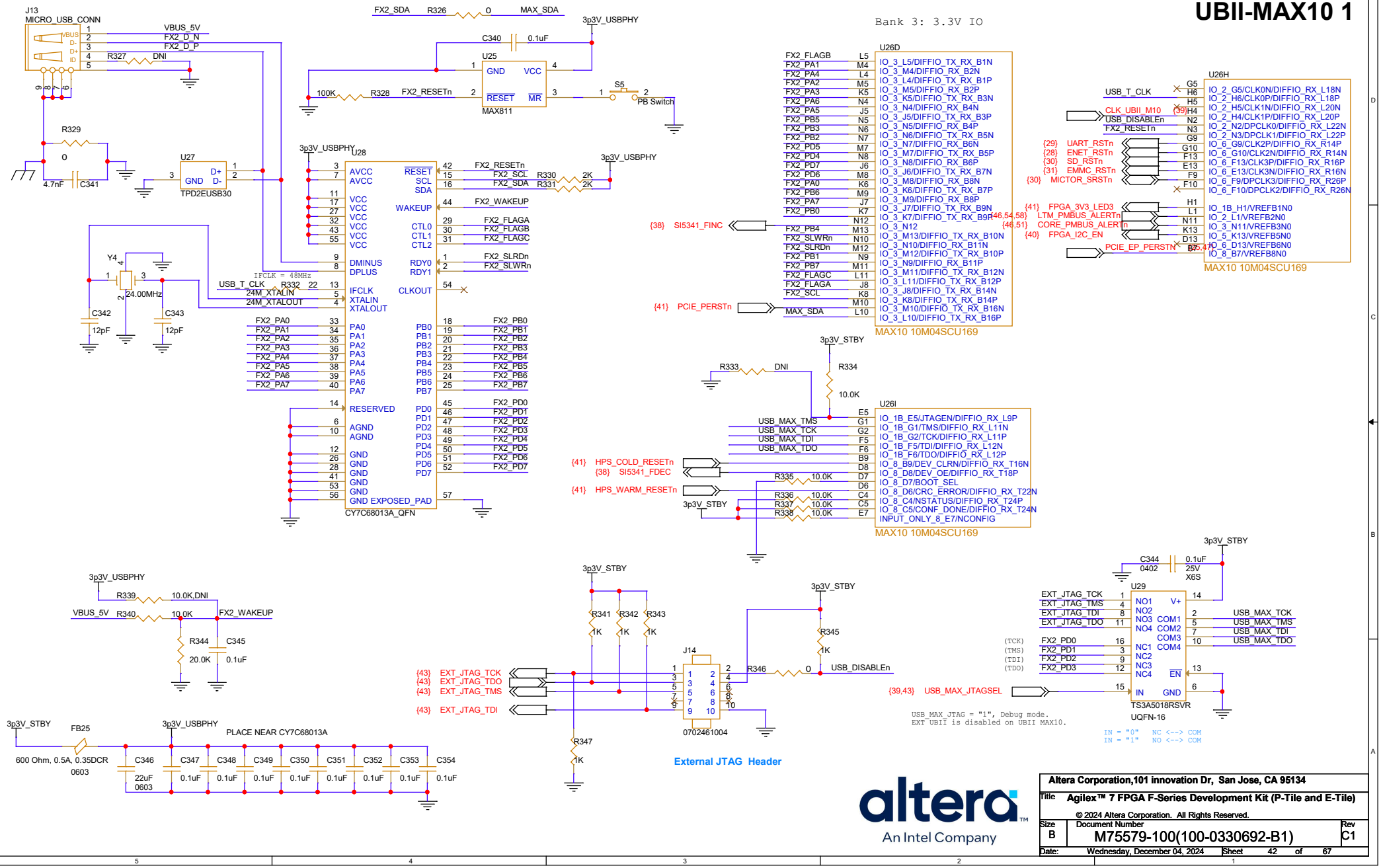
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 41 of 67

UBII-MAX10 1

Bank 3: 3.3V IO



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Size: B	Document Number: M75579-100(100-0330692-B1)	Rev: C1
Date: Wednesday, December 04, 2024	Sheet 42 of 67	

UBII-MAX10 2

Bank 5: 1.2V IO

U26E

{13} QSFPDD0_1V2_RESET_L — K10 IO_5_K10/DIFFIO_RX_R1P
{13} QSFPDD0_1V2_MODPRS_L — K11 IO_5_K11/DIFFIO_RX_R2P
{13} QSFPDD0_1V2_LPMODE — J10 IO_5_J10/DIFFIO_RX_R1N
{13} QSFPDD0_1V2_INT_L — L12 IO_5_L12/DIFFIO_RX_R2N
{13} QSFPDD1_1V2_RESET_L — K12 IO_5_K12/DIFFIO_RX_R7P
{13} QSFPDD1_1V2_MODPRS_L — L13 IO_5_L13
{13} QSFPDD1_1V2_MODSEL_L — J12 IO_5_J12/DIFFIO_RX_R7N
{13} QSFPDD1_1V2_INT_L — J9 IO_5_J9/DIFFIO_RX_R8P
{13} QSFPDD0_1V2_MODSEL_L — J13 IO_5_J13/DIFFIO_RX_R9P
{13} QSFPDD1_1V2_LPMODE — H10 IO_5_H10/DIFFIO_RX_R8N
{13,41} CPU_RESETn — H13 IO_5_H13/DIFFIO_RX_R9N
{13} FPGA_LED0 — H9 IO_5_H9/DIFFIO_RX_R10P
{13} FPGA_LED1 — G13 IO_5_G13/DIFFIO_RX_R11P
{13} FPGA_LED2 — H8 IO_5_H8/DIFFIO_RX_R10N
{13} FPGA_LED3 — G12 IO_5_G12/DIFFIO_RX_R11N

MAX10 10M04SCU169

Bank 8: 3.3V IO

U26G

{38,39,40,46,47,54} MAIN_I2C_SCL — C10 IO_8_C10/DIFFIO_RX_T14P
{38,39,40,46,47,54} MAIN_I2C_SDA — A8 IO_8_A8/DIFFIO_RX_T15P
{38,39} SI5341_ENn — C9 IO_8_C9/DIFFIO_RX_T14N
{38} SI5341_RSTn — A9 IO_8_A9/DIFFIO_RX_T15N
{23} QSFPDD0_3V3_RESET_L — B10 IO_8_B10/DIFFIO_RX_T16P
{23} QSFPDD0_3V3_MODPRS_L — A10 IO_8_A10/DIFFIO_RX_T17P
{23} QSFPDD0_3V3_LPMODE — A11 IO_8_A11/DIFFIO_RX_T17N
{23} QSFPDD0_3V3_INT_L — E8 IO_8_E8/DIFFIO_RX_T18N
{24} QSFPDD1_3V3_RESET_L — A7 IO_8_A7/DIFFIO_RX_T19P
{24} QSFPDD1_3V3_MODPRS_L — A6 IO_8_A6/DIFFIO_RX_T19N
{24} QSFPDD1_3V3_LPMODE — B6 IO_8_B6/DIFFIO_RX_T20P
{24} QSFPDD1_3V3_INT_L — A4 IO_8_A4/DIFFIO_RX_T21P
{24} QSFPDD1_3V3_MODSEL_L — B5 IO_8_B5/DIFFIO_RX_T20N
{23} QSFPDD0_3V3_MODSEL_L — A3 IO_8_A3/DIFFIO_RX_T21N
{47} PWR_MAX10_JTAG_TMS — PWR_MAX10_JTAG_TMS E6 IO_8_E6/DIFFIO_RX_T22P
{47} PWR_MAX10_JTAG_TCK — PWR_MAX10_JTAG_TCK B3 IO_8_B3/DIFFIO_RX_T23P
{25,47} PCIE_PWRBRKN — B4 IO_8_B4/DIFFIO_RX_T23N
{47} PWR_MAX10_JTAG_TDI — PWR_MAX10_JTAG_TDI A5 IO_8_A5/DIFFIO_RX_T25P
{47} PWR_MAX10_JTAG_TDO — PWR_MAX10_JTAG_TDO A2 IO_8_A2/DIFFIO_RX_T26P
{39,42} USB_MAX_JTAGSEL — B2 IO_8_B2/DIFFIO_RX_T26N

USB_MAX_JTAG = "1", Debug mode.
EXT_UBII is disabled on UBII MAX10.

MAX10 10M04SCU169

Bank 6: 1.8V IO

U26F

{30} HPS_JTAG_TCK — HPS_JTAG_TCK F12 IO_6_F12/DIFFIO_RX_R18P
{30} HPS_JTAG_TDI — HPS_JTAG_TDI E12 IO_6_E12/DIFFIO_RX_R18N
{26,41} FPGA_CVP_CONFDONE — C13 IO_6_C13
{26,41} FPGA_CONF_DONE — F8 IO_6_F8/DIFFIO_RX_R27P
{26} FPGA_INIT_DONE — B12 IO_6_B12/DIFFIO_RX_R28P
{26} FPGA_NCONFIG — E9 IO_6_E9/DIFFIO_RX_R27N
{30} HPS_JTAG_TMS — HPS_JTAG_TMS B11 IO_6_B11/DIFFIO_RX_R28N
{30} HPS_JTAG_TDO — HPS_JTAG_TDO C12 IO_6_C12/DIFFIO_RX_R29P
{26} HPS_RESETn — R354 0 B13 IO_6_B13/DIFFIO_RX_R30P
{26} FPGA_JTAG_TCK — FPGA_JTAG_TCK C11 IO_6_C11/DIFFIO_RX_R29N
{26} FPGA_JTAG_TDI — FPGA_JTAG_TDI A12 IO_6_A12/DIFFIO_RX_R30N
{26} FPGA_JTAG_TMS — FPGA_JTAG_TMS E10 IO_6_E10/DIFFIO_RX_R31P
{27} RSV_SD_RESETn — D9 IO_6_D9/DIFFIO_RX_R31N
{22} FPGA_PCIE_PERSTn — R357 0 D12 IO_6_D12/DIFFIO_RX_R33P
{26} FPGA_JTAG_TDO — FPGA_JTAG_TDO D11 IO_6_D11/DIFFIO_RX_R33N

MAX10 10M04SCU169

Bank 2: 3.3V IO

U26C

JTAG_INPUT_SOURCE — M3 IO_2_M3/PLL_L_CLKOUTN/DIFFIO_RX_L27N
{42} EXT_JTAG_TDI — EXT_JTAG_TDI L3 IO_2_L3/PLL_L_CLKOUTP/DIFFIO_RX_L27P
{42} EXT_JTAG_TCK — EXT_JTAG_TCK J1 IO_2_J1/DIFFIO_RX_L19N
PWR_MAX10_BYPASSn J2 IO_2_J2/DIFFIO_RX_L19P
{42} EXT_JTAG_TMS — EXT_JTAG_TMS M1 IO_2_M1/DIFFIO_RX_L21N
MICTOR_BYPASSn M2 IO_2_M2/DIFFIO_RX_L21P
L2 IO_2_L2
{25} PCIE_EP_3V3_I2C_SDA — K1 IO_2_K1/DIFFIO_RX_L28N
{25} PCIE_EP_3V3_I2C_SCL — K2 IO_2_K2/DIFFIO_RX_L28P
{42} EXT_JTAG_TDO — EXT_JTAG_TDO

MAX10 10M04SCU169

Bank 1A/1B: 3.3V IO

U26B

{41} FPGA_3V3_LED0 — D1 IO_1A_D1/DIFFIO_RX_L1N
{41} FPGA_3V3_LED1 — C2 IO_1A_C2/DIFFIO_RX_L1P
{25} PCIE_EP_JTAG_TCK — PCIE_EP_JTAG_TCK E3 IO_1A_E3/DIFFIO_RX_L3N
FPGA_BYPASSn E4 IO_1A_E4/DIFFIO_RX_L3P
{25} PCIE_EP_JTAG_TMS — PCIE_EP_JTAG_TMS C1 IO_1A_C1/DIFFIO_RX_L5N
{41} FPGA_3V3_LED2 — B1 IO_1A_B1/DIFFIO_RX_L5P
{25} PCIE_EP_JTAG_TDI — PCIE_EP_JTAG_TDI F1 IO_1A_F1/DIFFIO_RX_L7N
{46} PWR_GOOD — PWR_GOOD E1 IO_1A_E1/DIFFIO_RX_L7P
{25} PCIE_EP_JTAG_TDO — PCIE_EP_JTAG_TDO F4 IO_1B_F4/DIFFIO_RX_L14N
{40} FPGA_PMBUS_EN — G4 IO_1B_G4/DIFFIO_RX_L14P
{40} MAIN_PMBUS_EN — H2 IO_1B_H2/DIFFIO_RX_L16N
{40} HPS_I2C_EN — H3 IO_1B_H3/DIFFIO_RX_L16P

MAX10 10M04SCU169

U26J

A1 GND__A1
A13 GND__A13
B8 GND__B8
C3 GND__C3
D2 GND__D2
D5 GND__D5
E11 GND__E11
E2 GND__E2
F3 GND__F3
G7 GND__G7
H12 GND__H12
J4 GND__J4
L9 GND__L9
M6 GND__M6
N1 GND__N1
N13 GND__N13

MAX10 10M04SCU169

U26A

3p3V_STBY — F2 VCCIO1A__F2
G3 VCCIO1B__G3
K3 VCCIO2__K3
J3 VCCIO2__J3
L8 VCCIO3__L8
L7 VCCIO3__L7
L6 VCCIO3__L6
1p2V_PRE — J11 VCCIO5__J11
1p8V_PRE — 0603 — FB26 600 Ohm, 0.5A, 0.35DCR — 1p8V_UBII — 1p2V_UBII — H11 VCCIO5__H11
FB27 0603 600 Ohm, 0.5A, 0.35DCR — G11 VCCIO6__G11
F11 VCCIO6__F11
C8 VCCIO8__C8
C7 VCCIO8__C7
UBII_M10_VCCA — C6 VCCIO8__C6
3p3V_STBY — FB28 — D3 VCCA3__D3
600 Ohm, 0.5A, 0.35DCR — K4 VCCA1__K4
0603 — C380 10uF — C381 0.1uF — D10 VCCA2__D10
D4 VCCA3__D4
3p3V_STBY — K9 VCCA4__K9
H7 VCC_ONE__H7
G8 VCC_ONE__G8
G6 VCC_ONE__G6
F7 VCC_ONE__F7

MAX10 10M04SCU169

3p3V_STBY

R348 1K R349 1K R350 1K R351 1K

JTAG_INPUT_SOURCE
PWR_MAX10_BYPASSn
MICTOR_BYPASSn
FPGA_BYPASSn

SW4 — 1 2 3 4 — 8 7 6 5 — TDA04H0SB1

JTAG Master Selection:
USB_DISABLEn = 0: External JTAG
USB_DISABLEn = 1: On-Board UBII/PCIe EP Edge
JTAG_INPUT_SOURCE = 0: PCIe EP edge
JTAG_INPUT_SOURCE = 1: On-Board UBII

JTAG Chain:
SW4_2/3/4 = Low : Bypass
SW4_2/3/4 = High: Enable

3p3V_STBY

PWR_MAX10_JTAG_TMS R352 1K
PWR_MAX10_JTAG_TDI R353 1K
PWR_MAX10_JTAG_TCK R355 1K
PWR_GOOD R356 1K

Place R808~R810 near to U30

DNI C1525 10.0K DNI R831 EXT_JTAG_TCK

DNI C355 10.0K DNI R358 PCIE_EP_JTAG_TCK

R359 1K

PLACE CLOSE MAX II PWR PIN

3p3V_STBY — C356 10uF — C357 C358 C359 C360 C361 C362 C363 C364 C365 C366 C367 C708 0.1uF

1p8V_UBII — 1p2V_UBII

3p3V_STBY — C368 10uF — C369 C370 C371 C372 C373 C374 C375 C376 C377 C378 C379 0.1uF

UBII_M10_VCCA

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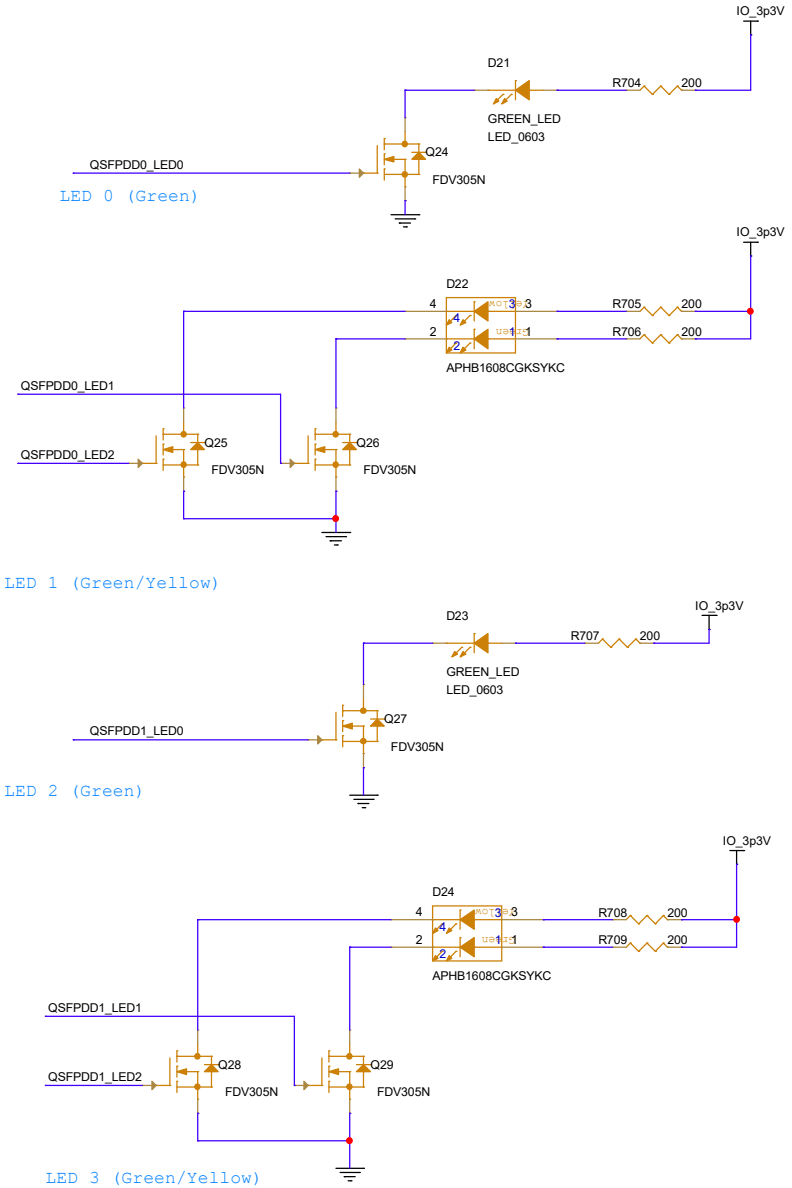
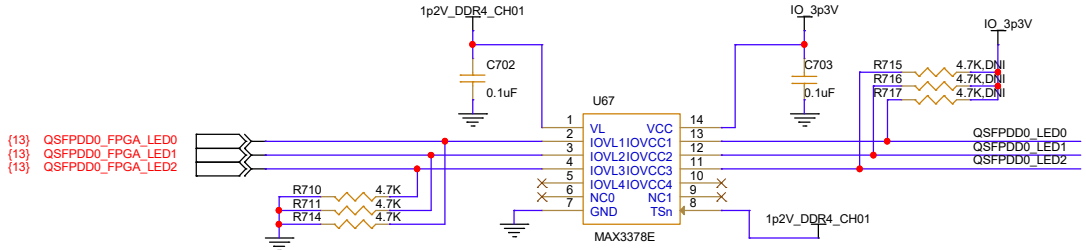
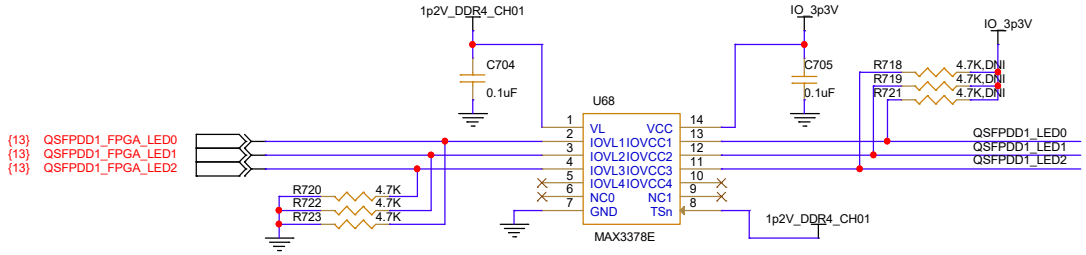
Title: Agilex™ 7 FPGA F-Series Development Kit (P-Tile and E-Tile)

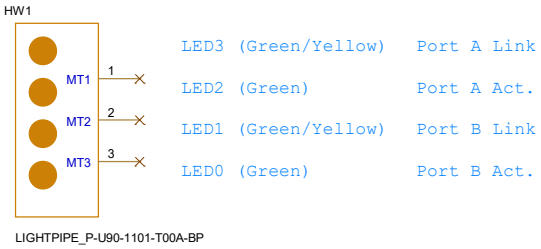
Size: B
Document Number: M75579-100(100-0330692-B1)
Rev: C1
Date: Wednesday, December 04, 2024
Sheet 43 of 67

QSFPDD LED









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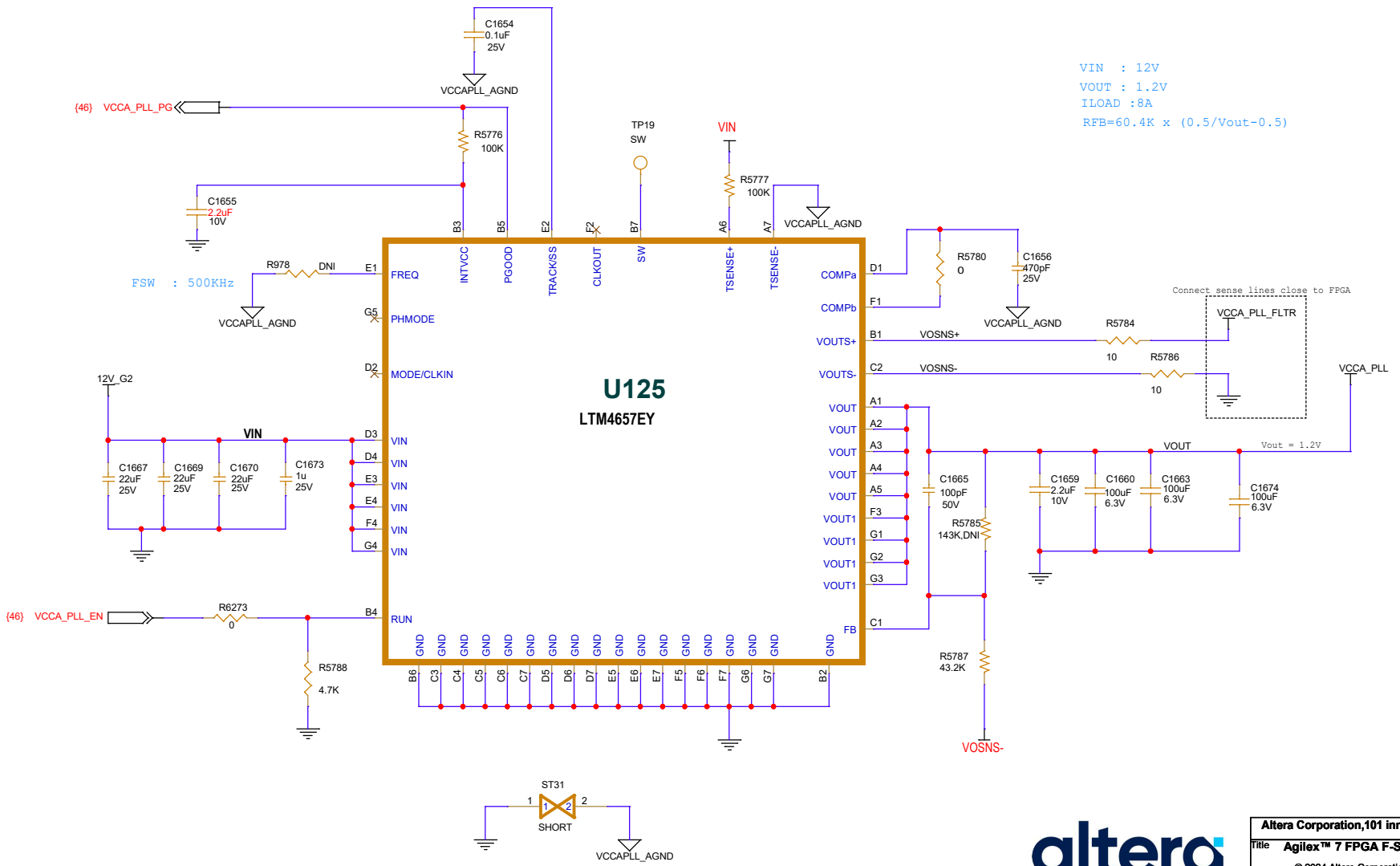
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 44 of 67

PWR - VCCA_PLL



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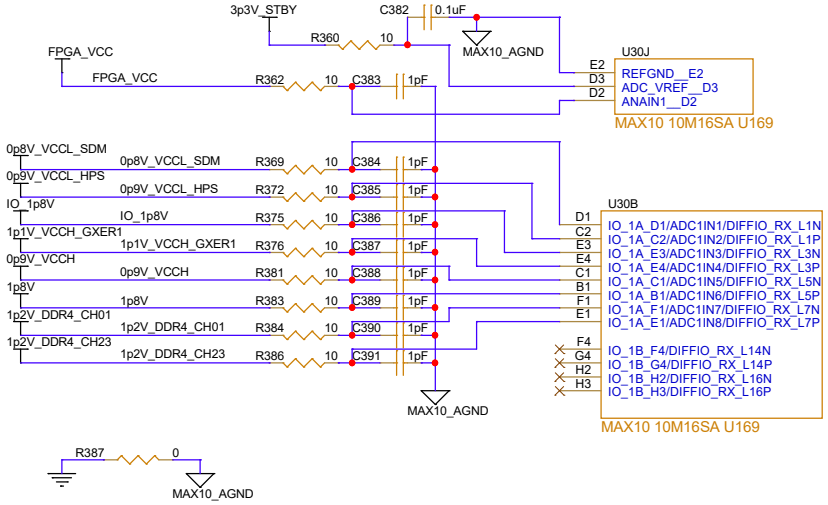
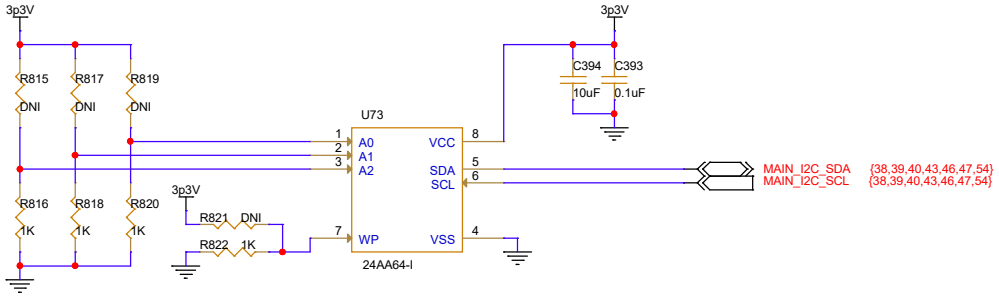
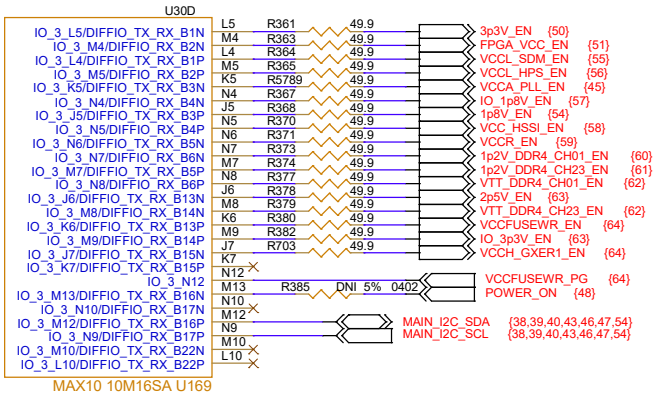
Size: B	Document Number: M75579-100(100-0330692-B1) Rev: C1
Date: Wednesday, December 04, 2024	Sheet 45 of 67

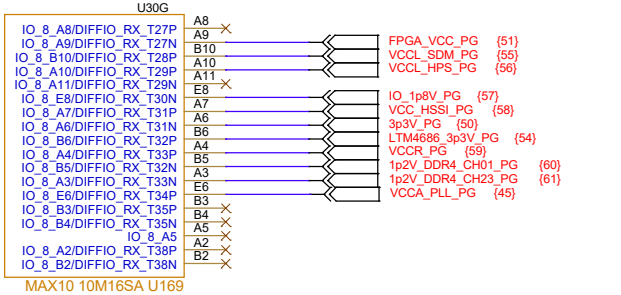
MAX® 10 PWR Manager 1

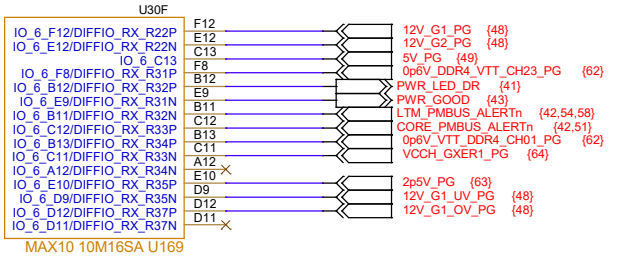




I2C Address = b'1010000'







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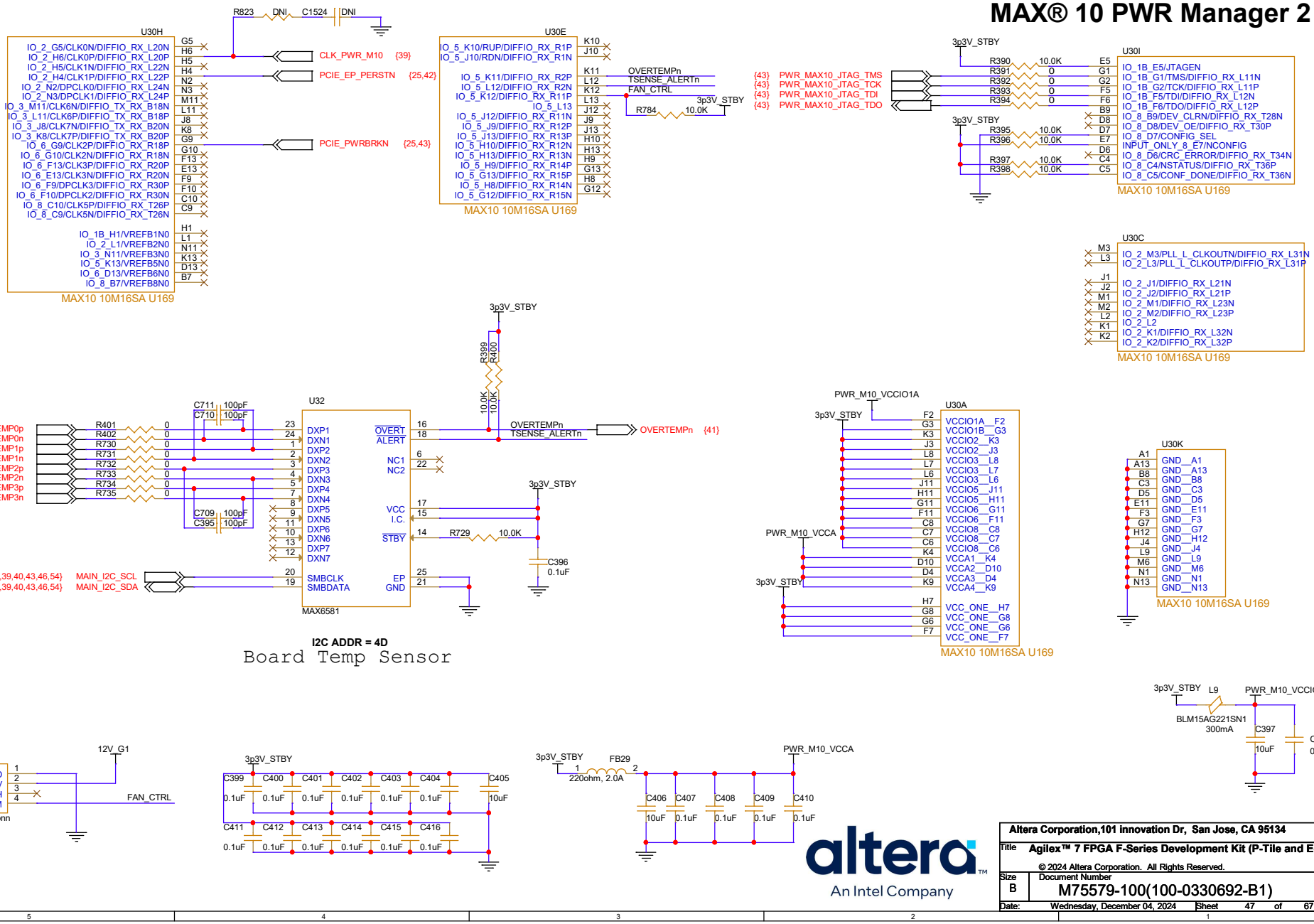
Size: B	Document Number: M75579-100(100-0330692-B1)	Rev: C1
Date: Wednesday, December 04, 2024	Sheet 46 of 67	

MAX® 10 PWR Manager 2



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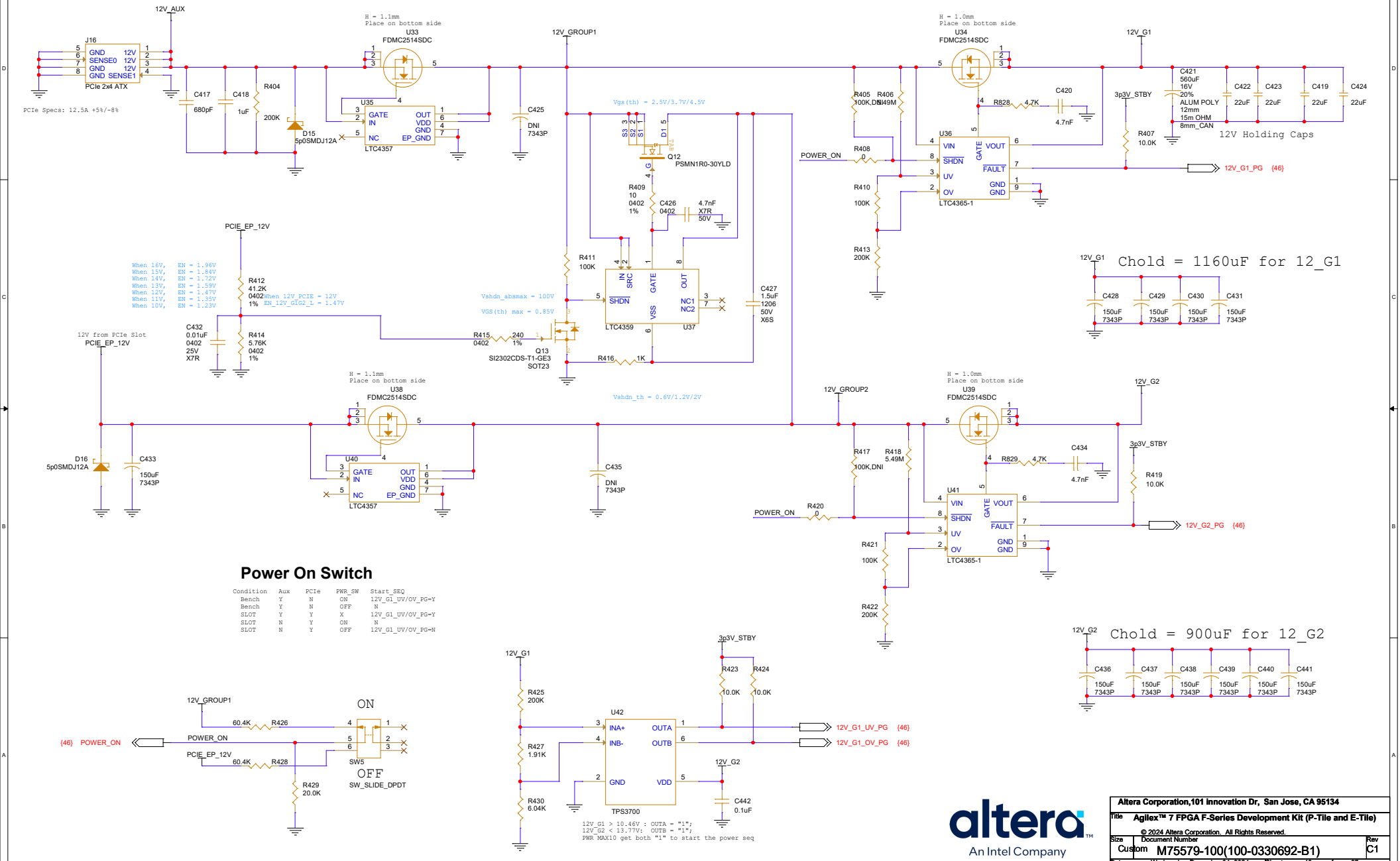
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 47 of 67

Power - Select Power Input



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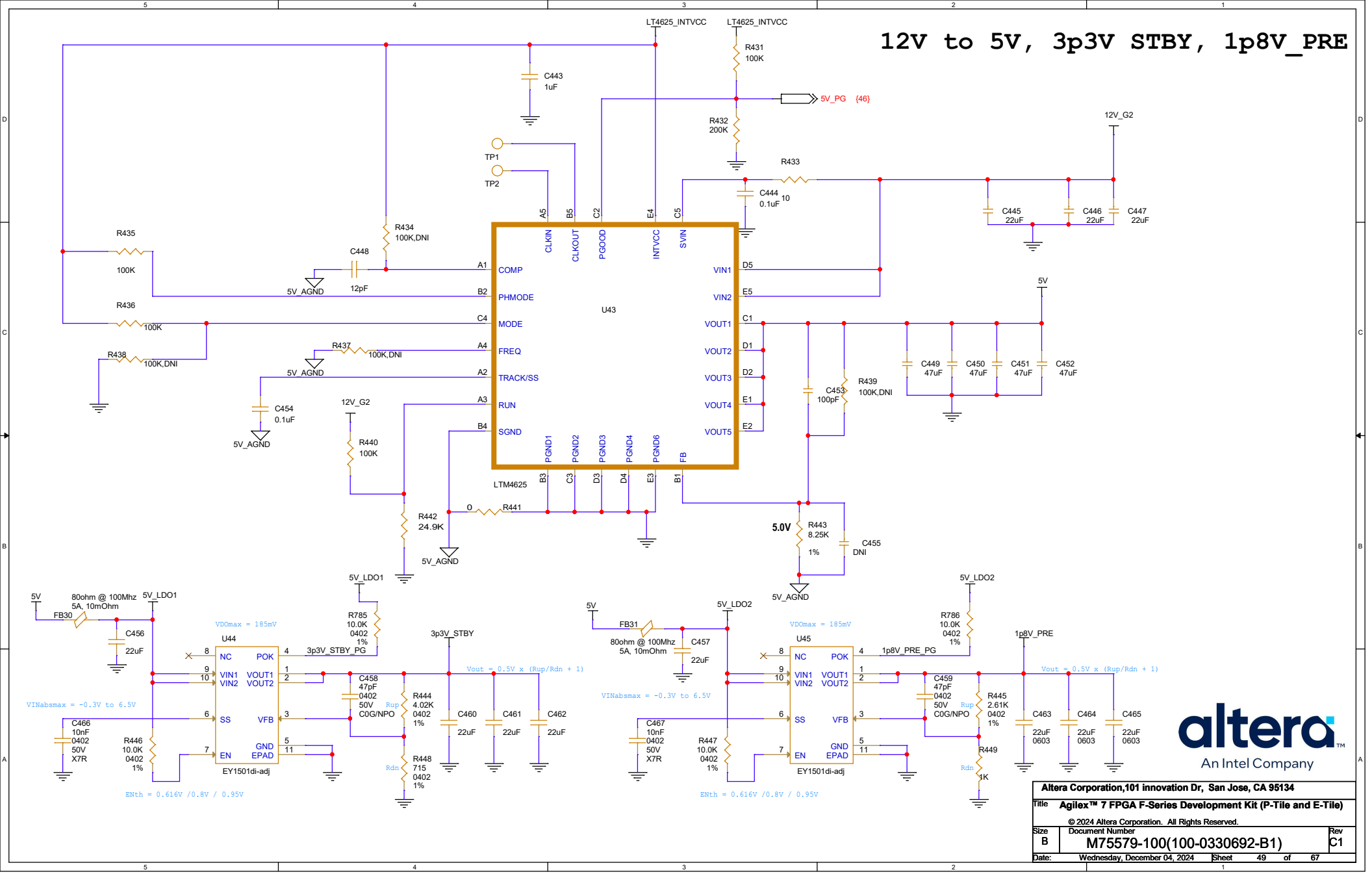
Size	Document Number	Rev
Custom	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 48 of 67

12V to 5V, 3p3V STBY, 1p8V_PRE



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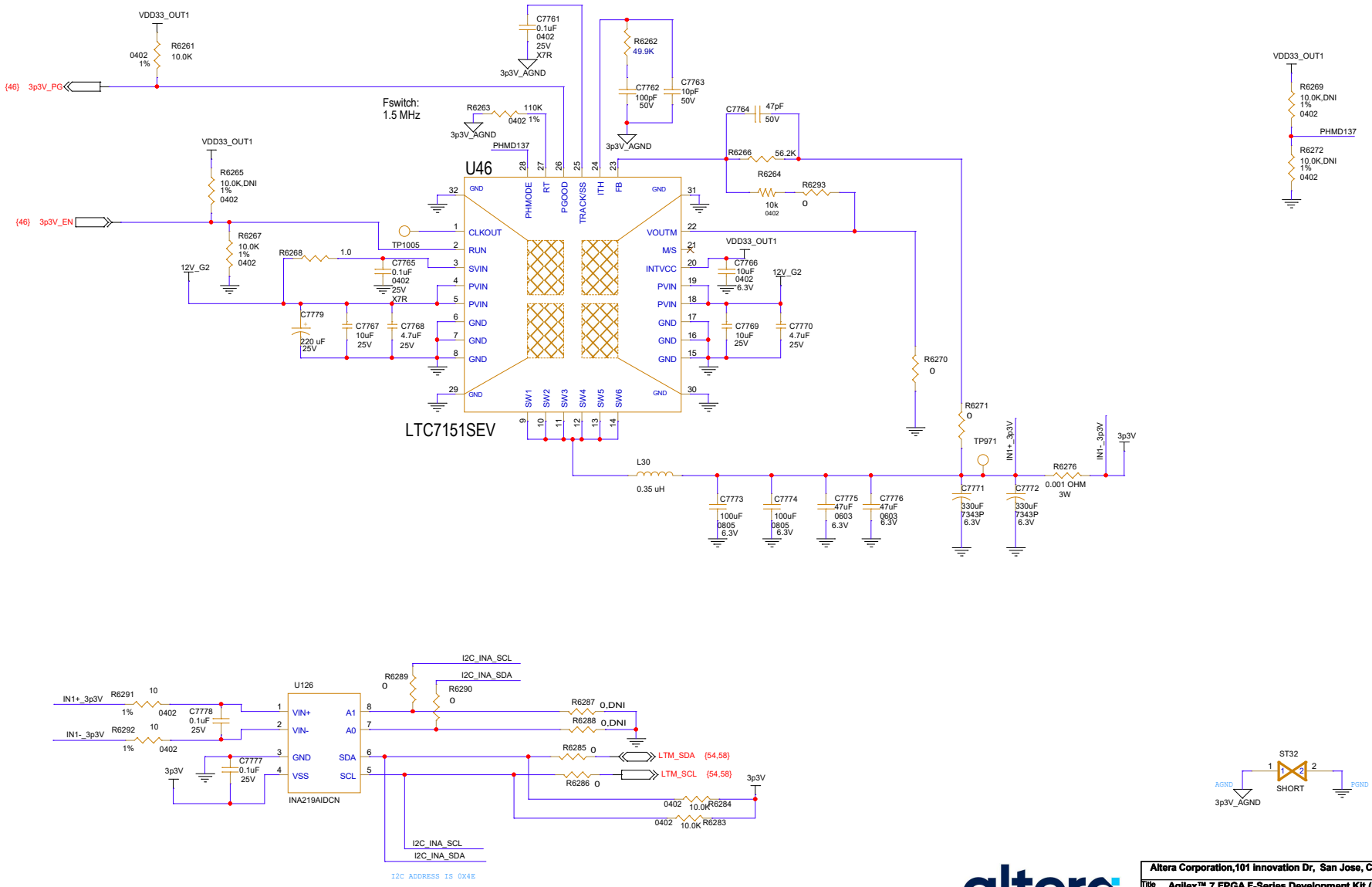
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 49 of 67

MAIN 12V to 3.3V



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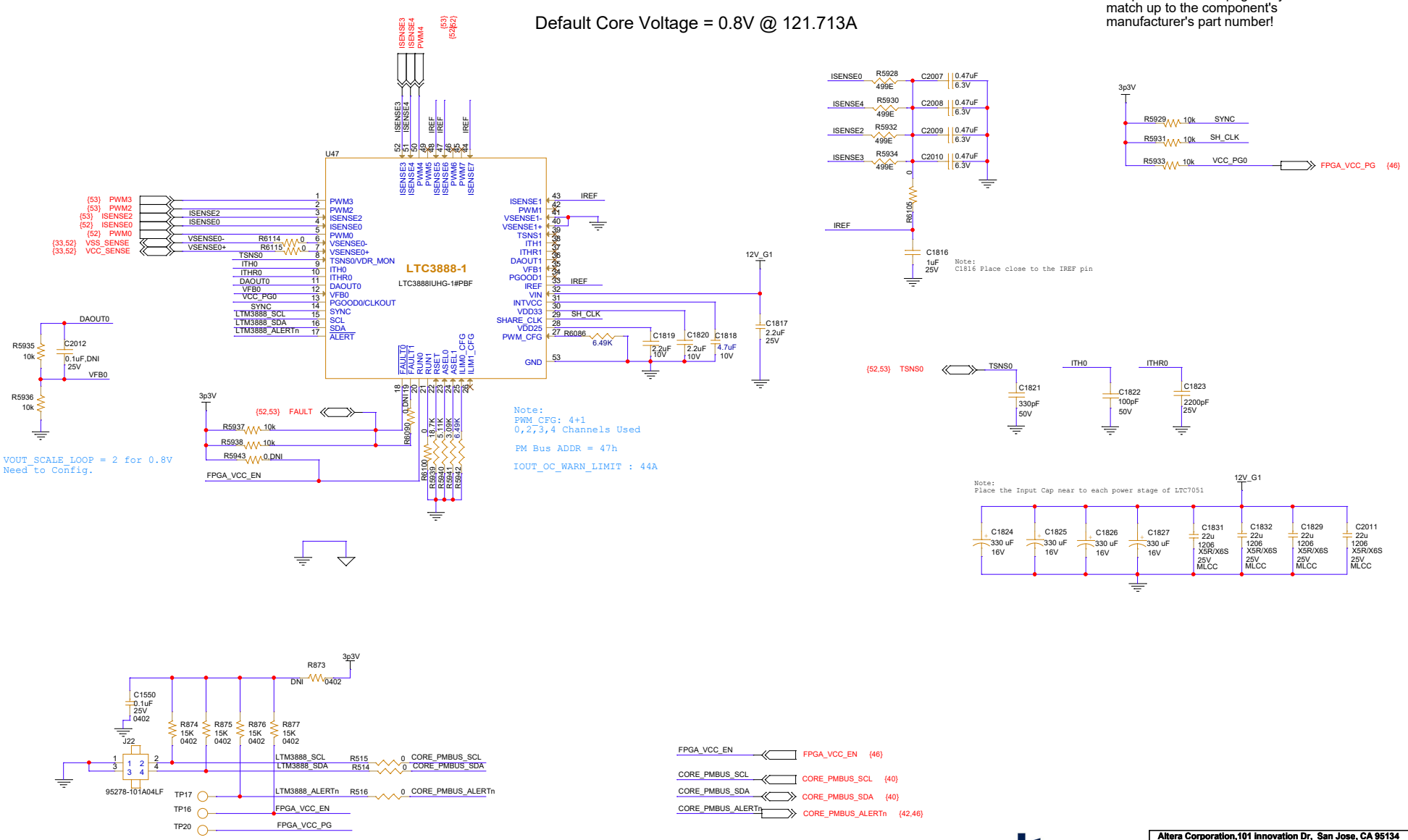
Size	Document Number	Rev
Custom	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 50 of 67

VCC Core Controller

Default Core Voltage = 0.8V @ 121.713A

NOTE: Part Attributes of components on this page may not match up to the component's manufacturer's part number!



Note: J22 part modified as 2*2 Vertical connector

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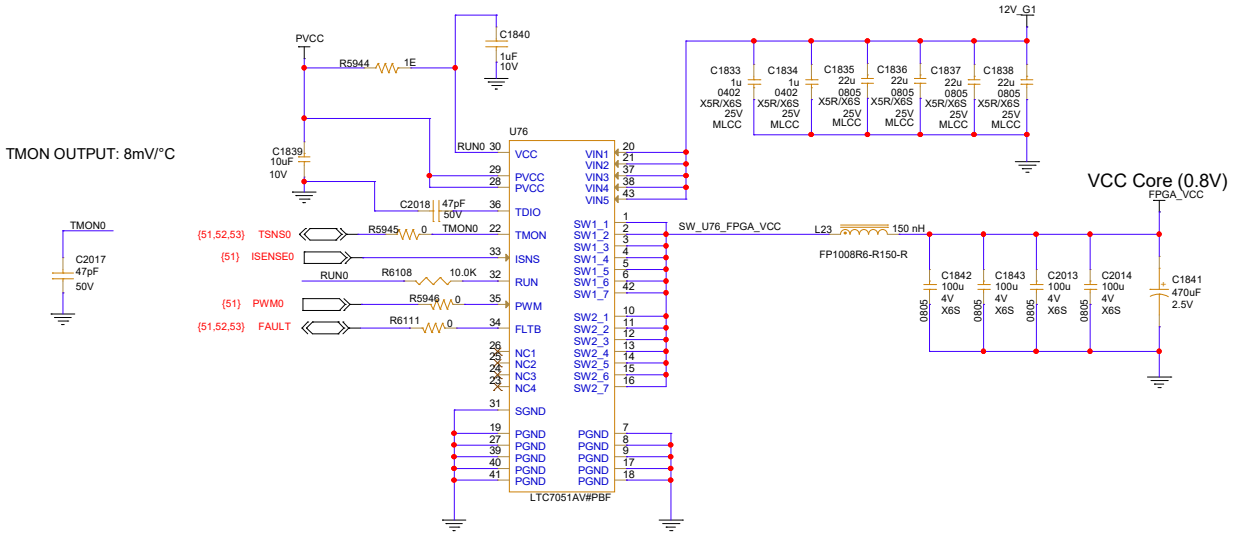
Size: Custom | Document Number: M75579-100(100-0330692-B1) | Rev: C1

Date: Wednesday, December 04, 2024 | Sheet 51 of 67

VCC Core Phase 1 - 2

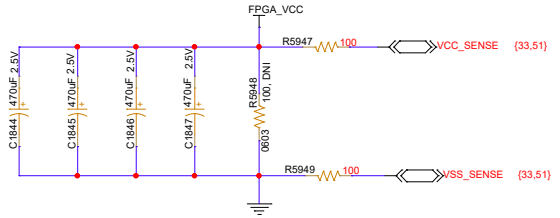
NOTE: Part Attributes of components on this page may not match up to the component's manufacturer's part number!

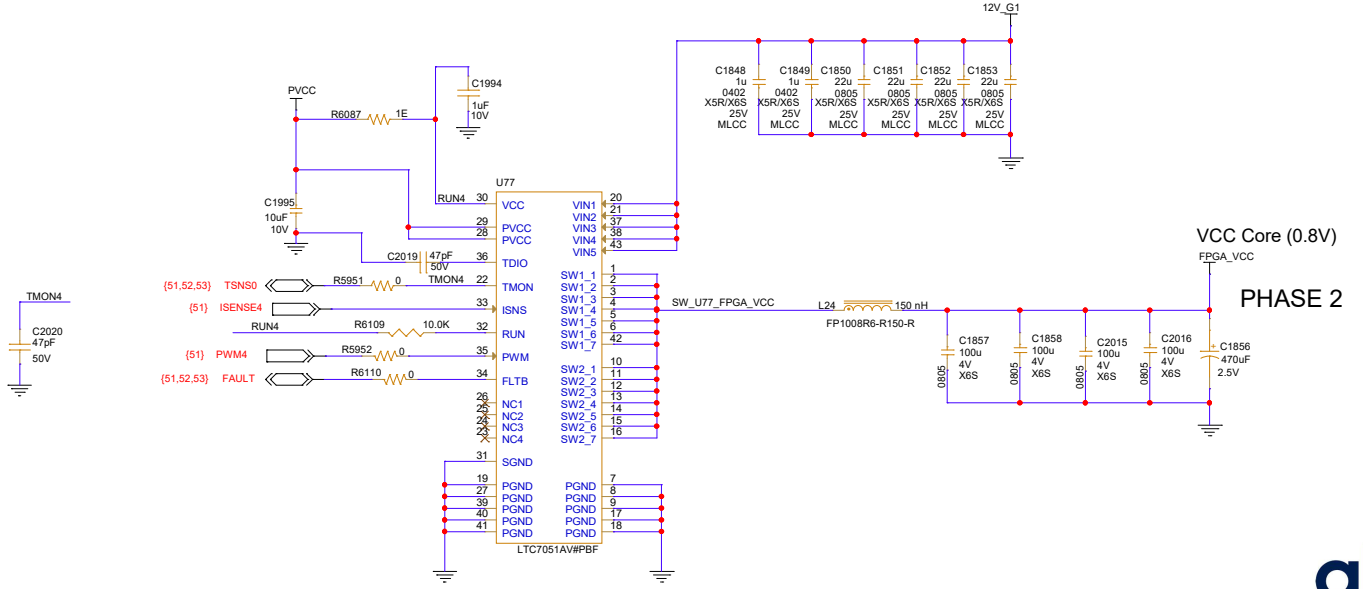
TMON OUTPUT: 8mV/°C



PHASE 1

FPGA_VCC = 0.8V @ 121.713A





PHASE 2

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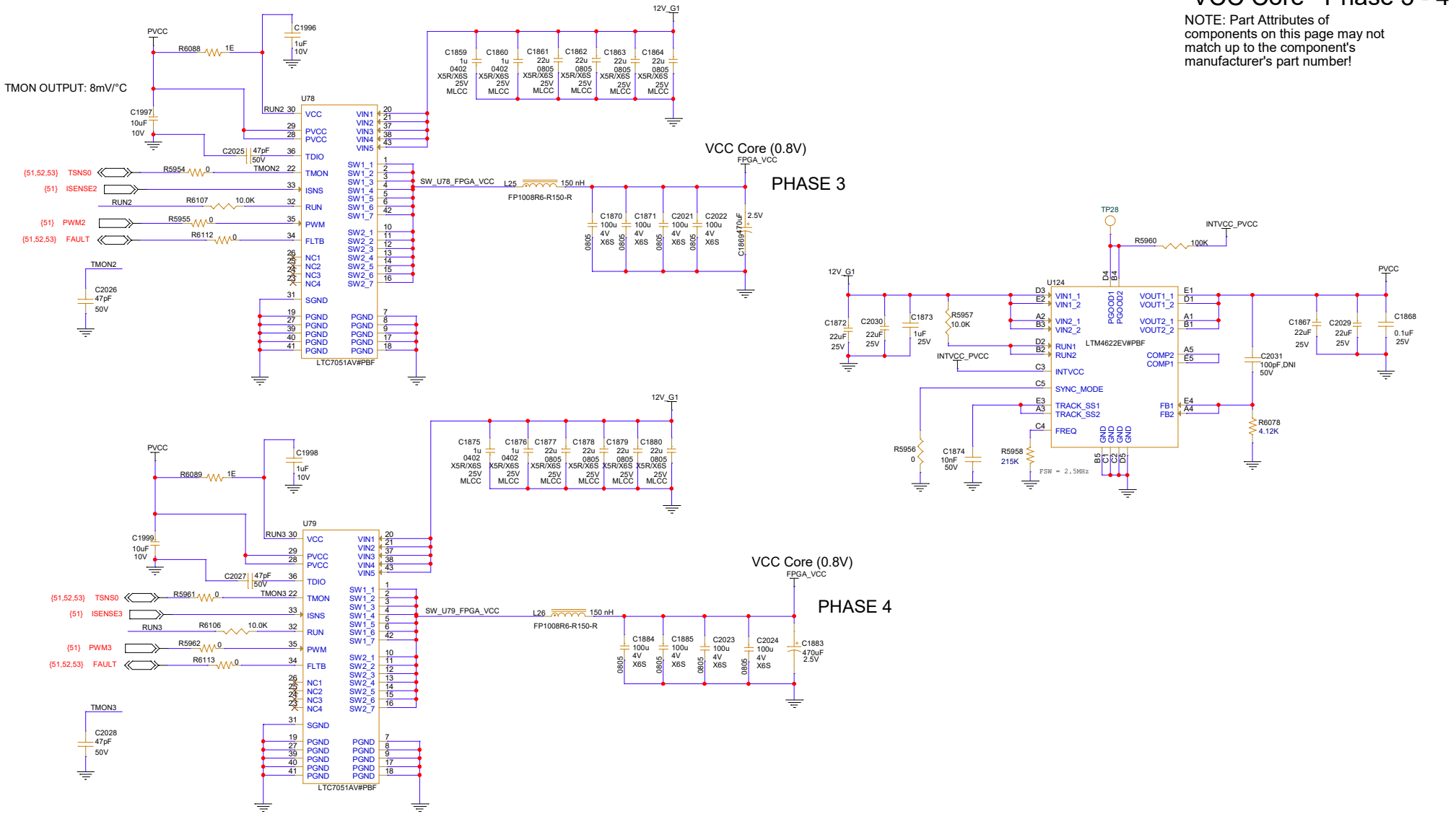
Size: Custom	Document Number: M75579-100(100-0330692-B1) Rev: C1
Date: Wednesday, December 04, 2024	Sheet 52 of 67

VCC Core Phase 3 - 4

NOTE: Part Attributes of components on this page may not match up to the component's manufacturer's part number!



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Size: Custom	Document Number: M75579-100(100-0330692-B1)	Rev: C1
Date: Wednesday, December 04, 2024	Sheet 53 of 67	

PWR - 1p8V

NOTE: U71 Default configured for LTM4686EV-1 uModule
If Changing to LTM4686EV
UnMount R5966,R5967 AND mount R5965

1.8V @ 4.506A

VIN : 12V
VOUT : 1V8
Tj : -40 C TO 125 C
ILOAD : 4.506A
I2C ADDR = 41h
FSW : 750KHz

5V Should be up before this rail is enabled.

Sense line place near to the load

I2C ADDR = 41h
FSW : 750KHz

NOTE:PLACE THESE RESISTORS NEAR TO IC.

LTM4686EV-1

LTM4686EV-1#PBF

TSW-103-08-G-S

SHORT

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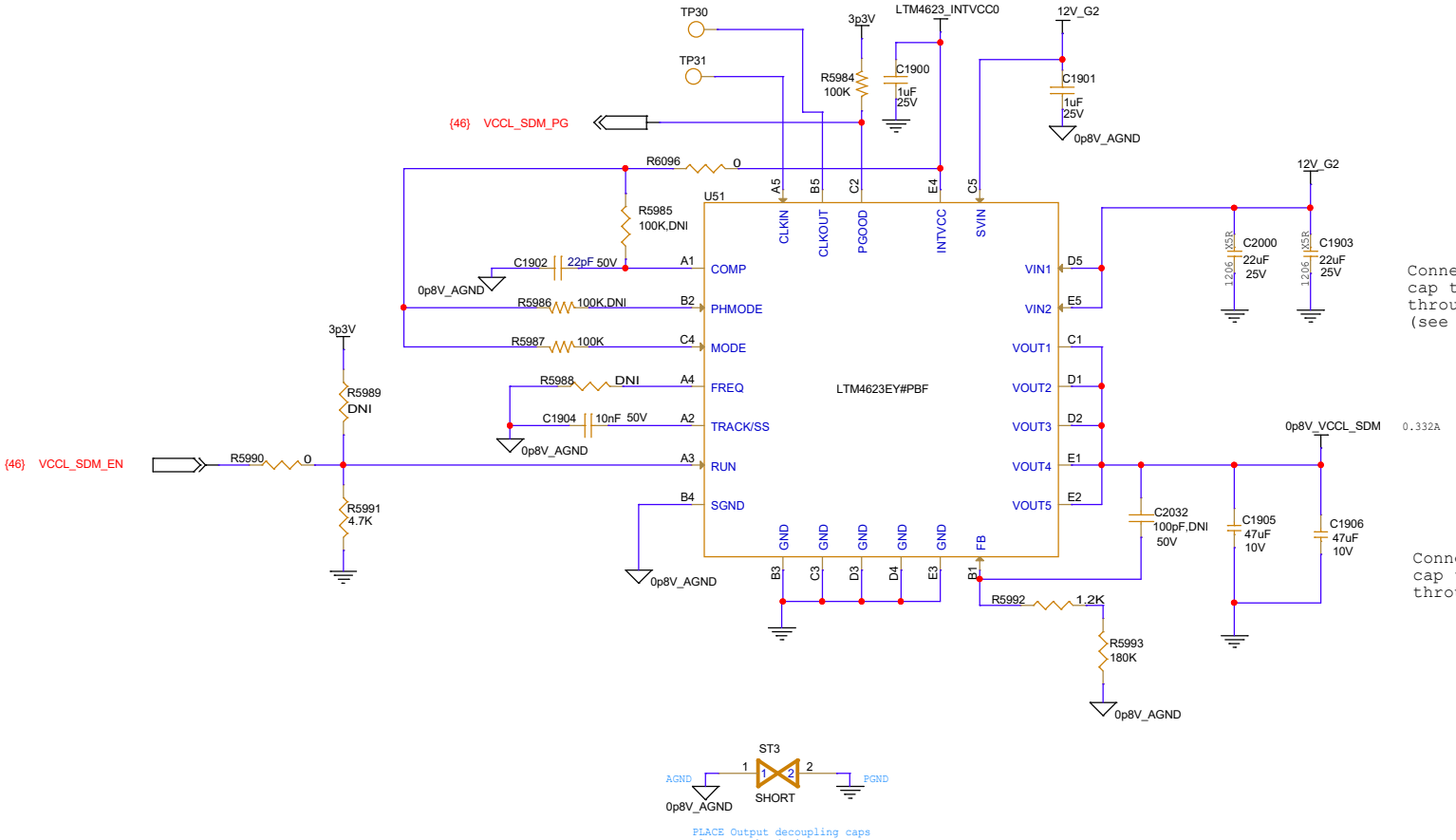
Size: Custom | Document Number: M75579-100(100-0330692-B1) | Rev: C1

Date: Wednesday, December 04, 2024 | Sheet 54 of 67

PWR - 0p8V_VCCL_SDM



VIN : 12V
VOUT : 0p8V
FSW : 1MHz
Tj : -40 C TO 125 C
ILOAD :0.332A
RFB=60.4K x (0.6/Vout-06)

Connect the input cap to the GND plane through multiple vias. (see the Gerber files)

Connect the output cap to the GND plane through multiple vias

PLACE Output decoupling caps close to the device. Connect AGND and PGND at the point of cap GND connection.

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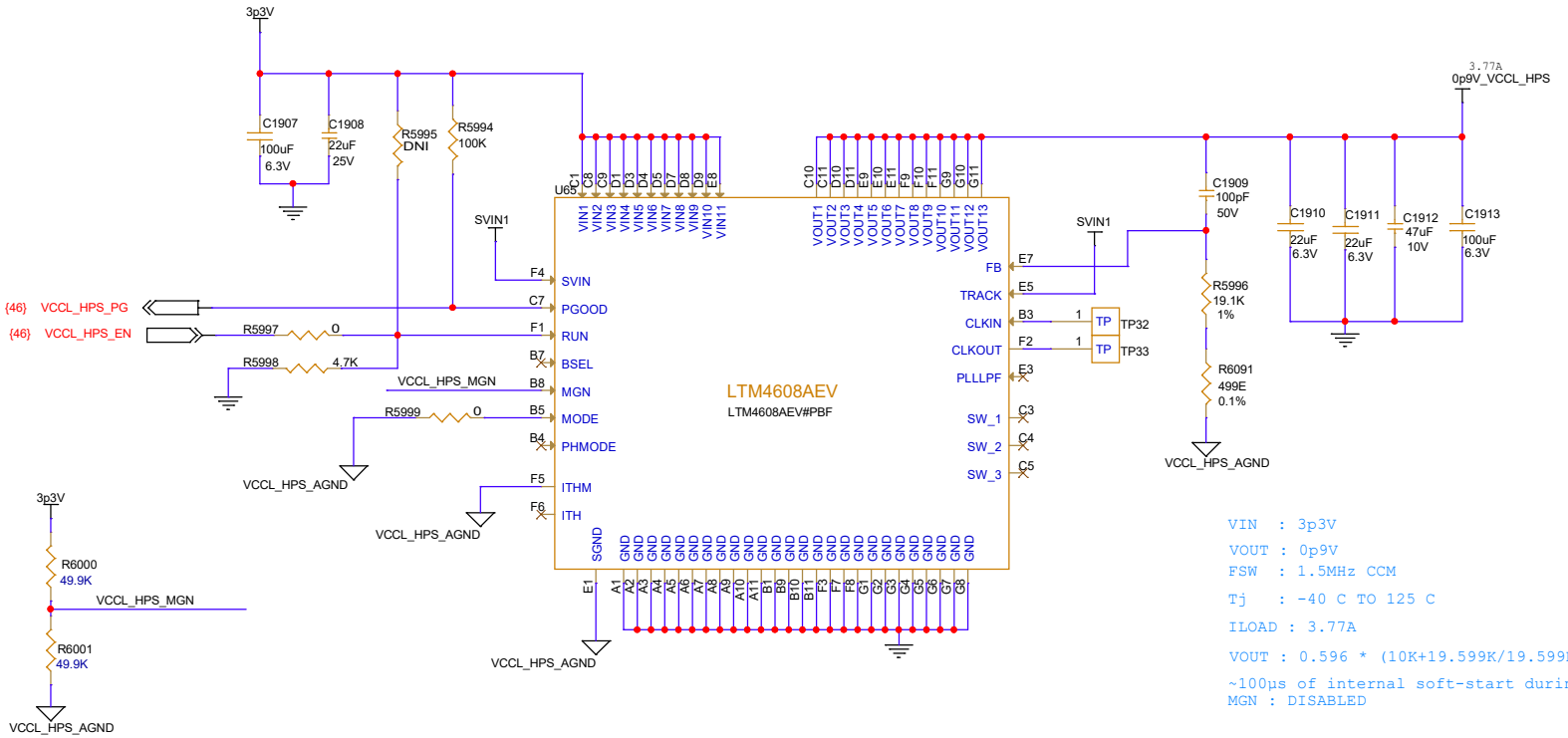
Size: B | Document Number: M75579-100(100-0330692-B1) | Rev: C1

Date: Wednesday, December 04, 2024 | Sheet 55 of 67

PWR- 0p9V_VCCL_HPS



VIN : 3p3V

VOUT : 0p9V

FSW : 1.5MHz CCM

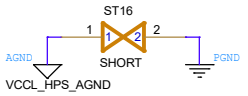
Tj : -40 C TO 125 C

ILOAD : 3.77A

VOUT : 0.596 * (10K+19.599K/19.599K)

~100µs of internal soft-start during start-up

MGN : DISABLED



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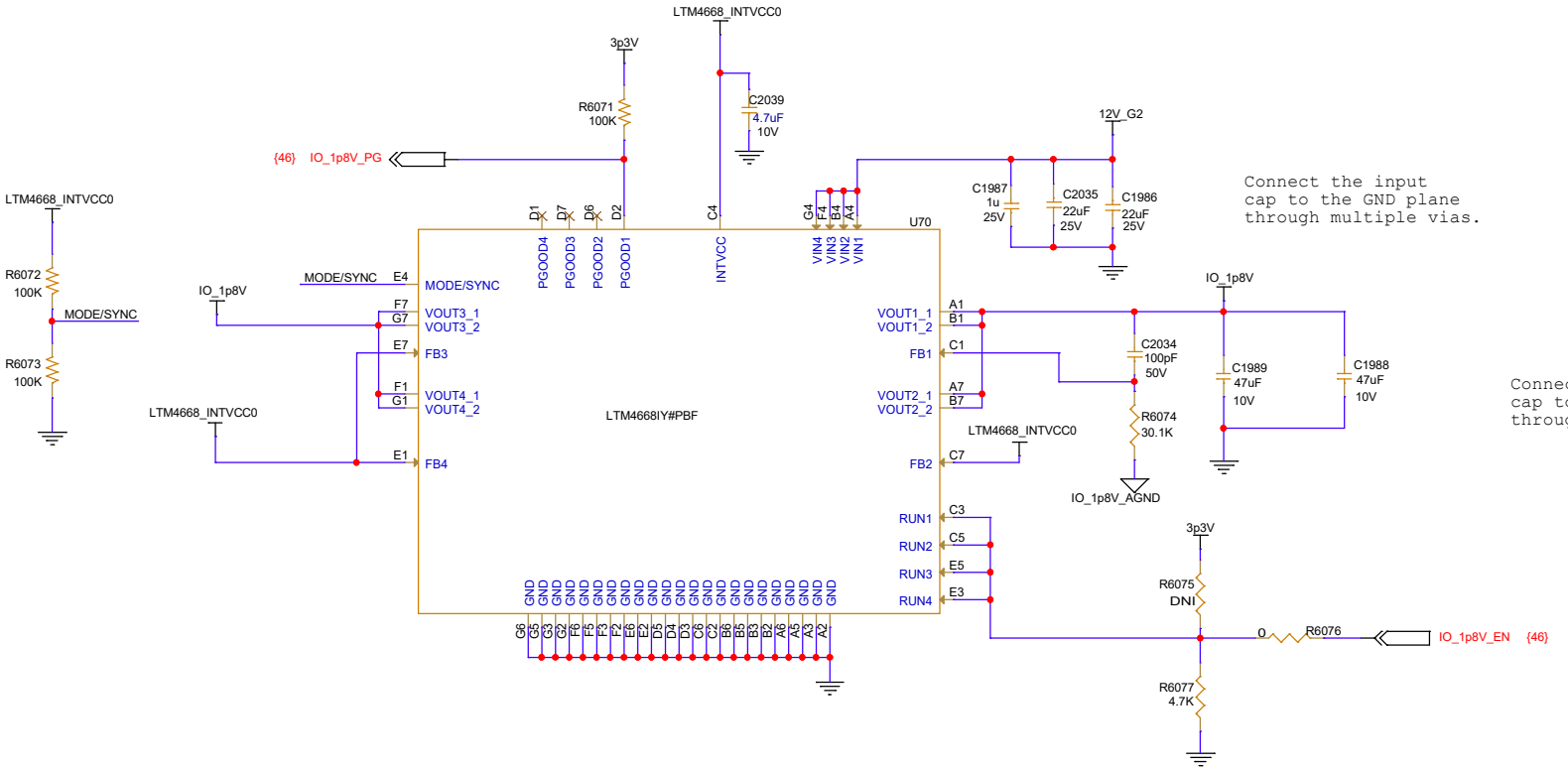
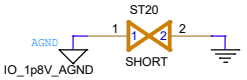
Size: B	Document Number: M75579-100(100-0330692-B1)	Rev: C1
Date: Wednesday, December 04, 2024	Sheet 56 of 67	

PWR - IO_1p8V



VIN : 12V
VOUT : 1p8V
FSW : 1 MHz
Tj : -40 C TO 125 C
ILOAD : 4A
RFB=60.4K x (0.6/Vout-06)



PLACE Output decoupling caps close to the device. Connect AGND and PGND at the point of cap GND connection.

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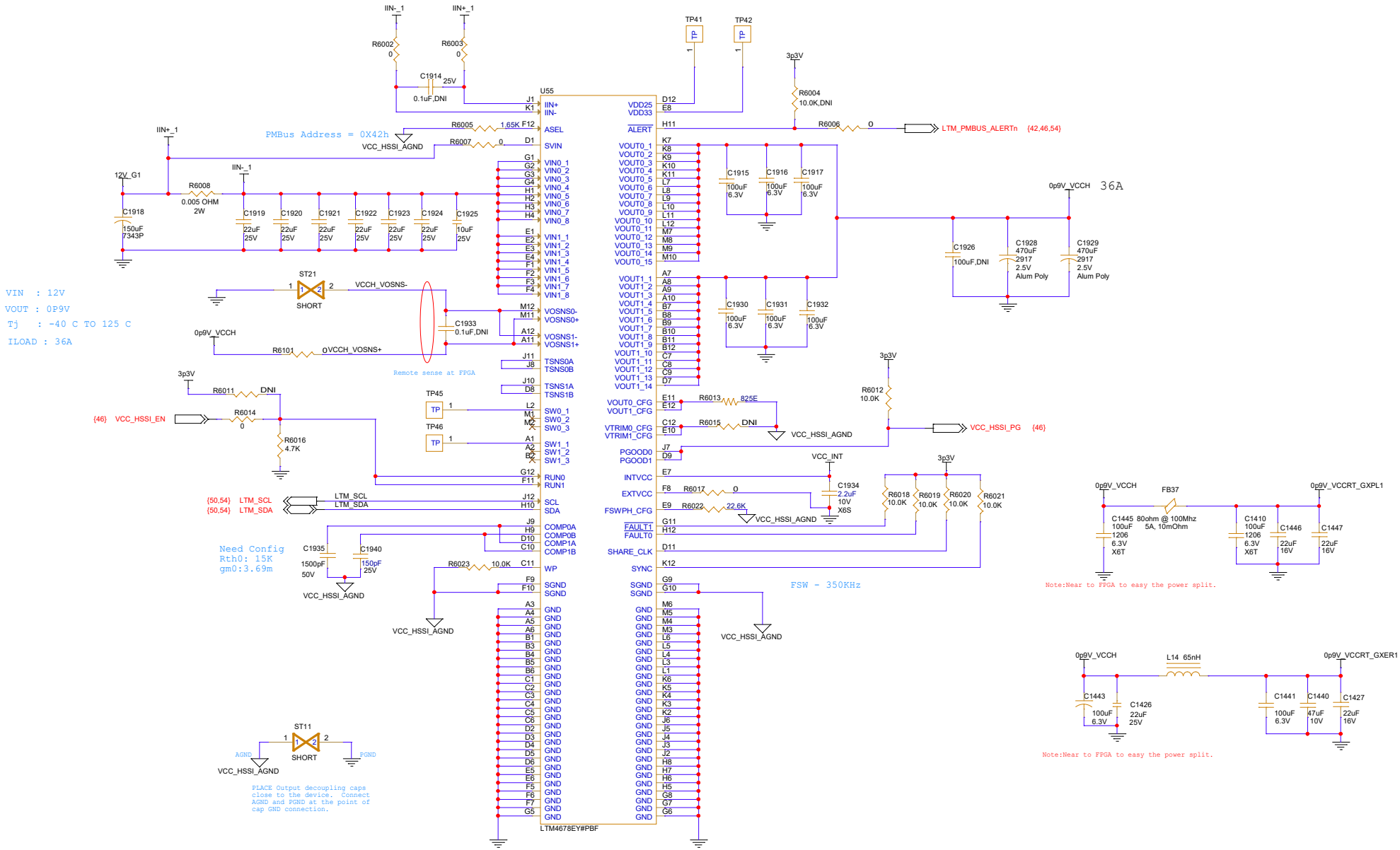
Size: B	Document Number: M75579-100(100-0330692-B1) Rev: C1
Date: Wednesday, December 04, 2024	Sheet 57 of 67

PWR - VCC_HSSI_GXER1/VCC_HSSI_GXPL1



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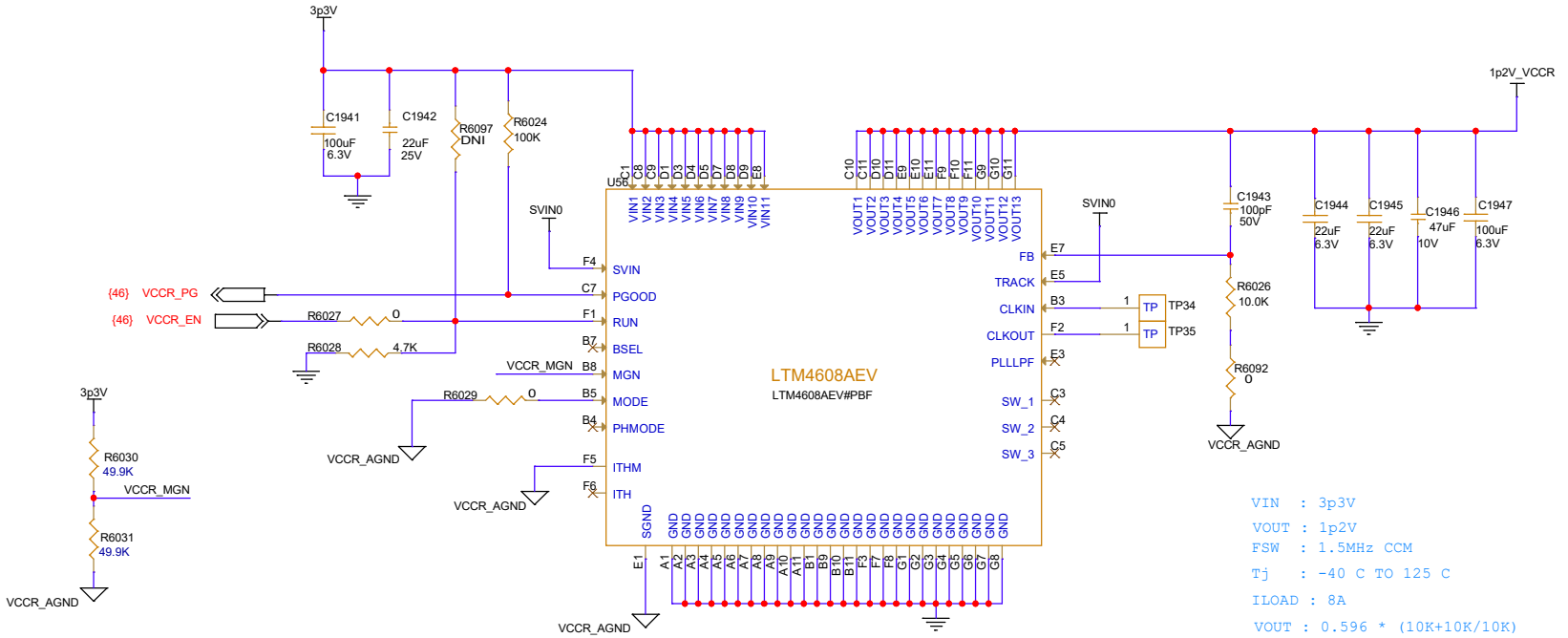
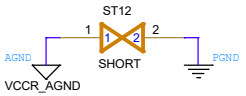
Size: Custom	Document Number: M75579-100(100-0330692-B1) Rev: C1
Date: Wednesday, December 04, 2024	Sheet 58 of 67





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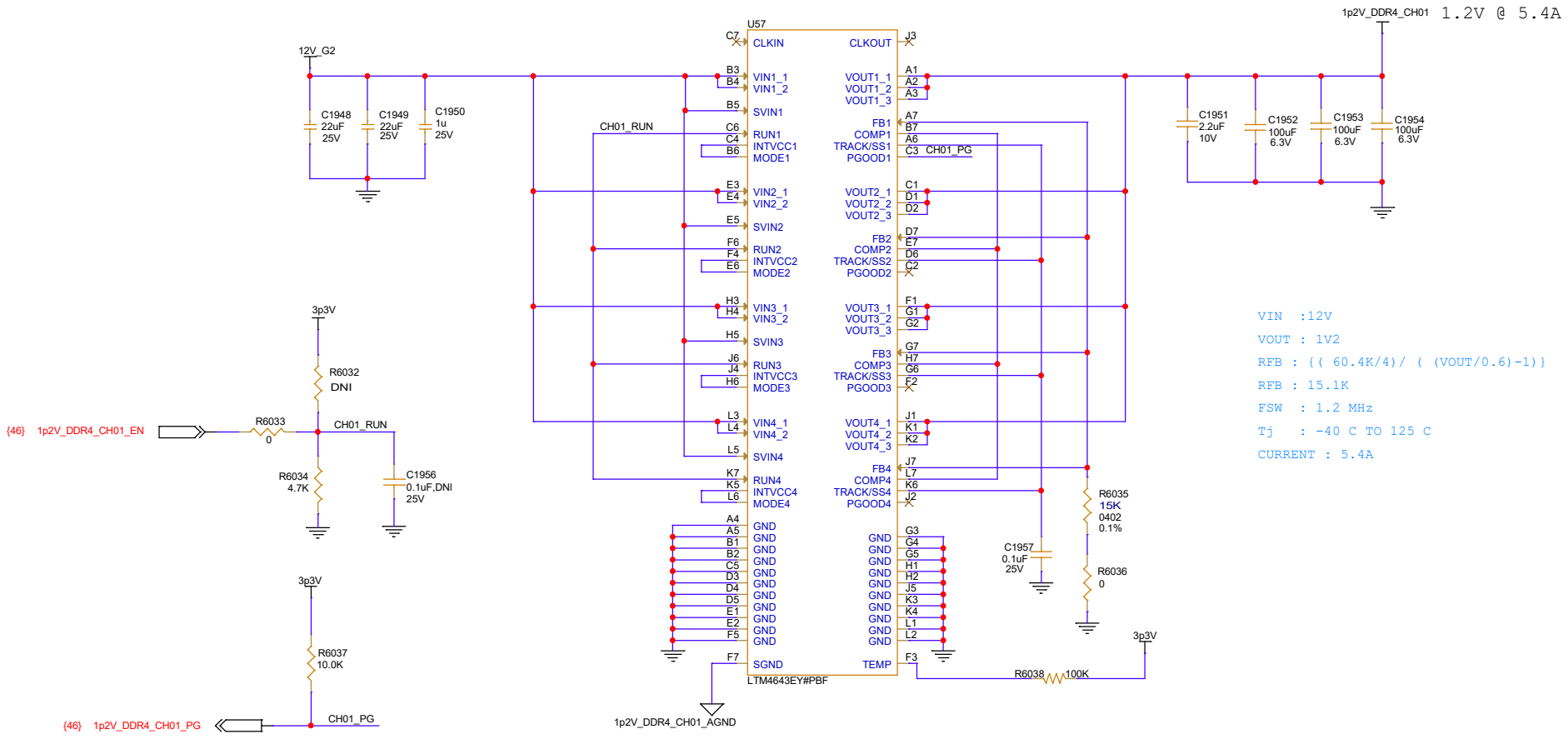
Size: B	Document Number: M75579-100(100-0330692-B1)	Rev: C1
Date: Wednesday, December 04, 2024	Sheet 59 of 67	

PWR - 1p2V_DDR4_CH01



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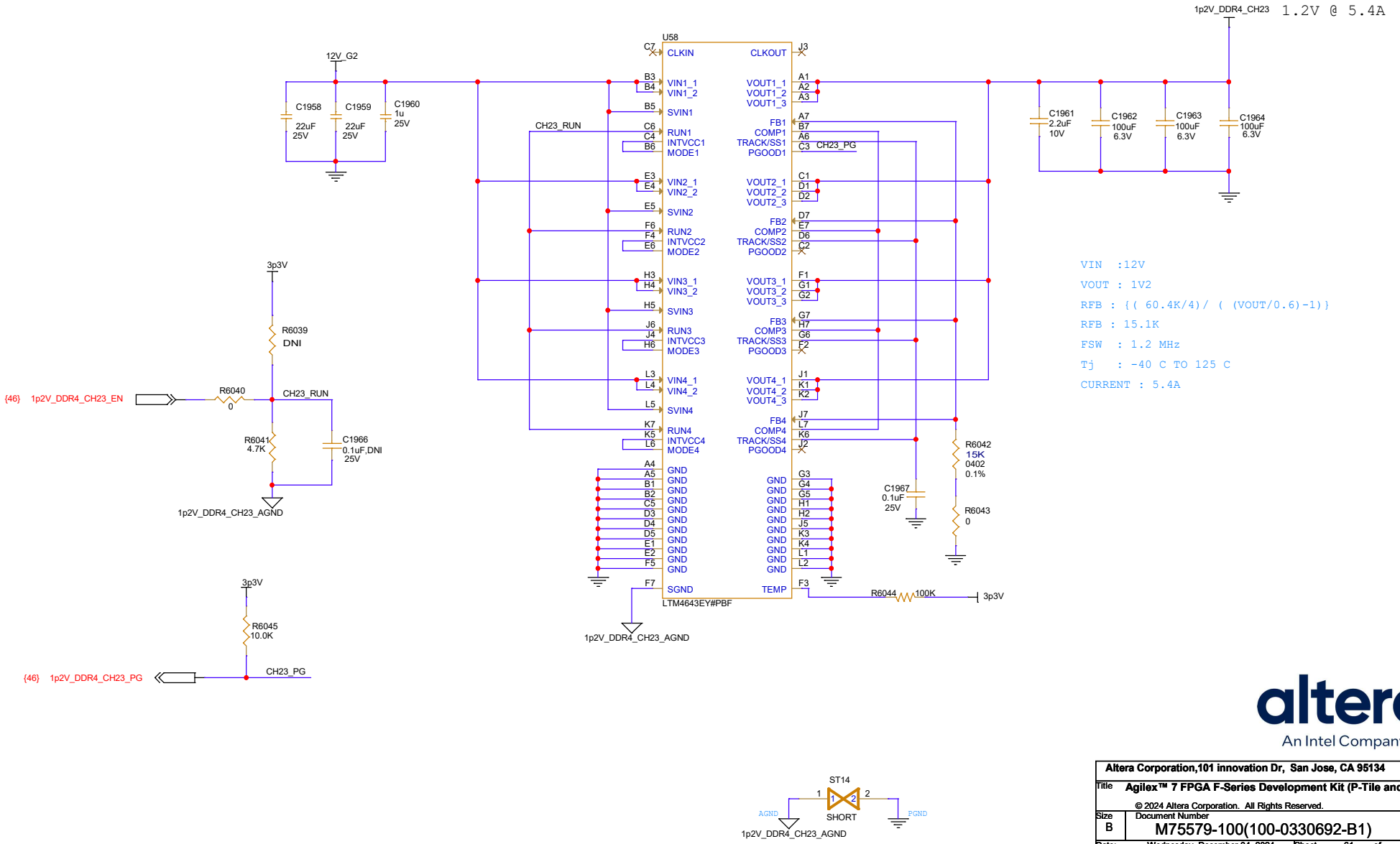
Title	Agilex™ 7 FPGA F-Series Development Kit (P-Tile and E-Tile)
Size: B	Document Number: M75579-100(100-0330692-B1) Rev: C1
Date: Wednesday, December 04, 2024	Sheet 60 of 67

PWR - 1p2V_DDR4_CH23



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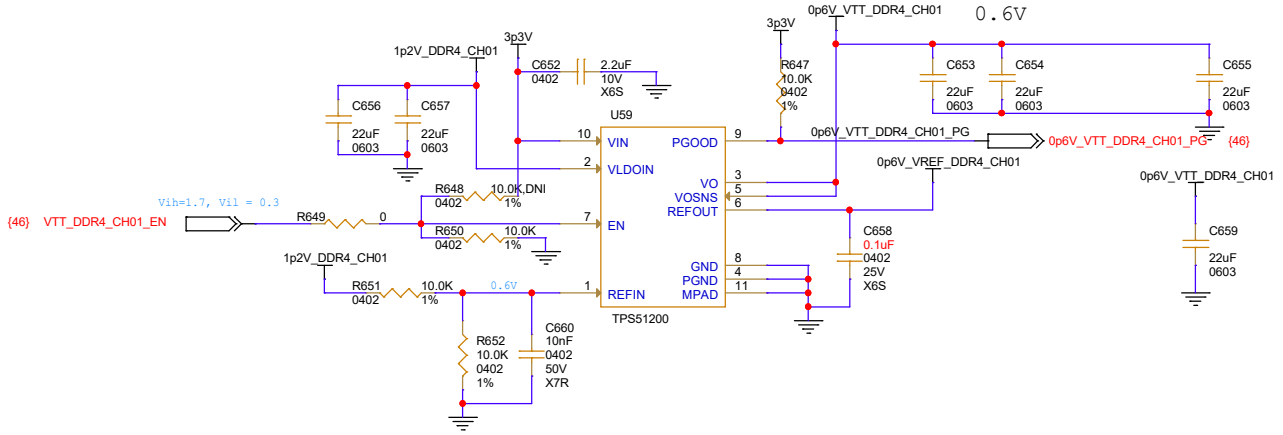
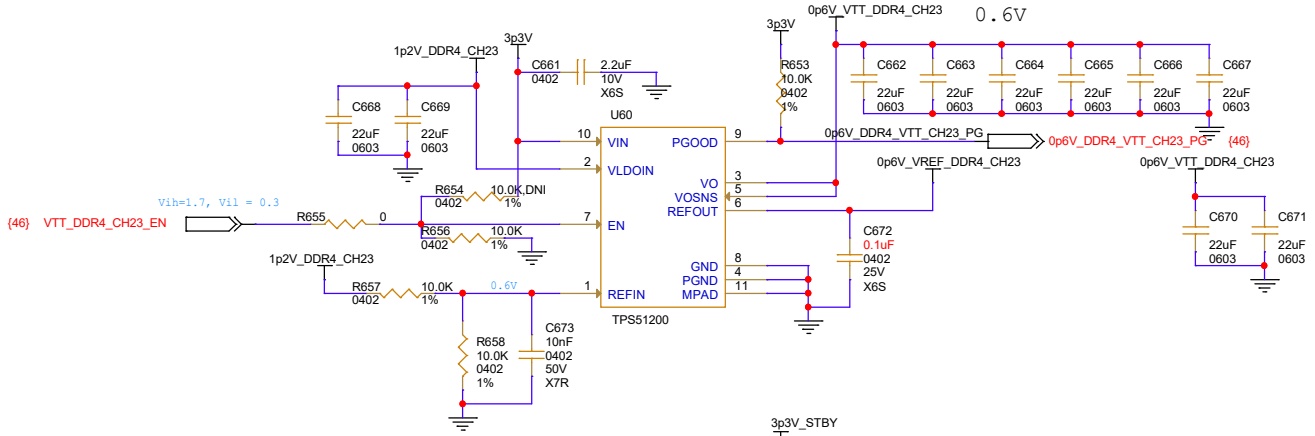
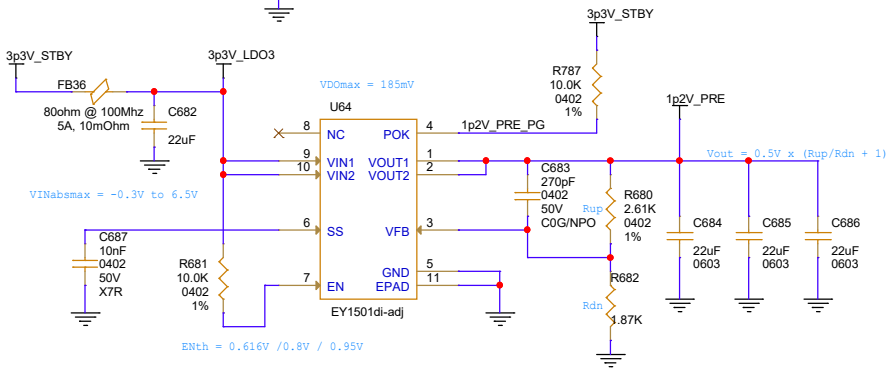
Size: B	Document Number: M75579-100(100-0330692-B1) Rev: C1
Date: Wednesday, December 04, 2024	Sheet 61 of 67

PWR - DDR4 VREF/VTT







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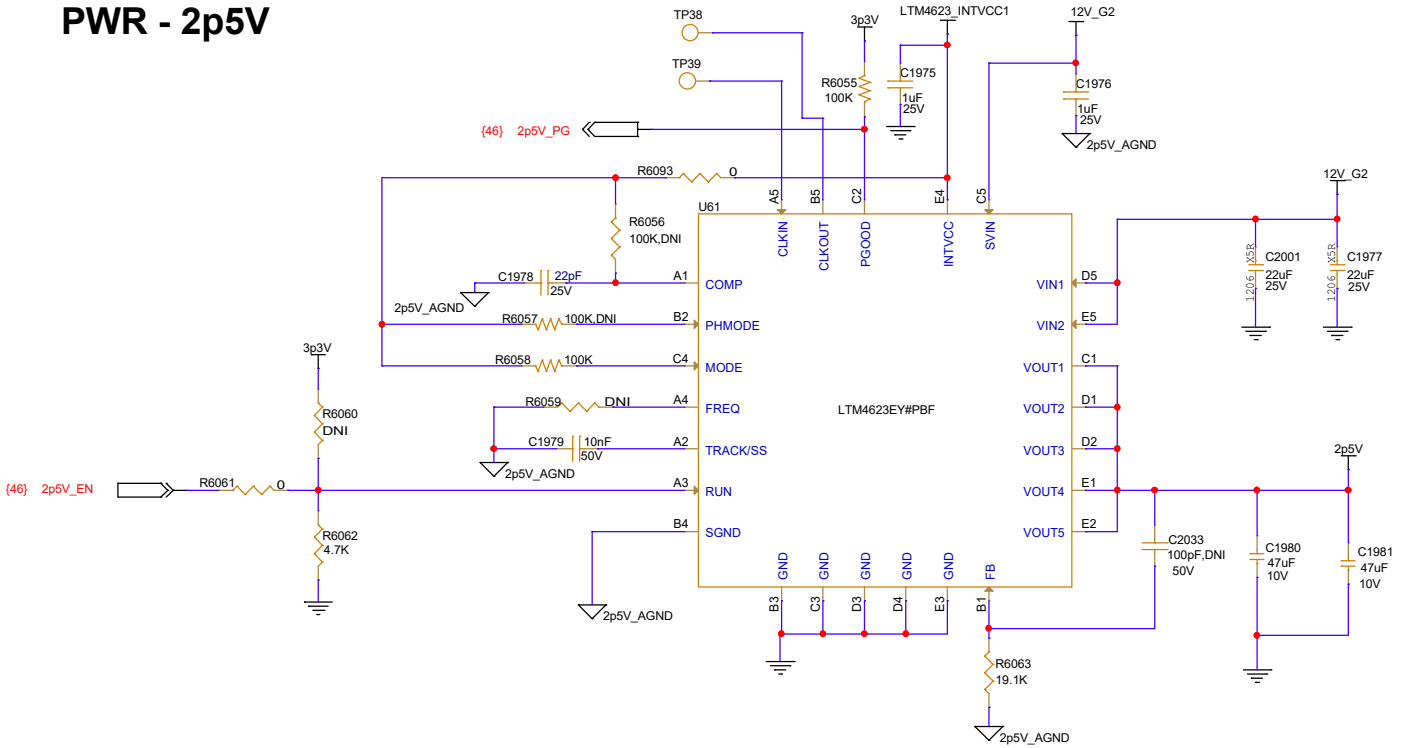
Size: B	Document Number: M75579-100(100-0330692-B1)	Rev: C1
Date: Wednesday, December 04, 2024	Sheet 62 of 67	

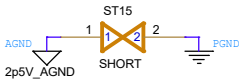
PWR - 2p5V



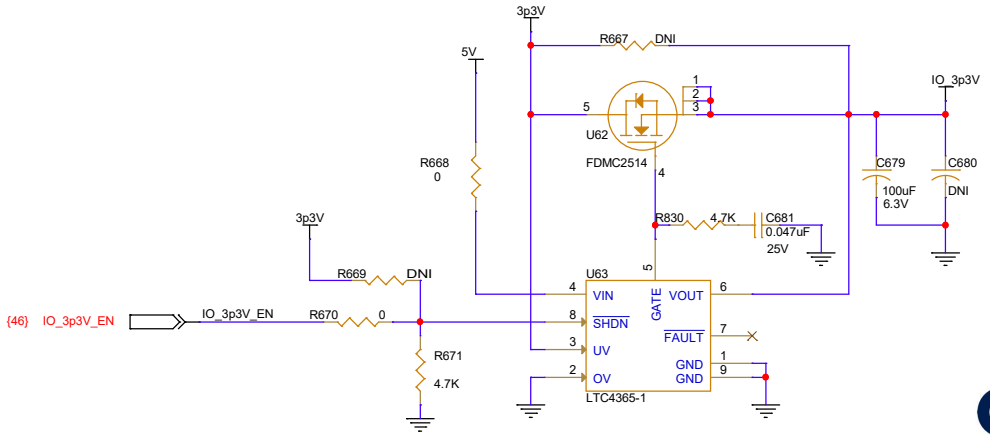
VIN : 12V
VOUT : 2p5V
FSW : 1MHz
Tj : -40 C TO 125 C
ILOAD : 3A
RFB=60.4K x (0.6/Vout-06)

Connect the input cap to the GND plane through multiple vias. (see the Gerber files)

Connect the output cap to the GND plane through multiple vias



PLACE Output decoupling caps close to the device. Connect AGND and PGND at the point of cap GND connection.



3.3V Enable Circuit

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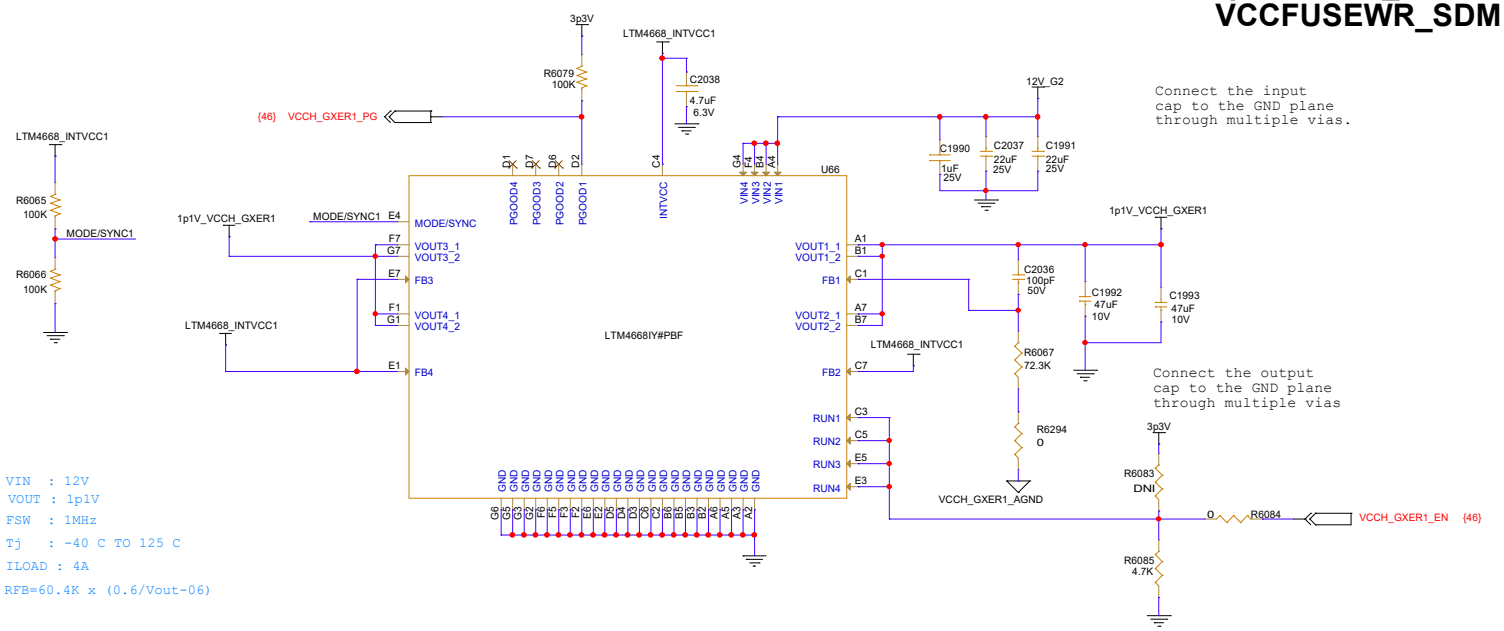
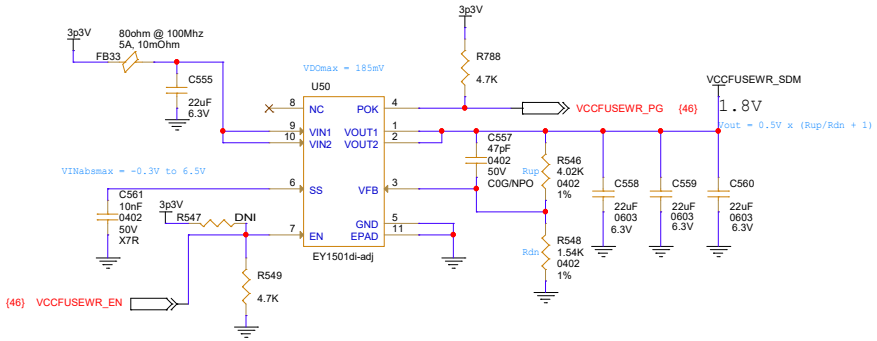
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 63 of 67

PWR - 1p1V VCCH_GXER1
VCCFUSEWR_SDM



PLACE Output decoupling caps close to the device. Connect AGND and PGND at the point of cap GND connection.



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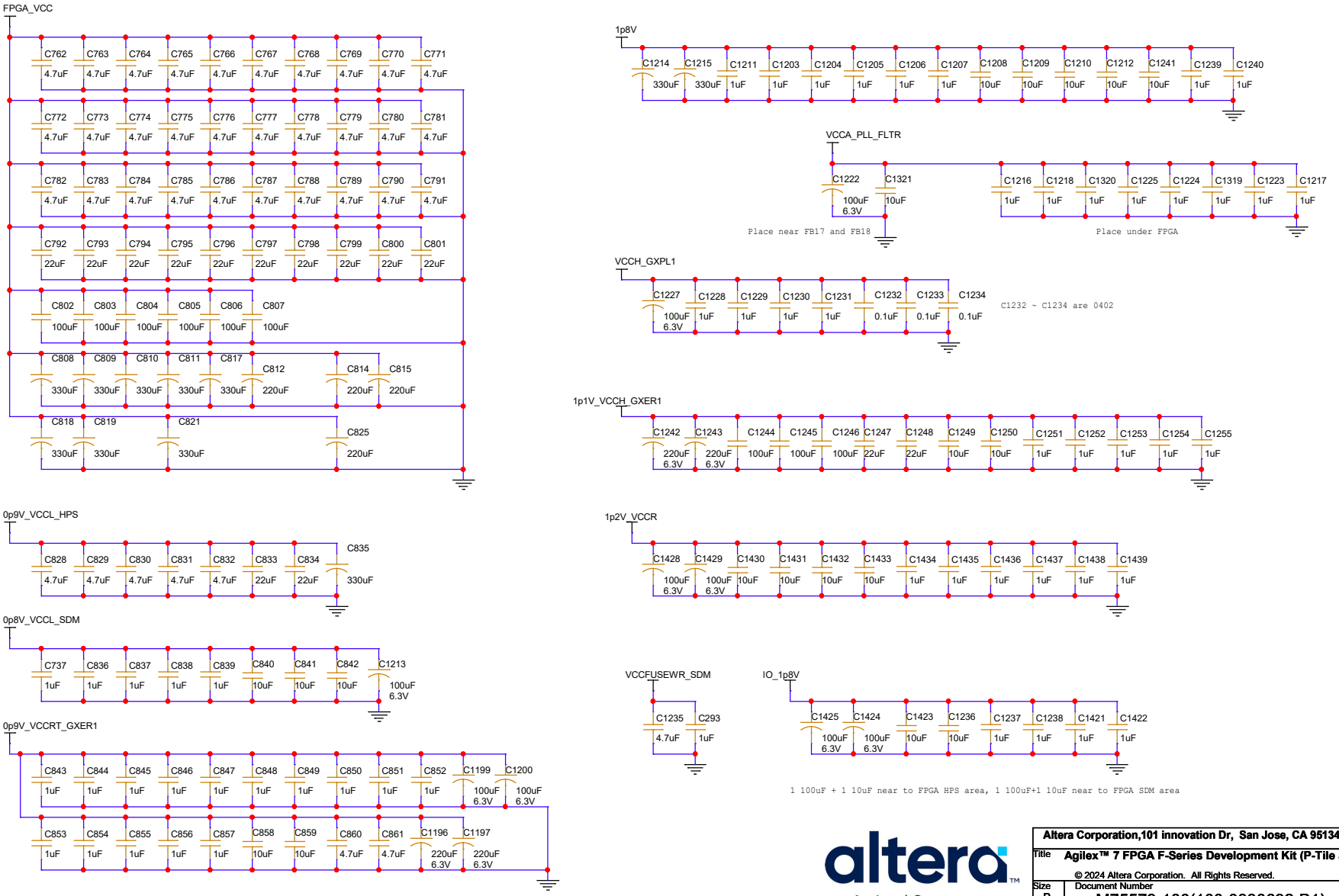
Size	Document Number	Rev
Custom	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 64 of 67

Decoupling - page 1



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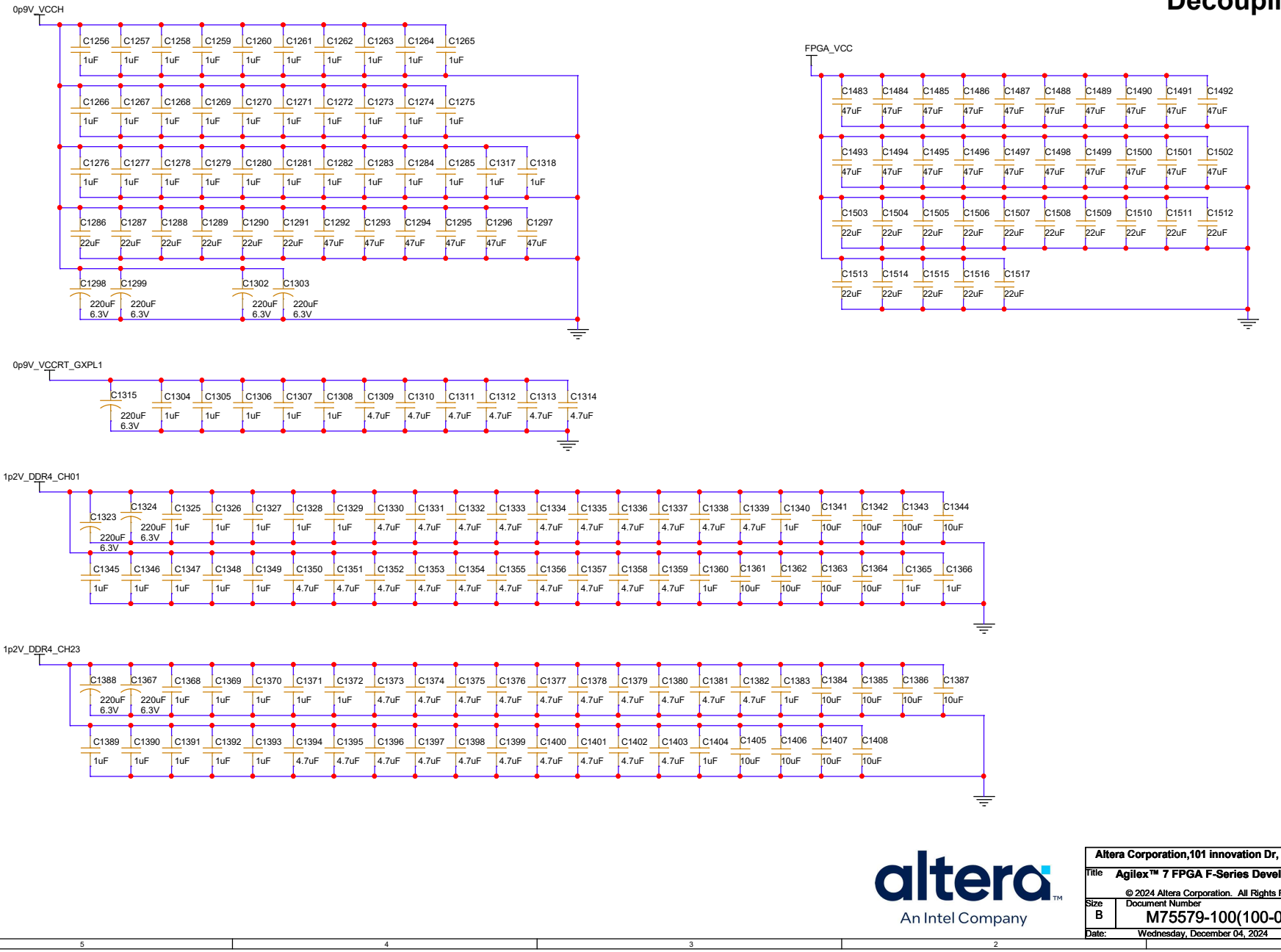
Size	Document Number	Rev
B	M75579-100(100-0330692-B1)	C1

Date: Wednesday, December 04, 2024 Sheet 65 of 67

Decoupling - page 2



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Size: B	Document Number: M75579-100(100-0330692-B1)	Rev: C1
Date: Wednesday, December 04, 2024	Sheet 66 of 67	

RE-SPIN CHANGES LIST FROM REV B0 TO REV C0

Sr.No	PAGE NO	REF DES	OLD IC NUMBER	NEW IC NUMER
1	50	U46	EM2130H01QI	LTC7151
2	51	U47	ED8401P01QJ	LTC3888IUHG-1#PBF
3	52	U76	ET6160LI	LTC7051AV#PBF
4	52	U77	ET6160LI	LTC7051AV#PBF
5	53	U78	ET6160LI	LTC7051AV#PBF
6	53	U79	ET6160LI	LTC7051AV#PBF
7	53	U124	ER3105DI	LTM4622EV#PBF
8	54	U71	EM2120H01QI	LTM4686EV-1
9	55	U51	EN6337QI	LTM4623EY#PBF
10	56	U65	EN6362QI	LTM4608AEV#PBF
11	57	U70	EN6347QI	LTM4668IY#PBF
12	58	U55	EM2140P01QJ	LTM4678EY#PBF
13	59	U56	EN6362QI	LTM4608AEV#PBF
14	60	U57	EN63A0QI	LTM4643EY#PBF
15	61	U58	EN63A0QI	LTM4643EY#PBF
16	63	U61	EN6337QI	LTM4623EY#PBF
17	64	U66	EN6347QI	LTM4668IY#PBF
18	45	U125	LTM4657EY	Input voltage changed to 12V
19	50	U126		INA219AIDCNR
20	43	J14		0702461004

REV B1 CHANGES

21	57,64	U66, U70	IC LTM4668IY#PBF U66, U70 PGood 2,3,4 pins are made it NC
22	51	J22	J22 connector modified from 2*5 to 2*2
23	51	J22	TP17, TP16 reused to LTM3888_ALERTn & FPGA_VCC_EN
24	51	J22	TP20 smd test point added to FPGA_VCC_PG

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Size: B | Document Number: M75579-100(100-0330692-B1) | Rev: C1

Date: Wednesday, December 04, 2024 | Sheet 67 of 67