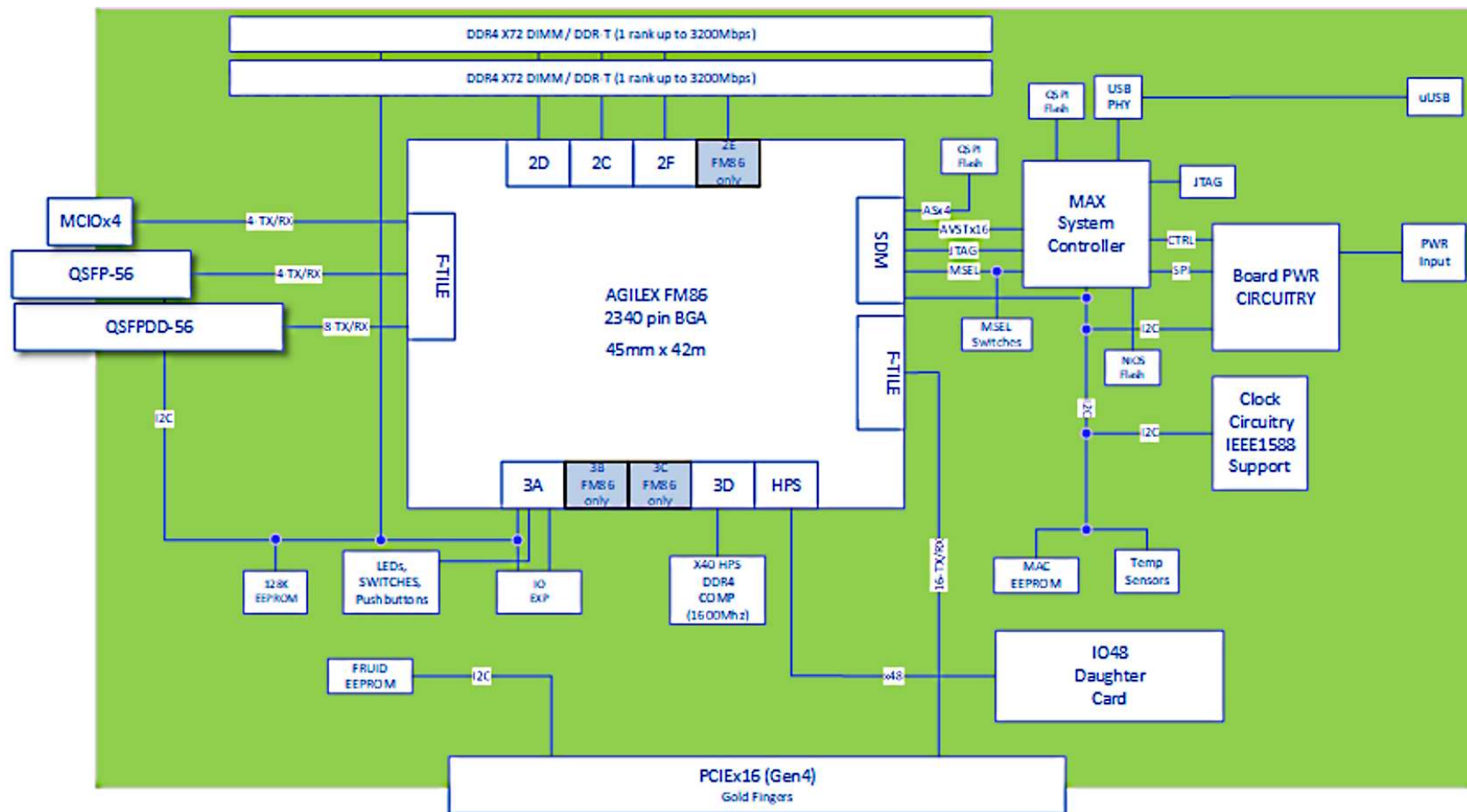


REV	DATE	PAGES	DESCRIPTION
A1	06/29/2021	All	Preliminary Release for checking
B1	01/03/2022	Pa58 Pa59 Pa64	Change U177/U78 pin / FN connection to 3V3_STBY Swap MAX_I2C_SCL/SDA connection on U93 Swap MAX_I2C_SCL/SDA connection on U96
C1	03/19/2024	Pa1 Pa2	Correct Table of Contents, Pa20, Pa21 Update Block Diagram. Remove Reference to U20-U2C and U12-U13A
D1	10/07/2024	Pa63 Pa66	Connect U8 AC25, U8 AC27, U8 AE25, U8 AE27 to FPGA_VCCIO_1V2 for FM76 package migration. Correct notes for CLK_SEL input of U26, U27.

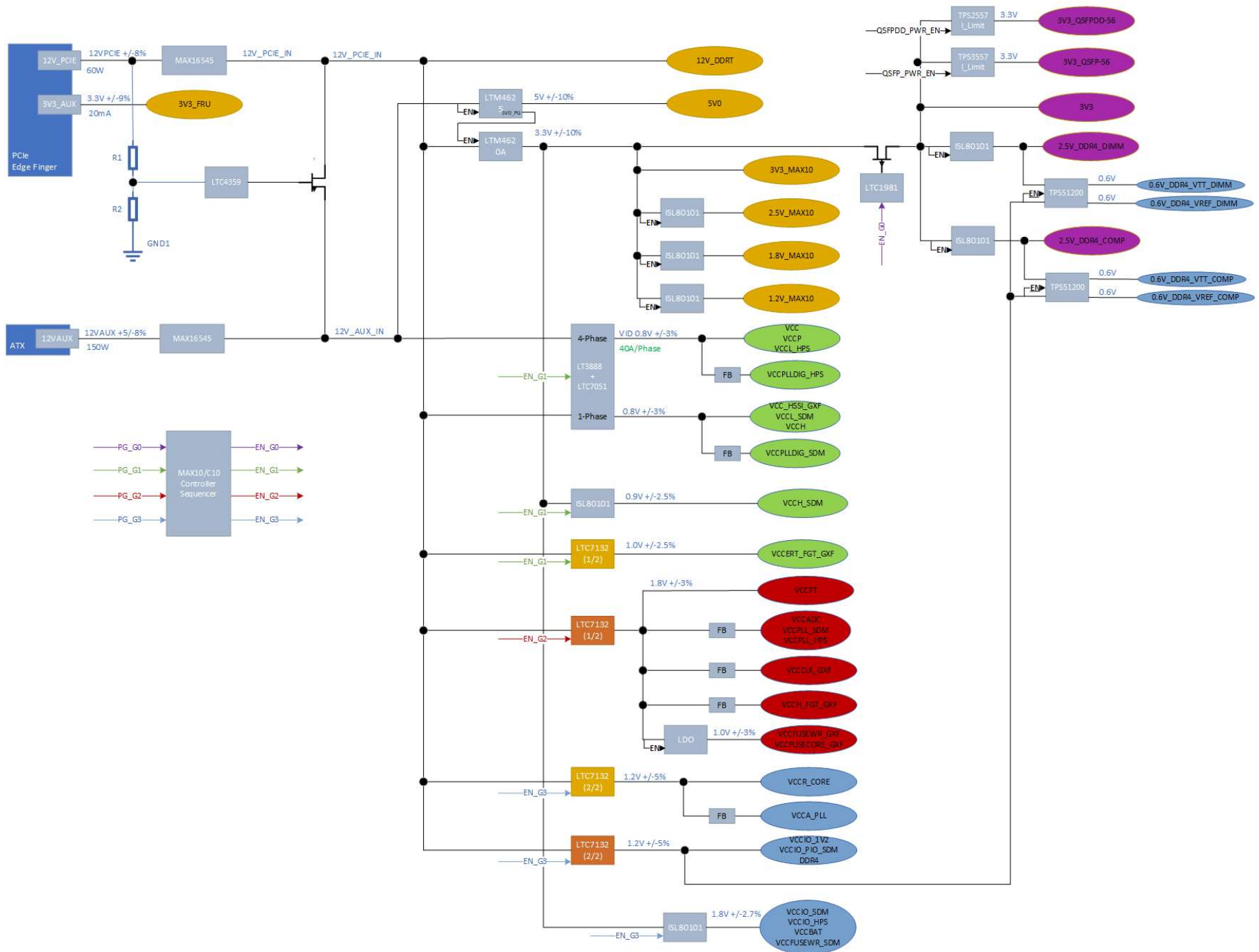
PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	Cover, Table of Contents, Notes	38	I2C Translators
2	Block Diagram	39	Buttons, Switches, LEDs
3	Power Tree Diagram	40	EEPROM, NIOS Flash
4	Clock Diagram	41	USB-Blaster II, JTAG
5	I2C Diagram	42	FPGA Decoupling
6	JTAG Diagram	43	Input Power HSC
7	Power Sequence Diagram	44	5V0, MAX: 2V5, 1V8, 1V2
8	PCIe Edge Finger	45	3V3_STBY, 3V3_SYS
9	FPGA Configuration Flash	46	VCC Controller
10	Max10 System Controller	47	VCC Phase 1
11	Agilex SDM	48	VCC Phase 2
12	Agilex Bank 2C - DDR4 DIMM1	49	VCC Phase 3
13	Agilex Bank 2D - DDR4 DIMM1	50	VCC Phase 4
14	Agilex Bank 2E - DDR4 DIMM2	51	VCC_HSSI_GXF Phase 5
15	Agilex Bank 2F - DDR4 DIMM2	52	VCC_H_SDM
16	Agilex Bank 3A - General IO's	53	VCCERT_FGT_GXF
17	Agilex Bank 3B - Unused IO's	54	VCCPT, VCCFUSEWR_GXF
18	Agilex Bank 3C - Unused IO's	55	VCCR_CORE
19	Agilex Bank 3D - DDR4 Component	56	VCCIO_1V2
20	Agilex F-Tile Bank 12C - QSFDD, QSF, CXL	57	VCCIO_SDM, VCCFUSEWR_SDM
21	Agilex F-Tile Bank 13A - PCIe Gen4x16	58	PG58 2V5_DDR4, DDR4 VTT, VREF
22	Agilex HPS, TEMPDIODE, DNU		
23	Agilex Power		
24	Agilex GND		
25	DDR4 / DDR-T Pin Mapping		
26	DDR4 / DDR-T DIMM1		
27	DDR4 / DDR-T DIMM2		
28	HPS DDR4 COMP 1 & 2		
29	HPS DDR4 COMP 3 & 4		
30	HPS DDR4 COMP 5, TERMINATION		
31	HPS IO48 Interface		
32	QSFDD-56		
33	QSF-56		
34	CXL Connector		
35	Clock 1 - IEEE 1588 Clocking		
36	Clock 2 - PCIe, CXL Refclocks		
37	Buffers, Translators		

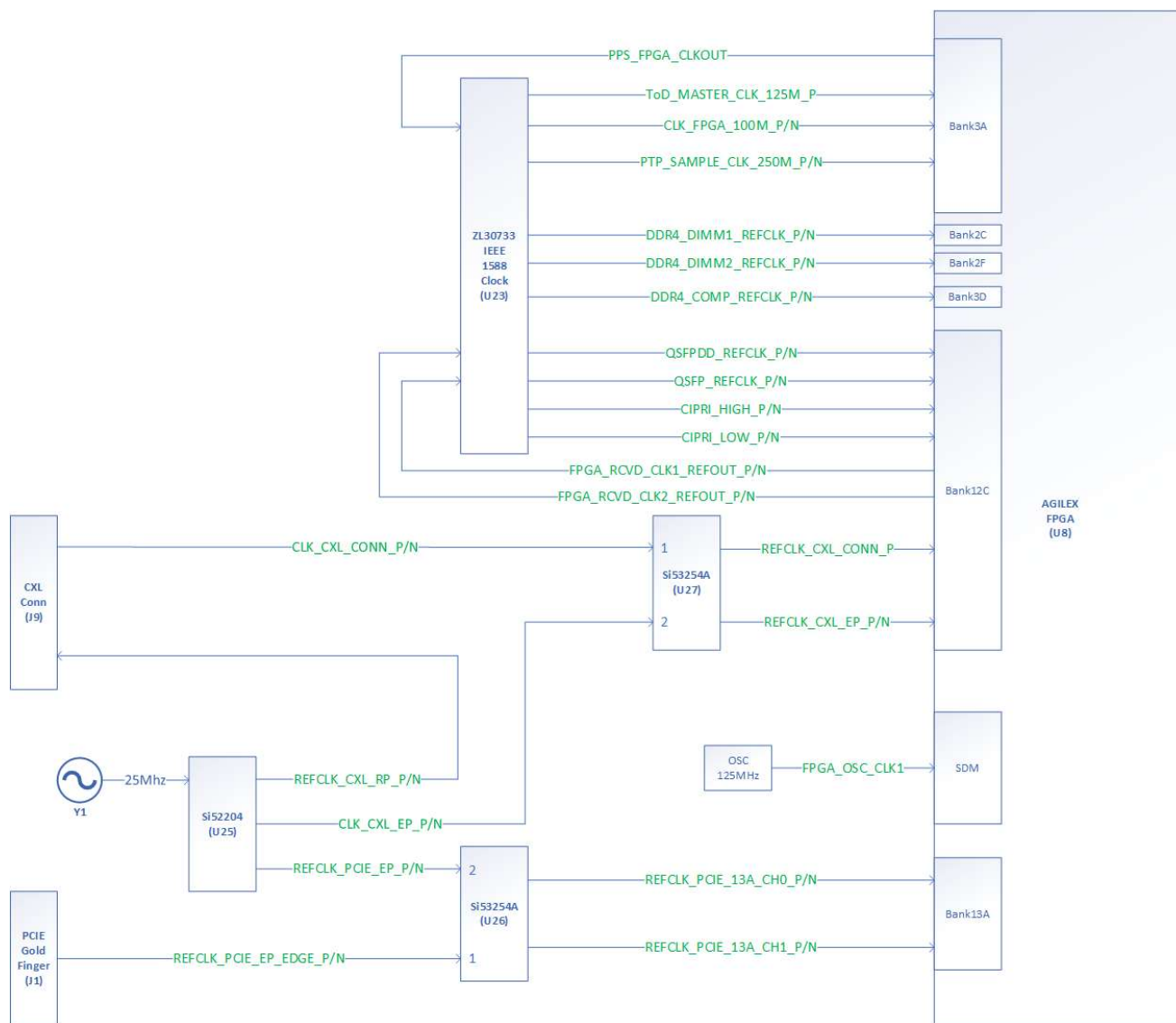
Name	Official Name	Board OPN	Board MMID	Device OPN	Device MMID
FM86 FPGA DK (ES)	Agilex F-Series FPGA Development Kit, Two F-Tile Edition (ES)	DK-DEV-AGF027F1ES	99ARL0	AGFB027R24C2E2VR0	99AKGJ
FM86 FPGA DK (Prod)	Agilex F-Series FPGA Development Kit, Two F-Tile Edition (Prod)	DK-DEV-AGF027FA	99ARL1	AGFB027R24C2E2V	TBD
FM76 FPGA DK	Agilex F-Series FPGA Development Kit, Two F-Tile and High-Performance Crypto Edition	DK-DEV-AGF023FA	99ARL2	AGFD023R24CE1VC	99CHRW

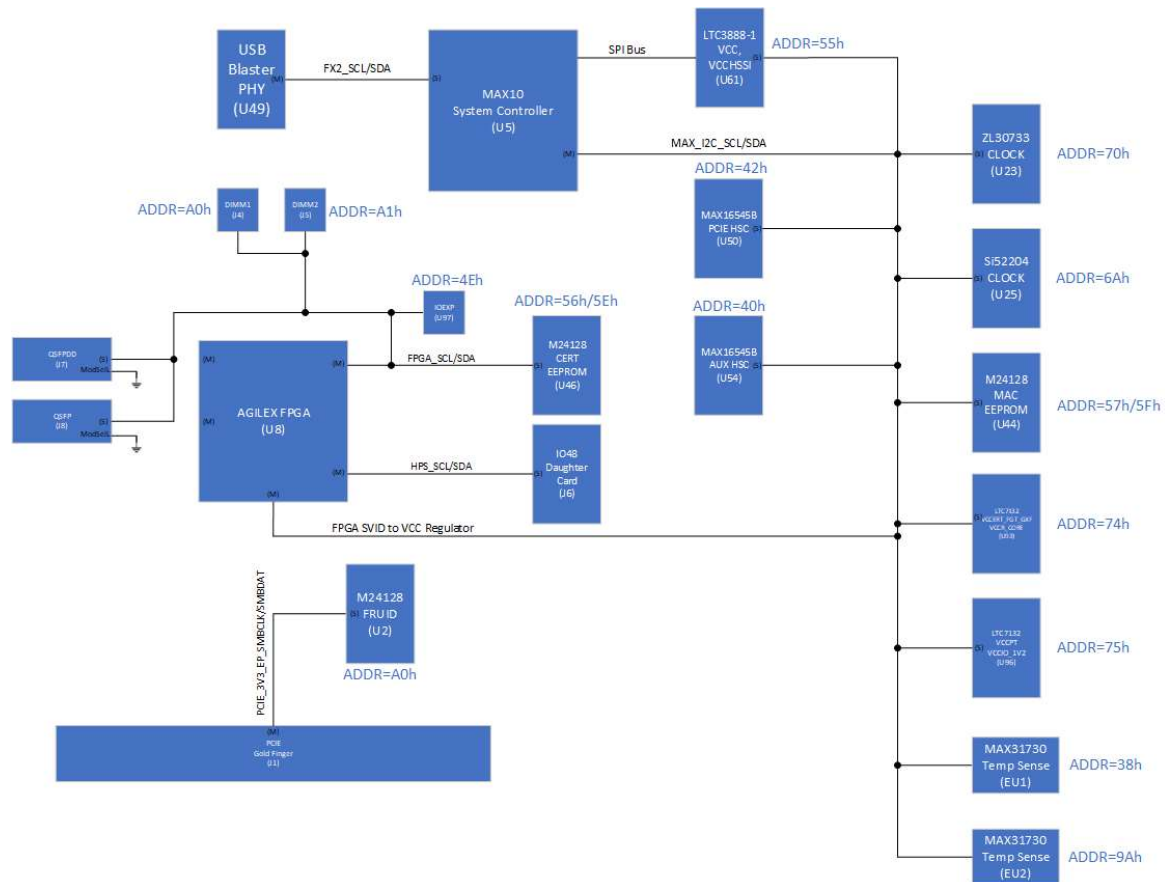
Altera, 101 Innovation Dr., San Jose CA 95134			
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Agilex FM86/FM76 DEVELOPMENT KIT			
Size	Document Number	Rev	
C	180-0330678-D1	D1	
Date:	Wednesday, December 18, 2024	Sheet	1 of 58

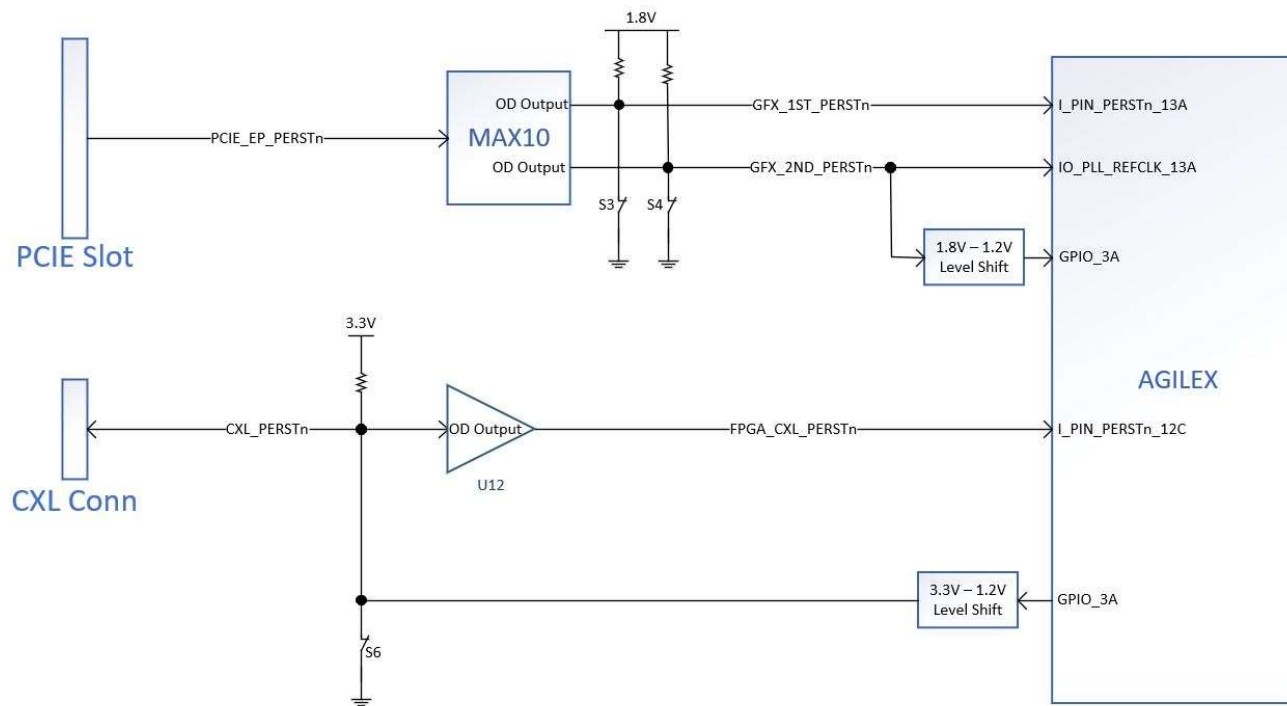
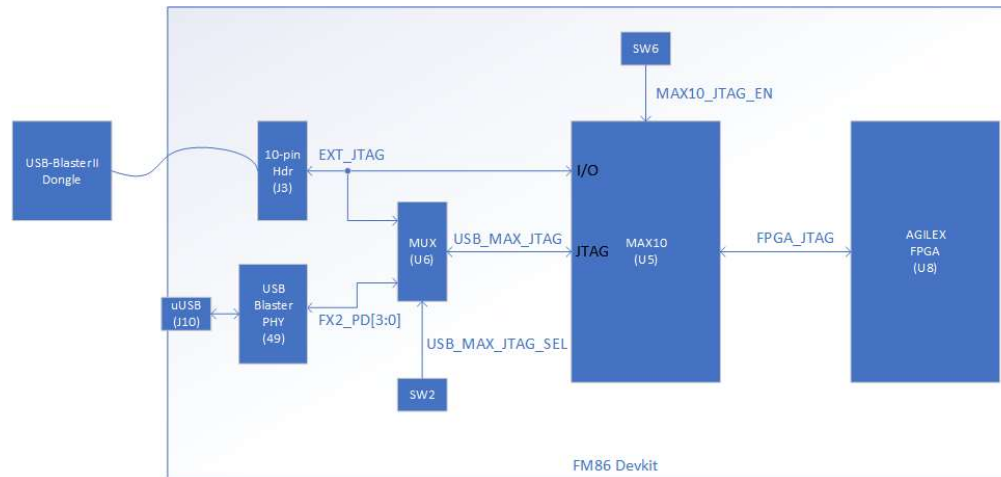


# Power Tree

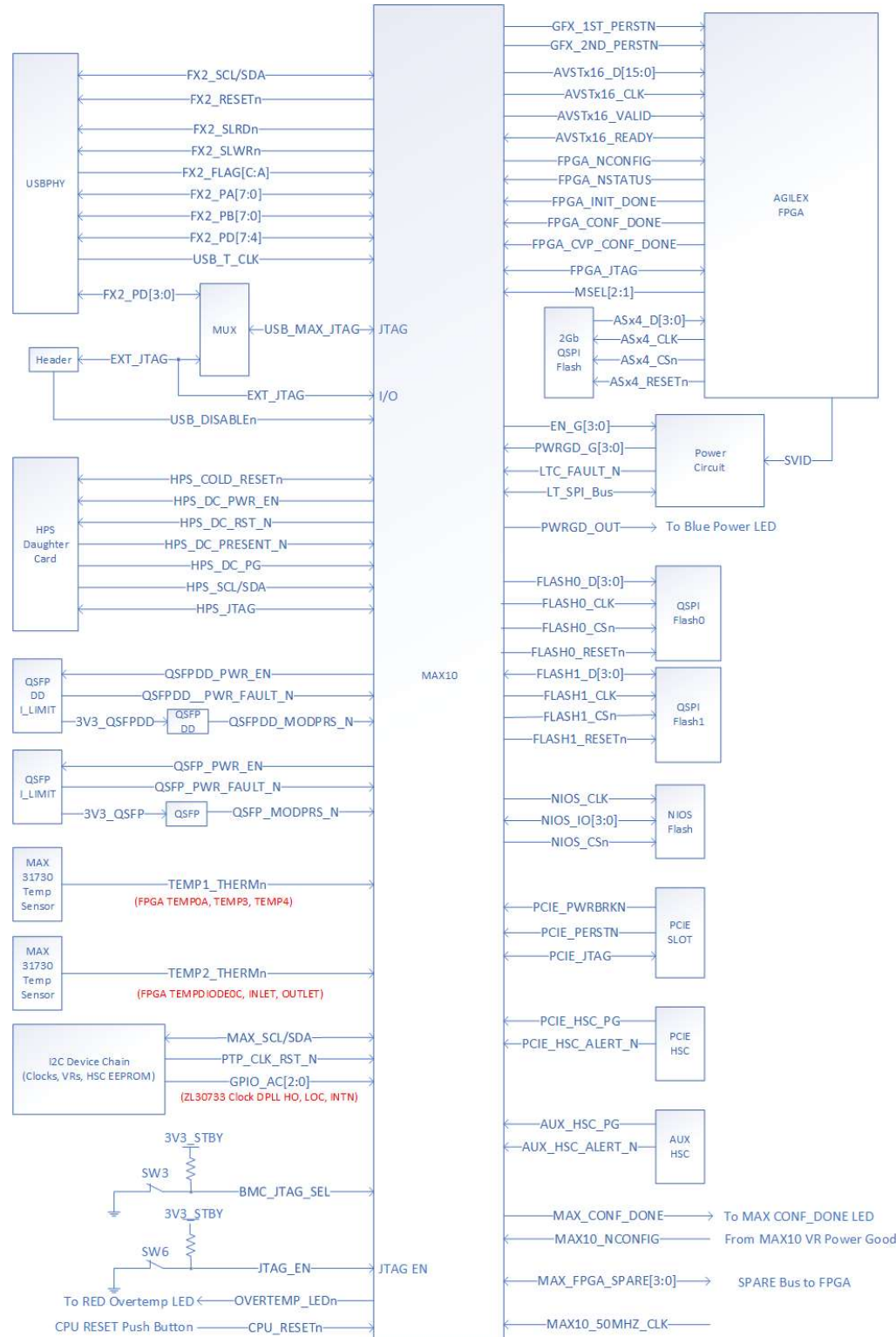




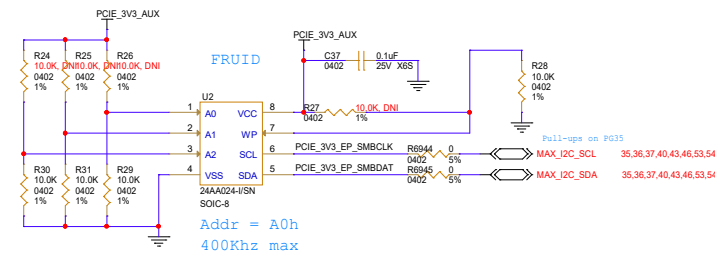
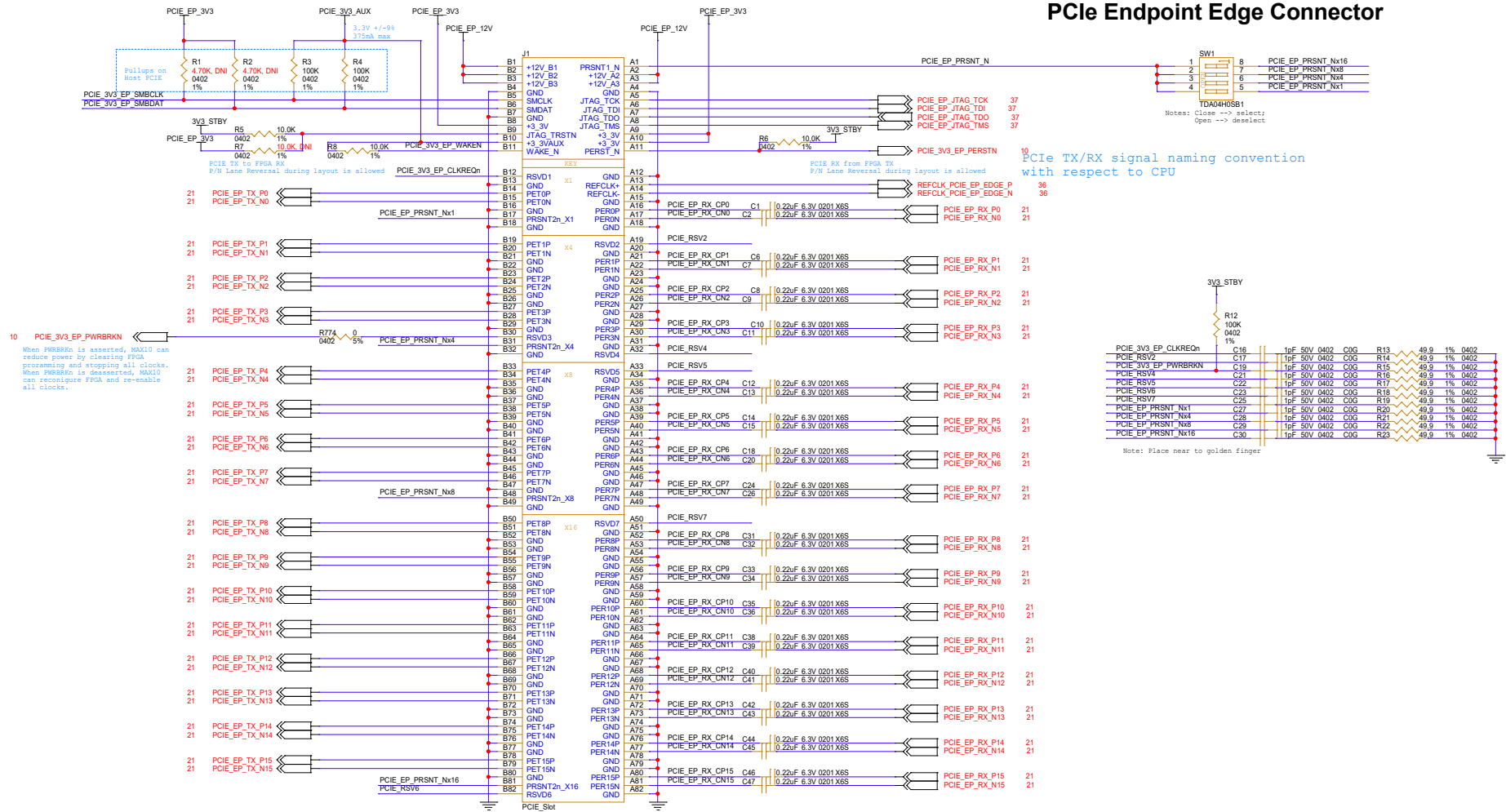








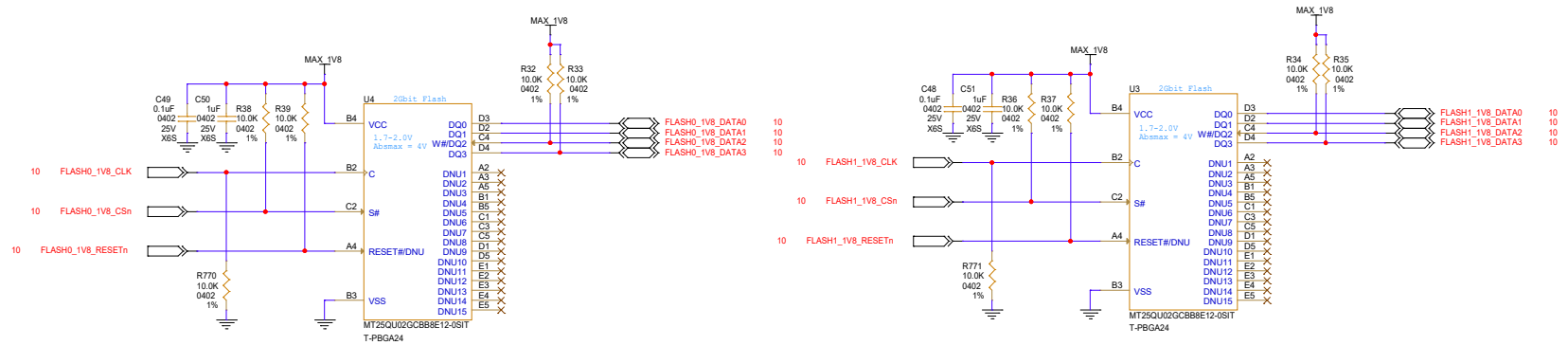
## PCIe Endpoint Edge Connector



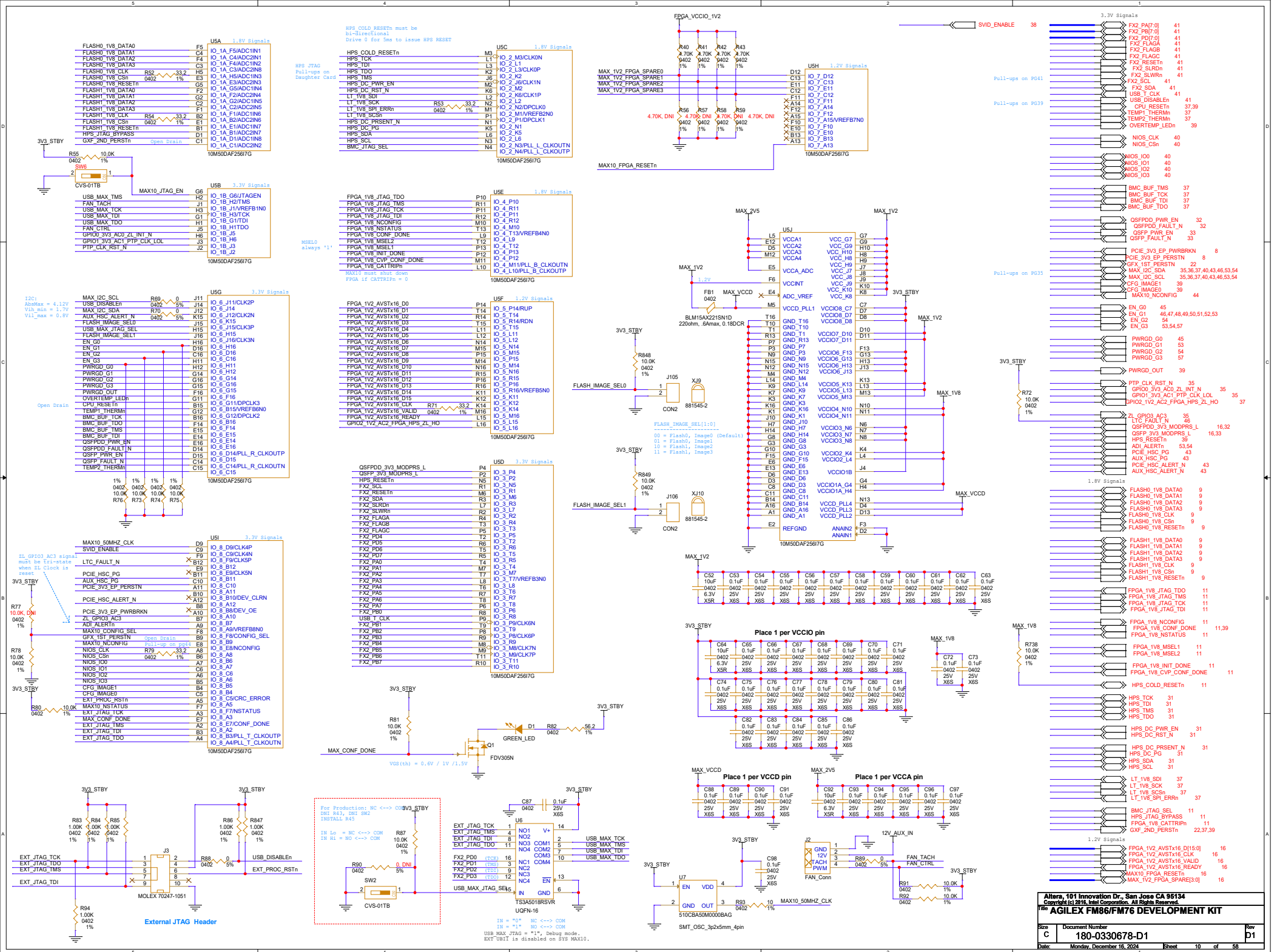


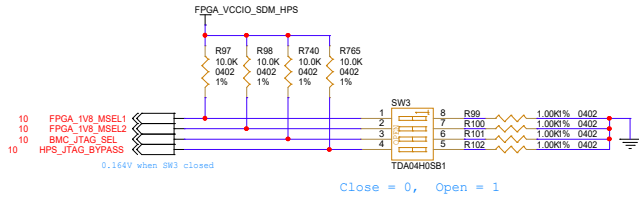
# QSPI Flash for FPGA Image

AGILEX AGF027 Bit Stream size = 833.4Mbits  
total FPGA image support = 4



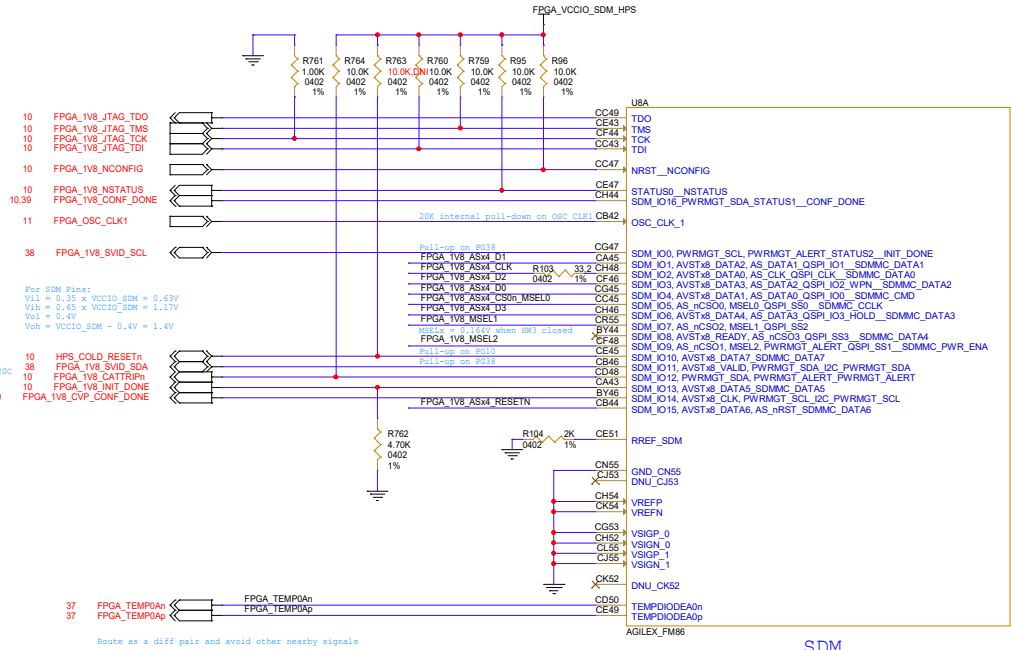
These are dual-die flash so each device is 2 loads on MAX10 IOs



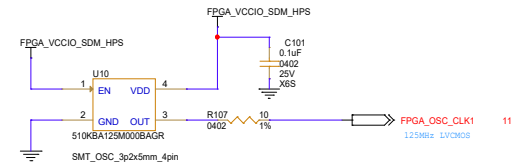
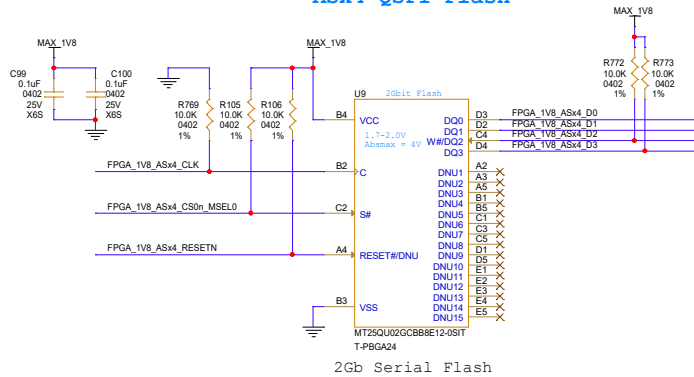


Config Mode	MSEL2	MSEL1	MSEL0
JTAG	1	1	1
AVST x16	1	0	1
AS x4 Fast (CVP)	0	0	1
AS x4 Norm	0	1	1

CATREF = 0 if FPGA Die Temp >= 120C

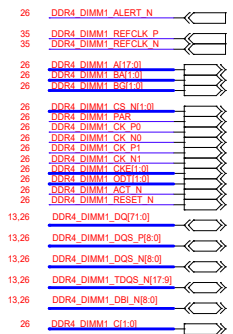


## ASx4 QSPI Flash



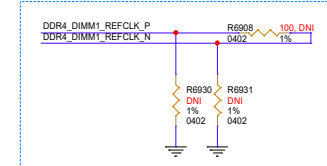
		U88			
Byte1: 8-15	DDR4 DIMM1 DQ14	DE17	IO, DIFF_RX_2C1N, DQ8	IO, CDR_DIFF_RX_2C13N, DQ12	CL25 DDR4 DIMM1 CK N1
	DDR4 DIMM1 DQ12	DF16	IO, DIFF_RX_2C1P, DQ8	IO, CDR_DIFF_RX_2C15P, DQ12	CK24 DDR4 DIMM1 CK P1
	DDR4 DIMM1 DQ15	DJ17	IO, DIFF_TX_2C1N, DQ8	IO, DIFF_TX_2C13N, DQ12	CK25
	DDR4 DIMM1 DQ15	DH16	IO, DIFF_TX_2C1P, DQ8	IO, DIFF_TX_2C14N, DQ12	CP24
	DDR4 DIMM1 TDOS N10	DE19	IO, DIFF_RX_2C2N, DQ8	IO, DIFF_RX_2C14P, DQ12	CL27
	DDR4 DIMM1 DBI N1	DF18	IO, DIFF_RX_2C2P, DQ8	IO, DIFF_TX_2C14N, DQ12	CL28
	DDR4 DIMM1 DQ5 N1	DJ19	IO, DIFF_RX_2C2P, DQ8	IO, DIFF_TX_2C14P, DQ12	CP28
	DDR4 DIMM1 DQ5 P1	DH18	IO, DIFF_TX_2C2N, DQ8N8	IO, DIFF_TX_2C14P, DQ12	CL30
	DDR4 DIMM1 DQ11	DE21	IO, DIFF_TX_2C2P, DQ8N8	IO, CDR_DIFF_RX_2C15N, DQ12	CK29
	DDR4 DIMM1 DQ8	DF20	IO, CDR_DIFF_RX_2C3N, DQ8	IO, DIFF_TX_2C15N, DQ12	CP29
Byte6: 48-55	DDR4 DIMM1 DQ9	DJ21	IO, CDR_DIFF_RX_2C3P, DQ8	IO, CDR_DIFF_RX_2C15P, DQ12	CK29
	DDR4 DIMM1 DQ10	DH20	IO, DIFF_TX_2C3N, DQ8	IO, DIFF_TX_2C16N, DQ13	CL31
	DDR4 DIMM1 DQ54	DA21	IO, DIFF_TX_2C3P, DQ8	IO, CDR_DIFF_RX_2C16P, DQ13	CK29
	DDR4 DIMM1 DQ52	CY20	IO, DIFF_RX_2C4N, DQ9	IO, DIFF_TX_2C16N, DQ13	CK29
	DDR4 DIMM1 DQ53	CC21	IO, DIFF_RX_2C4P, DQ9	IO, DIFF_TX_2C16P, DQ13	CK29
	DDR4 DIMM1 DQ55	DD20	IO, DIFF_TX_2C4N, DQ9	IO, DIFF_RX_2C17N, DQ13	CK29
	DDR4 DIMM1 TDOS N15	DA23	IO, DIFF_RX_2C5N, DQ9	IO, DIFF_RX_2C17P, DQ13	CK29
	DDR4 DIMM1 DBI N5	CY22	IO, DIFF_RX_2C5P, DQ9	IO, DIFF_TX_2C17N, DQ13	CK29
	DDR4 DIMM1 DQ5 N5	DC23	IO, DIFF_RX_2C5P, DQ9	IO, DIFF_TX_2C17P, DQ13	CK29
	DDR4 DIMM1 DQ5 P6	DD22	IO, PLL_2C_T_CLKOUT1N, DIFF_TX_2C5N, DQ8N8	IO, PLL_2C_B_CLKOUT1P, PLL_2C_B_CLKOUT1, PLL_2C_B_FB1, DIFF_TX_2C5P, DQ8N9	CK29
Byte1: 32-39	DDR4 DIMM1 DQ57	DA25	IO, PLL_2C_T_CLKOUT1P, PLL_2C_T_CLKOUT1, PLL_2C_T_FB1, DIFF_TX_2C5P, DQ8N9	IO, PLL_2C_B_CLKOUT1P, PLL_2C_B_CLKOUT1, PLL_2C_B_FB1, DIFF_TX_2C5P, DQ8N9	CK29
	DDR4 DIMM1 DQ48	CY24	IO, CDR_DIFF_RX_2C6N, DQ9	IO, CDR_DIFF_RX_2C18N, DQ13	CK29
	DDR4 DIMM1 DQ50	CC25	IO, RZQ, B_2C, CDR_DIFF_RX_2C6P, DQ9	IO, RZQ, B_2C, CDR_DIFF_RX_2C18P, DQ13	CK29
	DDR4 DIMM1 DQ49	DD24	IO, CLK_T_2C_IN, DQ9	IO, CLK_B_2C_IN, DIFF_TX_2C18N, DQ13	CK29
	DDR4 DIMM1 DQ38	DE23	IO, CLK_T_2C_IP, DQ9	IO, CLK_B_2C_IP, DIFF_TX_2C18P, DQ13	CK29
	DDR4 DIMM1 DQ37	DF22	IO, CLK_T_2C_IN, DQ10	IO, CLK_B_2C_IN, CDR_DIFF_RX_2C18N, DQ14	CK29
	DDR4 DIMM1 DQ38	DJ23	IO, CLK_T_2C_OP, DQ10	IO, CLK_B_2C_OP, CDR_DIFF_RX_2C18P, DQ14	CK29
	DDR4 DIMM1 DQ39	DH22	IO, DIFF_TX_2C7N, DQ10	IO, DIFF_TX_2C19N, DQ14	CK29
	DDR4 DIMM1 TDOS N13	DE25	IO, DIFF_TX_2C7P, DQ10	IO, DIFF_TX_2C19P, DQ14	CK29
	DDR4 DIMM1 DBI N4	DF24	IO, PLL_2C_T_CLKOUT0N, DIFF_RX_2C8N, DQ10	IO, PLL_2C_B_CLKOUT0N, DIFF_RX_2C20N, DQ14	CK29
Byte1: 0-7	DDR4 DIMM1 DQ5 N4	DJ25	IO, PLL_2C_T_CLKOUT0P, PLL_2C_T_CLKOUT0, PLL_2C_T_FB0, DIFF_RX_2C8P, DQ10	IO, PLL_2C_B_CLKOUT0P, PLL_2C_B_CLKOUT0, PLL_2C_B_FB0, DIFF_RX_2C20P, DQ14	CK29
	DDR4 DIMM1 DQ5 P4	DH24	IO, DIFF_TX_2C8N, DQ8N10	IO, DIFF_TX_2C20N, DQ8N14	CK29
	DDR4 DIMM1 DQ33	DE27	IO, DIFF_TX_2C8P, DQ8N10	IO, DIFF_TX_2C20P, DQ8N14	CK29
	DDR4 DIMM1 DQ34	DF26	IO, CDR_DIFF_RX_2C9N, DQ10	IO, CDR_DIFF_RX_2C21N, DQ14	CK29
	DDR4 DIMM1 DQ35	DJ27	IO, CDR_DIFF_RX_2C9P, DQ10	IO, DIFF_TX_2C21N, DQ14	CK29
	DDR4 DIMM1 DQ32	DH26	IO, DIFF_TX_2C9P, DQ10	IO, CDR_DIFF_RX_2C22N, DQ15	CK29
	DDR4 DIMM1 DQ4	DA27	IO, DIFF_TX_2C10N, DQ11	IO, CDR_DIFF_RX_2C22P, DQ15	CK29
	DDR4 DIMM1 DQ5	CY26	IO, DIFF_RX_2C10P, DQ11	IO, DIFF_TX_2C22N, DQ15	CK29
	DDR4 DIMM1 DQ6	CC27	IO, DIFF_TX_2C10P, DQ11	IO, DIFF_TX_2C22P, DQ15	CK29
	DDR4 DIMM1 DQ7	DD26	IO, DIFF_TX_2C10P, DQ11	IO, DIFF_RX_2C23N, DQ15	CK29
Byte1: 0-7	DDR4 DIMM1 TDOS N9	DA29	IO, DIFF_RX_2C11N, DQ11	IO, DIFF_RX_2C23P, DQ15	CK29
	DDR4 DIMM1 DBI N0	CY28	IO, DIFF_RX_2C11P, DQ11	IO, DIFF_TX_2C23P, DQ15	CK29
	DDR4 DIMM1 DQ5 P0	DD28	IO, DIFF_TX_2C11N, DQ8N11	IO, DIFF_TX_2C23P, DQ15	CK29
	DDR4 DIMM1 DQ3	DA31	IO, CDR_DIFF_RX_2C12N, DQ11	IO, CDR_DIFF_RX_2C24N, DQ15	CK29
	DDR4 DIMM1 DQ2	CY30	IO, CDR_DIFF_RX_2C12P, DQ11	IO, CDR_DIFF_RX_2C24P, DQ15	CK29
	DDR4 DIMM1 DQ0	DC31	IO, DIFF_TX_2C12N, DQ11	IO, DIFF_TX_2C24N, DQ15	CK29
	DDR4 DIMM1 DQ1	DD30	IO, DIFF_TX_2C12P, DQ11	IO, DIFF_TX_2C24P, DQ15	CK29
					CK29
					CK29
					CK29

Place near R20 pin



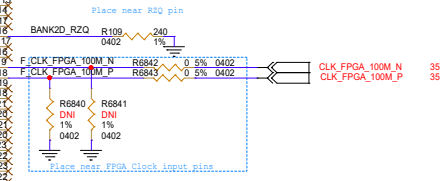
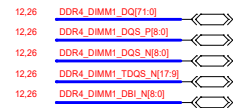
BANK 2C available in both FM86, FM76

External termination for tuning since OCT +/-40ohm accuracy.  
OCT should be turned off when external termination is used



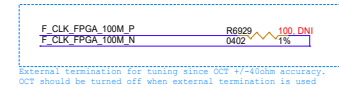
		U8C	
Byte2: 16-23	DDR4_DIMM1_DQ21	DE3	IO, DIFF_RX_2D1N, DQ0
	DDR4_DIMM1_DQ26	DE2	IO, DIFF_RX_2D1P, DQ0
	DDR4_DIMM1_DQ23	DE5	IO, DIFF_TX_2D1N, DQ0
	DDR4_DIMM1_DQ22	DF4	IO, DIFF_TX_2D1P, DQ0
	DDR4_DIMM1_DQS_N11	DE7	IO, DIFF_RX_2D2N, DQ0
	DDR4_DIMM1_DBI_N2	DF6	IO, DIFF_RX_2D2P, DQ0
	DDR4_DIMM1_DQS_N2	DJ7	IO, DIFF_TX_2D2N, DQ0
	DDR4_DIMM1_DQS_P2	DH6	IO, DIFF_TX_2D2P, DQ0
	DDR4_DIMM1_DQ18	DE9	IO, CDR, DIFF_RX_2D3N, DQ0
	DDR4_DIMM1_DQ16	DF8	IO, CDR, DIFF_RX_2D3P, DQ0
Byte7: 56-63	DDR4_DIMM1_DQ19	DJ9	IO, DIFF_TX_2D3N, DQ0
	DDR4_DIMM1_DQ17	DH8	IO, DIFF_RX_2D4N, DQ1
	DDR4_DIMM1_DQ21	DA0	IO, DIFF_TX_2D4P, DQ1
	DDR4_DIMM1_DQ22	CY8	IO, DIFF_TX_2D4N, DQ1
	DDR4_DIMM1_DQ20	DC9	IO, DIFF_TX_2D4P, DQ1
	DDR4_DIMM1_DQ23	DQ9	IO, DIFF_TX_2D4N, DQ1
	DDR4_DIMM1_DQS_N16	DA11	IO, DIFF_TX_2D4P, DQ1
	DDR4_DIMM1_DBI_N7	CY10	IO, DIFF_TX_2D4N, DQ1
	DDR4_DIMM1_DQS_N7	DC11	IO, DIFF_RX_2D5P, DQ1
	DDR4_DIMM1_DQS_P7	DD10	IO, PLL_2D_T_CLKOUT1N, DIFF_TX_2D5N, DQS_N1
Byte3: 24-31	DDR4_DIMM1_DQ58	DA13	IO, PLL_2D_T_CLKOUT1P, PLL_2D_T_CLKOUT1, PLL_2D_T_FB1, DIFF_TX_2D5P, DQS1
	DDR4_DIMM1_DQ56	CY12	IO, CDR, DIFF_RX_2D6N, DQ1
	DDR4_DIMM1_DQ57	DC13	IO, RZQ_T_2D, CDR, DIFF_RX_2D6P, DQ1
	DDR4_DIMM1_DQ59	DD12	IO, CLK_T_2D_1N, DIFF_TX_2D6N, DQ1
	DDR4_DIMM1_DQ31	DE11	IO, CLK_T_2D_1P, DIFF_TX_2D6P, DQ1
	DDR4_DIMM1_DQ28	DF10	IO, CLK_T_2D_0N, DIFF_RX_2D7N, DQ2
	DDR4_DIMM1_DQ30	DJ11	IO, CLK_T_2D_0P, DIFF_RX_2D7P, DQ2
	DDR4_DIMM1_DQ29	DH10	IO, DIFF_TX_2D7N, DQ2
	DDR4_DIMM1_DQS_N12	DE13	IO, DIFF_TX_2D7P, DQ2
	DDR4_DIMM1_DBI_N3	DF12	IO, PLL_2D_T_CLKOUT0N, DIFF_RX_2D8N, DQ2
Byte5: 40-47	DDR4_DIMM1_DQ53	DJ13	IO, PLL_2D_T_CLKOUT0P, PLL_2D_T_CLKOUT0, PLL_2D_T_FB0, DIFF_RX_2D8P, DQ2
	DDR4_DIMM1_DQS_P3	DH12	IO, DIFF_TX_2D8N, DQS_N2
	DDR4_DIMM1_DQ24	DE15	IO, DIFF_TX_2D8P, DQS2
	DDR4_DIMM1_DQ25	DF14	IO, CDR, DIFF_RX_2D9N, DQ2
	DDR4_DIMM1_DQ26	DJ15	IO, CDR, DIFF_RX_2D9P, DQ2
	DDR4_DIMM1_DQ27	DH14	IO, DIFF_TX_2D9N, DQ2
	DDR4_DIMM1_DQ45	DA15	IO, DIFF_TX_2D9P, DQ2
	DDR4_DIMM1_DQ44	CY14	IO, DIFF_RX_2D10N, DQ3
	DDR4_DIMM1_DQ46	DC15	IO, DIFF_TX_2D10P, DQ3
	DDR4_DIMM1_DQ47	DD14	IO, DIFF_TX_2D10N, DQ3

IO, CDR, DIFF_RX_2D13N, DQ4	CL13
IO, CDR, DIFF_RX_2D13P, DQ4	CL14
IO, DIFF_TX_2D13N, DQ4	CL15
IO, DIFF_TX_2D13P, DQ4	CL16
IO, DIFF_RX_2D14N, DQ4	CL17
IO, DIFF_RX_2D14P, DQ4	CL18
IO, DIFF_TX_2D14N, DQS_N4	CL19
IO, DIFF_TX_2D14P, DQS_P4	CL20
IO, CDR, DIFF_RX_2D15N, DQ4	CL21
IO, CDR, DIFF_RX_2D15P, DQ4	CL22
IO, DIFF_TX_2D15N, DQ4	CL23
IO, DIFF_TX_2D15P, DQ4	CL24
IO, CDR, DIFF_RX_2D16N, DQ5	CL25
IO, CDR, DIFF_RX_2D16P, DQ5	CL26
IO, DIFF_TX_2D16N, DQ5	CL27
IO, DIFF_TX_2D16P, DQ5	CL28
IO, DIFF_RX_2D17N, DQ5	CL29
IO, DIFF_RX_2D17P, DQ5	CL30
IO, PLL_2D_B_CLKOUT1N, DIFF_TX_2D17N, DQS_N5	CL31
IO, PLL_2D_B_CLKOUT1P, PLL_2D_B_CLKOUT1, PLL_2D_B_FB1, DIFF_TX_2D17P, DQS_P5	CL32
IO, CDR, DIFF_RX_2D18N, DQ5	CL33
IO, RZQ_T_2D, CDR, DIFF_RX_2D18P, DQ5	CL34
IO, CLK_B_2D_1N, DIFF_TX_2D18N, DQ5	CL35
IO, CLK_B_2D_1P, DIFF_TX_2D18P, DQ5	CL36
IO, CLK_B_2D_0N, CDR, DIFF_RX_2D19N, DQ5	CL37
IO, CLK_B_2D_0P, CDR, DIFF_RX_2D19P, DQ5	CL38
IO, DIFF_TX_2D19N, DQ6	CL39
IO, DIFF_TX_2D19P, DQ6	CL40
IO, PLL_2D_B_CLKOUT0N, DIFF_RX_2D20N, DQ6	CL41
IO, PLL_2D_B_CLKOUT0P, PLL_2D_B_CLKOUT0, PLL_2D_B_FB0, DIFF_RX_2D20P, DQ6	CL42
IO, DIFF_TX_2D20N, DQS_N6	CL43
IO, DIFF_TX_2D20P, DQS_P6	CL44
IO, CDR, DIFF_RX_2D21N, DQ6	CL45
IO, CDR, DIFF_RX_2D21P, DQ6	CL46
IO, DIFF_TX_2D21N, DQ6	CL47
IO, DIFF_TX_2D21P, DQ6	CL48
IO, CDR, DIFF_RX_2D22N, DQ7	CL49
IO, CDR, DIFF_RX_2D22P, DQ7	CL50
IO, DIFF_TX_2D22N, DQ7	CL51
IO, DIFF_TX_2D22P, DQ7	CL52
IO, DIFF_RX_2D23N, DQ7	CL53
IO, DIFF_RX_2D23P, DQ7	CL54
IO, DIFF_TX_2D23N, DQS_N7	CL55
IO, DIFF_TX_2D23P, DQS_P7	CL56
IO, CDR, DIFF_RX_2D24N, DQ7	CL57
IO, CDR, DIFF_RX_2D24P, DQ7	CL58
IO, DIFF_TX_2D24N, DQ7	CL59
IO, DIFF_TX_2D24P, DQ7	CL60



ECU: 64-71

BANK 2D available in both FM86, FM76

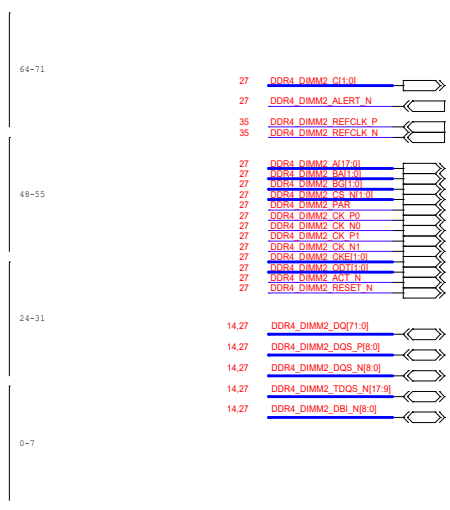
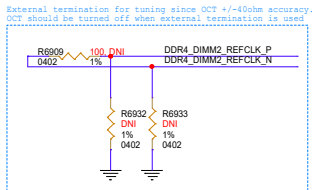


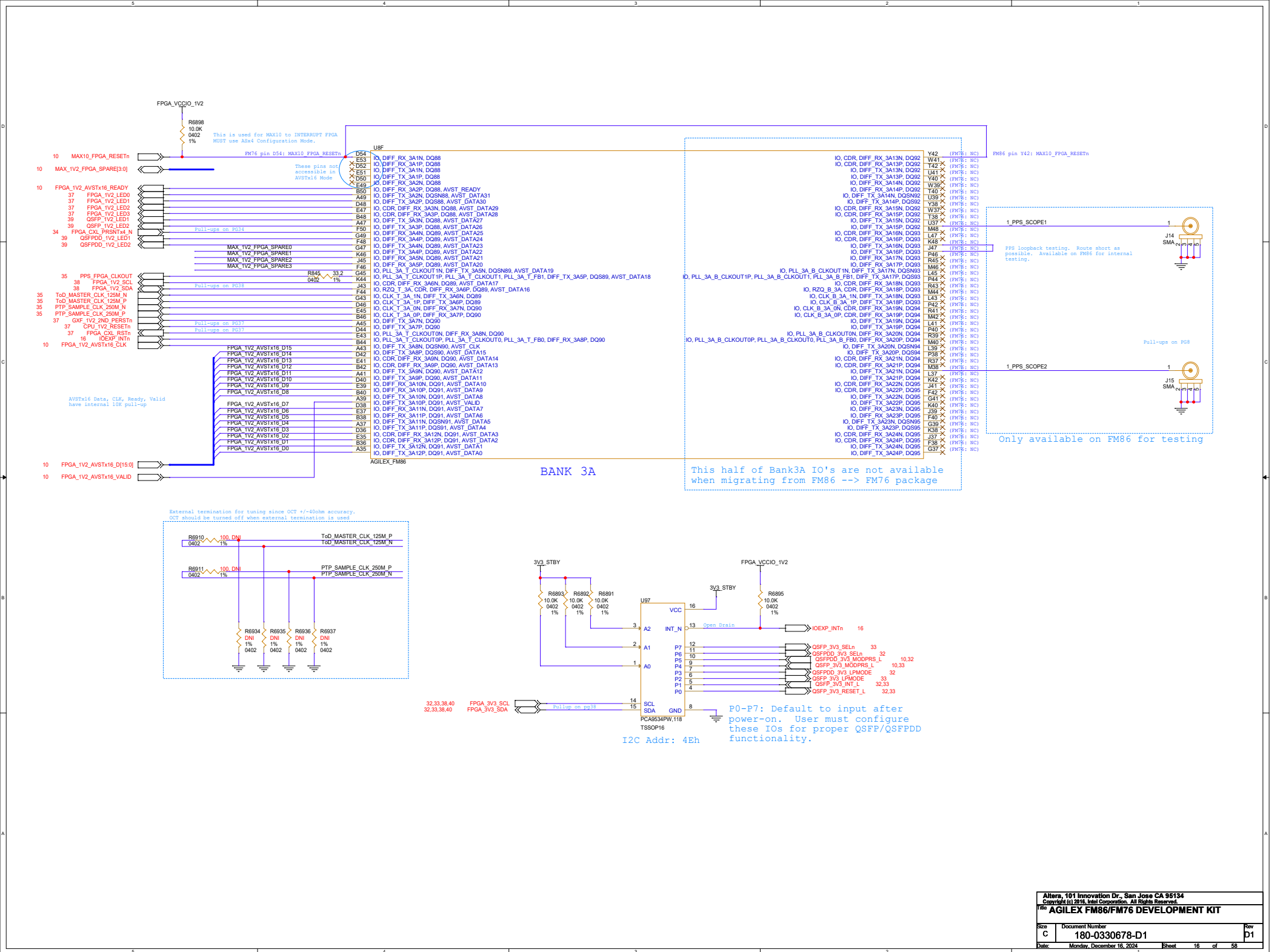
		UBD			
(F7671: NC)		D0R4 DMM2 D045	DA65	IO, DIFF_RX_2E10N, DQ24	DE45 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D044	CY54	IO, DIFF_RX_2E10N, DQ24	DE44 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D047	DC55	IO, DIFF_RX_2E10P, DQ24	DJ45 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D046	DC54	IO, DIFF_TX_2E10N, DQ22	DJ44 (F7671: NC)
(F7671: NC)		D0R4 DMM2 TDG3 N14	DA53	IO, DIFF_TX_2E10P, DQ24	DE43 (F7671: NC)
(F7671: NC)		D0R4 DMM2 DBI N5	CY52	IO, DIFF_RX_2E10N, DQ22	DJ43 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D08 N6	DC53	IO, DIFF_RX_2E10P, DQ22	DE42 (F7671: NC)
(F7671: NC)	40-47	D0R4 DMM2 D08 P5	DS52	IO, DIFF_TX_2E20N, DQ32N4	DH42 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D042	DA51	IO, DIFF_TX_2E20P, DQ32N4	DH41 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D040	DC51	IO, CDR, DIFF_RX_2E30N, DQ24	DE41 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D041	DC51	IO, CDR, DIFF_RX_2E12P, DQ22	DJ41 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D043	DA50	IO, CDR, DIFF_RX_2E10P, DQ22	DJ40 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D060	DE53	IO, DIFF_TX_2E30P, DQ24	CN53 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D061	DF52	IO, DIFF_RX_2E40N, DQ25	CM52 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D062	DC51	IO, DIFF_RX_2E40P, DQ25	CM51 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D063	DH50	IO, DIFF_TX_2E40N, DQ25	CT52 (F7671: NC)
(F7671: NC)		D0R4 DMM2 TDG3 N16	DE49	IO, DIFF_RX_2E40P, DQ25	CT51 (F7671: NC)
(F7671: NC)		D0R4 DMM2 DBI N7	DF48	IO, DIFF_RX_2E30N, DQ25	CL51 (F7671: NC)
(F7671: NC)	56-63	D0R4 DMM2 D08 N7	DJ49	IO, DIFF_RX_2E30P, DQ25	CL50 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D08 P7	DH49	IO, PLL_2E_T_CLKOUT1N, DIFF_TX_2E50N, DQ32N5	CM50 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D057	DE47	IO, PLL_2E_T_CLKOUT1P, PLL_2E_T_CLKOUT1P, PLL_2E_T_F80, DIFF_TX_2E50P, DQ32S5	CN51 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D056	DF46	IO, CDR, DIFF_RX_2E50N, DQ25	CM51 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D060	DA47	IO, R20_1_2E_CDR, DIFF_RX_2E60P, DQ25	CM50 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D058	DH46	IO, CLK_1_2E_IN, DIFF_TX_2E60N, DQ25	CL49 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D012	DA48	IO, CLK_1_2E_P, DIFF_TX_2E60P, DQ25	CK48 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D015	CY49	IO, CLK_1_2E_P, DIFF_RX_2E70N, DQ26	CK47 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D015	DC49	IO, CLK_1_2E_OP, DIFF_RX_2E70P, DQ26	CK46 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D014	DF48	IO, DIFF_TX_2E70N, DQ26	CN47 (F7671: NC)
(F7671: NC)		D0R4 DMM2 TDG3 N10	DA47	IO, DIFF_TX_2E70P, DQ26	CN46 (F7671: NC)
(F7671: NC)		D0R4 DMM2 DBI N7	CY46	IO, PLL_2E_T_CLKOUT0N, DIFF_RX_2E50N, DQ26	CN45 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D08 N7	DF47	IO, PLL_2E_T_CLKOUT0P, PLL_2E_T_CLKOUT0P, PLL_2E_T_F80, DIFF_RX_2E60P, DQ26	CN44 (F7671: NC)
(F7671: NC)	8-15	D0R4 DMM2 D08 P1	DD46	IO, DIFF_TX_2E60N, DQ32N6	CN45 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D08	DA45	IO, DIFF_TX_2E60P, DQ32N6	CK49 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D011	CT44	IO, CDR, DIFF_TX_2E34N, DQ31	CK48 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D09	DC45	IO, CDR, DIFF_RX_2E34P, DQ31	CK47 (F7671: NC)
(F7671: NC)		D0R4 DMM2 D010	DD44	IO, DIFF_TX_2E34N, DQ31	CN48 (F7671: NC)
(F7671: NC)				IO, DIFF_TX_2E34P, DQ31	CN49 (F7671: NC)
AGILEX_FM86					

BANK 2E available only in FM86, not FM76



BANK 2F available in both FM86, FM76





Bank3B is not available in Agilex FM76.  
So no IO's will be used to support Migration from FM86 --> FM76.

U8G		
(FM76: NC)	X K36	IO, DIFF_RX_3B1N, DQ80
(FM76: NC)	X J35	IO, DIFF_RX_3B1P, DQ80
(FM76: NC)	X F36	IO, DIFF_TX_3B1N, DQ80
(FM76: NC)	X G35	IO, DIFF_TX_3B1P, DQ80
(FM76: NC)	X K34	IO, DIFF_RX_3B2N, DQ80
(FM76: NC)	X J33	IO, DIFF_RX_3B2P, DQ80
(FM76: NC)	X F34	IO, DIFF_TX_3B2N, DQ80
(FM76: NC)	X G33	IO, DIFF_TX_3B2P, DQ80
(FM76: NC)	X K32	IO, CDR, DIFF_RX_3B3N, DQ80
(FM76: NC)	X J31	IO, CDR, DIFF_RX_3B3P, DQ80
(FM76: NC)	X F32	IO, DIFF_TX_3B3N, DQ80
(FM76: NC)	X G31	IO, DIFF_TX_3B3P, DQ80
(FM76: NC)	X D34	IO, DIFF_RX_3B4N, DQ81
(FM76: NC)	X E33	IO, DIFF_RX_3B4P, DQ81
(FM76: NC)	X R34	IO, DIFF_TX_3B4N, DQ81
(FM76: NC)	X A33	IO, DIFF_TX_3B4P, DQ81
(FM76: NC)	X D32	IO, DIFF_RX_3B5N, DQ81
(FM76: NC)	X E31	IO, DIFF_RX_3B5P, DQ81
(FM76: NC)	X B32	IO, PLL_3B_T_CLKOUT1N, DIFF_TX_3B5N, DQ81
(FM76: NC)	X A31	IO, PLL_3B_T_CLKOUT1P, PLL_3B_T_CLKOUT1, PLL_3B_T_FB1, DIFF_TX_3B5P, DQ81
(FM76: NC)	X D30	IO, CDR, DIFF_RX_3B6N, DQ81
(FM76: NC)	X E29	IO, RZQ, T_3B, CDR, DIFF_RX_3B6P, DQ81
(FM76: NC)	X B30	IO, CLK, T_3B_1N, DIFF_TX_3B6N, DQ81
(FM76: NC)	X A29	IO, CLK, T_3B_1P, DIFF_TX_3B6P, DQ81
(FM76: NC)	X K30	IO, CLK, T_3B_0N, CDR, DIFF_RX_3B7N, DQ82
(FM76: NC)	X J29	IO, CLK, T_3B_0P, CDR, DIFF_RX_3B7P, DQ82
(FM76: NC)	X F30	IO, DIFF_TX_3B7N, DQ82
(FM76: NC)	X G29	IO, DIFF_TX_3B7P, DQ82
(FM76: NC)	X K28	IO, PLL_3B_T_CLKOUT0N, DIFF_RX_3B8N, DQ82
(FM76: NC)	X J27	IO, PLL_3B_T_CLKOUT0P, PLL_3B_T_CLKOUT0, PLL_3B_T_FB0, DIFF_RX_3B8P, DQ82
(FM76: NC)	X F28	IO, DIFF_TX_3B8N, DQ82
(FM76: NC)	X G27	IO, DIFF_TX_3B8P, DQ82
(FM76: NC)	X K26	IO, CDR, DIFF_RX_3B9N, DQ82
(FM76: NC)	X J25	IO, CDR, DIFF_RX_3B9P, DQ82
(FM76: NC)	X F26	IO, DIFF_TX_3B9N, DQ82
(FM76: NC)	X G25	IO, DIFF_TX_3B9P, DQ82
(FM76: NC)	X D28	IO, DIFF_RX_3B10N, DQ83
(FM76: NC)	X E27	IO, DIFF_RX_3B10P, DQ83
(FM76: NC)	X B28	IO, DIFF_TX_3B10N, DQ83
(FM76: NC)	X A27	IO, DIFF_TX_3B10P, DQ83
(FM76: NC)	X D26	IO, DIFF_RX_3B11N, DQ83
(FM76: NC)	X E25	IO, DIFF_RX_3B11P, DQ83
(FM76: NC)	X B26	IO, DIFF_TX_3B11N, DQ83
(FM76: NC)	X A25	IO, DIFF_TX_3B11P, DQ83
(FM76: NC)	X D24	IO, CDR, DIFF_RX_3B12N, DQ83
(FM76: NC)	X E23	IO, CDR, DIFF_RX_3B12P, DQ83
(FM76: NC)	X B24	IO, DIFF_TX_3B12N, DQ83
(FM76: NC)	X A23	IO, DIFF_TX_3B12P, DQ83

AGILEX_FM86		
(FM76: NC)	X K36	IO, CDR, DIFF_RX_3B13N, DQ84
(FM76: NC)	X J35	IO, CDR, DIFF_RX_3B13P, DQ84
(FM76: NC)	X F36	IO, DIFF_TX_3B13N, DQ84
(FM76: NC)	X G35	IO, DIFF_TX_3B13P, DQ84
(FM76: NC)	X K34	IO, DIFF_RX_3B14N, DQ84
(FM76: NC)	X J33	IO, DIFF_RX_3B14P, DQ84
(FM76: NC)	X F34	IO, DIFF_TX_3B14N, DQ84
(FM76: NC)	X G33	IO, DIFF_TX_3B14P, DQ84
(FM76: NC)	X K32	IO, CDR, DIFF_RX_3B15N, DQ84
(FM76: NC)	X J31	IO, CDR, DIFF_RX_3B15P, DQ84
(FM76: NC)	X F32	IO, DIFF_TX_3B15N, DQ84
(FM76: NC)	X G31	IO, DIFF_TX_3B15P, DQ84
(FM76: NC)	X D34	IO, CDR, DIFF_RX_3B16N, DQ85
(FM76: NC)	X E33	IO, CDR, DIFF_RX_3B16P, DQ85
(FM76: NC)	X R34	IO, DIFF_TX_3B16N, DQ85
(FM76: NC)	X A33	IO, DIFF_TX_3B16P, DQ85
(FM76: NC)	X D32	IO, DIFF_RX_3B17N, DQ85
(FM76: NC)	X E31	IO, DIFF_RX_3B17P, DQ85
(FM76: NC)	X B32	IO, PLL_3B_B_CLKOUT1N, DIFF_TX_3B17N, DQ85
(FM76: NC)	X A31	IO, PLL_3B_B_CLKOUT1P, PLL_3B_B_FB1, DIFF_TX_3B17P, DQ85
(FM76: NC)	X D30	IO, CDR, DIFF_RX_3B18N, DQ85
(FM76: NC)	X E29	IO, RZQ, T_3B, CDR, DIFF_RX_3B18P, DQ85
(FM76: NC)	X B30	IO, CLK, B_3B_1N, DIFF_TX_3B18N, DQ85
(FM76: NC)	X A29	IO, CLK, B_3B_1P, DIFF_TX_3B18P, DQ85
(FM76: NC)	X K30	IO, CLK, B_3B_0N, CDR, DIFF_RX_3B19N, DQ86
(FM76: NC)	X J29	IO, CLK, B_3B_0P, CDR, DIFF_RX_3B19P, DQ86
(FM76: NC)	X F30	IO, DIFF_TX_3B19N, DQ86
(FM76: NC)	X G29	IO, DIFF_TX_3B19P, DQ86
(FM76: NC)	X K28	IO, PLL_3B_B_CLKOUT0N, DIFF_RX_3B20N, DQ86
(FM76: NC)	X J27	IO, PLL_3B_B_CLKOUT0P, PLL_3B_B_FB0, DIFF_RX_3B20P, DQ86
(FM76: NC)	X F28	IO, DIFF_TX_3B20N, DQ86
(FM76: NC)	X G27	IO, DIFF_TX_3B20P, DQ86
(FM76: NC)	X K26	IO, CDR, DIFF_RX_3B21N, DQ86
(FM76: NC)	X J25	IO, CDR, DIFF_RX_3B21P, DQ86
(FM76: NC)	X F26	IO, DIFF_TX_3B21N, DQ86
(FM76: NC)	X G25	IO, DIFF_TX_3B21P, DQ86
(FM76: NC)	X D28	IO, CDR, DIFF_RX_3B22N, DQ87
(FM76: NC)	X E27	IO, CDR, DIFF_RX_3B22P, DQ87
(FM76: NC)	X B28	IO, DIFF_TX_3B22N, DQ87
(FM76: NC)	X A27	IO, DIFF_TX_3B22P, DQ87
(FM76: NC)	X D26	IO, DIFF_RX_3B23N, DQ87
(FM76: NC)	X E25	IO, DIFF_RX_3B23P, DQ87
(FM76: NC)	X B26	IO, DIFF_TX_3B23N, DQ87
(FM76: NC)	X A25	IO, DIFF_TX_3B23P, DQ87
(FM76: NC)	X D24	IO, CDR, DIFF_RX_3B24N, DQ87
(FM76: NC)	X E23	IO, CDR, DIFF_RX_3B24P, DQ87
(FM76: NC)	X B24	IO, DIFF_TX_3B24N, DQ87
(FM76: NC)	X A23	IO, DIFF_TX_3B24P, DQ87

BANK 3B available only in FM86, not FM76

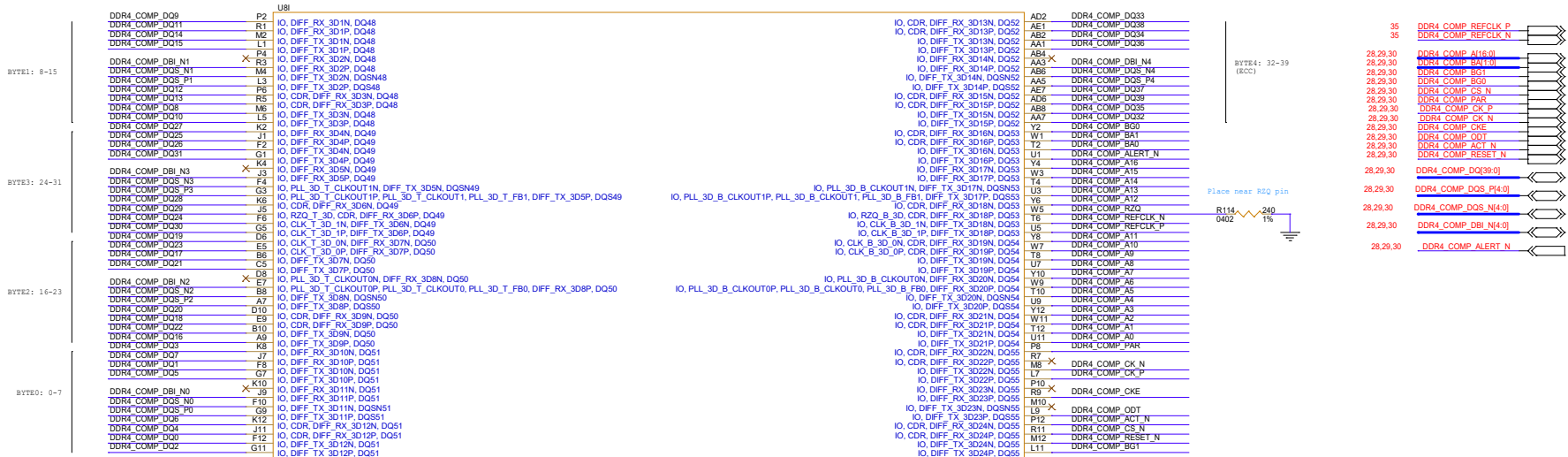
Bank3C is not available in Agilex FM76.  
So no IO's will be used to support Migration from FM86 --> FM76.

Only half of Bank3C migrates from FM86 --> FM76

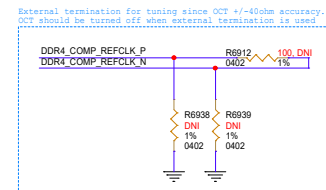
USH			
(FM76: NC)	X D12	IO, DIFF_RX_3C1N, DQ56	Y14
(FM76: NC)	X E11	IO, DIFF_RX_3C1P, DQ56	W15
(FM76: NC)	X B12	IO, DIFF_TX_3C1N, DQ56	T14
(FM76: NC)	X A11	IO, DIFF_TX_3C1N, DQ56	U13
(FM76: NC)	X D14	IO, DIFF_TX_3C1P, DQ56	Y16
(FM76: NC)	X E13	IO, DIFF_RX_3C2N, DQ56	W15
(FM76: NC)	X B14	IO, DIFF_RX_3C2P, DQ56	T16
(FM76: NC)	X A13	IO, DIFF_TX_3C2N, DQ56	U15
(FM76: NC)	X D16	IO, DIFF_TX_3C2P, DQ56	W18
(FM76: NC)	X E15	IO, CDR, DIFF_RX_3C3N, DQ56	Y18
(FM76: NC)	X B16	IO, CDR, DIFF_RX_3C3P, DQ56	T18
(FM76: NC)	X A15	IO, DIFF_TX_3C3N, DQ56	U17
(FM76: NC)	X D14	IO, DIFF_TX_3C3P, DQ56	Y17
(FM76: NC)	X J13	IO, DIFF_RX_3C4N, DQ57	R13
(FM76: NC)	X E14	IO, DIFF_RX_3C4P, DQ57	M14
(FM76: NC)	X C14	IO, DIFF_TX_3C4N, DQ57	L13
(FM76: NC)	X K16	IO, DIFF_TX_3C4P, DQ57	P16
(FM76: NC)	X J15	IO, DIFF_RX_3C5N, DQ57	R15
(FM76: NC)	X F16	IO, DIFF_RX_3C5P, DQ57	M16
(FM76: NC)	G15	IO, PLL_3C_T_CLKOUT1N, DIFF_TX_3C5N, DQ56	L15
(FM76: NC)	X K16	IO, PLL_3C_T_CLKOUT1P, PLL_3C_T_CLKOUT1, PLL_3C_T_FB1, DIFF_TX_3C5P, DQ57	F16
(FM76: NC)	X J17	IO, CDR, DIFF_RX_3C6N, DQ57	R17
(FM76: NC)	X F18	IO, R2Q, T_3C, CDR, DIFF_RX_3C6P, DQ57	M18
(FM76: NC)	G17	IO, CLK, T_3C, IN, DIFF_TX_3C6N, DQ57	L17
(FM76: NC)	X D16	IO, CLK, T_3C-1P, DIFF_TX_3C6P, DQ57	P16
(FM76: NC)	X E17	IO, CLK, T_3C-0N, DIFF_RX_3C7N, DQ58	R19
(FM76: NC)	X B18	IO, CLK, T_3C-0P, DIFF_RX_3C7P, DQ58	M20
(FM76: NC)	X A17	IO, DIFF_TX_3C7N, DQ58	L19
(FM76: NC)	D20	IO, DIFF_TX_3C7P, DQ58	P22
(FM76: NC)	X E19	IO, PLL_3C_T_CLKOUT0N, DIFF_RX_3C8N, DQ58	R21
(FM76: NC)	X B20	IO, PLL_3C_T_CLKOUT0P, PLL_3C_T_CLKOUT0, PLL_3C_T_FB0, DIFF_RX_3C8P, DQ58	M22
(FM76: NC)	X A19	IO, DIFF_TX_3C8N, DQ58	L21
(FM76: NC)	X D22	IO, DIFF_TX_3C8P, DQ58	P24
(FM76: NC)	X E21	IO, CDR, DIFF_RX_3C9N, DQ58	R23
(FM76: NC)	X B22	IO, CDR, DIFF_RX_3C9P, DQ58	M24
(FM76: NC)	X A21	IO, DIFF_TX_3C9N, DQ58	L23
(FM76: NC)	X K20	IO, DIFF_TX_3C9P, DQ58	Y20
(FM76: NC)	X F19	IO, DIFF_RX_3C10N, DQ59	W19
(FM76: NC)	X D20	IO, DIFF_RX_3C10P, DQ59	Y20
(FM76: NC)	X G19	IO, DIFF_TX_3C10N, DQ59	U19
(FM76: NC)	X D22	IO, DIFF_TX_3C10P, DQ59	Y22
(FM76: NC)	X J21	IO, DIFF_RX_3C11N, DQ59	W21
(FM76: NC)	X F22	IO, DIFF_RX_3C11P, DQ59	Y22
(FM76: NC)	X G21	IO, DIFF_TX_3C11N, DQ59	U21
(FM76: NC)	X D24	IO, DIFF_TX_3C11P, DQ59	Y24
(FM76: NC)	X J23	IO, CDR, DIFF_RX_3C12N, DQ59	W23
(FM76: NC)	X F24	IO, CDR, DIFF_RX_3C12P, DQ59	Y24
(FM76: NC)	X G23	IO, DIFF_TX_3C12N, DQ59	U23
(FM76: NC)	X	IO, DIFF_TX_3C12P, DQ59	Y24
AGILEX_FM86			

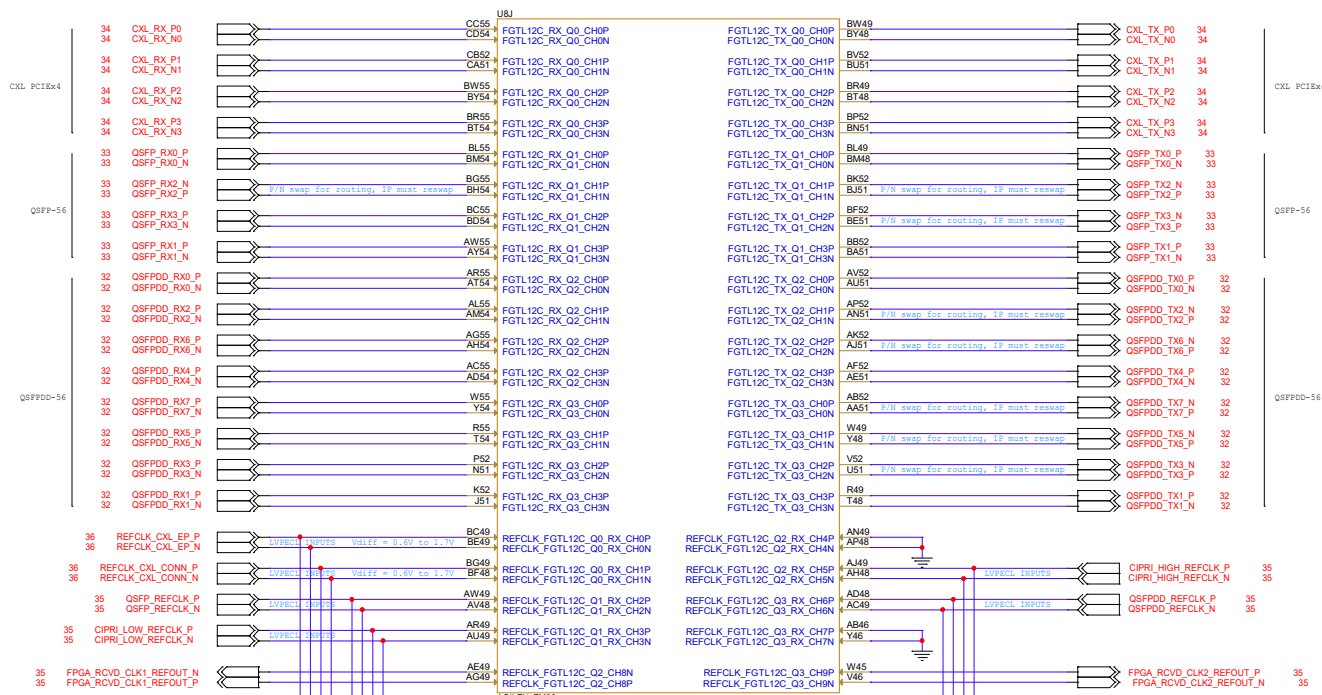
Not available in FM76

Available in FM86 and FM76

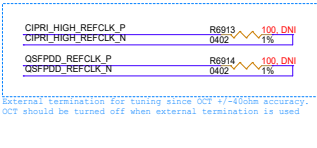
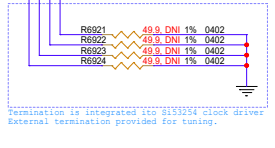
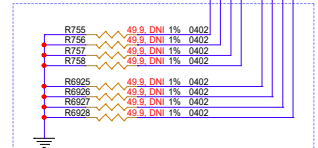
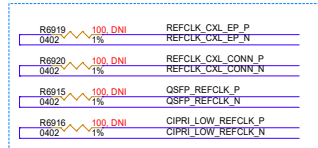


BANK 3D available in both FM86, FM76





### BANK 12C, F-TILE



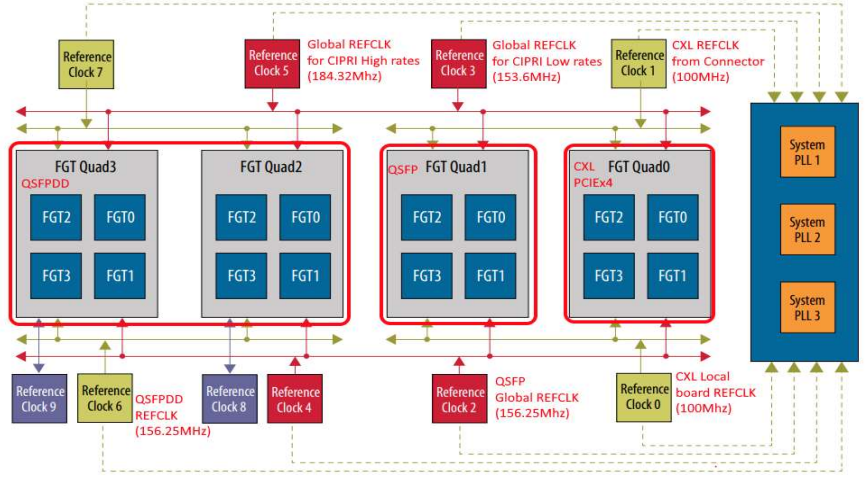
External termination for tuning since OCT +/-400m accuracy. OCT should be turned off when external termination is used

Termination is integrated into S153254 clock driver. External termination provided for tuning.

Termination is integrated into S153254 clock driver. External termination provided for tuning.

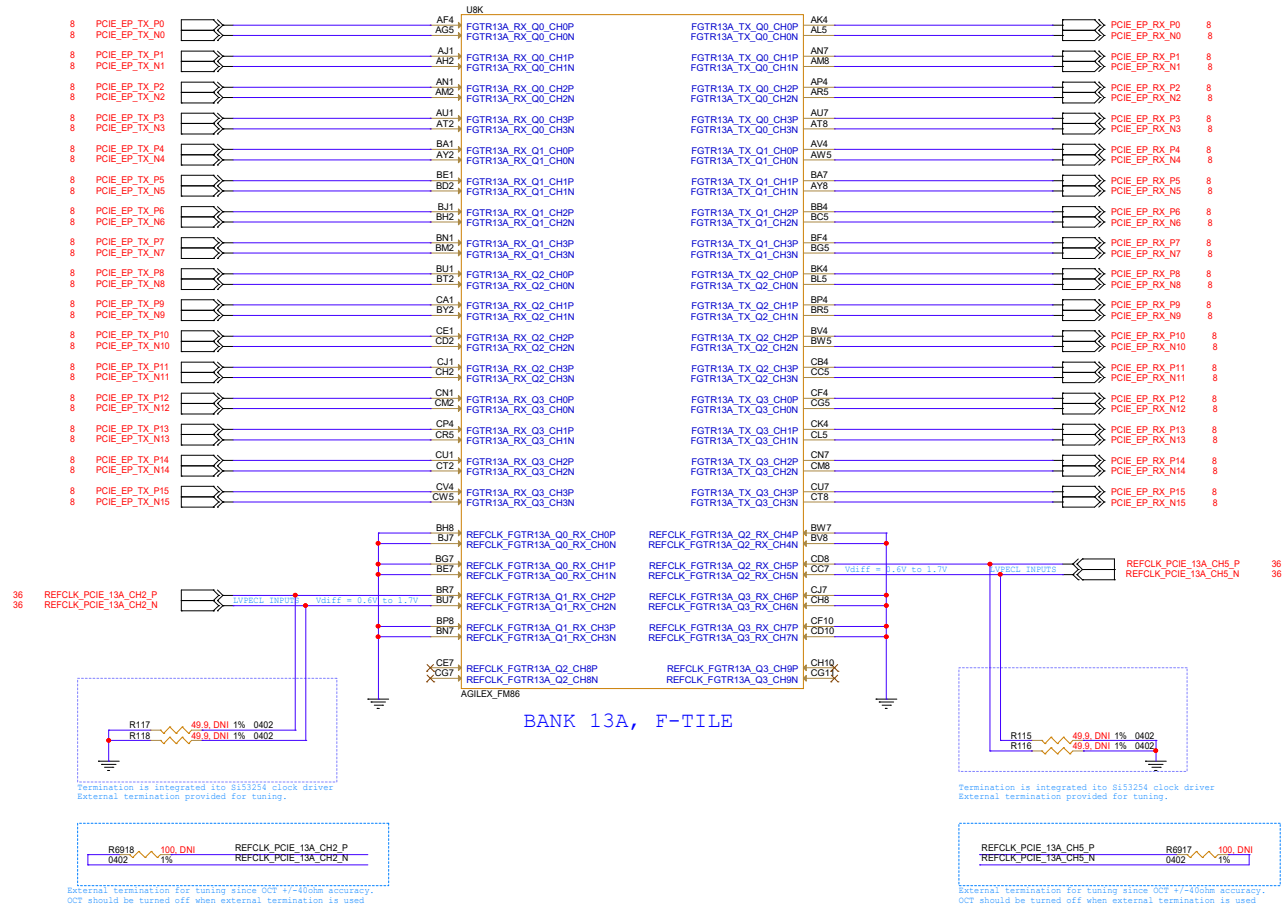
External termination for tuning since OCT +/-400m accuracy. OCT should be turned off when external termination is used

### FGT and System PLL Reference Clock Network



Global Reference Clock  
Regional Reference Clock  
Local Reference Clock (Bidirectional)  
RefClk to FGT PMA  
RefClk to System PLL







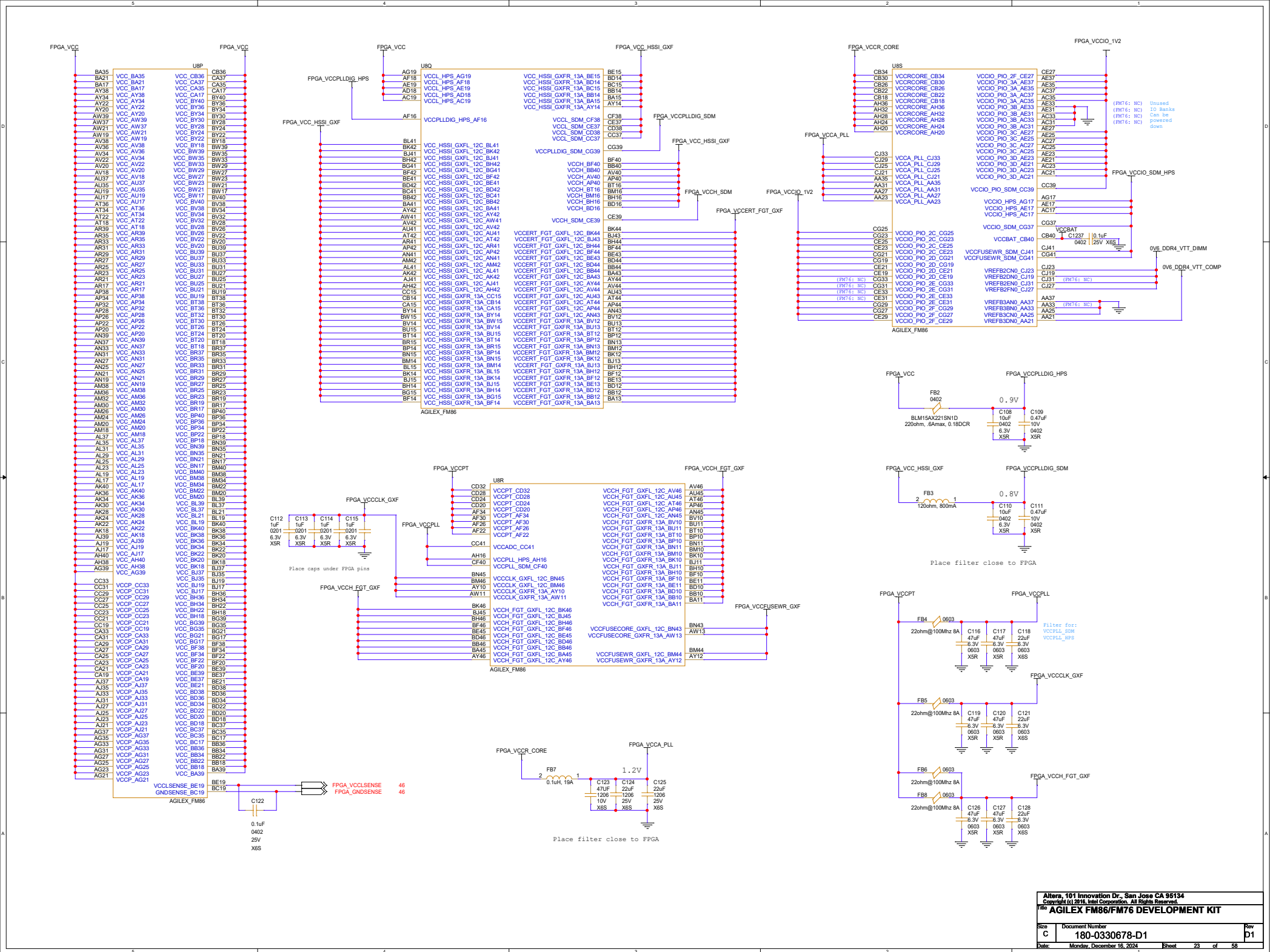


Diagram showing the pinout and internal connections of the AGILEX FM86/FM76 Development Kit. The diagram is organized into four main sections, each representing a different type of connector or interface:

- U8T (Top Left):** A 100-pin connector with pins labeled Y52 to H18. It includes a ground symbol at the bottom.
- U8U (Top Right):** A 100-pin connector with pins labeled CU37 to CF34. It includes a ground symbol at the bottom.
- U8V (Bottom Left):** A 100-pin connector with pins labeled BW53 to BU5. It includes a ground symbol at the bottom.
- U8W (Bottom Right):** A 100-pin connector with pins labeled AV8 to AH22. It includes a ground symbol at the bottom.

The diagram illustrates the internal connections between these connectors and the AGILEX FM86/FM76 Development Kit. The connections are shown as lines connecting the pins to the internal components of the kit. The diagram is labeled "AGILEX FM86/FM76 DEVELOPMENT KIT" at the bottom center.

# DDR4/DDR-T DIMM Pin Map

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	VTT	145	VTT	38	DQ24	182	VSS	75	CLK0#	219	CLK14	108	DQ40	252	VSS
2	VSS	146	VREFCA	39	VSS	183	DQ25	76	VDD	220	VDD	109	VSS	253	DQ41
3	DQ4	147	VSS	40	DQS12	184	VSS	77	VTT	221	VTT	110	DQS14	254	VSS
4	VSS	148	DQ5	41	DQS12#	185	DQS13#					111	DQS14#	255	DQS5#
5	DQ0	149	VSS	42	VSS	186	DQS3					112	VSS	256	DQS5
6	VSS	150	DQ1	43	DQ30	187	VSS					113	DQ45	257	VSS
7	DQS0	151	VSS	44	VSS	188	DQ31					114	VSS	258	DQ47
8	DQS0#	152	DQS0#	45	DQ26	189	VSS	78	EVENT	222	PARITY	115	DQ42	259	VSS
9	VSS	153	DQS0	46	VSS	190	DQ27	79	A0	223	VDD	116	VSS	260	DQ43
10	DQ6	154	VSS	47	CB4	191	VSS	80	VDD	224	BA1	117	DQ52	261	VSS
11	VSS	155	DQ7	48	VSS	192	CB5	81	BA0	225	A10	118	VSS	262	DQ53
12	DQ2	156	VSS	49	CB0	193	VSS	82	RASH/A16	226	VDD	119	DQ43	263	VSS
13	VSS	157	DQ3	50	VSS	194	CB1	83	VDD	227	RFU	120	VSS	264	DQ49
14	DQ12	158	VSS	51	DQS17	195	VSS	84	CS0#	228	WE#/A14	121	DQS15	265	VSS
15	VSS	159	DQ13	52	DQS17#	196	DQS8#	85	VDD	229	VDD	122	DQS15#	266	DQS6#
16	DQ8	160	VSS	53	VSS	197	DQS8	86	CASH/A15	230	SAVE#	123	VSS	267	DQS6
17	VSS	161	DQ9	54	CB6	198	VSS	87	ODT0	231	VDD	124	DQ54	268	VSS
18	DQS10	162	VSS	55	VSS	199	CB7	88	VDD	232	A13	125	VSS	269	DQS5
19	DQS10#	163	DQS1#	56	CB2	200	VSS	89	CS1#	233	VDD	126	DQ50	270	VSS
20	VSS	164	DQS1	57	VSS	201	CB3	90	VDD	234	A17	127	VSS	271	DQS1
21	DQ14	165	VSS	58	RESET#	202	VSS	91	ODT1	235	C2	128	DQ60	272	VSS
22	VSS	166	DQ15	59	VDD	203	CKE1	92	VDD	236	VDD	129	VSS	273	DQ51
23	DQ10	167	VSS	60	CKE0	204	VDD	93	C0	237	C1	130	DQ36	274	VSS
24	VSS	168	DQ11	61	VDD	205	RFU	94	VSS	238	SA2	131	VSS	275	DQ57
25	DQ20	169	VSS	62	ACT#	206	VDD	95	DQ36	239	VSS	132	DQS16	276	VSS
26	VSS	170	DQ21	63	BG0	207	BG1	96	VSS	240	DQ37	133	DQS16#	277	DQS7#
27	DQ16	171	VSS	64	VDD	208	ALERT#	97	DQ32	241	VSS	134	VSS	278	DQS7
28	VSS	172	DQ17	65	A12	209	VDD	98	VSS	242	DQ33	135	DQ52	279	VSS
29	DQS11	173	VSS	66	A9	210	A11	99	DQS13	243	VSS	136	VSS	280	DQ63
30	DQS11#	174	DQS2#	67	VDD	211	A7	100	DQS13#	244	DQS4#	137	DQ58	281	VSS
31	VSS	175	DQS2	68	A8	212	VDD	101	VSS	245	DC154	138	VSS	282	DQ59
32	DQ22	176	VSS	69	A6	213	A5	102	DQ38	246	VSS	139	SA0	283	VSS
33	VSS	177	DQ23	70	VDD	214	A4	103	VSS	247	DQ39	140	SA1	284	VDDSPD
34	DQ18	178	VSS	71	A3	215	VDD	104	DQ34	248	VSS	141	SCL	285	SDA
35	VSS	179	DQ19	72	A1	216	A2	105	VSS	249	DQ35	142	VPP	286	VPP
36	DQ28	180	VSS	73	VDD	217	VDD	106	DQ44	250	VSS	143	VPP	287	VPP
37	VSS	181	DQ29	74	CLK0	218	CLK1	107	VSS	251	DQ45	144	RFU	288	VPP

DDR-T DIMM Pin Map is Identical to standard DDR4 DIMM Pin Map except the DDR-T protocol repurposes five of these pins:

CS1# (pin 89) : Grant, GNT# <0> Input

CKE1 (pin 203) : Request, REQ# <0> Output

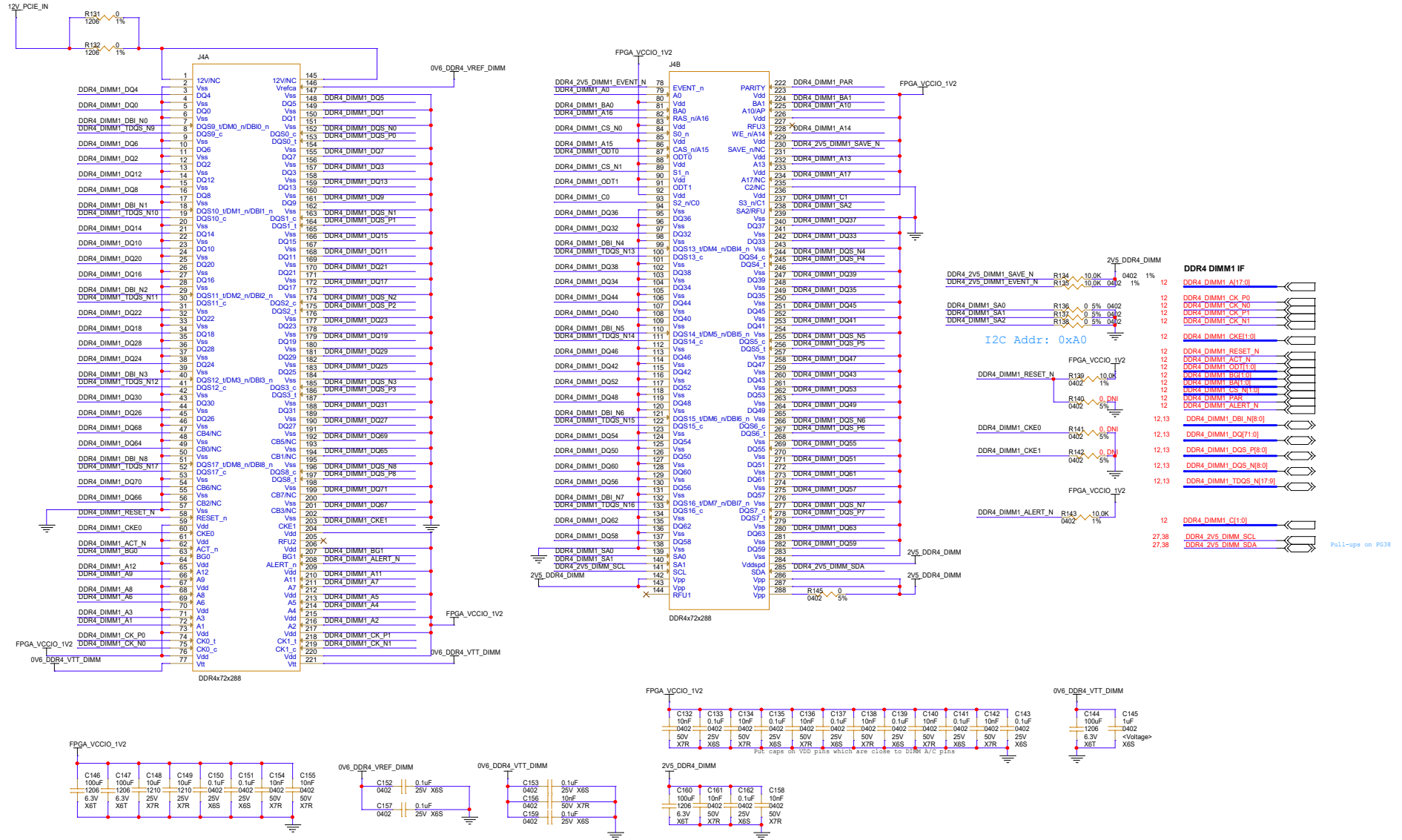
ODT1 (pin 91) : Error, ERR# Output

CLK1 (pin 218):Early Read ID, ERID<0> Output

CLK1# (pin 219):Early Read ID, ERID<1> Output



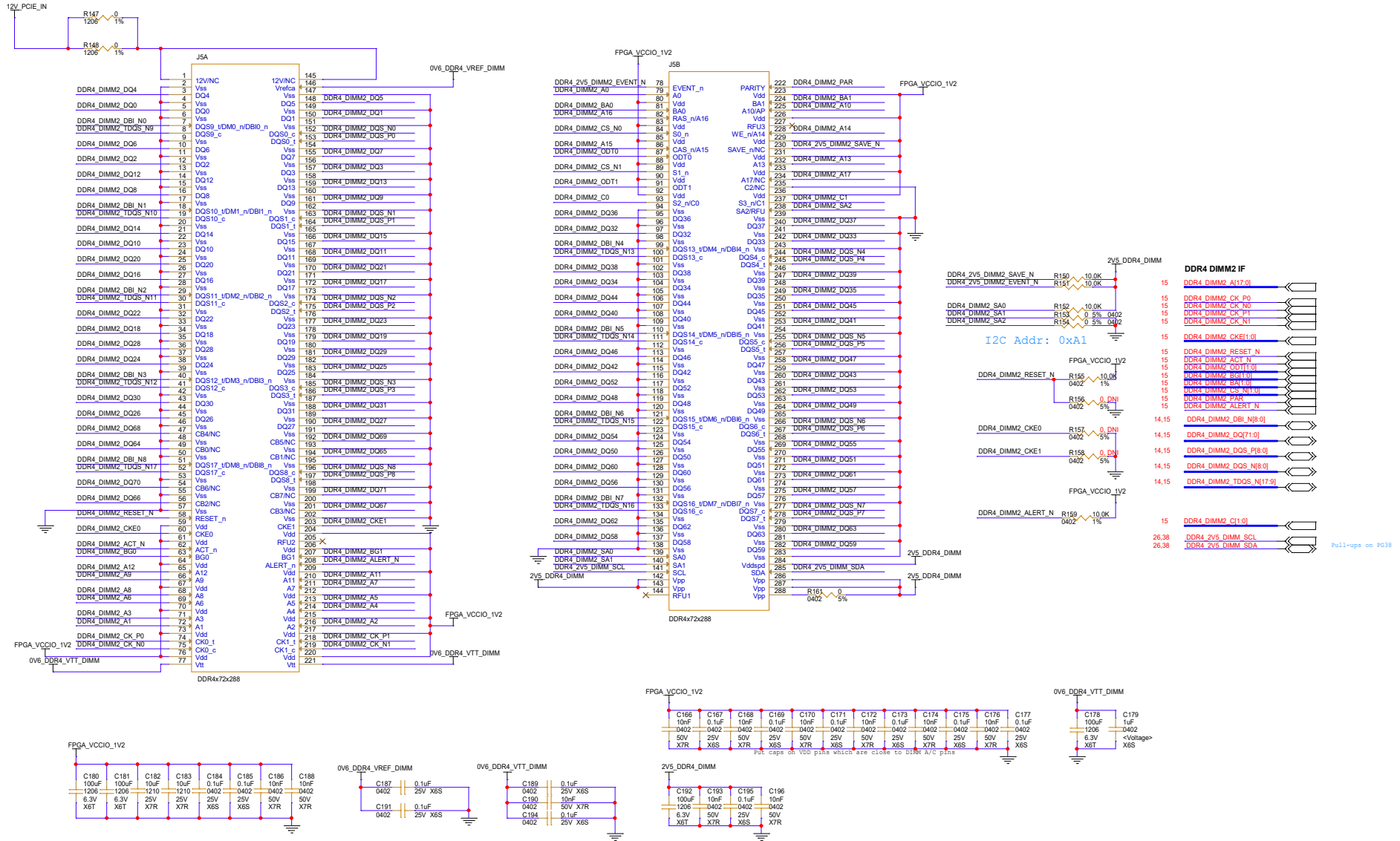
### DDR4/DDR-T DIMM 1





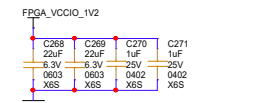
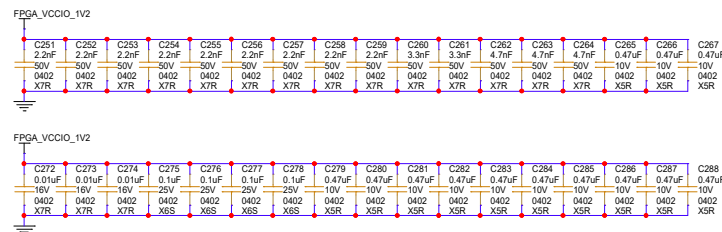
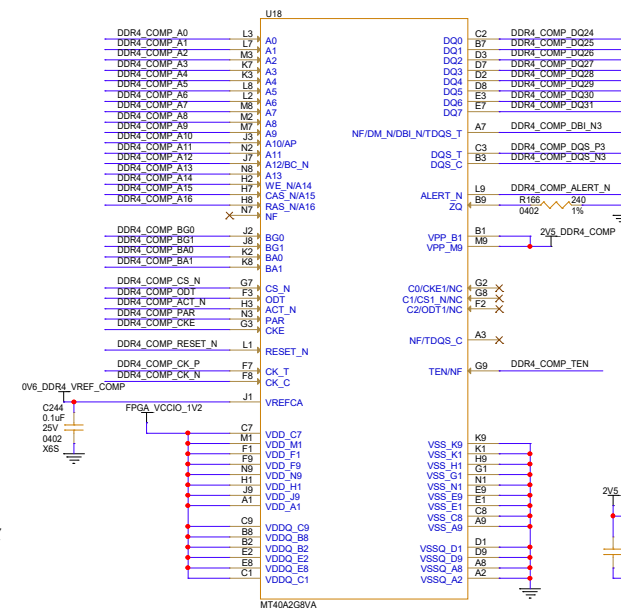
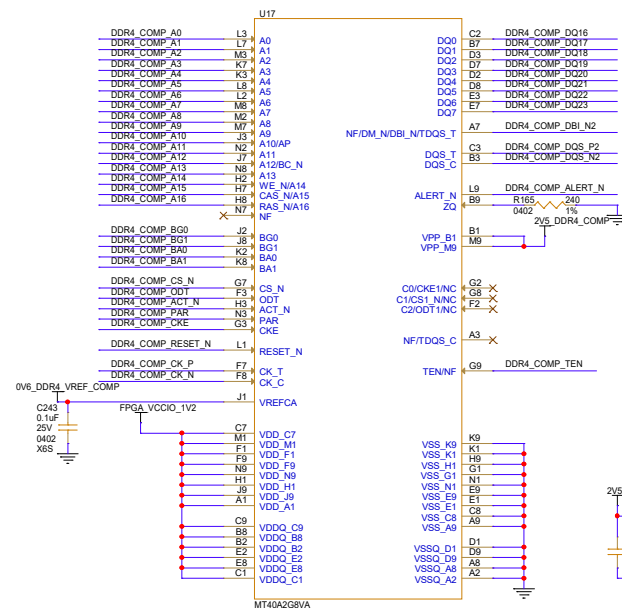
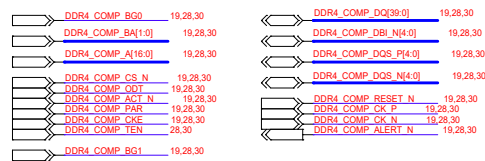
# DDR4/DDR-T DIMM 2

Note: DIMM2 not available on FM76 Devkit

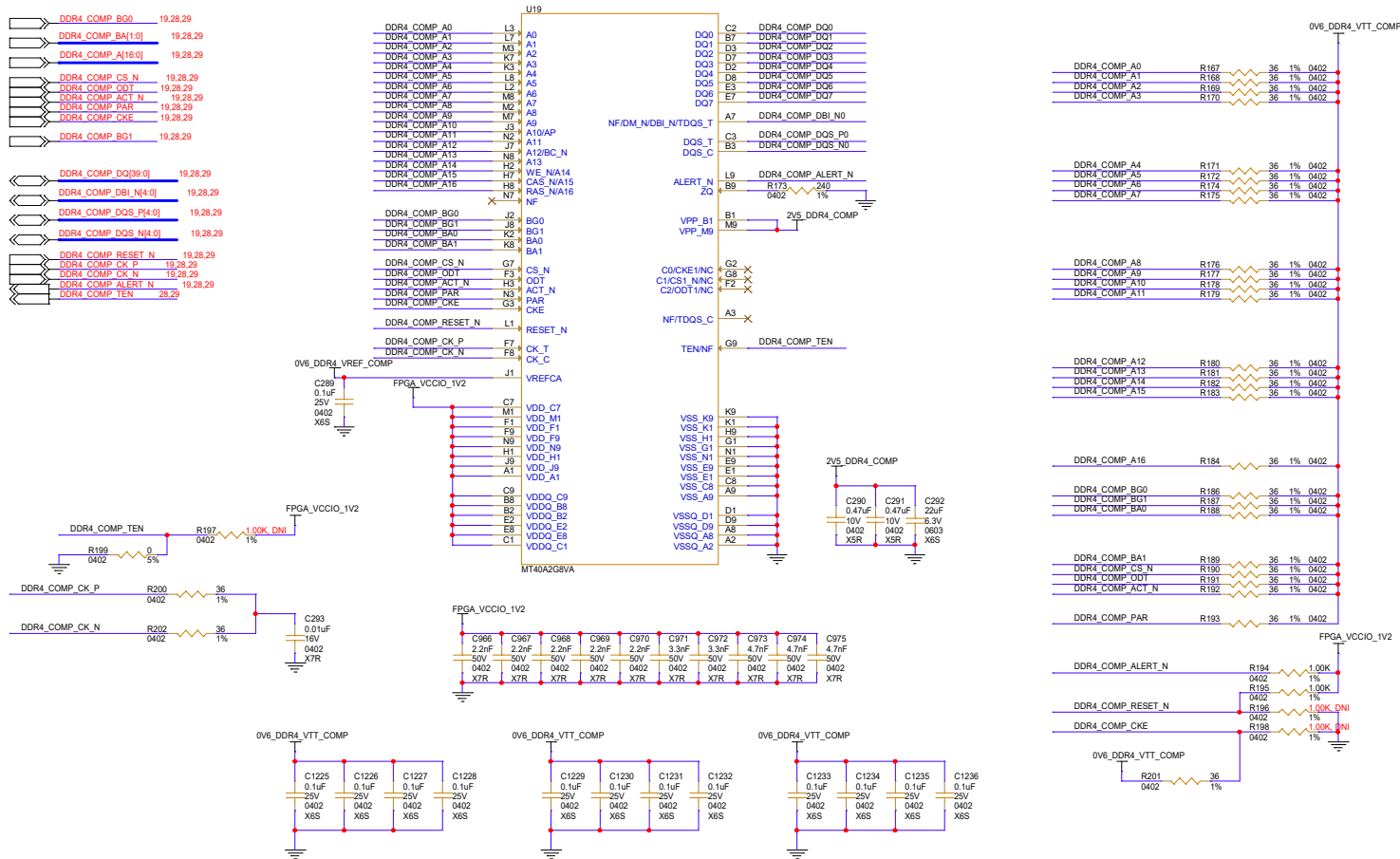


Altera, 101 Innovation Dr., San Jose CA 95134 Copyright (c) 2015, Intel Corporation. All Rights Reserved.				
Info <b>AGILEX FM86/FM76 DEVELOPMENT KIT</b>				
Size	Document Number			Rev
C	180-0330678-D1			D1
Date:	Monday, December 16, 2024	Sheet	28	of 58

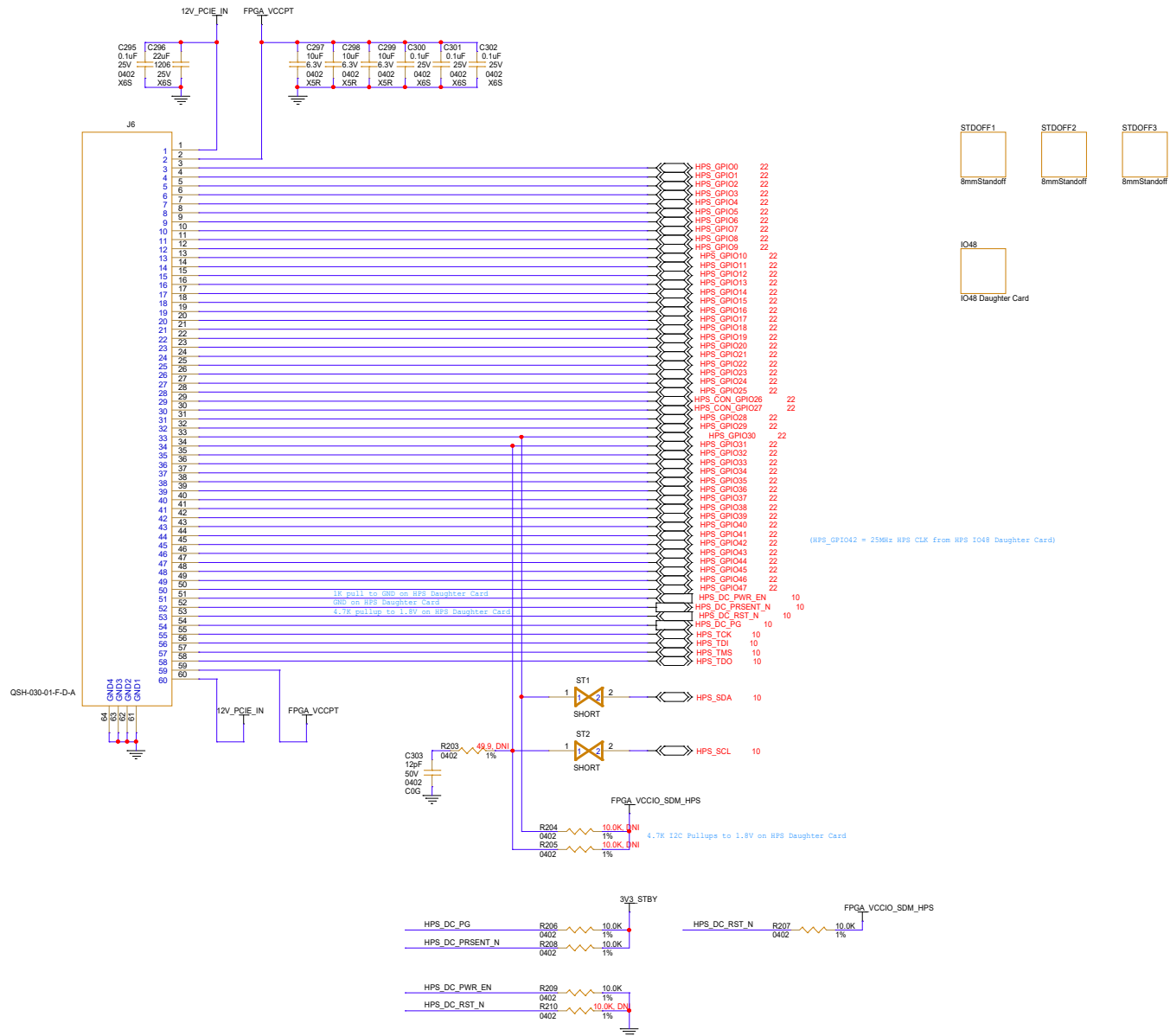
### DDR4 COMPONENT #3/#4

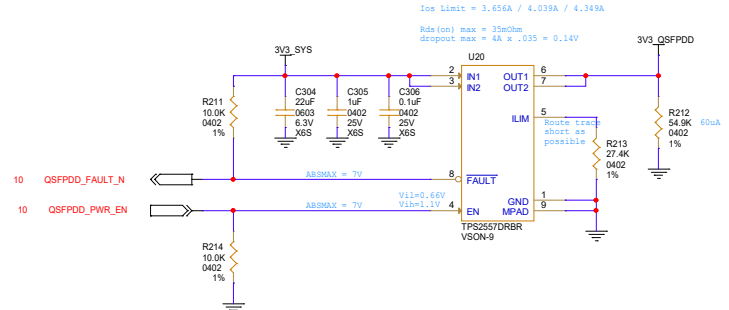


# DDR4 COMPONENT #5 & Termination



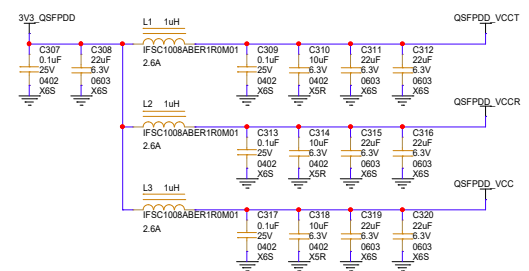
# HPS IO-48 Daughter Card Connector



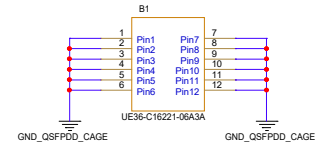


## QSPDD-56

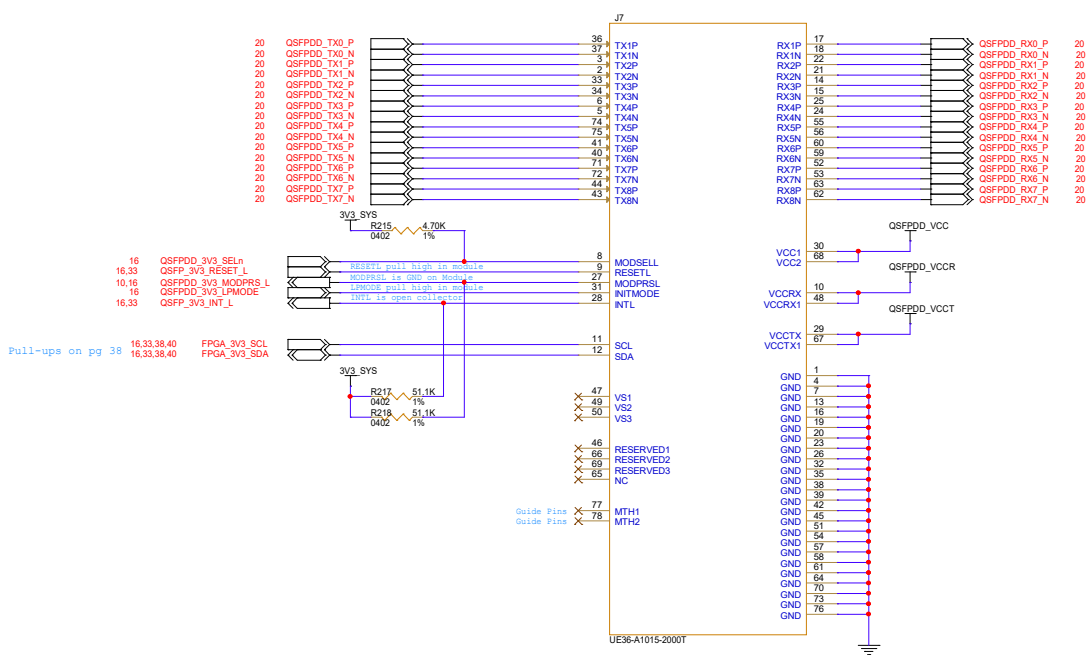
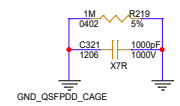
- NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.
- NOTE 2: zQSPF 100-ohm termination is implemented via the FPGA on-chip termination.
- NOTE 3: DC blocking capacitors are in the module for RX and TX.
- NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



Place close to QSPDD Connector

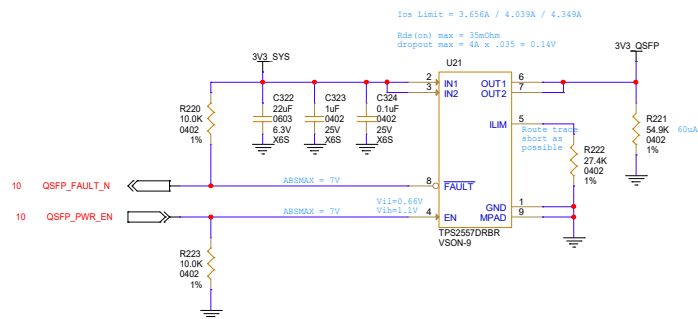


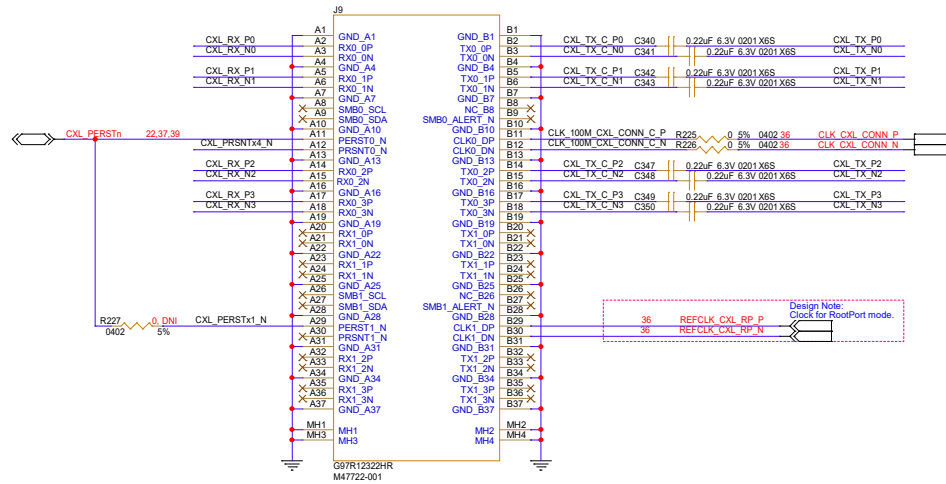
Amphenol UE36-C16221-06A4A



Amphenol UE36-A1015-2000T





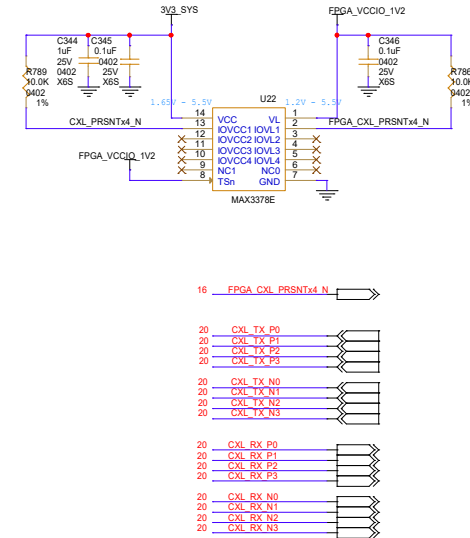


CXL Interface is designed to support the FM85 Devkit M.2 Daughter Card (M-Key for PCIe4 and SATA). When connecting to this card, FM86 Devkit CXL channels will be connected to M.2 channels 8-11 (J5) on the daughter card. PCIe\_100M\_ROOT0\_P/N clock must be selected as the default PCIe clock on the M.2 Daughter Card.

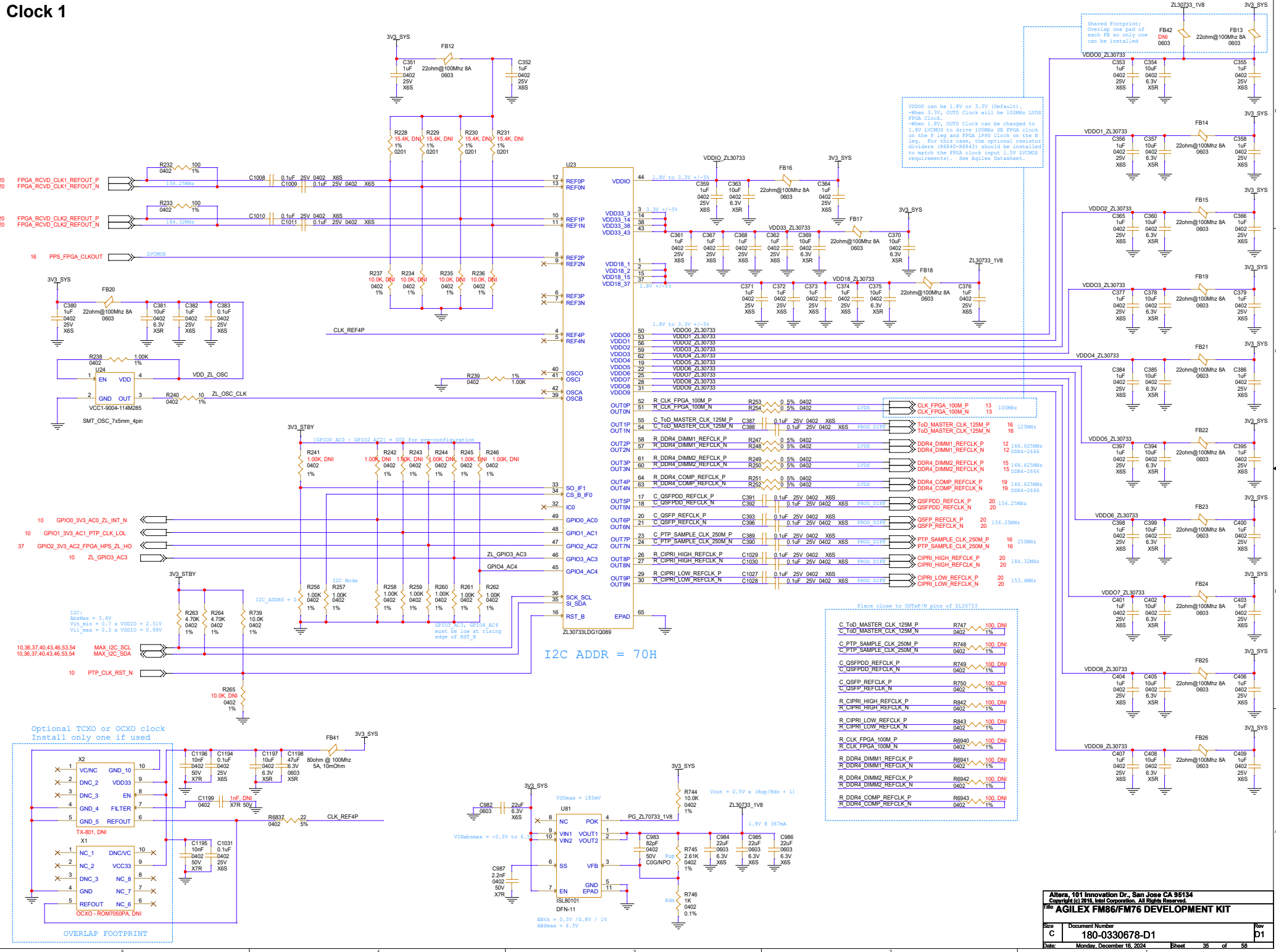
For FM86 Devkit to FM86 Devkit communication using PCIe4 over CXL with one devkit configured as the RP and the other as the EP, you must use the local PCIe CLK from U25 (REFCLK\_CXL\_RP\_P/N) for each board

I2C is not supported.

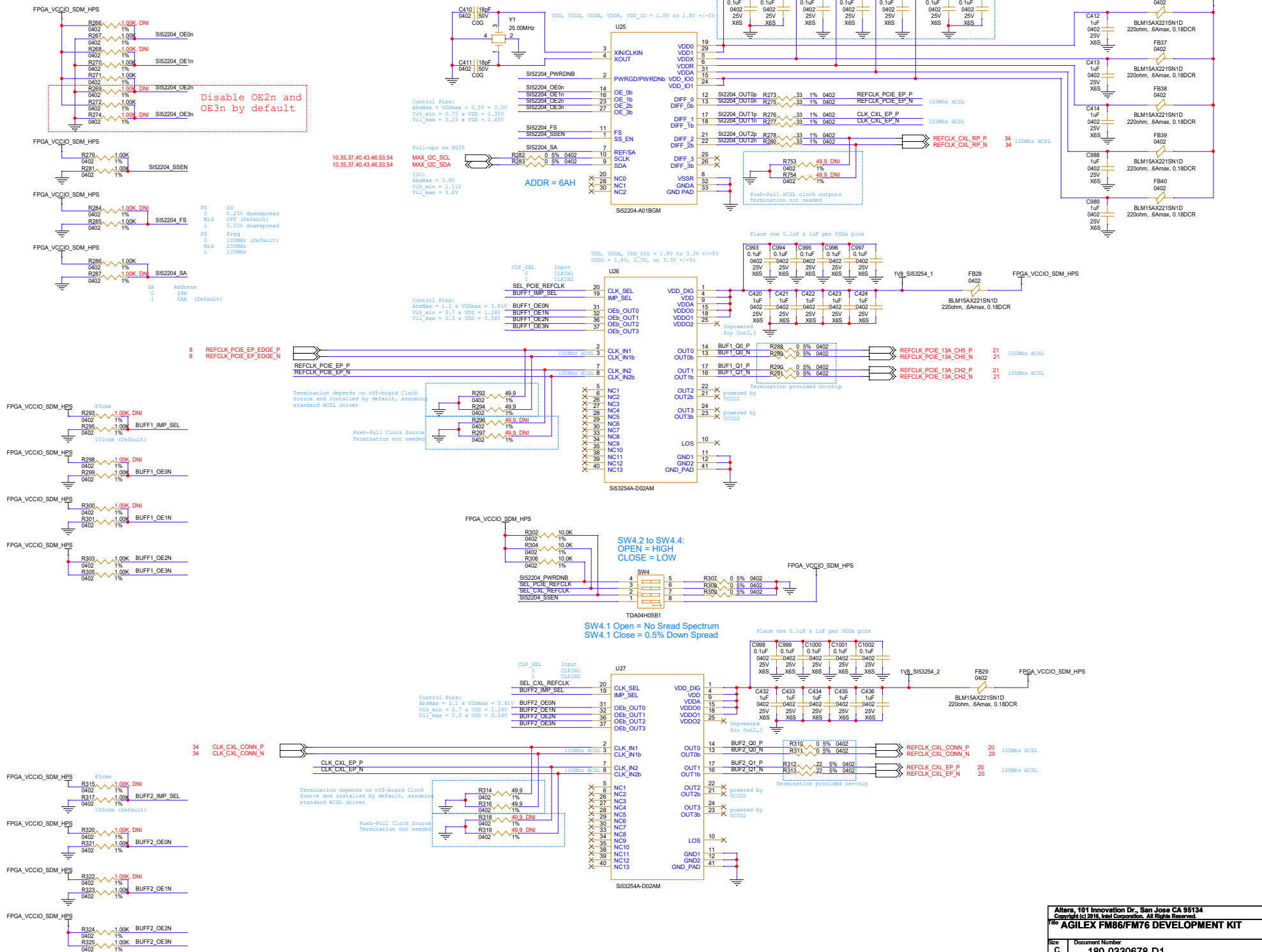
## CXL Connector

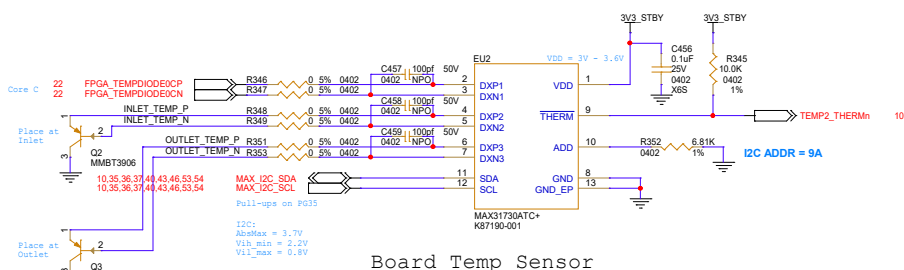
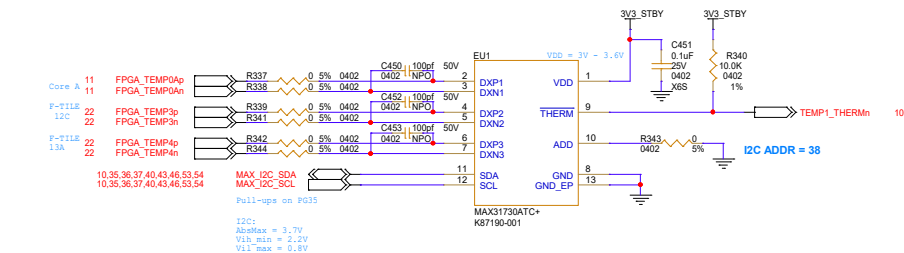
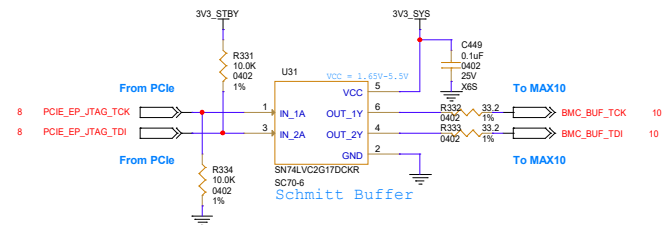
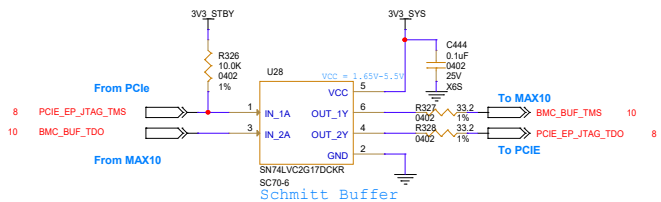


## Clock 1

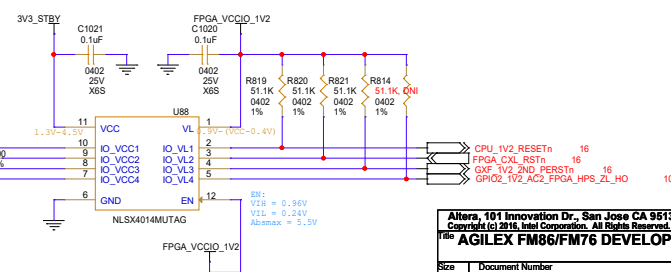
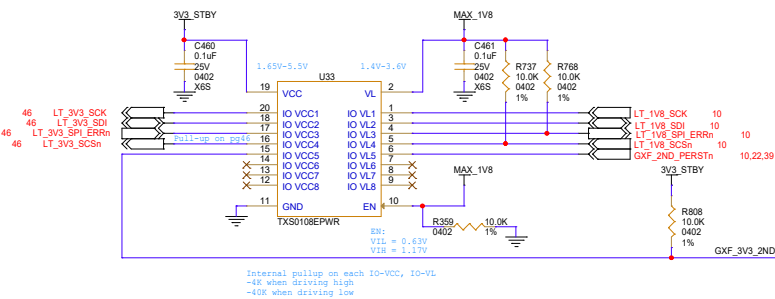


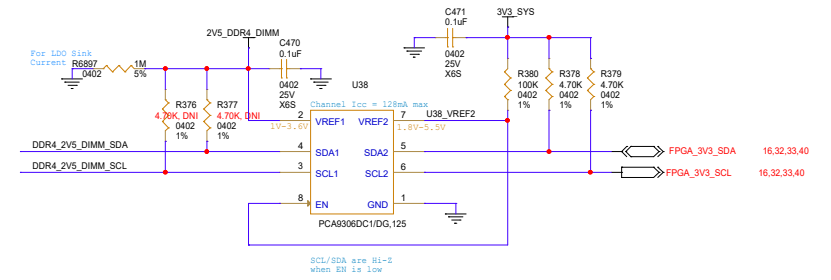
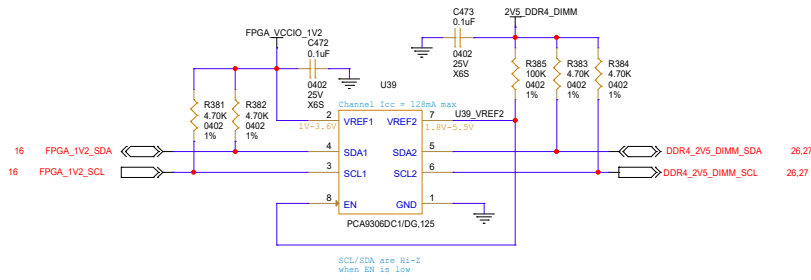
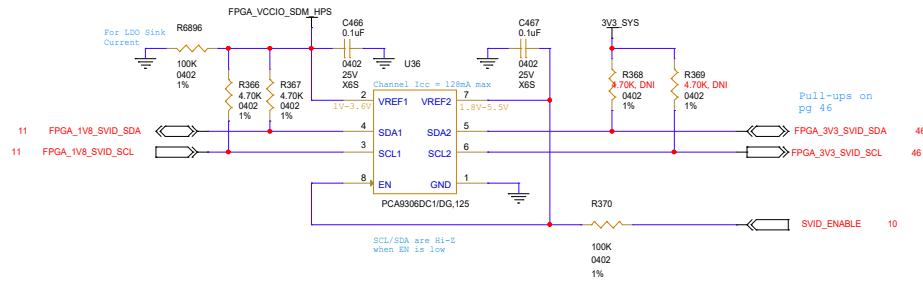
## Clock 2





### Board Temp Sensor

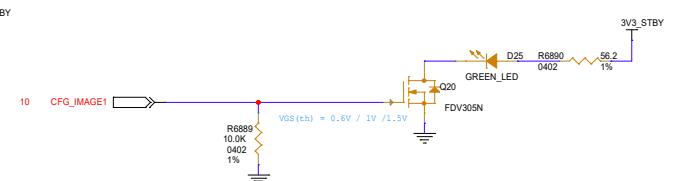
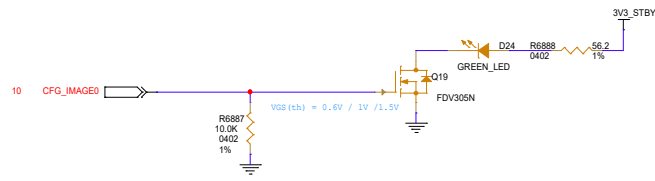
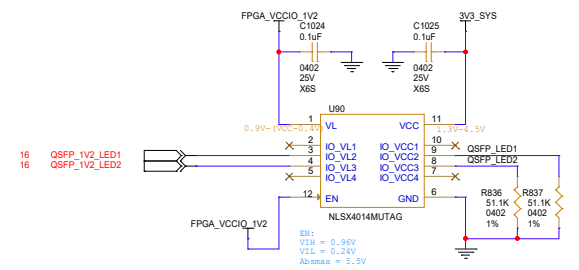
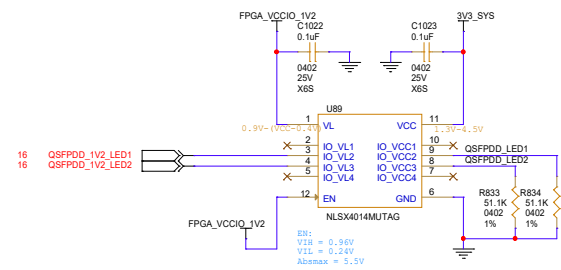
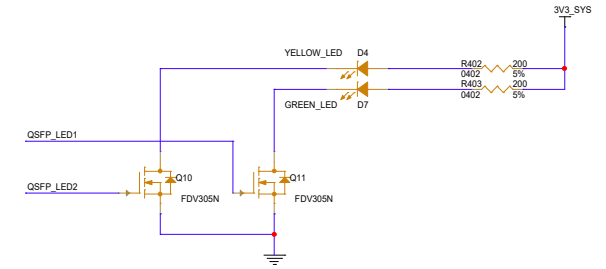
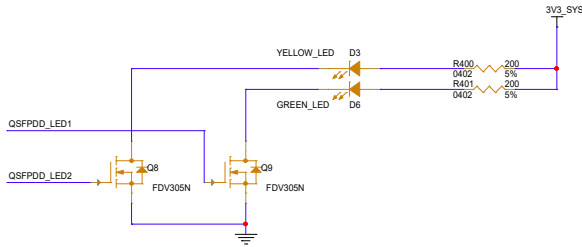
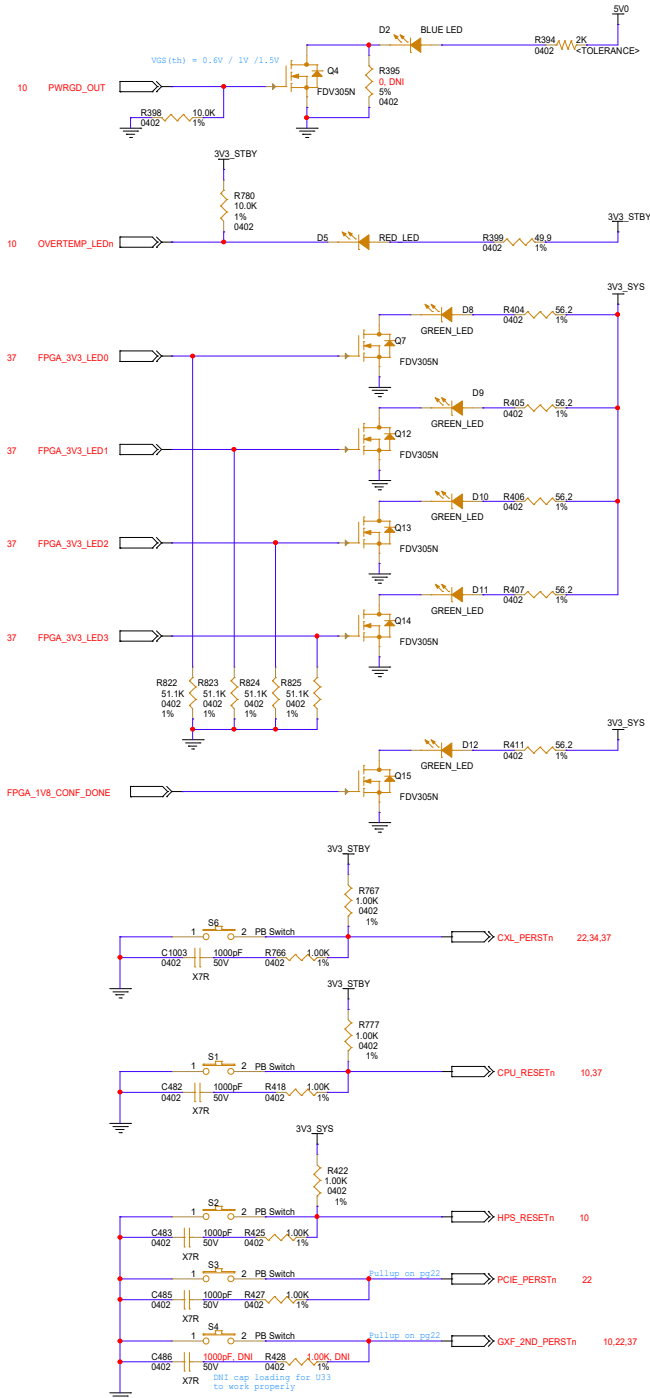




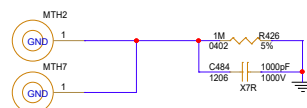


# LEDs And PushButtons

## POWER LED



Large Mounting holes on the rear of board



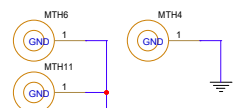
Large Mounting holes on the front of board

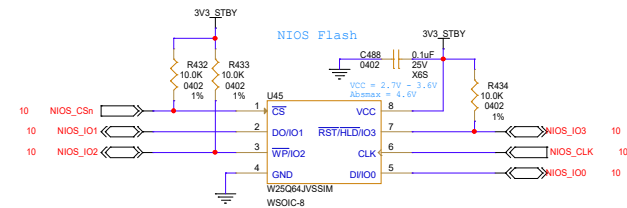
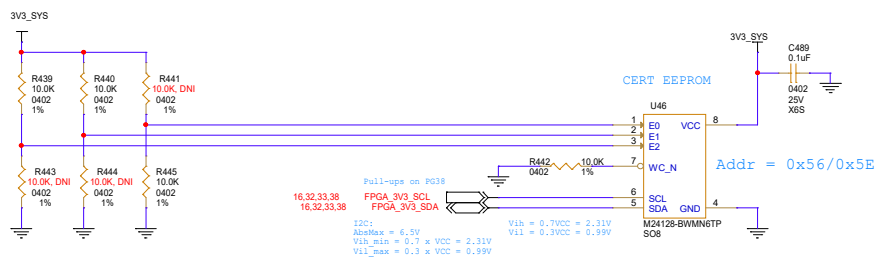
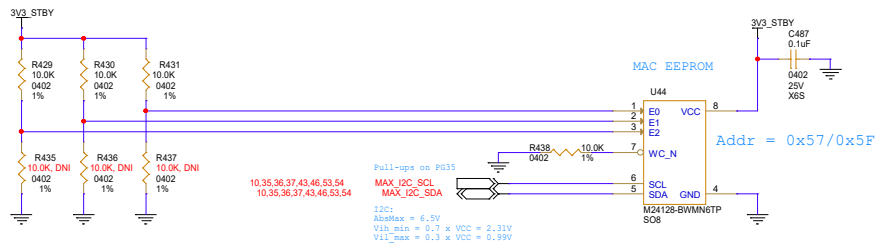


Large Mounting holes for heatsink

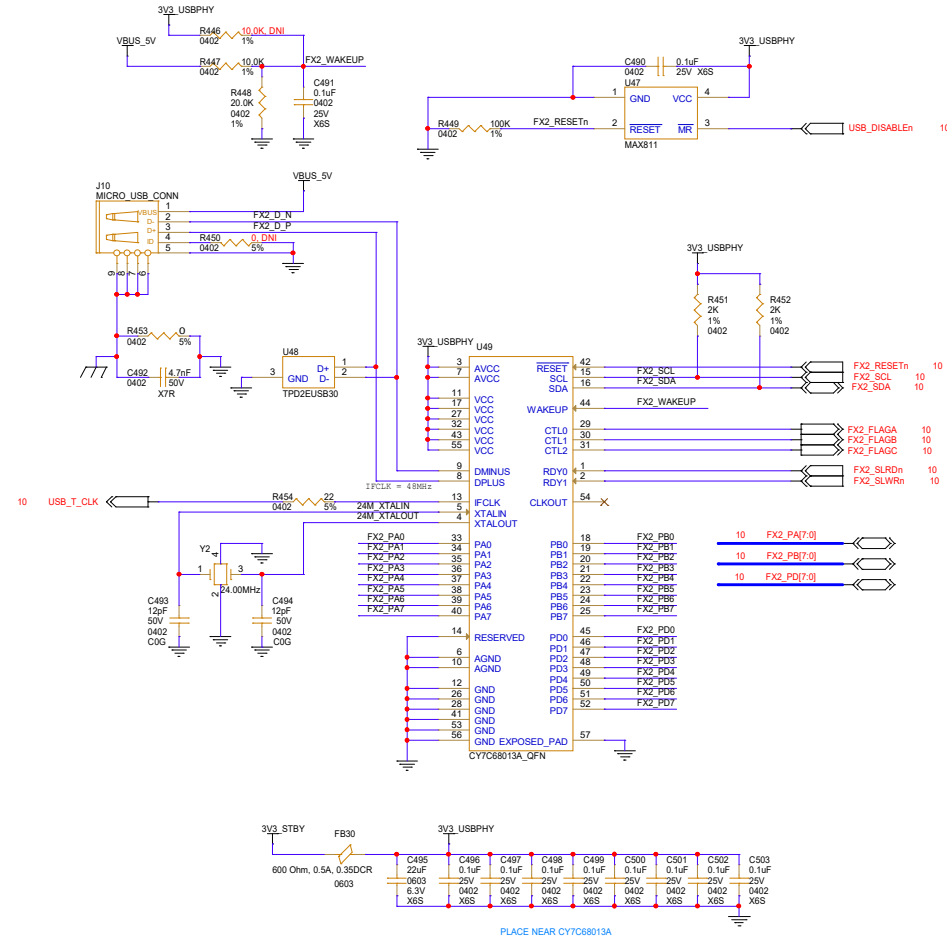


Large Mounting holes for IO48 Daughter Card





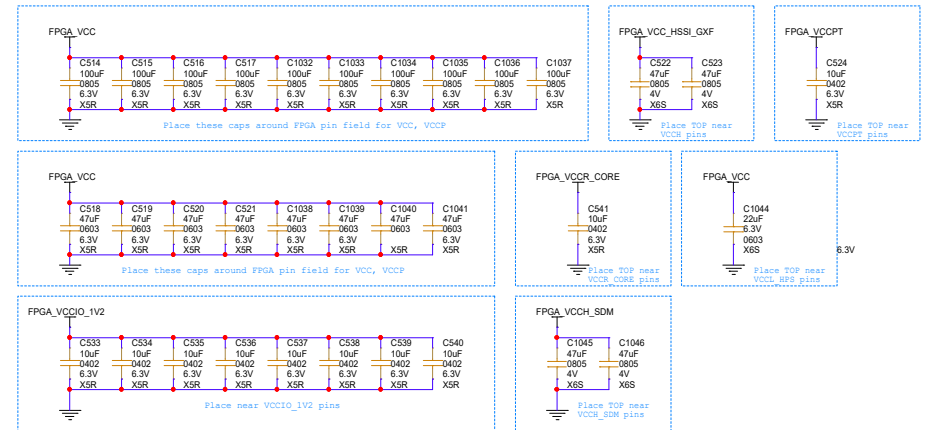
# USB-BlasterII Phy



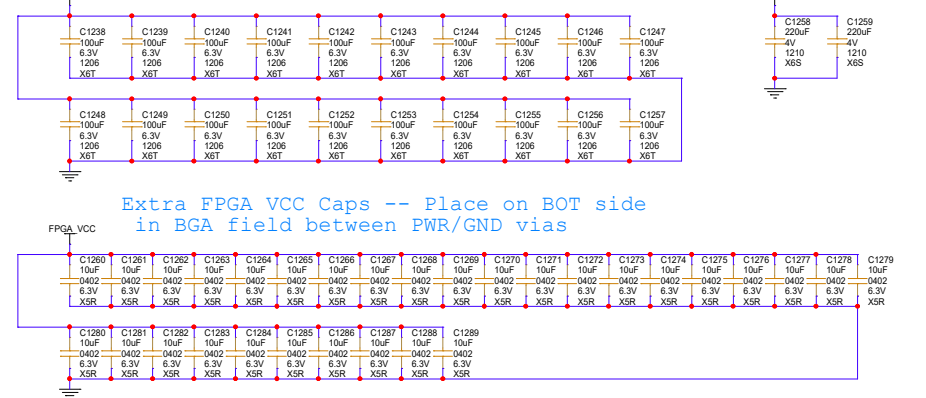
# FPGA Core Decoupling

Place on TOP Side

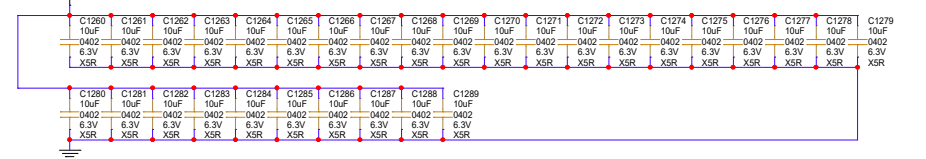
Place on BOT Side



Extra FPGA VCC Caps -- Place on BOT side periphery, 2-GND vias each cap gnd pad minimum



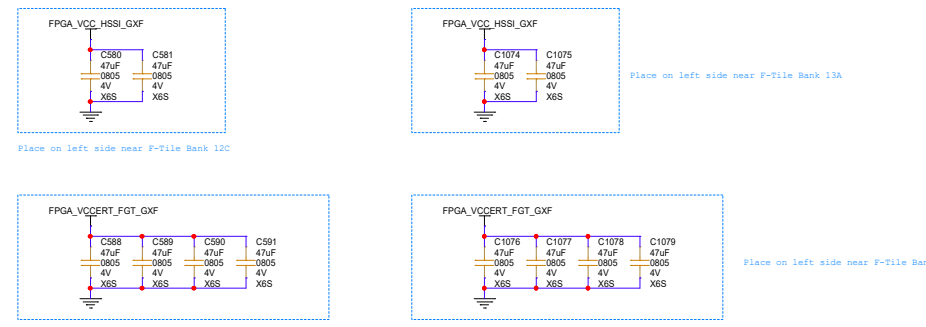
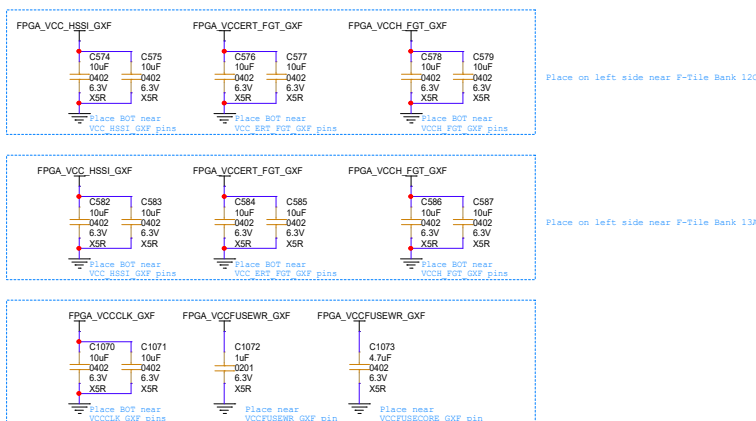
Extra FPGA VCC Caps -- Place on BOT side in BGA field between PWR/GND vias



# FPGA F-Tile Decoupling

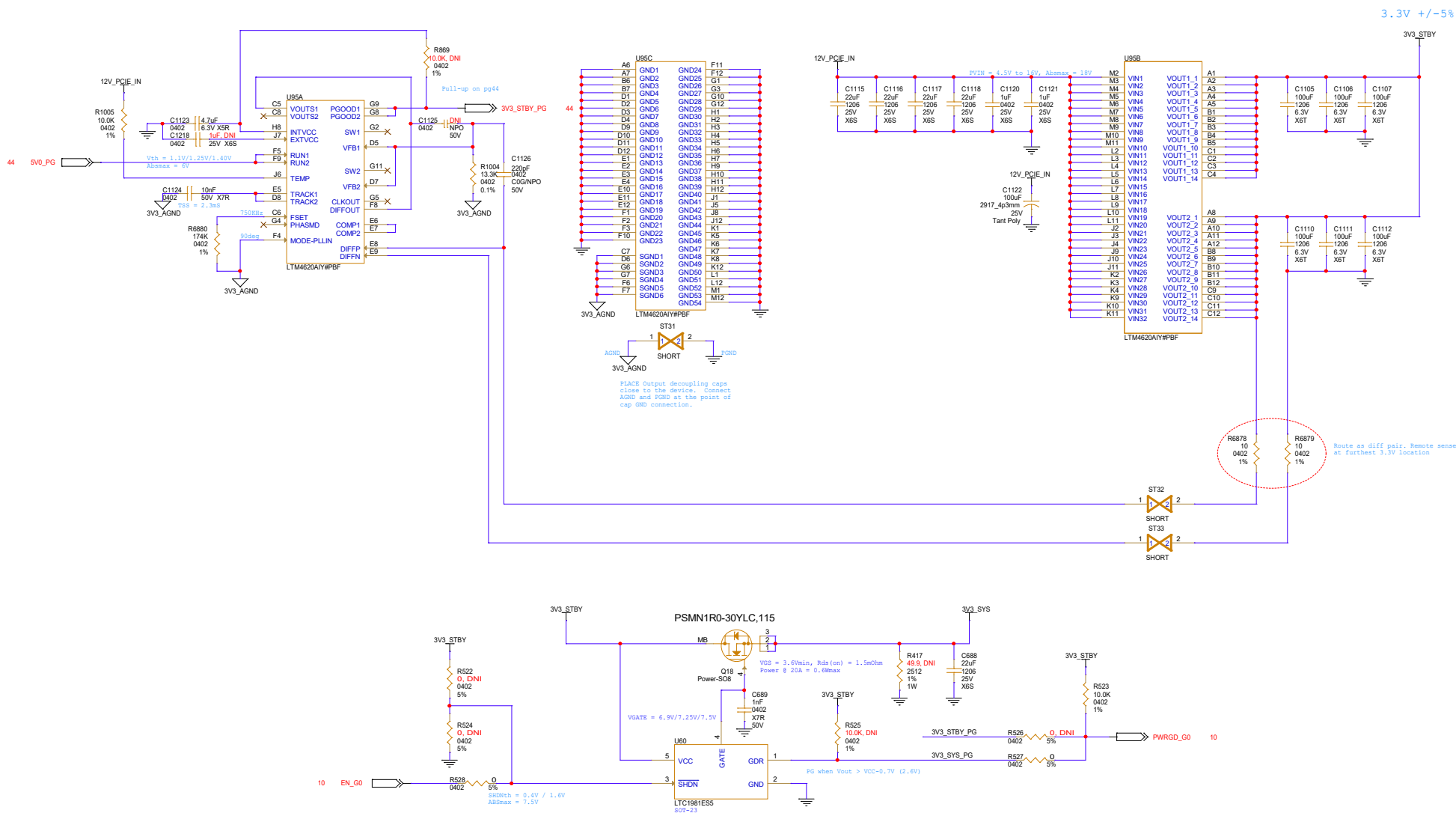
Place on TOP Side

Place on BOT Side



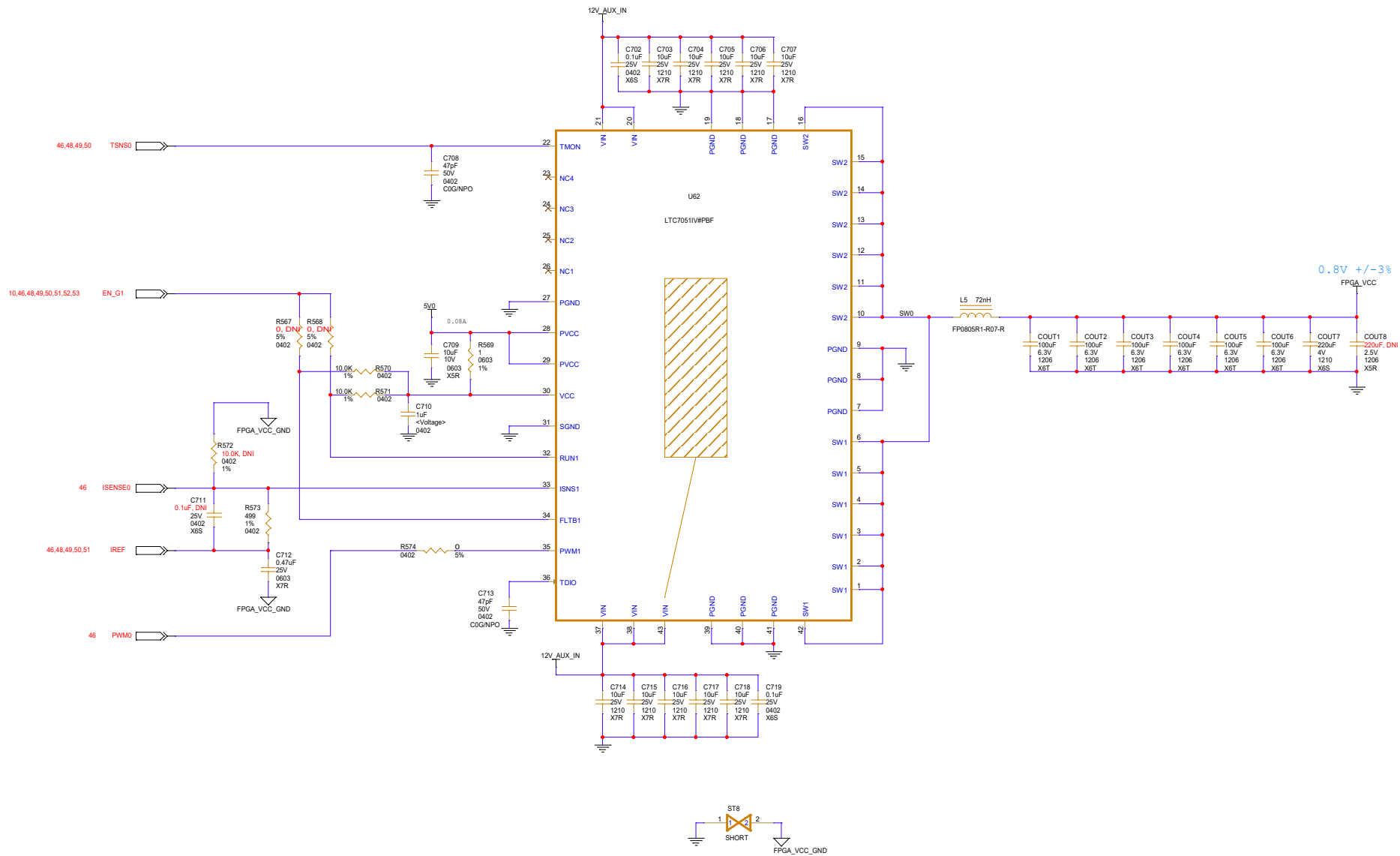


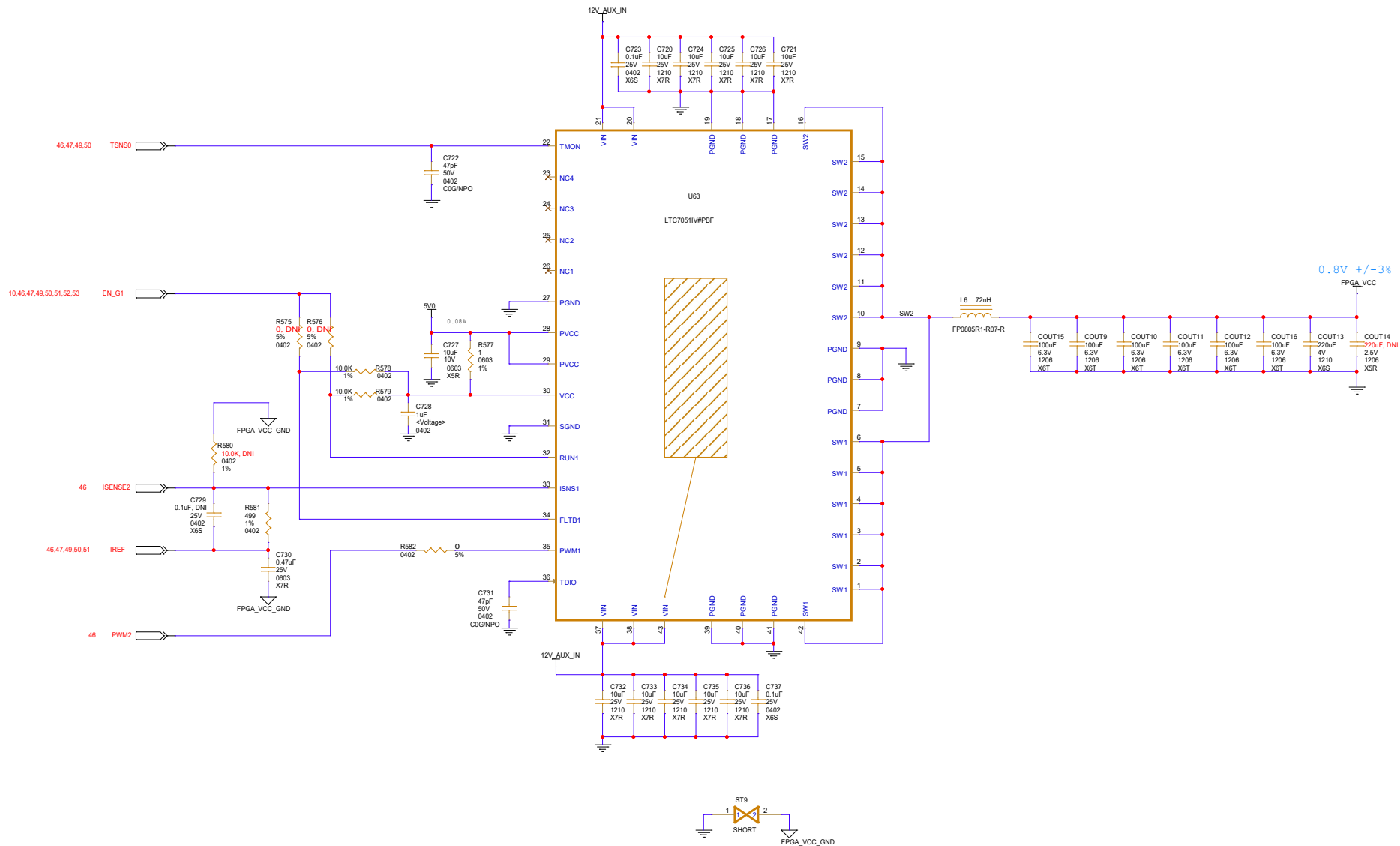


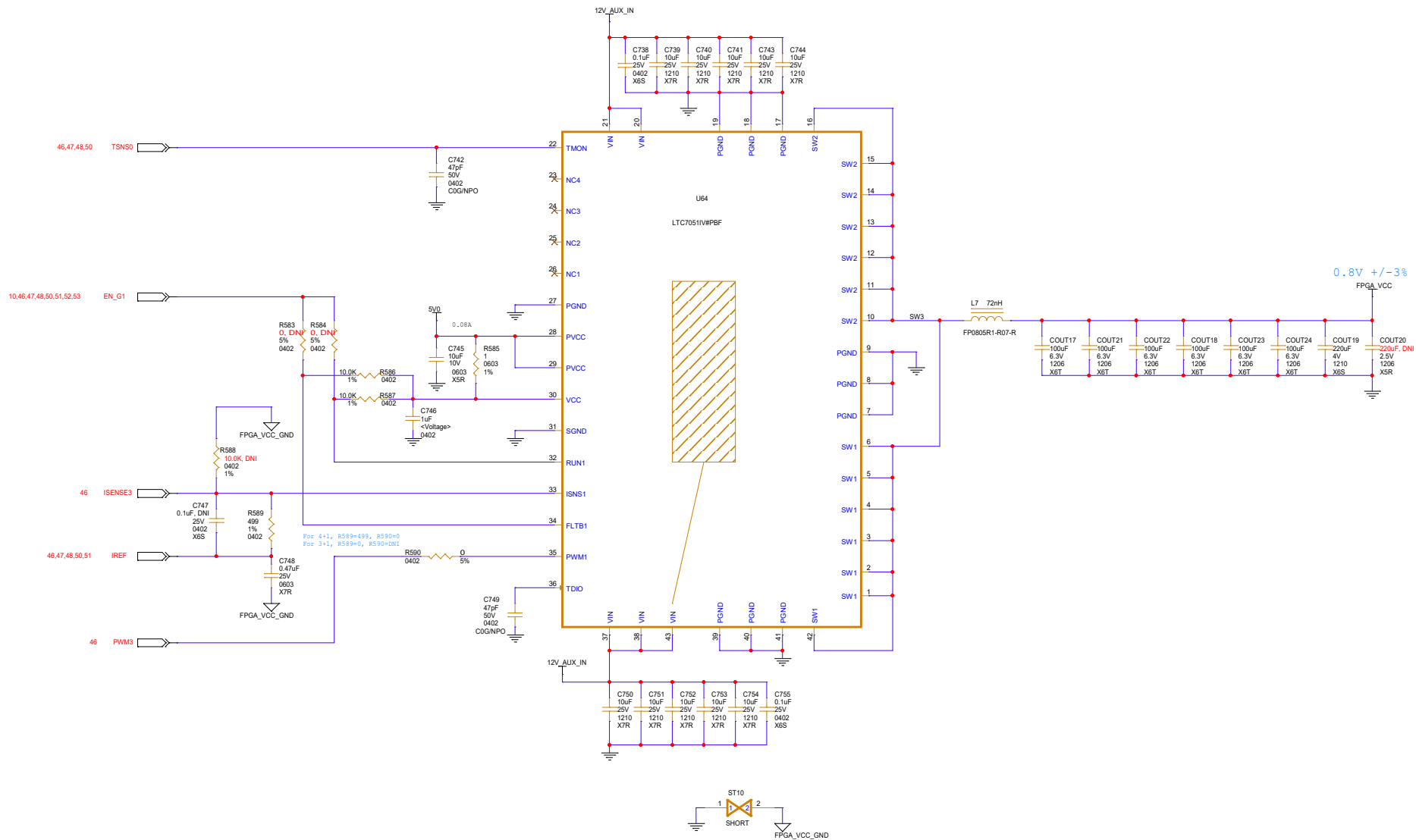


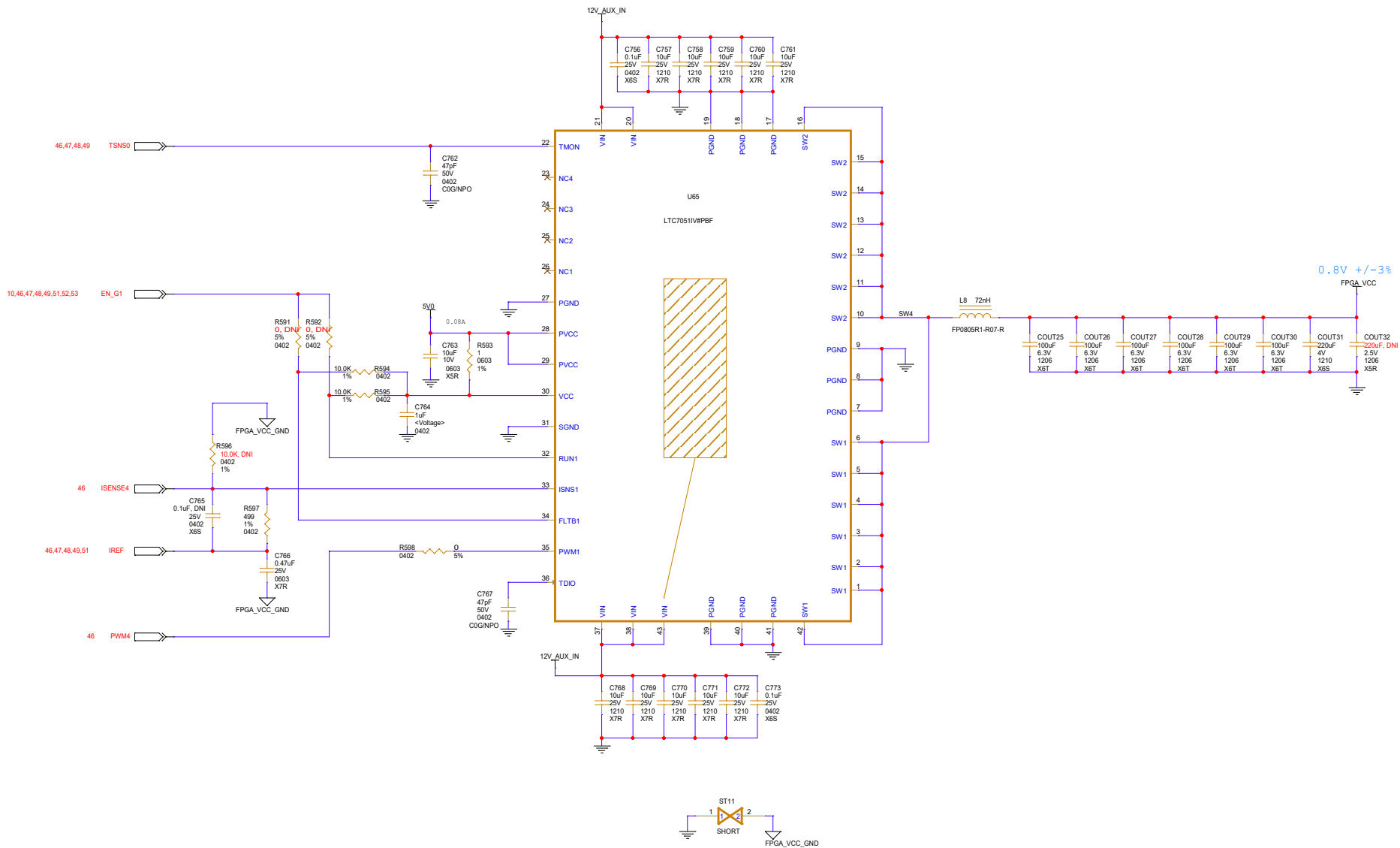




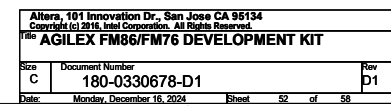




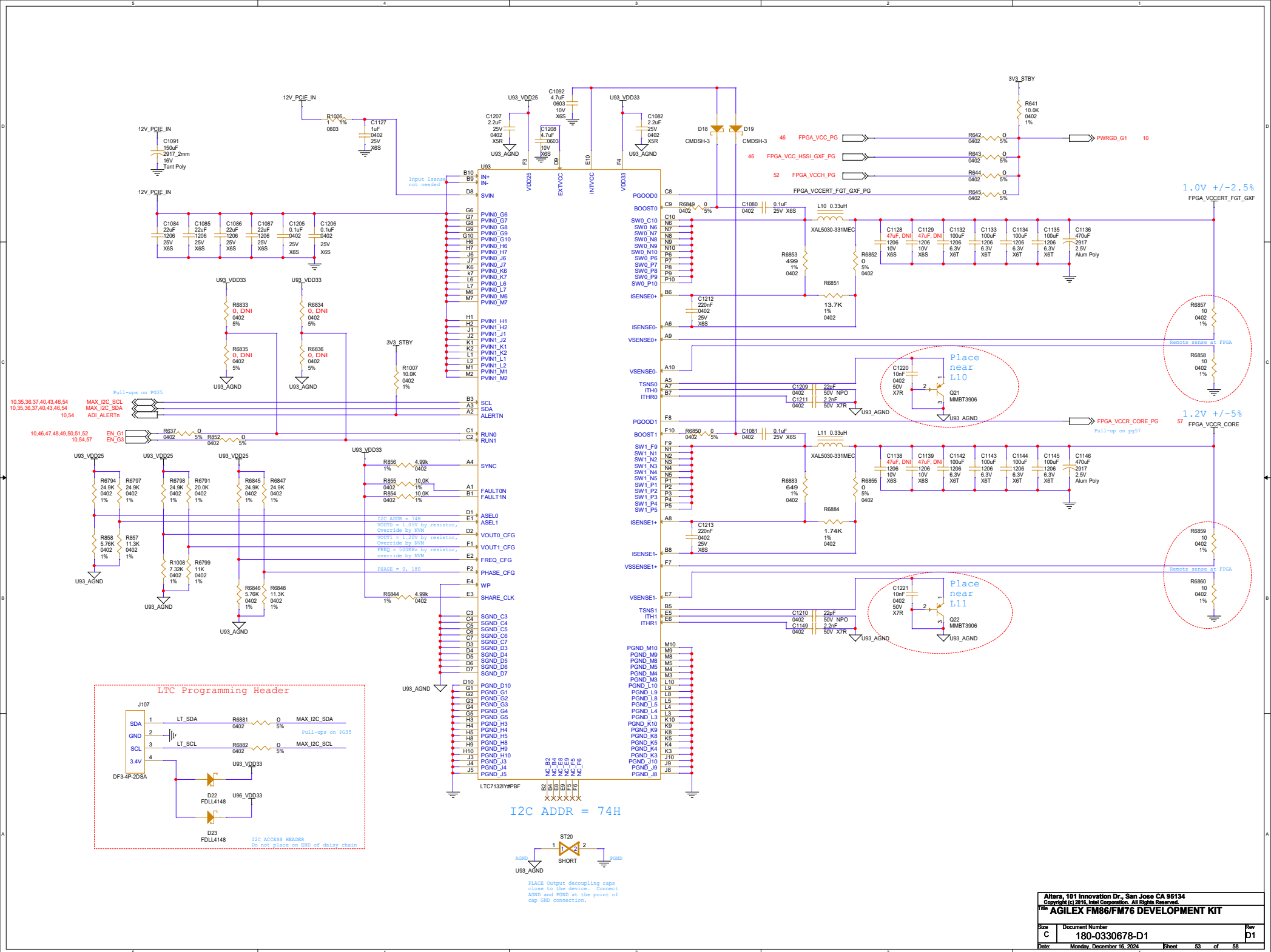




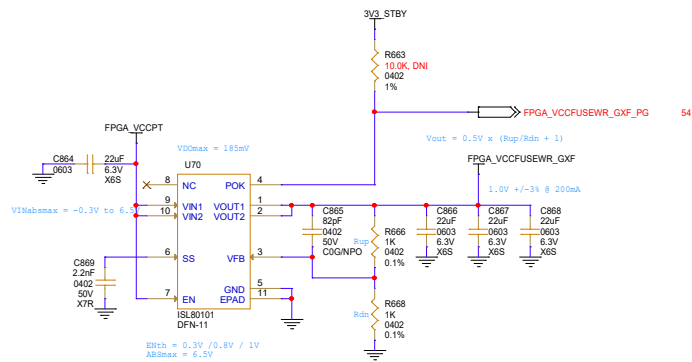












# VCCBAT Circuit intended for FM76 Device with Crypto Support

