

# Agilex<sup>™</sup> 7 FPGA F-Series Development Kit User Guide

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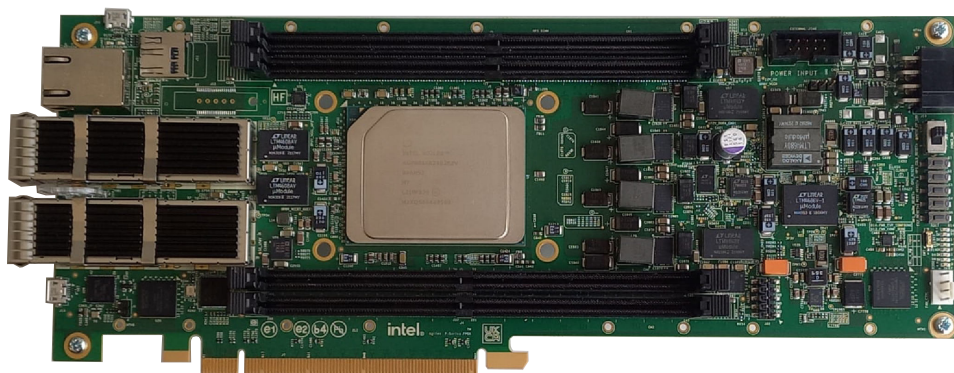
## 1. Overview

Agilex™ 7 FPGA F-Series Development Kit is a complete design environment that includes both hardware and software you need to develop Agilex 7 FPGA designs. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Agilex 7 FPGA F-Series designs.

**Table 1. Ordering Information**

Development Kit Version	Ordering Code	Device Part Number	Serial Number Identifier
Agilex 7 FPGA F-Series Development Kit (Production 2 P-Tile & E-Tile) Power Solution 2	DK-DEV-AGF014EB	AGFB014R24B2E2V	Above 20500
Agilex 7 FPGA F-Series Development Kit (Production 1 P-Tile & E-Tile) Power Solution 1	DK-DEV-AGF014EA	AGFB014R24B2E2V	Above 20220
Agilex 7 FPGA F-Series Development Kit (ES -3V)	DK-DEV-AGF014E3ES	AGFB014R24A2E3VR0	Under 20000
Agilex 7 FPGA F-Series Development Kit (ES -2V)	DK-DEV-AGF014E2ES	AGFB014R24A2E2VR0	Above 20000

**Figure 1. Agilex 7 FPGA F-Series Development Kit—Top View**



Refer to the *Appendix A—Development Kit Components* section for more details about the components on the Agilex 7 FPGA F-Series Development Kit.

**Note:** The -3V and -2V versions of the Agilex 7 FPGA F-Series Development Kit use different power solutions for VCC core. Refer to the power tree diagrams in the *Appendix A.8—Power* section for additional information.

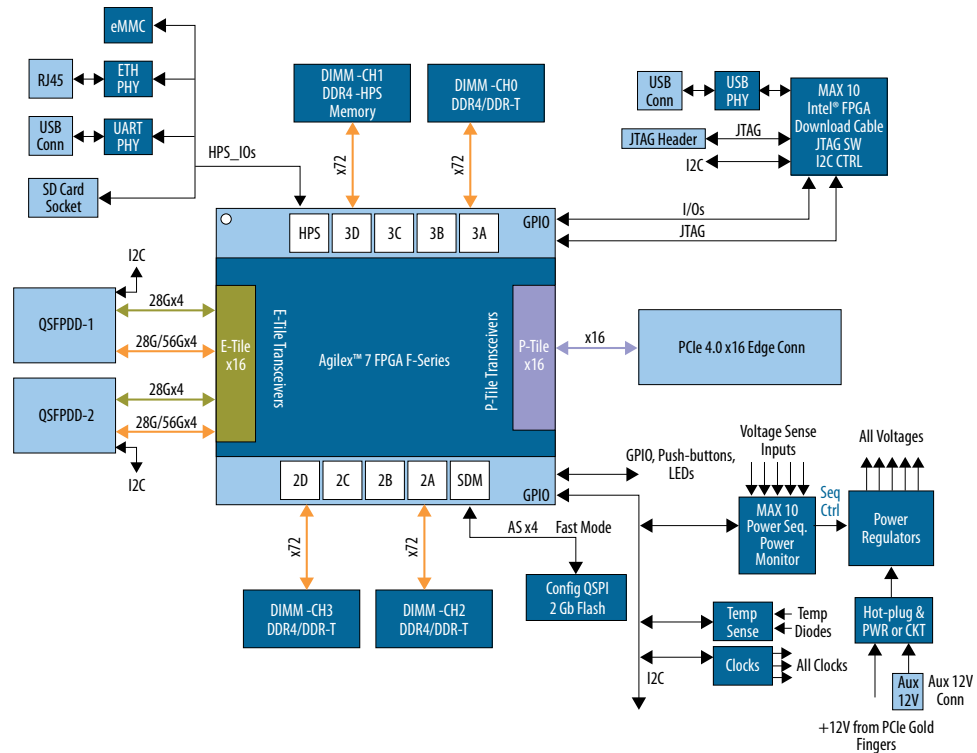
### Related Information

- [Development Kit Components](#) on page 36

- [Power](#) on page 42

## 1.1. Block Diagram

Figure 2. Agilx 7 FPGA F-Series Development Kit Block Diagram



## 1.2. Feature Summary

- Agilx 7 FPGA F-Series, 1400 KLE, 2486- (R24A and R24B) packages
- 2x Standard QSFDD supports both optical and electrical cable interfaces connected to E-Tile transceivers
- PCIe\* 4.0 x16 golden fingers connected to P-Tile transceivers, supports x1/x4/x8/x16 modes
- 3x 288-pin DDR4 DIMM sockets to support 72 bits DDR4/DDR-T module in FPGA fabric interface
- 1x 288-pin DDR4 DIMM socket to support 72 bits DDR4 module for HPS memory interface
- 2 Gb QSPI Flash for active serial FPGA configuration (AS x4 mode)
- Programmable clock resource for transceiver (XCVR), memory and FPGA fabric
- HPS interface supporting: ETH, UART, SD card socket, eMMC, and Mictor connector

**Note:** Golden Software Reference Design for HPS (GSRD) is not currently available for this development kit.

## 1.3. Box Contents

- Agilex 7 FPGA F-Series development board
- DDR4 DIMM module
- USB2.0 Micro cable
- Ethernet cable
- 240 W power adapter and NA/EU/JP/UK cords
- ATX power convert cable - 24 pin to 6 pin.

*Note:* Only one DIMM module is provided with each development kit.

### Related Information

[Agilex 7 FPGA F-Series Development Kit Website](#)

## 1.4. Recommended Operating Conditions

**Table 2. Recommended Operating Conditions**

Operating Condition	Range of Values
Ambient operating temperature range	0°C to 45 °C
ICC load current	100 A
ICC load transient percentage	200 A/uS
FPGA maximum power supported by active heat sink/fan	150 W

### Related Information

[Handling the Board](#) on page 7



## 2. Getting Started

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### 2.1. Before You Begin

You must check the kit contents and inspect the boards to verify that you received all of the items in the box before using the kit of installing the software.

In case any of the items are missing, you must contact Altera before you proceed.

**Important:** Read the [Appendix C.1—Safety and Regulatory Information](#) for safe operation and regulatory adherence.

### 2.2. Handling the Board

When handling the board, it is important to observe static discharge precautions.

**Caution:** Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

**Caution:** This development kit should not be operated in a vibration environment.

### 2.3. Software and Driver Installation

This section explains how to install the following software and driver:

- Quartus® Prime Pro Edition software
- Intel® SoC FPGA Embedded Development Suite (SoC EDS)
- Agilex 7 FPGA F-Series Development Kit software
- Intel FPGA Download Cable II

#### 2.3.1. Installing the Quartus Prime Pro Edition Software

1. Download the Quartus Prime Pro Edition software from the [FPGA Software Download Center](#) webpage of the Intel website.
2. Follow the on-screen instructions to complete the installation process. Choose an installation directory that is relative to the Quartus Prime Pro Edition software installation directory.

If you have difficulty installing the Quartus Prime software, refer to the *Intel FPGA Software Installation and Licensing*.

#### Related Information

- [Quick-Start for Quartus Prime Pro Edition Software](#)
- [Quartus Prime Pro Edition User Guide: Getting Started](#)

- [Intel FPGA Software Installation and Licensing](#)

### 2.3.2. Installing the Intel SoC EDS

The Intel SoC FPGA Embedded Development Suite (SoC EDS) is a comprehensive software tool suite for embedded software development on Altera® system-on-chip (SoC) devices. It contains development tools, utility programs, run-time software, and application examples to expedite firmware and application software of SoC embedded systems.

As a part of the Intel SoC EDS, the Arm® Development Studio 5 (DS-5) Intel SoC FPGA Edition Toolkit provides a comprehensive set of embedded development tools for Altera's SoC FPGAs.

**Note:** Use the Quartus Prime Pro Edition software version 19.4 or later for this development kit test and debug.

For more information and steps to install the Intel SoC EDS Tool Suite, refer to the links below.

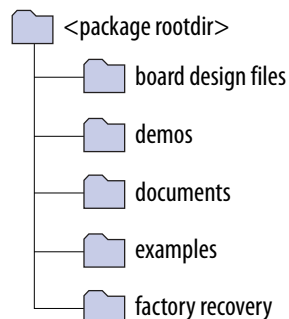
#### Related Information

- [Intel SoC FPGA Embedded Development Suite \(SoC EDS\) User Guide](#)
- [Arm® Development Studio for Intel SoC FPGA](#)

### 2.3.3. Installing the Development Kit

1. Download the Agilex 7 FPGA F-Series Development Kit installer package from the [Agilex 7 FPGA F-Series Development Kit](#) webpage on the Intel website.
2. Unzip the Agilex 7 FPGA F-Series Development Kit installer package. The package creates the directory structure shown in the figure below.

**Figure 3. Agilex 7 FPGA F-Series Development Kit Directory Structure**



3. For the latest issues and release notes, Altera recommends that you review the `readme.txt` located in the root directory of the kit installation.



**Table 3. Installed Development Kit Directory Description**

Directory Name	Description of Directory Contents
board_design_files	Contains schematic, layout, assembly, and Bill of Material (BOM) board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications when available.
documents	Contains the development kit documentation.
examples	Contains the sample design files for the Agilex 7 FPGA F-Series Development Kit: <ul style="list-style-type: none"><li>Board Test System: BTS GUI, Power GUI, and Clock GUI</li><li>Golden Top project for pinout assignments management</li><li>Design Examples: Memory, XCVR, GPIO, and PCIe 4.0</li></ul>
factory_recovery	Contains the original image/binary programmed onto the board before shipment. Use this image to restore the board with its original factory content.

### 2.3.4. Installing the Intel FPGA Download Cable II Driver

The Agilex 7 FPGA F-Series Development Kit includes onboard Intel FPGA Download Cable II circuits for FPGA and system MAX<sup>®</sup> 10 programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable II driver on the host computer.

Installation instructions for the Intel FPGA Download Cable II driver for your operating system are available on the Intel website.

On the Intel website, navigate to the *Cable and Adapter Drivers Information* link to locate the table entry for your configuration and click the link to access the instructions.

#### Related Information

- [Cable and Adapter Drivers Information](#)
- [Intel FPGA Download Cable II User Guide](#)

## 3. Development Kit Setup

The instructions in this chapter explain how to setup the Agilex 7 FPGA F-Series Development Kit for specific use cases.

### 3.1. Default Settings

The Agilex 7 FPGA F-Series Development Kit ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the factory default switch settings table given below to return the board to its factory settings before proceeding forward.

**Note:** "X" refers to Don't Care in the table below.

**Table 4. Factory Default Switch Settings**

Switch	Default Position	Function
SW1[1:3]	OFF/ON/ON	Configuration mode setting bits. By default, AS -> FAST mode
SW2[1:4]	OFF/OFF/OFF/OFF	Select the resource of the System MAX 10 JTAG from USB PHY. Enable Si5341's outputs Power up Si52202 Enable UART interface
SW3[1:4]	OFF/OFF/OFF/OFF	Enable all the I <sup>2</sup> C level shifter.
SW4[1:4]	OFF/ON/ON/OFF	Select on-board Intel FPGA Download Cable as JTAG master when external JTAG header is absent. Bypass PWR MAX 10 in JTAG chain. Bypass FPGA HPS in JTAG chain. Enable FPGA in JTAG chain.
SW5	SW5.5 to SW5.6	Power off the board.
SW6[1:4]	ON/OFF/OFF/OFF	PCIe x16 mode is selected.
SW7.1	ON	Select local clock as PCIe reference clock.

### 3.2. Powering Up the Development Kit

#### Running the Board as a Standalone Work Bench

Use the provided 240 W power adapter to supply power through J16. After power adapter is plugged into J16 and SW5 is set to the ON position, one blue LED (D8) illuminates, indicating that the board has powered up successfully.

### **Running the Board in PCIe Socket as an Add-in Card**

Use the provided 240 W power adapter to supply power through J16. After the power adapter is plugged into J16 and the board is plugged into the PCIe socket of the server or PC, the board powers up when the server or PC is powered. One blue LED (D8) illuminates, indicating that the board has powered up successfully.



## 4. Board Test System

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The Agilex 7 FPGA F-Series Development Kit includes design examples and an application called the Board Test System (BTS) to test the functionality of this board.

### 4.1. Set Up the BTS GUI Running Environment

You need to download and install **Java runtime environment** and Quartus Prime software on your systems to run the BTS GUI, including the Power Monitor and Clock Controller GUI. **Java runtime environment** includes **OpenJDK** and **OpenJFX**, whose installation is a one-time procedure. If you have completed it before, you do not need to do it again unless the Java version upgrade is needed.

#### 4.1.1. Downloading OpenJDK

1. Download the Temurin\* OpenJDK. Refer to the related information for the download link.
2. Select Architecture x64, Package Type JRE, and Version 11.
  - a. For the **Windows** system, choose the JRE.zip format file.
  - b. For the **Linux** system, choose the JRE.tar.gz format file.

*Note:* Download the latest version to update the JDK version. The following version was tested: 11.0.21+9

#### Related Information

[Temurin\\* OpenJDK](#)

#### 4.1.2. Downloading OpenJFX

Follow these steps to download the OpenJFX:

1. Download the OpenJFX from the [Gluon](#) page.
2. Select the JavaFX version 17.0.2.
3. For the **Windows** system option, download the JavaFX Windows x64 SDK.
4. For the **Linux** system option, download the JavaFX Linux x64 SDK.

#### 4.1.3. Installing OpenJDK and OpenJFX

You have two downloaded compressed files. Follow these steps to install them.

Follow these steps to install the downloaded zip files:

1. On **Windows** system, Altera recommends you to unzip the files and put them in the following directory:

- C:\Program Files\Java\jre
- C:\Program Files\Java\jfx

*Note:* The unzipped folder name of JRE is jdk-11.0.xx+x-jre (for example, jdk-11.0.15+10-jre). Rename it to *jre*.

The unzipped folder name of JFX is javafx-sdk-17.0.2. Rename it to *jfx*.

2. On the **Linux** system, Altera recommends that you unzip the files and rename the folders using the following commands:

```
# unzip openjfx-17.0.2_linux-x64_bin-sdk.zip -d /opt/Java/  
# tar zxvf OpenJDK11U-jre_x64_linux_hotspot_11.0.15_10.tar.gz -C /opt/Java/  
# cd /opt/Java  
# mv javafx-sdk-17.0.2 jfx  
# mv jdk-11.0.15+10-jre jre
```

You have the following two directories on your **Linux** system:

- /opt/Java/jre
- /opt/Java/jfx

#### 4.1.4. Setting Up the Quartus Prime Software for BTS Operation

You must install the Quartus Prime software to support the silicon on the development kit. The recommended version is located in the `README.txt` file in the `examples\board_test_system` directory. If you choose to install individual files, you must install Agilex 7 Device Support.

The BTS communicates over JTAG to a test design running in the FPGA. The BTS shares the JTAG with other applications such as the Nios® II JTAG Debug Module and the Signal Tap Logic Analyzer. Altera recommends closing other applications before using BTS, as the GUI is designed based on the Quartus Prime software.

The BTS relies on the Quartus Prime software's specific library. Before running the BTS, open the Quartus Prime software to automatically set the environment variable `QUARTUS_ROOTDIR`. You can also change it through **Environment Variables** in the **System Properties** in Windows\*. The BTS uses this environment variable to locate the Quartus Prime library.

##### Related Information

[Installing the Quartus Prime Pro Edition Software](#) on page 7

#### 4.1.5. Running the BTS GUI

With the power to the board off, follow these steps:

1. Connect the USB cable to your PC and the board.
2. Check that the development board switches and jumpers are set according to your preferences. Refer to the [Development Kit Setup](#) section.
3. Check the external modules status: QSFPDD/DDR4 DIMM.
4. Turn on the board power switch.

**Note:** To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The BTS cannot run correctly unless the USB cable is attached, and the board is on.

To run the BTS, navigate to the `<package dir>\examples\board_test_system` directory. The BTS release folder always includes the following files:

**Figure 4. BTS Folder**

Name	Type
image	File folder
lib	File folder
BoardTestSystem.bat	Windows Batch File
BoardTestSystem.sh	Shell Script
bts.jar	JAR File
ClockController.bat	Windows Batch File
ClockController.sh	Shell Script
PowerMonitor.bat	Windows Batch File
PowerMonitor.sh	Shell Script
README.TXT	TXT File

You can run the BTS GUI with the following scripts:

1. On the **Windows** system, double-click the .bat files to run the BTS, **Clock Controller**, or **Power Monitor** GUI.

**Figure 5. Windows Console**

```

Select C:\windows\System32\cmd.exe
*****
*          BOARD TEST SYSTEM          *
*****

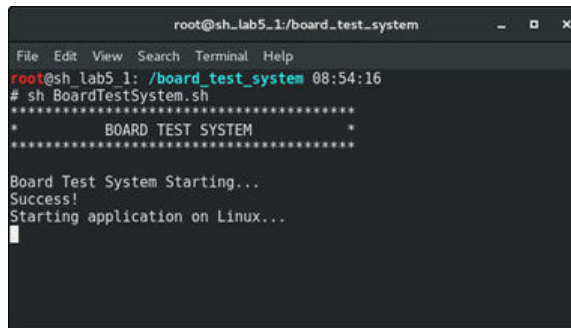
Board Test System starting...

E:\board_test_system>"C:\Program Files\Java\jre\bin\java.exe" --module-path "C:\Program Files\Java\jfx\lib" --add-module
s javafx.controls,javafx.fxml,javafx.web -jar bts.jar
Success!
Starting application on Windows 11...

```

2. On the **Linux** system, run the shell script with root privilege.

**Figure 6. Linux Console**



```
root@sh_lab5_1:/board_test_system
File Edit View Search Terminal Help
root@sh lab5 1: /board_test_system 08:54:16
# sh BoardTestSystem.sh
*****
*          BOARD TEST SYSTEM          *
*****
Board Test System Starting...
Success!
Starting application on Linux...
```

*Note:* The .bat or shell script checks the Java environment settings, copies necessary files, and prompts if the environment is not set up correctly.

The GUI displays the application tab corresponding to the design running in the FPGA. If the design loaded in the FPGA is not supported by the BTS GUI, a message prompting you to configure your board with a valid BTS design appears. Refer to *The Configure Menu* section.

#### Related Information

[The Configure Menu](#) on page 15

## 4.2. Test the Functionality of the Development Kit

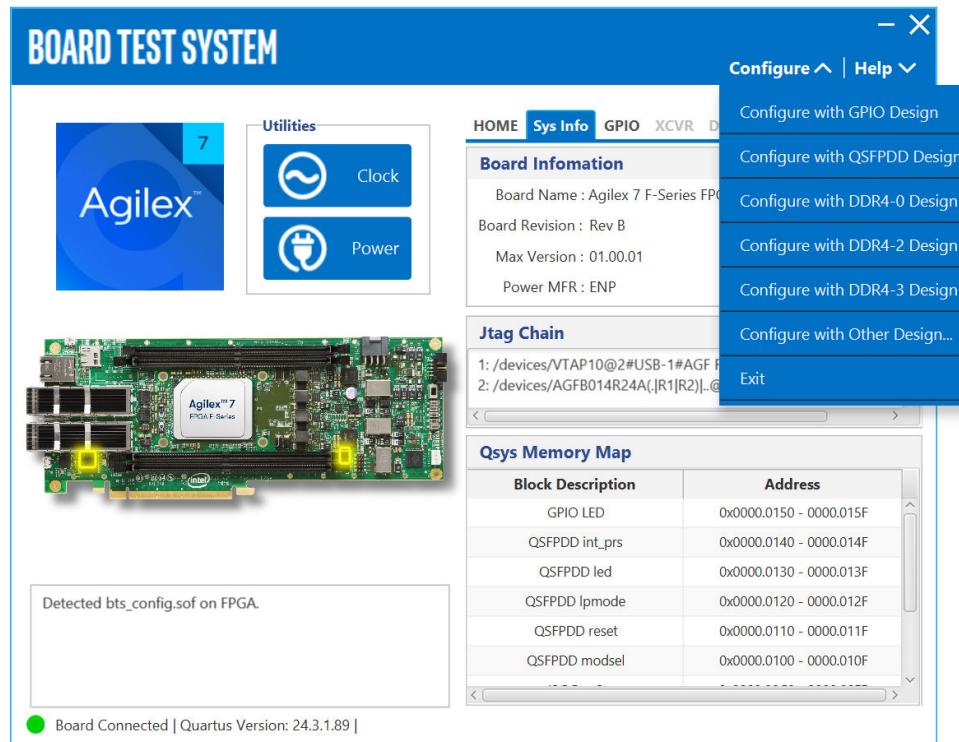
This section describes each control in the Board Test System (BTS).

The BTS checks for hardware faults before you can use the board. If one or more BTS test items fail, it indicates either a wrong hardware setting or a hardware fault on a specific interface.

### 4.2.1. The Configure Menu

Use the **Configure** menu to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

**Figure 7. The Configure Menu**



To configure the FPGA with a test system design, perform the following steps:

1. On the **Configure** menu, click the **Configure** command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click **Configure** to download the corresponding design's SRAM Object File (.sof) to the FPGA. The download process usually takes less than a minute.

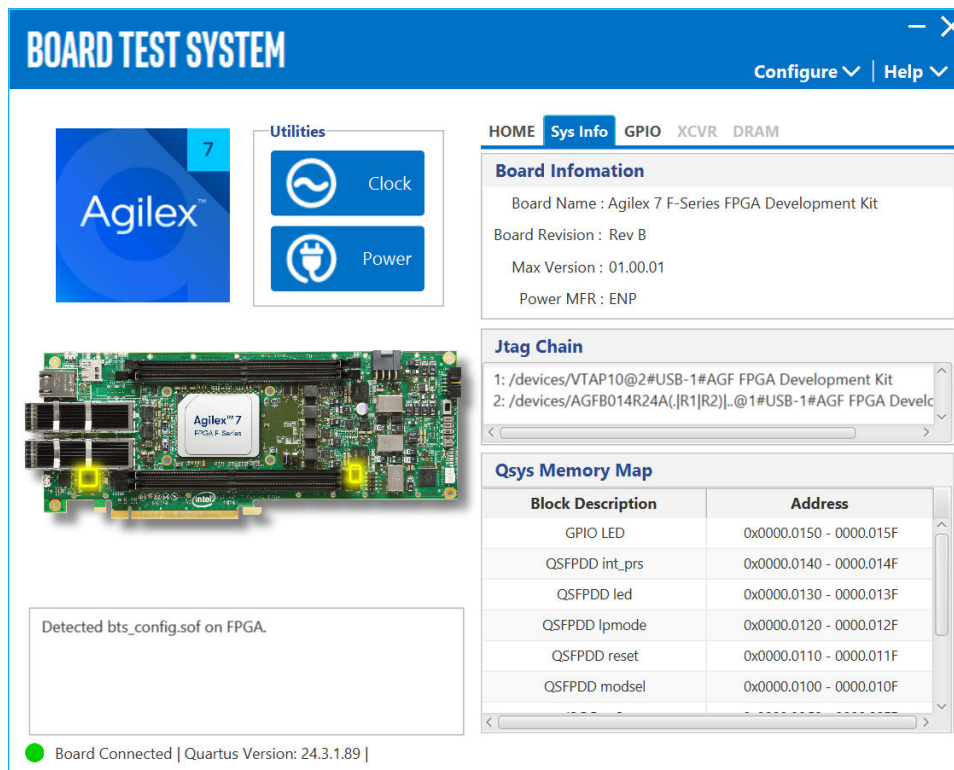
When configuration finishes, the design begins running in the FPGA. The corresponding Graphical User Interface (GUI) application tabs that interface with the design are now enabled. If you use the Quartus Prime Programmer for configuration, rather than the BTS GUI, you may need to restart the GUI.

### 4.2.2. The Sys Info Tab

The **Sys Info** tab shows information about the board's current configuration. The tab displays the board information, JTAG chain devices, and Qsys memory map for the `bts_config.sof` design and other details stored on the board.



**Figure 8. The Sys Info Tab**



The following sections describe the controls on the **System Info** tab.

### Board Information

The **Board Information** control displays static information about your board.

- **Board Name:** Indicates the official name of the board given by the BTS.
- **Board Revision:** Indicates the revision of the board.
- **Max Version:** Indicates the version of the system MAX 10.
- **Power MFR:** Indicates the FPGA Power manufacture.

### JTAG Chain

The **JTAG Chain** control shows all the devices currently in the JTAG chain.

*Note:*

The system MAX 10 (VTAP) is always on the JTAG chain, but change the settings of SW4 to low or high to bypass or enable power MAX 10, HPS, and Agilex 7 FPGA. The system MAX 10 and FPGA should all be in the JTAG chain when configured and running the BTS GUI.

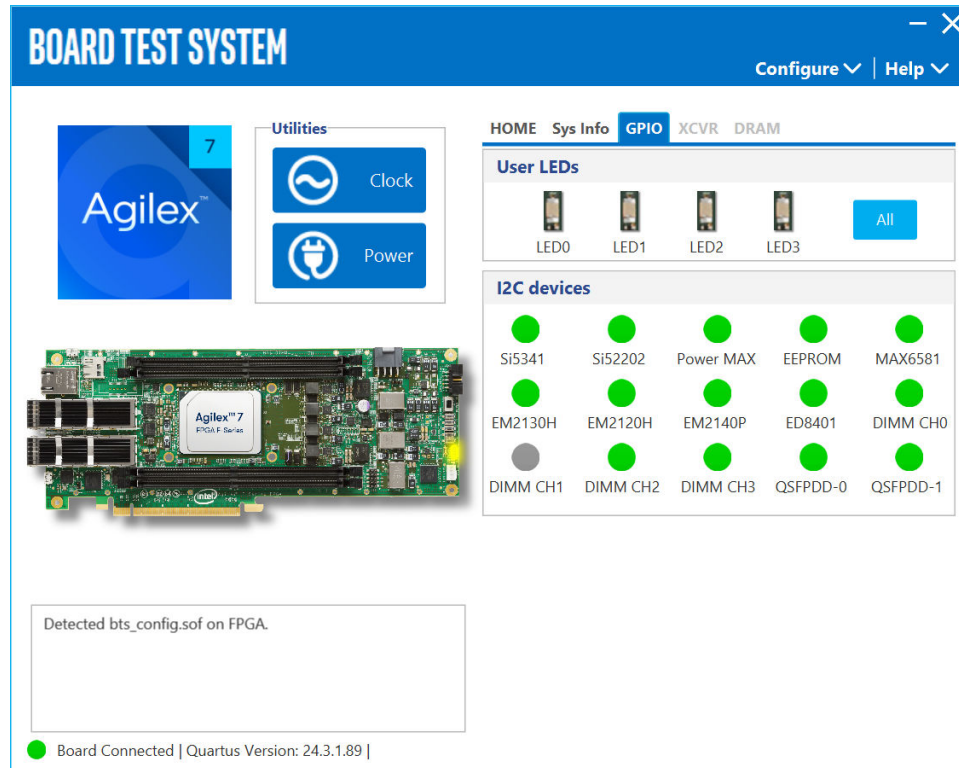
### Qsys Memory Map

The **Qsys Memory Map** control shows the memory map of the `bts_config.sof` design running on your board. This can be visible when the `bts_config.sof` design is running on board.

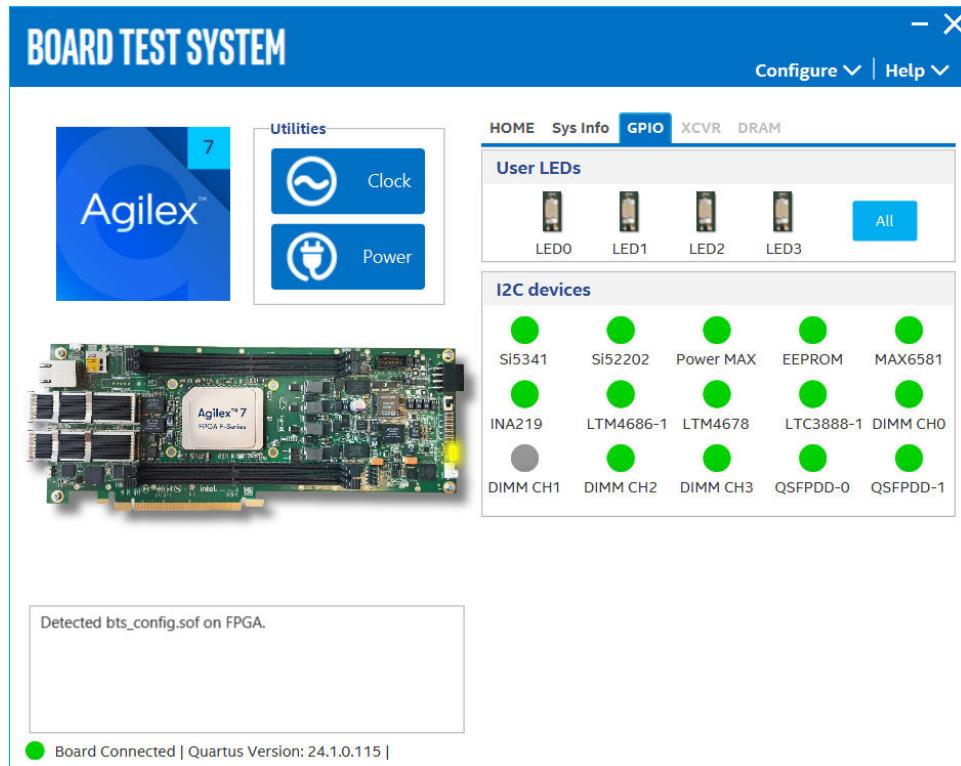
### 4.2.3. The GPIO Tab

The **GPIO** tab allows you to interact with all the general-purpose user I/O (GPIO) components on your board. You can turn LEDs on or off and detect I<sup>2</sup>C target devices connection status.

**Figure 9. The GPIO Tab (for the Agilex 7 DK-DEV-AGF014EA Development Kit)**



**Figure 10. The GPIO Tab (for the Agilex 7 DK-DEV-AGF014EB Development Kit)**



The following sections describe the controls on the **GPIO** tab.

#### User LEDs

The User LEDs control displays the current state of the user LEDs. Toggle the LED buttons to turn the board LEDs on and off.

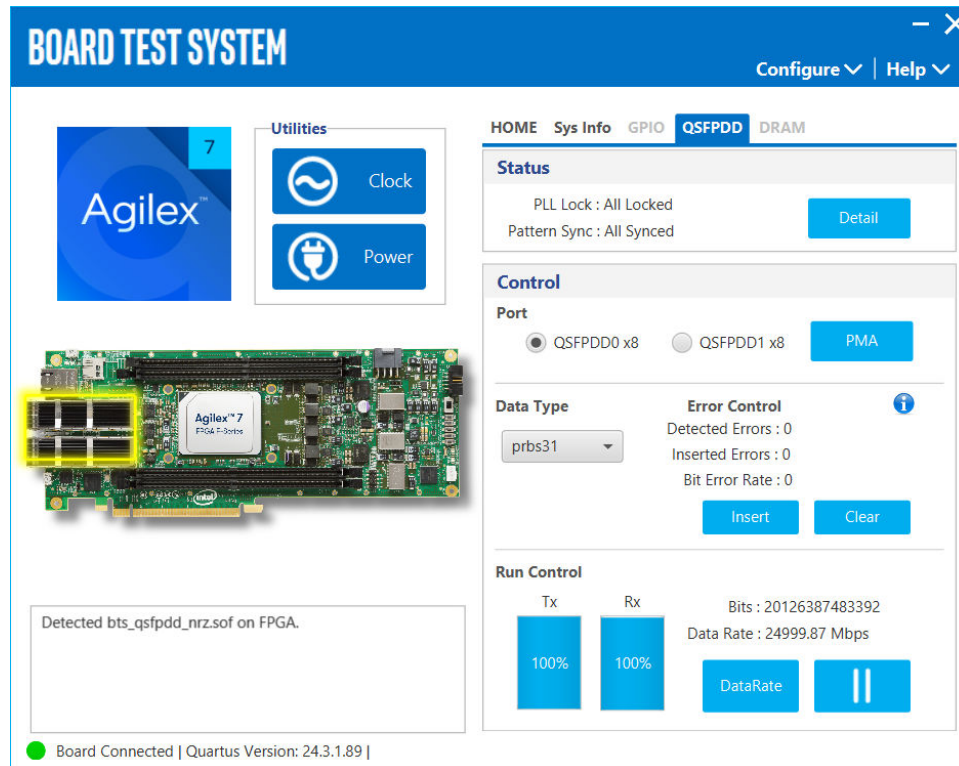
#### I2C devices

The read-only I<sup>2</sup>C target devices control displays the connection status of devices which can be accessed by I<sup>2</sup>C bus. Unplug some devices to see the graphical display change.

### 4.2.4. The QSPFDD Tab

The **QSPFDD** tab allows you to run transceivers QSPFDDx8 loopback tests on your board. You can run the test using either electrical loopback modules or optical fiber modules.

**Figure 11. The QSPDD Tab**



The following sections describe controls in the **QSPDD** tab.

### Status

The **Status** control displays the following status information during the loopback test:

- **PLL Lock:** Shows the PLL locked or unlocked state
- **Pattern Sync:** Shows the pattern synced or not state. The pattern is considered synced when the start of the data sequence is detected.
- **Detail:** Shows the PLL lock and pattern sync status.

### Control

Use the following controls to select an interface to apply PMA settings, data type and error control:

- **QSPDD0 x8**
- **QSPDD1 x8**

### PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback:** Routes signals between the transmitter and the receiver.
- **VOD:** Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap:**
  - **Pre-tap 1:** Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
  - **Pre-tap 2:** Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - **Pre-tap 3:** Specifies the amount of pre-emphasis on the third pre-tap of the transmitter buffer.
  - **Post-tap 1:** Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.
- **Equalizer:** Specifies the RX tuning mode for receiver equalizer.

Figure 12. QSFDD-PMA Setting

**PMA SETTING**
— ✕

	Serial Loopback	VOD	Pre-emphasis tap				Equalizer
			Pre-tap 1	Pre-tap 2	Pre-tap 3	Post-tap 1	
<input type="checkbox"/> All CH	<input type="checkbox"/>	0	0	0	0	10	Stop
CH0	<input type="checkbox"/>	0	0	0	0	10	Stop
CH1	<input type="checkbox"/>	0	0	0	0	10	Stop
CH2	<input type="checkbox"/>	0	0	0	0	10	Stop
CH3	<input type="checkbox"/>	0	0	0	0	10	Stop
CH4	<input type="checkbox"/>	0	0	0	0	10	Stop
CH5	<input type="checkbox"/>	0	0	0	0	10	Stop
CH6	<input type="checkbox"/>	0	0	0	0	10	Stop
CH7	<input type="checkbox"/>	0	0	0	0	10	Stop

### Data Type

The **Data Type** control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:

- **PRBS:** Pseudo-random 7-bit sequences (default)
- **PRBS15:** Pseudo-random 15-bit sequences
- **PRBS23:** Pseudo-random 23-bit sequences
- **PRBS31:** Pseudo-random 31-bit sequences

### Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the received bit stream.
- **Inserted Errors:** Displays the number of errors inserted into the transmit data stream.
- **Bit Error Rate:** Calculates the bit error rate of the transmit data stream.
- **Insert:** Insert a one-word error into the transmit data stream each time you click the button. **Insert** error is only enabled during transaction performance analysis.
- **Clear:** Resets the **Detected Errors** counter and **Inserted Errors** counter to zeros.

### Run Control

- **TX and RX performance bars:** Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Start:** This control initiates the loopback tests.
- **Data Rate:** Displays the XCVR type and data rate of each channel.

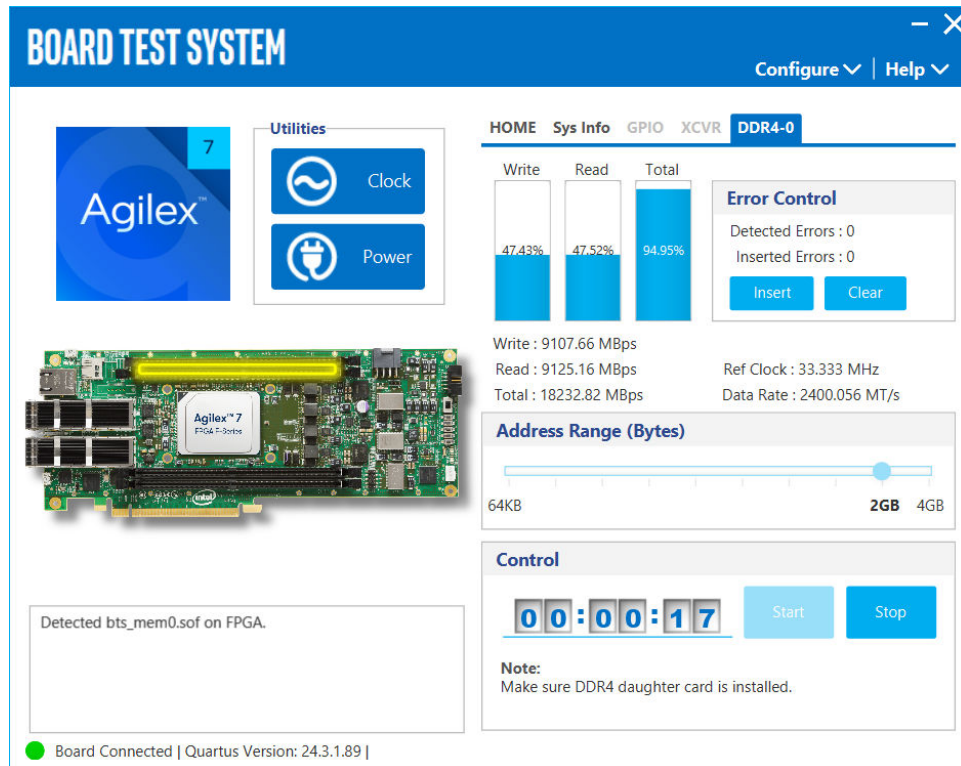
**Figure 13. XCVR—Data Rate**

Data Rate		
Channel	XCVR Type	Frequency
0	GXE	24999.94 Mbps
1	GXE	24999.81 Mbps
2	GXE	24999.94 Mbps
3	GXE	24999.81 Mbps
4	GXE	24999.94 Mbps
5	GXE	24999.81 Mbps
6	GXE	24999.94 Mbps
7	GXE	24999.94 Mbps

### 4.2.5. The DDR4-0 Tab

This tab allows you to read and write DDR4-0 memory on your board.

Figure 14. The DDR4-0 Tab



The following sections describe the controls on the **DDR4-0** tab.

### Start

Initiates DDR4 memory transaction performance analysis.

### Stop

Terminates transaction performance analysis.

### Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write, Read and Total performance bars:** Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps), Read (MBps) and Total (MBps):** Show the number of bytes analyzed per second.
- **Data Bus:** 72 bits (8 bits ECC) wide, reference clock is 33.33 MHz and the frequency is 1100 MHz double data rate 2400 MT/s.

### Error Control

This control displays data errors detected during analysis and allows you to insert errors:



- **Detected Errors:** Displays the number of data errors detected in the hardware.
- **Inserted Errors:** Displays the number of errors inserted into the transaction stream.
- **Insert:** Inserts a one-word error into the transaction stream each time you click the button. **Insert** error is only enabled during transaction performance analysis.
- **Clear:** Resets the **Detected Errors** and **Inserted Errors** counters to zeroes.

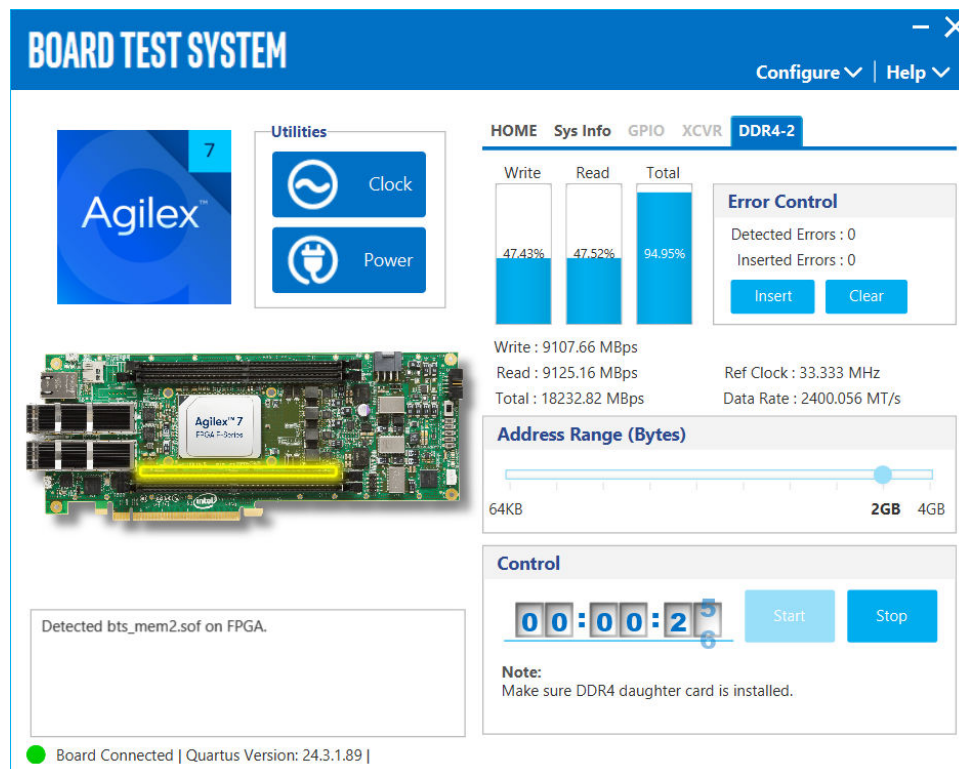
#### Number of Addresses to Read and Write

Determines the number of addresses to use in each iteration of reads and writes.

### 4.2.6. The DDR4-2 Tab

This tab allows you to read and write DDR4-2 memory on your board.

**Figure 15. The DDR4-2 Tab**



The following sections describe the controls on the **DDR4-2** tab.

#### Start

Initiates DDR4 memory transaction performance analysis.

#### Stop

Terminates transaction performance analysis.



### Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write, Read and Total performance bars:** Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps), Read (MBps) and Total (MBps):** Show the number of bytes analyzed per second.
- **Data Bus:** 72 bits (8 bits ECC) wide, reference clock is 33.33 MHz and the frequency is 1200 MHz double data rate 2400 MT/s.

### Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the hardware.
- **Inserted Errors:** Displays the number of errors inserted into the transaction stream.
- **Insert:** Inserts a one-word error into the transaction stream each time you click the button. **Insert** error is only enabled during transaction performance analysis.
- **Clear:** Resets the **Detected Errors** and **Inserted Errors** counters to zeroes.

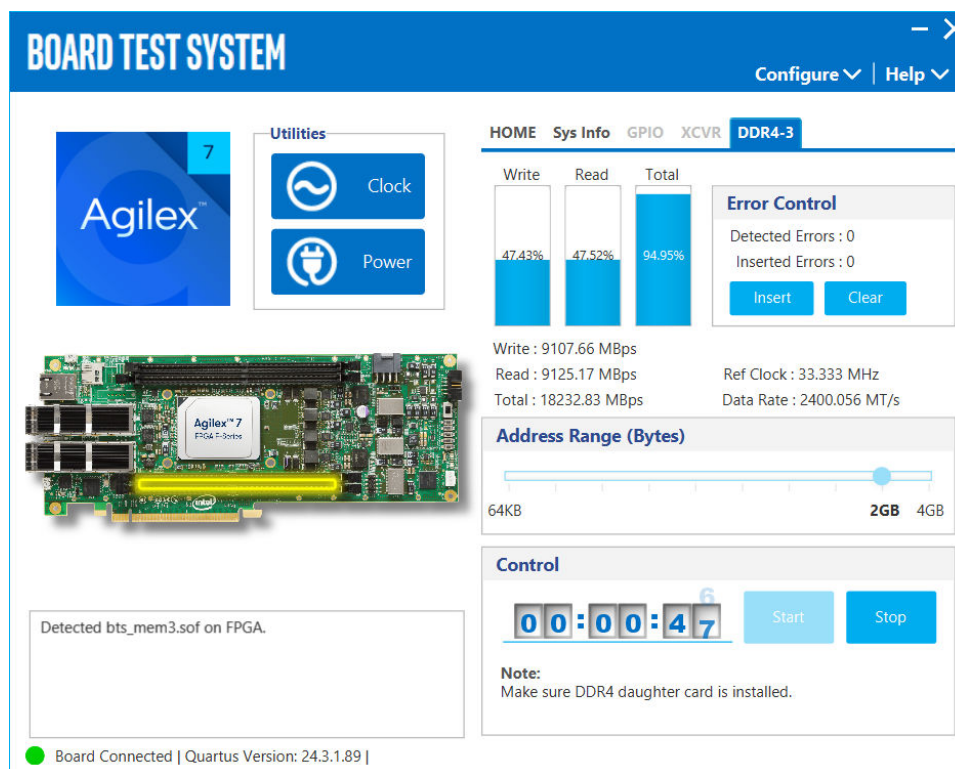
### Number of Addresses to Read and Write

Determines the number of addresses to use in each iteration of reads and writes.

## 4.2.7. The DDR4-3 Tab

This tab allows you to read and write DDR4-3 memory on your board.

**Figure 16. The DDR4-3 Tab**



The following sections describe the controls on the **DDR4-3** tab.

### Start

Initiates DDR4 memory transaction performance analysis.

### Stop

Terminates transaction performance analysis.

### Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write, Read and Total performance bars:** Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps), Read (MBps) and Total (MBps):** Show the number of bytes analyzed per second.
- **Data Bus:** 72 bits (8 bits ECC) wide, reference clock is 33.33 MHz and the frequency is 1200 MHz double data rate 2400 MT/s.

### Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the hardware.
- **Inserted Errors:** Displays the number of errors inserted into the transaction stream.
- **Insert:** Inserts a one-word error into the transaction stream each time you click the button. **Insert** error is only enabled during transaction performance analysis.
- **Clear:** Resets the **Detected Errors** and **Inserted Errors** counters to zeroes.

#### Number of Addresses to Read and Write

Determines the number of addresses to use in each iteration of reads and writes.

### 4.3. Control On-Board Clock through Clock Controller GUI

The **Clock Controller** application can change on-board Si5341 programmable PLLs to any customized frequency between 10 MHz and 750 MHz for differential output and 10 MHz to 350 MHz for LVCMOS single-ended output.

The instructions to run the **Clock Controller** GUI are stated in the [Running the BTS GUI](#) section. Alternatively, you can start using the **Clock Controller** feature by selecting the **Clock** icon on the BTS GUI.

The **Clock Controller** communicates with the System MAX 10 device through either a USB port J13 or a 10-pin JTAG header J14. The system MAX 10 controls these programmable clock parts through a 2-wire I<sup>2</sup>C bus.

*Note:* You cannot run the stand-alone **Clock Controller** application when the BTS or **Power Monitor** GUI is running at the same time.

**Figure 17. Clock Controller GUI**

**CLOCK CONTROLLER**

**Si5341**

**Frequency(MHz)**

OUT0	Enable ▾	156.25000	OUT5	Enable ▾	322.56263
OUT1	Enable ▾	33.33300	OUT6	Enable ▾	100.00000
OUT2	Enable ▾	33.33300	OUT7	Enable ▾	50.00000
OUT3	Enable ▾	33.33300	OUT8	Enable ▾	125.00000
OUT4	Enable ▾	33.33300	OUT9	Enable ▾	25.00000

F\_vco:  
14000.00000 MHz

Default Read Set Import

Connected to the target

The following sections describe the **Clock Controller** buttons.

#### Read

Reads the current frequency setting for the oscillator associated with the active tab.

#### Default

Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

#### Set

Sets the programmable oscillator frequency for the selected clock to the value in the CLKx output controls for the Si5338. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies.

### Import

You can generate the register list from the Skyworks\* ClockBuilder Pro tool and import it into Si5341 to update the settings of the RAM. Register changes are volatile after power cycling.

### Related Information

- [Running the BTS GUI](#) on page 13
- [Skyworks Solution](#)  
More information about the ClockBuilder Pro software.

## 4.4. Control On-Board Power Regulator through Power Monitor GUI

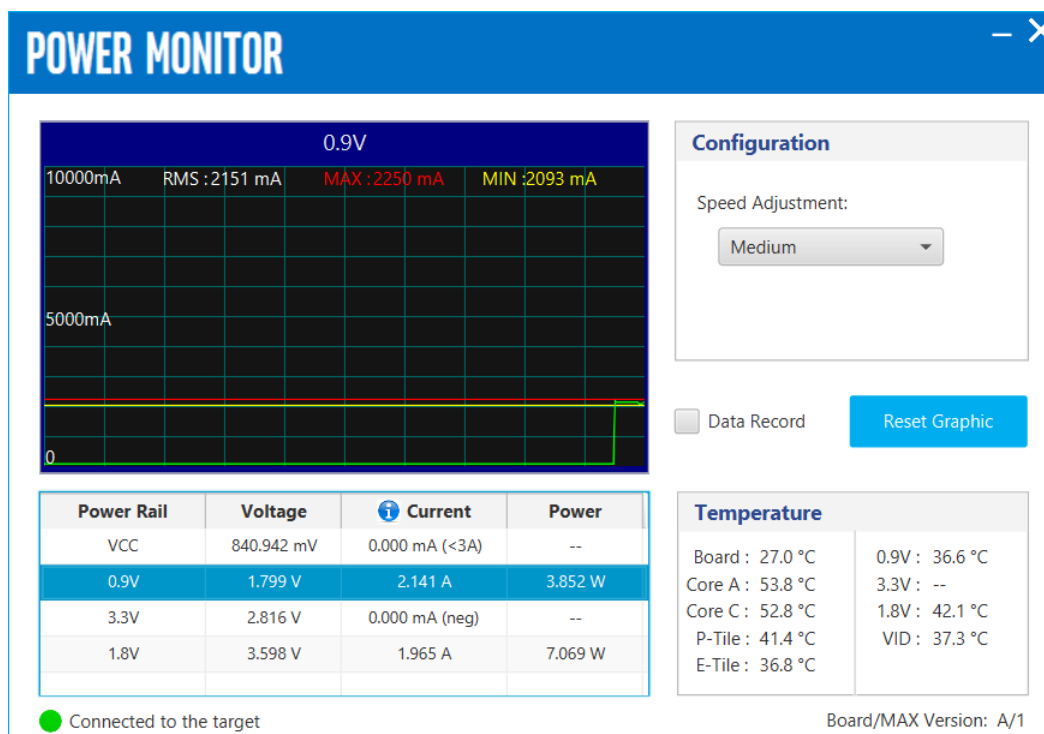
The **Power Monitor** application reports most power rails voltage, current, and power information on the board. It also collects temperature from FPGA die, power modules, and diodes assembled on PCB.

The **Power Monitor** GUI communicates with the system MAX 10 through either USB port J13 or 10-pin JTAG header J14. The system MAX 10 monitors and controls power regulator, and the temperature, voltage, and current sensing chips through a 2-wire serial bus.

The instructions to run the **Power Monitor** GUI are stated in the [Running the BTS GUI](#) section. Alternatively, you can start using the **Clock Controller** feature by selecting the **Power** icon on the BTS GUI.

**Note:** You cannot run the stand-alone **Power Monitor** application when the BTS or the **Clock Controller** GUI is running at the same time.

**Figure 18. Power Monitor GUI**



### Temperature

- **Board:** PCB surface temperature near U32.
- **E-Tile/P-Tile/Core A/Core C:** FPGA dies' internal TSD.
- **0.9V/3.3V/1.8V:** Regulator U55/U46/U71.

### Related Information

Running the BTS GUI on page 13

## 4.5. Identify Test Pass or Fail based on BTS GUI Test Status

### DDR4 DIMMs

Plug the DDR4 DIMM module, which is shipped alone with this development kit, in J1/J2/J3/J4. The BTS GUI only supports fabric memory interfaces, namely DDR4 #0, #2, and #3.

### QSFPDD/QSFP28

Plug QSFPDD/QSFP28 loopback module in J5/J6 before you configure QSFPDD NRZ example build through the BTS GUI. The pseudo random bitstream (PRBS) traffic is running at 25 Gbps for NRZ build, but you can manually try it out PAM4 at 50 Gbps with hard PRBS pattern with temporary PAM4 build in the installer package.

## 5. Development Kit Hardware and Configuration

The Agilex 7 FPGA F-Series Development Kit only supports AS x4 configuration mode on the board. You need to change either the hardware setting or re-program system images. or both, for the case.

The table below show which configuration mode it supports:

**Table 5. Supported Configuration Mode**

SW1[1:3]	MSEL[2:0]	Configuration Mode
OFF/ON/ON	001	AS - Fast Mode (Default Setting)
OFF/OFF/ON	011	AS - Normal Mode

### 5.1. Configure the FPGA and Access HPS Debug Access Port by JTAG

JTAG access does not rely on the SW1 settings and the system MAX 10 image.

Plug the USB cable to J13 or Intel FPGA Download Cable to J14.

Open the Quartus Prime programmer, system console to configure Agilex 7 FPGA SDM, system MAX 10 and PCIe JTAG nodes.

Open the Arm Development Studio 5\* (DS-5\*) Intel SoC FPGA Edition to connect and communicate with the HPS debug access port (DAP) through the same JTAG interface.

**Note:** By default, the HPS and FPGA SDM JTAG nodes are chained together internally. SW4 bypasses or enables both nodes at the same time.

If the attestation or Black Key Provisioning (BKP), or both, is enabled on the Agilex 7 device, you must use the updated SDM firmware and TCK guidelines (JTAG clock).

- You must update to the SDM firmware delivered with the Quartus Prime Pro Edition software version 21.3 and beyond.
- For the TCK pin, you must either leave the TCK pin unconnected, or connect the TCK pin to the VCCIO\_SDM supply using a 10-k $\Omega$  pull-up resistor.

**Note:** The existing guidance in the *Agilex 7 Device Family Pin Connection Guidelines: F-Series and I-Series* to connect TCK to a 1-k  $\Omega$  pull-down resistor is included for noise suppression. The change in guidance to a 10-k  $\Omega$  pull-up resistor is not expected to affect the device functionally.

For more information about connecting the TCK pin, refer to the *Agilex 7 Device Family Pin Connection Guidelines: F-Series and I-Series*.

### Related Information

[Agilex 7 Device Family Pin Connection Guidelines: F-Series and I-Series](#)

## 5.2. Configure the FPGA Device by AS Modes (Default Mode)

The default SW1 setting and system MAX 10 image support AS configuration mode. Power on and observe FPGA D13 Configuration LED behavior.

The Agilex 7 FPGA F-Series Development Kit also supports some HPS interfaces. You can demonstrate the following HPS functions on this board:

- 10/100/1000 Mbps Ethernet PHY: U7\_KSZ9031 and RJ45 connector J8
- USB UART for communication port: micro USB connector J10
- SD socket: J11
- eMMC on board: U16\_MTFC8GAKAJCN-4M
- Mictor Connector for debug: J12





## 6. Custom Projects for the Development Kit

### 6.1. Add SmartVID settings in the QSF file

Agilex 7 FPGA assembled on this development kit enables SmartVID feature by default.

You must put the constraints listed below into your project QSF file to avoid the Quartus Prime software from generating an error due to incomplete SmartVID settings.

Open your project QSF file and copy and paste constraint scripts listed below into the file. You must ensure that there are no other similar settings with different values.

```
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS 47
set_global_assignment -name PWRMGT_SLAVE_DEVICE1_ADDRESS 00
set_global_assignment -name PWRMGT_SLAVE_DEVICE2_ADDRESS 00
set_global_assignment -name ACTIVE_SERIAL_CLOCK_AS_FREQ_100MHZ
set_global_assignment -name USE_PWRMGT_SCL SDM_IO14
set_global_assignment -name USE_PWRMGT_SDA SDM_IO11
set_global_assignment -name USE_CONF_DONE SDM_IO16
```

#### For Agilex 7 FPGA F-Series Development Kit (DK-DEV-AGF014E3ES and DK-DEV-AGF014EB)

```
set_global_assignment -name PWRMGT_BUS_SPEED_MODE "100 KHZ"
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE OTHER
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "LINEAR FORMAT"
set_global_assignment -name PWRMGT_LINEAR_FORMAT_N "-12"
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE ON
```

#### For Agilex 7 FPGA F-Series Development Kit (DK-DEV-AGF014E2ES and DK-DEV-AGF014EA)

```
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE ED8401
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "LINEAR FORMAT"
set_global_assignment -name PWRMGT_LINEAR_FORMAT_N "-13"
set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE OFF
```

### 6.2. Golden Top

You can use the Golden Top project as the starting point. It contains the constraints, pin locations, defines I/O standards, direction, and general termination.

**Note:** The Golden Top project is slightly different from the Agilex 7 FPGA F-Series Development Kit's -3V version to -2V version. Refer to corresponding Golden Top project in installer package for more information.

## 7. Document Revision History for the Agilex 7 FPGA F-Series Development Kit User Guide

Document Version	Changes
2025.01.16	<ul style="list-style-type: none"> <li>Updated the <i>Overview</i> chapter: <ul style="list-style-type: none"> <li>Retitled figures in <i>Block Diagram</i> for clarity.</li> <li>Moved content about feature summary of the Agilex 7 FPGA F-Series Development Kit in <i>Block Diagram</i> to a new topic—<i>Feature Summary</i>.</li> <li>Updated Figure: <i>Agilex 7 FPGA F-Series Development Kit Block Diagram</i>.</li> <li>Retitled topic <i>Operating Conditions</i> to <i>Recommended Operating Conditions</i>.</li> <li>Removed information about handling precautions from <i>Recommended Operating Conditions</i>.</li> </ul> </li> <li>Updated the <i>Getting Started</i> chapter: <ul style="list-style-type: none"> <li>Added new topics: <ul style="list-style-type: none"> <li><i>Before You Begin</i></li> <li><i>Handling the Board</i></li> <li><i>Installing the Quartus Prime Pro Edition Software</i></li> <li><i>Installing the Intel SoC EDS</i></li> <li><i>Installing the Development Kit</i></li> <li><i>Installing the Intel FPGA Download Cable II Driver</i></li> </ul> </li> <li>Removed <i>Design Examples</i>.</li> </ul> </li> <li>Updated the <i>Powering Up the Development Kit</i> chapter: <ul style="list-style-type: none"> <li>Retitled chapter title <i>Powering Up the Development Kit</i> to <i>Development Kit Setup</i>.</li> <li>Updated information and retitled topic title <i>Power Up</i> to <i>Powering Up the Development Kit</i>.</li> </ul> </li> <li>Updated the <i>Board Test System</i> chapter: <ul style="list-style-type: none"> <li>Updated Figure: <i>Windows Console</i> in the <i>Running the BTS GUI</i> section.</li> <li>Retitled topic <i>Installing the Quartus Prime Software</i> to <i>Setting Up the Quartus Prime Software for BTS Operation</i>.</li> <li>Updated all the figures in the <i>Test the Functionality of the Development Kit</i> section.</li> <li>Updated the <i>Control On-Board Power Regulator through Power Monitor GUI</i> section.</li> <li>Updated the data bus information under the <i>Performance Indicators control</i> section in the following topics: <ul style="list-style-type: none"> <li><i>The DDR4-0 Tab</i></li> <li><i>The DDR4-2 Tab</i></li> <li><i>The DDR4-3 Tab</i></li> </ul> </li> </ul> </li> <li>Updated <i>Configure the FPGA Device by AS Modes (Default Mode)</i> in the <i>Development Kit Hardware and Configuration</i> chapter.</li> <li>Updated <i>Add SmartVID settings in the QSF file</i> in the <i>Custom Project for the Development Kit</i> chapter.</li> <li>Updated Table: <i>SW5 Pin Connections</i> in <i>Switches</i> under the <i>Development Kit Components</i> appendix chapter.</li> <li>Added new appendix chapter—<i>Development Resources</i>.</li> <li>Retitled appendix chapter <i>Additional Information</i> to <i>Safety and Regulatory Compliance Information</i>.</li> <li>Restructured the document to improve clarity and for ease of reference.</li> <li>Updated the document for the latest branding standards.</li> </ul>
2024.01.18	Removed <i>Quick Start Guide</i> .
continued...	

Document Version	Changes
2023.11.30	<ul style="list-style-type: none"> <li>Added Figure: <i>Power Tree (for the Agilex 7 DK-DEV-AGF014EB Development Kit—Power Solution 2)</i>.</li> <li>Added Figure: <i>The GPIO Tab (for the Agilex 7 DK-DEV-AGF014EB Development Kit)</i>.</li> <li>Updated Figure: <i>The GPIO Tab (for the Agilex 7 DK-DEV-AGF014EA Development Kit)</i>.</li> <li>Updated Table: <i>Ordering Information</i>.</li> <li>Updated the <i>Agilex 7 FPGA</i> section.</li> <li>Updated the <i>JTAG Chain and Header</i> section.</li> <li>Updated the <i>Power</i> section.</li> </ul>
2023.09.13	Updated the device part number of the <i>Agilex 7 FPGA F-Series Development Kit (Production -2V)</i> in Table: <i>Ordering Information</i> .
2023.06.26	<ul style="list-style-type: none"> <li>Updated product family name to "Agilex 7".</li> <li>Updated development kit name to Agilex 7 FPGA F-Series Development Kit.</li> <li>Retitled the document from <i>Agilex F-Series FPGA Development Kit User Guide</i> to <i>Agilex 7 FPGA F-Series Development Kit User Guide</i>.</li> </ul>
2022.12.30	<ul style="list-style-type: none"> <li>Added Section: <i>Setting Up the BTS GUI Running Environment</i></li> <li>Moved <i>Control on-board clock through Clock Controller GUI</i> and <i>Control on-board power regulator through Power Monitor GUI</i> to the <i>Board Test System</i> section.</li> </ul>
2022.09.30	Updated the <i>Additional Information</i> section to include the UKCA declaration.
2022.06.21	Updated the <i>Configure the FPGA and access HPS Debug Access Port by JTAG</i> section to provide more details on the TCK guidelines if attestation or Black Key Provisioning is enabled.
2022.02.21	Updated the settings in the <i>For Agilex 7 F-Series FPGA Development Kit (-3V version)</i> subsection.
2021.08.13	<ul style="list-style-type: none"> <li>Added Figure: <i>Power Tree Block Diagram (-2V Production Device)</i>.</li> <li>Updated Table: <i>Ordering Information</i> to include production device.</li> <li>Updated Table: <i>Power Sequence Groups</i> to include a note for VCCA_PLL power rail.</li> <li>Updated the description for <code>power_max10</code> directory in Table: <i>Installed Development Kit Directory Structure</i>.</li> <li>Updated the feature summary in the <i>Block Diagram</i> section.</li> <li>Updated the <i>Software and Driver Installation</i> section to include references to the <i>Agilex 7 FPGAs and SoCs Device Overview</i> and <i>Agilex 7 Device Data Sheet</i>.</li> <li>Updated the <i>A.1. Agilex 7 FPGA</i> section.</li> <li>Updated the <i>A.4. Memory Interfaces</i> section.</li> </ul>
2020.09.02	Updated note in <i>Box Contents</i> .
2020.07.09	Added Board Test System (BTS) information.
2020.05.15	Engineering Silicon (ES) release.
2020.02.11	Initial release.



## A. Development Kit Components

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### A.1. Agilex 7 FPGA

Agilex 7 FPGA F-Series F2486A or F2486B

- Part Number:
  - AGFB014R24BE2V (-2V production version)
  - AGFB014R24BE2V (-2V production version, Rev A1)
  - AGFB014R24A2E3VR0 (-3V ES version)
  - AGFB014R24A2E2VR0 (-2V ES version)
- F2486A or F2486B FBGA Package 55 mm x 42.5 mm
- 1473 KLEs
- 9200 18x19 Multipliers
- 36 Mb eSRAM
- 16 x 28 Gbps NRZ transceivers (E-Tile)
- 16 x 17.4 Gbps NRZ transceivers (P-Tile)
- 1x PCIe 4.0 x16 Hard IP blocks
- 1x 100G Ethernet MAC Hard IP blocks
- 768 GPIO

### A.2. Configuration Support

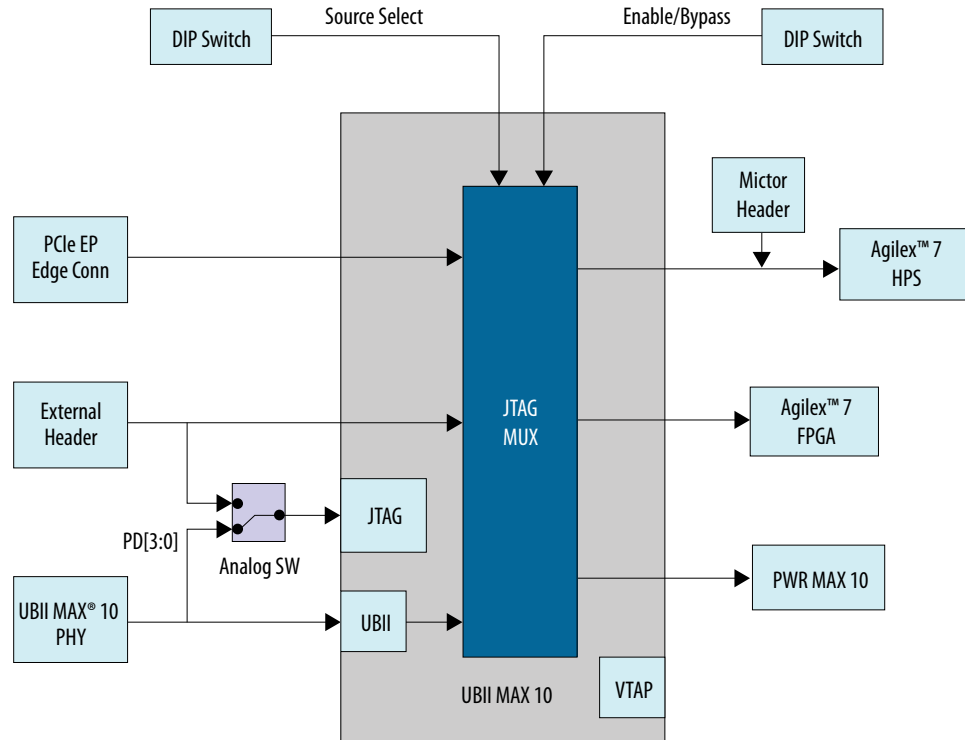
This development kit supports two configuration methods. A DIP switch is used to select between JTAG only mode and AS x4 configuration mode by manipulating the MSEL pins.

1. AS x4 Mode. MT25QU02GCBB3E12-1SIT is a QSPI FLASH on board to support AS x4 configuration mode.
2. JTAG Mode.
  - a. JTAG via 10-pin header for connecting an Altera standard UB2/UB1 dongle. The header shall be a right angle shrouded type connector and it is accessible through the PCIe bracket.
  - b. On-board Intel FPGA Download Cable

#### A.2.1. JTAG Chain and Header

The following figure shows the JTAG chain connections. An option to bypass the Agilex 7 FPGA during board bring up is provided but not shown in the figure.

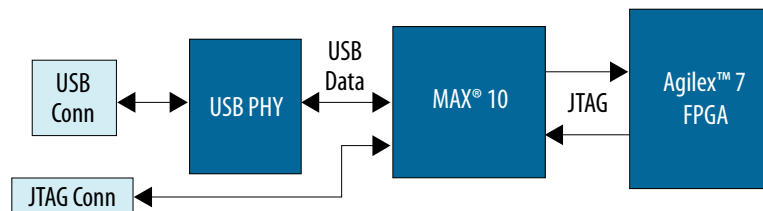
**Figure 19. JTAG Chain on the Development Kit**



The JTAG chain allows programming of the Agilex 7 FPGA and the MAX 10 CPLD devices using the external Intel FPGA Download Cable II dongle. The dongle can be used to program both the Agilex 7 FPGA and MAX 10 CPLD via the external 2x5 pin 0.1" programming header. This header uses a shrouded vertical connector and is designed to be accessible from the PCIe bracket side. This avoids having to remove the PC case to program the device when the board is installed in a closed system.

## A.2.2. On-board Intel FPGA Download Cable II

**Figure 20. Intel FPGA Download Cable II Block Diagram**



The embedded Intel FPGA Download Cable II core for USB-based configuration of the Agilex 7 FPGA is implemented using a TYPE B USB connector, a CY7C68013A USB2 PHY device, and a MAX 10 device. This allows for the configuration of the Agilex 7 FPGA using a USB cable directly connected to a PC running Quartus Prime software without requiring the external Intel FPGA Download Cable II dongle.

This design converts USB data to interface with the Agilex 7's dedicated JTAG port. Four LEDs are provided to indicate Intel FPGA Download Cable II activity. Two of them monitor the JTAG data-in and data-out signals; the remaining two monitor System Console activity. The embedded Intel FPGA Download Cable is automatically disabled when an external Intel FPGA Download Cable II dongle is connected to the JTAG chain.

### A.3. Clocks

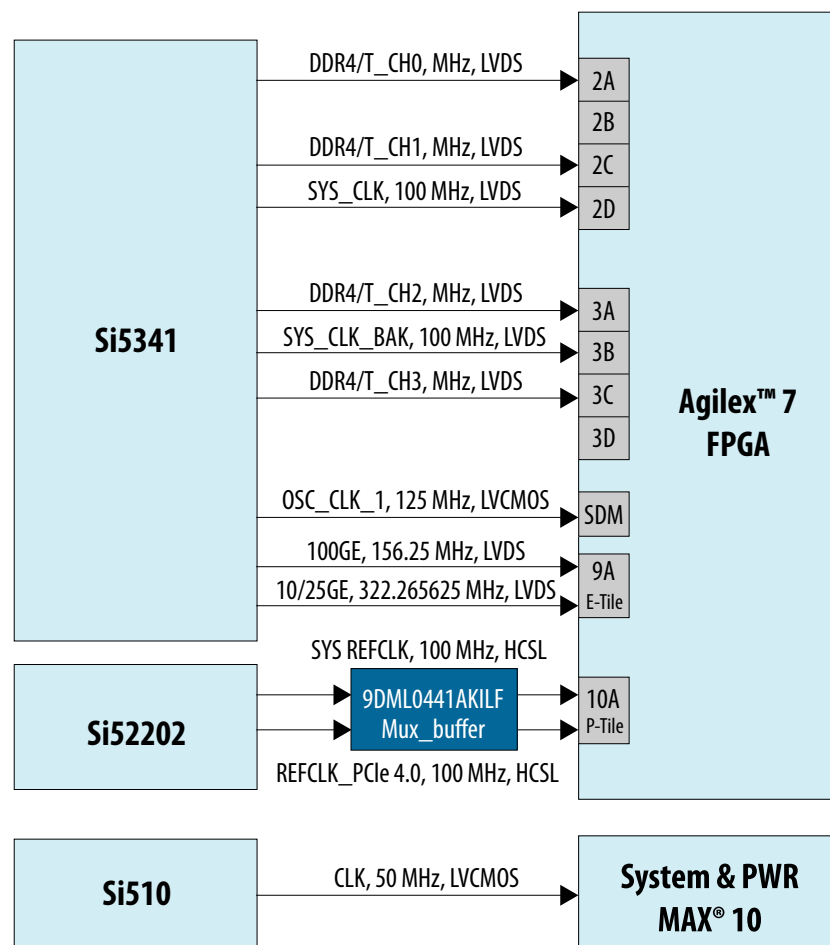
There are three clock devices in the Agilex 7 FPGA F-Series Development Kit: Si5341, Si52202, and Si510.

Si5341 provides most of clocks to the Agilex 7 FPGA including reference clocks for the memory interfaces, QSFP-DD, and the FPGA SDM or fabric core.

Si52202 provides the dedicated reference clock as an local clock option of the PCIe 4.0 by choosing in clock buffer 9DML0441AKILF. Another input of the clock buffer is from the PCIe golden finger as a system clock of the PCIe 4.0.

Si510 provides a 50 MHz clock to the system MAX 10 and the power MAX 10.

**Figure 21. Clocking in the Agilex 7 FPGA F-Series Development Kit**



## A.4. Memory Interfaces

The Agilex 7 FPGA F-Series Development Kit has four channels of 288 pin DDR4 DIMM 72-bit interfaces: DDR4 DIMM CH0, DDR4 DIMM CH1, DDR4 DIMM CH2, and DDR4 DIMM CH3.

DDR4 DIMM CH1 is designed for HPS dedicated applications. The other three memory channels are for FPGA general usage and support both DDR4 and DDR-T (Intel Optane™ PMem modules).

- DDR4 DIMM CH0 is located in FPGA Bank 3A and 3B. It supports both DDR4 and DDR-T modules.
- DDR4 DIMM CH1 is located in FPGA Bank 3C and 3D. It only supports DDR4 module.
- DDR4 DIMM CH2 is located in FPGA Bank 2A and 2B. It supports both DDR4 and DDR-T modules.
- DDR4 DIMM CH3 is located in FPGA Bank 2C and 2D. It supports both DDR4 and DDR-T modules.

## A.5. Transceiver Interfaces

Two transceiver banks are present on the Agilex 7 FPGA F-Series Development Kit:

- Bank 9A is used for two standard QSFP-DD optical modules (J5 and J6) and support up to 200 Gbps with hard IP for each QSFP-DD module
- Bank 10A is fully compliant with PCIe 4.0 x16 and are connected to the golden finger J7 in this PCIe add-in card

## A.6. HPS Interface

The Agilex 7 FPGA F-Series Development Kit enables the HPS function and supports several HPS interfaces:

- RJ 45 supporting Ethernet 10/100/1000 Mbps by RGMII
- UART port by USB (Micro) connector
- Micro SD card socket
- Mictor Connector for HPS JTAG
- eMMC (8 GB x 8)

**Note:** Golden Software Reference Design for HPS (GSRD) is not currently available for this development kit.

## A.7. General Input and Output

### A.7.1. Switches

**Table 6. SW1 Pin Connections**

SW1 Pin	Board Label	Function	Default Settings
SW1 . 1	MSEL0	Mode select 0 for configuration	OFF
SW1 . 2	MSEL1	Mode select 1 for configuration	ON
SW1 . 3	MSEL2	Mode select 2 for configuration	ON

**Table 7. SW2 Pin Connections**

SW2 Pin	Board Label	Function	Default Settings
SW2 . 1	USB MAX JTAG SEL	ON: UBII MAX10 JTAG select External JTAG HEADER. OFF: UBII MAX 10 JTAG select USB PHY.	OFF
SW2 . 2	SI5341 Enable	ON: Disable SI5341's outputs OFF: Enable SI5341's outputs	OFF
SW2 . 3	SI52202 Power Down	ON: Power down SI52202 OFF: Power up SI52202	OFF
SW2 . 4	UART Enable	ON: Disable UART OFF: Enable UART	OFF

**Table 8. SW3 Pin Connections**

SW3 Pin	Board Label	Function	Default Settings
SW3 . 1	FPGA I2C Enable	ON: Isolate FPGA from main I <sup>2</sup> C chain. OFF: connect FPGA to main I <sup>2</sup> C chain.	OFF
SW3 . 2	HPS I2C Enable	ON: Isolate HPS from main I <sup>2</sup> C chain. OFF: connect HPS to main I <sup>2</sup> C chain.	OFF
SW3 . 3	Main PMBUS Enable	ON: Isolate power module of VCC_core from main I <sup>2</sup> C chain. OFF: connect power module of VCC_core to main I <sup>2</sup> C chain.	OFF
SW3 . 4	FPGA PMBUS Enable	ON: Isolate power module of VCC_core from SDM PMBUS. OFF: connect power module of VCC_core to SDM PMBUS.	OFF



**Table 9. SW4 Pin Connections**

SW4 Pin	Board Label	Function	Default Settings
SW4 . 1	JTAG Input Source	ON: Select PCIe edge as JTAG master when external JTAG is absent. OFF: Select On-Board Intel FPGA Download Cable as JTAG master when external JTAG is absent.	OFF
SW4 . 2	Power MAX 10 Bypass	ON: Bypass the power MAX 10 in the JTAG chain.	ON
SW4 . 3	Mictor Bypass	ON: Bypass HPS in the JTAG chain. OFF: Enable HPS in the JTAG chain.	ON
SW4 . 4	FPGA Bypass	ON: Bypass FPGA in the JTAG chain. OFF: Enable FPGA in the JTAG chain.	OFF

**Table 10. SW5 Pin Connections**

SW5 Pin	Board Label	Function	Default Settings
SW5	Power ON/OFF	Power on/off the board	OFF

**Table 11. SW6 Pin Connections**

SW6 Pin	Board Label	Function	Default Settings
SW6 . 1	PCIe EP Present x16	ON: x16 select OFF: x16 deselect	ON
SW6 . 2	PCIe EP Present x8	ON: x8 select OFF: x8 deselect	OFF
SW6 . 3	PCIe EP Present x4	ON: x4 select OFF: x4 deselect	OFF
SW6 . 4	PCIe EP Present x1	ON: x1 select OFF: x1 deselect	OFF

**Table 12. SW7 Pin Connections**

SW7 Pin	Board Label	Function	Default Settings
SW7 . 1	SEL_A_B	ON: select SI52202 as clock source for PCIe 4.0 OFF: select PCIe edge as clock source for PCIe 4.0	OFF

## A.7.2. Buttons

**Table 13. Buttons on the Development Kit**

Board Reference	Type	Description
S1	HPS cold reset	Cold reset to HPS
S2	CPU reset	Fabric core reset
<i>continued...</i>		

Board Reference	Type	Description
S3	PCIe reset	PCIe Hard IP reset
S4	HPS warm reset	Warm reset to HPS
S5	System MAX 10 reset	On-board Intel FPGA Download Cable Reset

### A.7.3. LEDs

**Table 14. LEDs on the Development Kit**

Board Reference	Schematic Signal Name	Agilex 7 FPGA Pin Number	I/O Standard
D7	FPGA_3V3_LED0	C30	1.2V LVCMOS
D9	FPGA_3V3_LED1	A30	1.2V LVCMOS
D10	FPGA_3V3_LED2	D31	1.2V LVCMOS
D12	FPGA_3V3_LED3	B31	1.2V LVCMOS
D13	FPGA_CONF_DONE	CA60	1.8V LVCMOS
D14	FPGA_CVP_CONFDONE	CA58	1.8V LVCMOS
D8	PWR_LED_DR	B12 (Max10_U30)	3.3V LVCMOS
D11	OVERTEMPn	K11 (Max10_U30)	3.3V LVCMOS
D21	QSFPDD0_LED0	H19	1.2V LVCMOS
D22 (Bi-color)	QSFPDD0_LED1	F19	1.2V LVCMOS
	QSFPDD0_LED2	J20	1.2V LVCMOS
D23	QSFPDD1_LED0	G20	1.2V LVCMOS
D24 (Bi-color)	QSFPDD1_LED1	H21	1.2V LVCMOS
	QSFPDD1_LED2	F21	1.2V LVCMOS

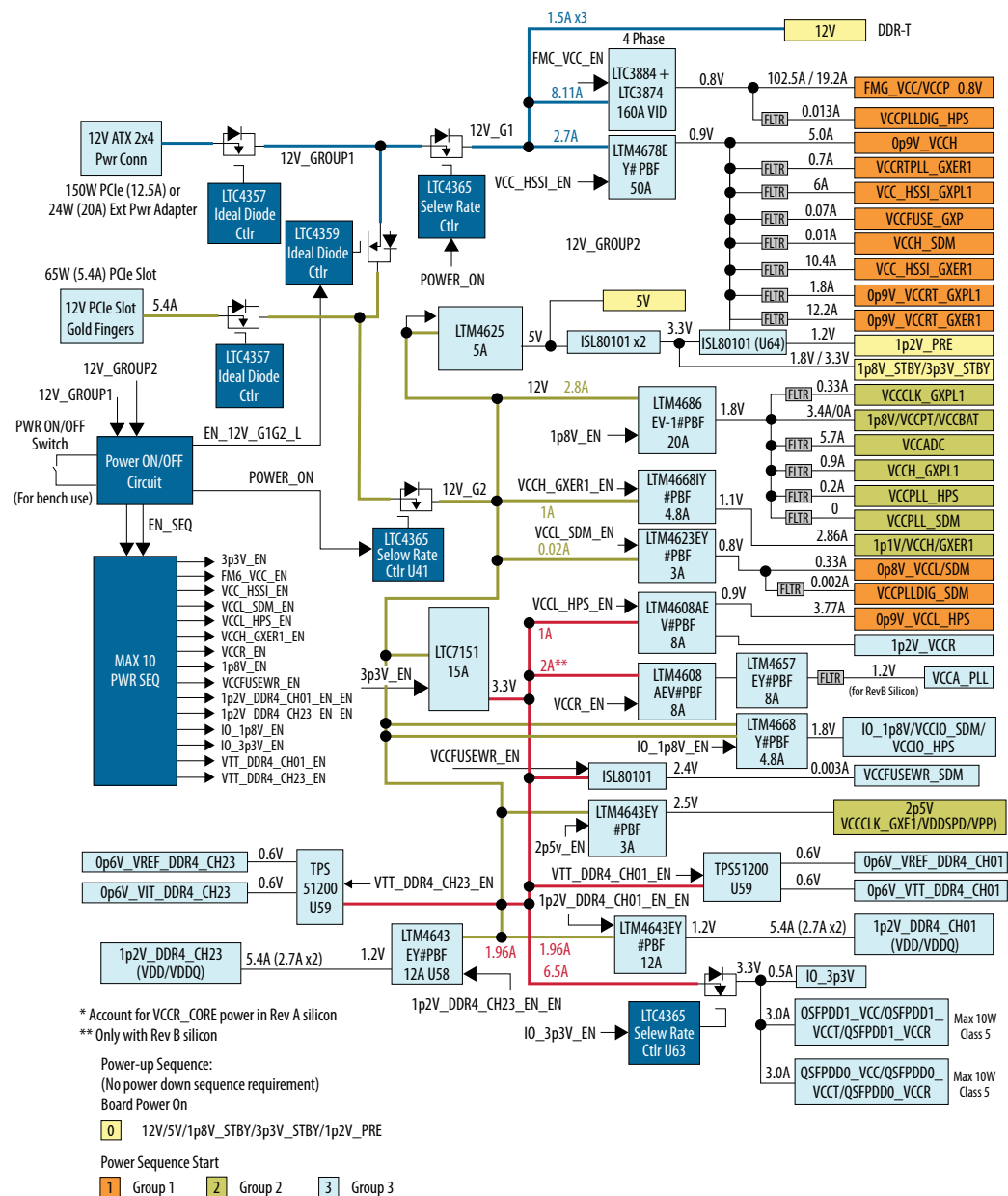
### A.8. Power

The power to the Agilex 7 FPGA F-Series Development Kit is provided from the PCIe slot (up to 75 W) and a secondary auxiliary 2x4 PCIe power connector capable of an additional 150 W. The development kit does not power up until both the +12 V rails from the PCIe slot and the secondary auxiliary PCIe power connector are detected.

The development kit can also operate as a stand-alone bench top board for laboratory evaluation when an external 12 V power supply is connected to its 2x4 PCIe power connector. In this mode, the external supply provides a total of 240 W power for both the VCC core and other power rails on the board. An on-board slide switch is used to start the power for the standalone mode.

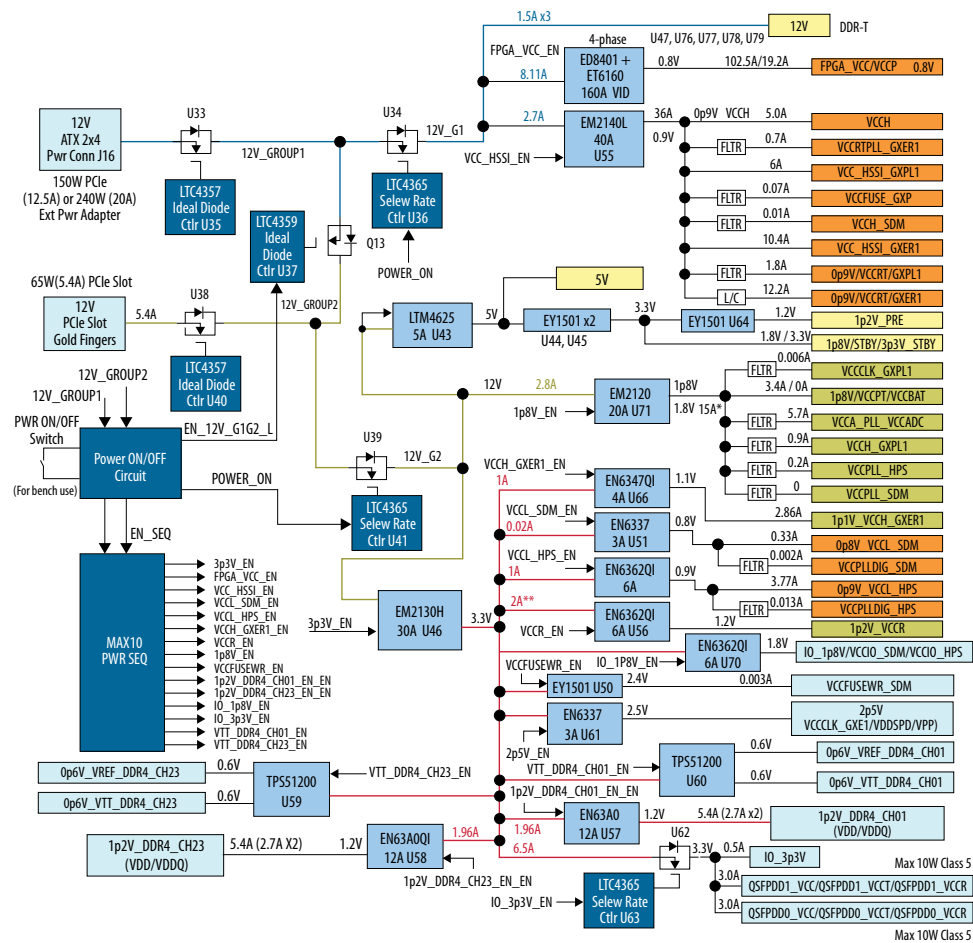
A MAX 10 power sequencer is used to manage the power-up sequencing needed to meet the Agilex 7 FPGA power sequencing requirements. No power-down sequencing is required on the Agilex 7 FPGA.

**Figure 22. Power Tree—Agilex 7 FPGA F-Series Development Kit (DK-DEV-AGF014EB)**





**Figure 24. Power Tree—Agilex 7 FPGA F-Series Development Kit (DK-DEV-AGF014E2ES)**



Power-up Sequence:

(No power down sequence requirement)

Board Power On

① 12V/5V/1p8V\_STBY/3p3V\_STBY/1p2V\_PRE

Power Sequence Start

1 Group 1

② Group 2

Group 2

1.5A x3

12V

000 I

 [Send Feedback](#)

**Table 15. Power Sequence Groups**

Group Number	Voltage Rails
Group1	VCC, VCCP, VCCL_HPS, VCCL_SDM, VCCH, VCC_HSSI_GXER, VCC_HSSI_GXPL, VCCH, VCCRT_GXER, VCCRT_GXPL
Group2	VCCPT, VCCBAT, VCCH_GXER, VCCH_GXPL, VCCA_PLL <sup>(1)</sup> , VCCPLL_SDM, VCCADC, VCCPLL_HPS, VCCCLK_GXER
Group3	VCCIO, VCCIO_SDM, VCCIO_HPS, VCCFUSEWR_SDM

### A.8.2. Power Measurement

Power measurement is provided for your evaluation to help correlate actual power versus EPE tool. Voltage measurements is provided for eight FPGA power rails by using an 8-channel ADC embedded in the power MAX 10. Current measurements used by the internal measurement on power modules are digital power module and support PMBUS access.

The current for the four groups of power rails can be read through the **Power Monitor** GUI. The power rails have the following current monitor:

- VCC and VCCP
- VCCH, VCC\_HSSI, VCCRT\_GXER, and VCCRT\_GXPL
- VCCPT, VCCH\_GXPL, and VCCA\_PLL
- 3.3V

### A.8.3. Temperature Monitor

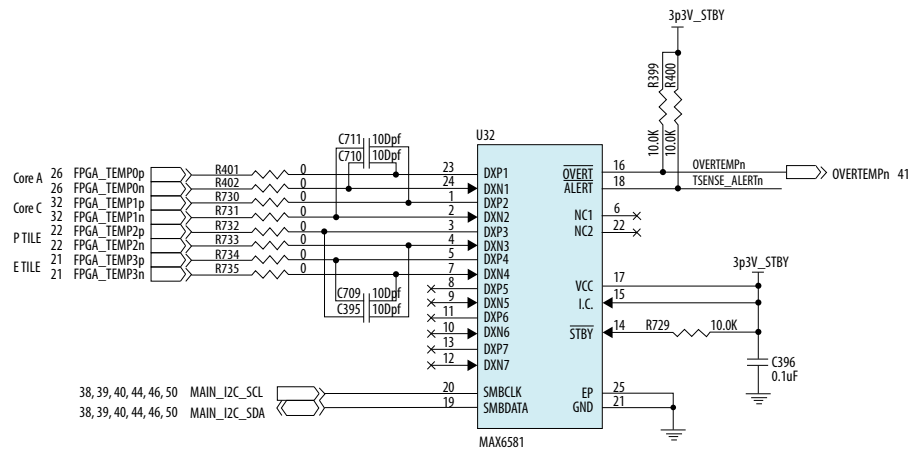
An 8-channel temperature sensor device, MAX6581, monitors the temperature of the Agilex 7 FPGA including fabric core and transceivers. Temperature monitoring of the board ambient is also done by MAX6581 with its embedded temperature sensor diode.

MAX6581 connects to the MAX 10 system controller by a 2-wire I<sup>2</sup>C interface. Additionally, the OVERTEMP<sub>n</sub> and ALERT<sub>n</sub> signals from MAX6581 are also routed to the power MAX 10 CPLD to allow it to immediately sense a temperature fault condition if the board gets too hot.

An over temperature warning LED (red-colored) is connected to the MAX 10 device so software can indicate a visual over temperature warning. This LED indicates the temperature fault condition and that the fan should be running. The fan is controlled by the OVERTEMP\_OUT signal from the MAX 10 and can be controlled by software. The temperature fault set points can be programmed into MAX6581 by the I<sup>2</sup>C bus through the system MAX 10.

<sup>(1)</sup> VCCA\_PLL is in Group 2 for ES device and Group 3 for production device.

**Figure 26. MAX6581 Temperature Sensor Circuit**





## B. Developer Resources

Use the following links to check the Intel website for other related information.

**Table 16.     Agilex 7 FPGA F-Series Development Kit References**

Reference	Description
<a href="#">Agilex 7 FPGA F-Series Development Kit page</a>	Latest board design files, reference designs, and kit installation for Windows* and Linux*.
<a href="#">Agilex 7 FPGA Board Design Guided Journey</a>	The interactive FPGA Board Guided Journey provides step-by-step guidance for developing printed circuit boards (PCBs) using Agilex 7 devices.
<a href="#">AN 958: Board Design Guidelines</a>	Board design-related resources for Altera devices. Its goal is to help you implement successful high-speed PCBs that integrate device(s) and other elements.
<a href="#">Agilex 7 Power Management User Guide</a>	Describes the Agilex 7 devices power-optimization features, power-up and power-down sequences, power distribution network, voltage and temperature monitoring systems with a design example to read the TSDs, and power optimization techniques.
<a href="#">Agilex 7 Power Distribution Network Design Guidelines</a>	Provides information for the Agilex 7 device family power distribution network (PDN) design guidelines.
<a href="#">FPGA SmartVID</a>	SmartVID is a feature on select Altera FPGAs where the device identifies the optimal voltage that it should be operated at, and provides this information to the power regulator via the PMBus. The term represents Smart Voltage Identification (SmartVID).
<a href="#">SmartVID Debug Checklist and Voltage Regulator Guidelines</a>	Provides the checklist to assist you to rule out the possible causes of configuration failure due to SmartVID.
<a href="#">Agilex 7 Configuration User Guide</a>	Provides the configuration process, the device pins required for configuration, the available configuration schemes, remote system updates, and debugging. This user guide also provides an overview of the secure device manager (SDM) which manages security for the configuration bitstream.
<a href="#">Documentation: Agilex 7</a>	Agilex 7 device documentation.
<a href="#">Cadence* Capture CIS Schematic Symbols</a>	Agilex 7 OrCAD symbols.



## C. Safety and Regulatory Compliance Information

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### C.1. Safety and Regulatory Information



#### **ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE**

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE & UKCA mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

### C.1.1. Safety Warnings



#### Power Supply Hazardous Voltage

AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

#### Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

	<b>WARNING</b>	
<b>RISK OF ELECTRIC SHOCK</b>		
Connect only to a properly earth grounded outlet. Apparaten skall anslutas till jordat uttag när den ansluts till ett nätverk.		

#### System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached to is also connected to properly wired and grounded receptacles.

	<b>WARNING</b>	
<b>RISK OF ELECTRIC SHOCK</b>		
Do not attempt to modify or use the supplied AC power cord if it is not the exact type and rating required.		

### Power Cord Requirements

The plug on the power cord must be a grounding-type male plug designed for use in your region. It must have certification marks showing certification by an agency in your region. The connector that plugs into the appliance inlet of the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord, and do not use it with adapters. Use only certified power supply cord with appropriate gauge, designed for use in your region.



### Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

### Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

## C.1.2. Safety Cautions

	<b>CAUTION</b>	
	<b>Hot Surfaces and Sharp Edges</b>	
<p><b>Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp pins and edges on some boards. Contact should be avoided.</b></p>		

### Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.



### Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

### Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, you are required to take measures to eliminate this interference.

### Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.



### Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

**Attention:** Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

### Lithium Ion Battery Warnings



**Lithium Battery:** Risk of explosion if the lithium battery is replaced by an incorrect type. Risk of fire, explosion, or chemical burn if the battery is mistreated (punctured or crushed). Do not attempt to disassemble. Do not incinerate. Observe proper polarity when replacing battery. Do not dispose—the battery is intended to be serviced and disposed by qualified Intel service personnel only.

**Perchlorate Material:** Special handling may apply. For more details, refer to [www.dtsc.ca.gov/hazardouswaste/perchlorate](http://www.dtsc.ca.gov/hazardouswaste/perchlorate). This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product includes a battery which contains perchlorate material.

### Taiwan battery recycling:



廢電池請回收

(Translation - please recycle batteries)

**Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of product in unsorted municipal waste.**

## C.2. Compliance Information

### CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

