



# **Intel® MAX® 10 FPGA (10M08S, 144-EQFP) Evaluation Kit User Guide**



**Online Version**



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**812857**

**2023.01.08**

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## 1. Overview

The Intel® MAX® 10 Evaluation Kit is an entry-level board for evaluating the Intel MAX 10 FPGA technology, MPS Power Modules, and Intel Enpirion® PowerSoC regulators. You can use this kit to do the following:

- Develop designs for the 10M08S, 144-EQFP FPGA
- Measure FPGA power (VCC\_CORE and VCC\_IO)
- Bridge between different I/O voltages
- Read and write to the FPGA's NOR flash memory
- Use the FPGA's analog-to-digital converter (ADC) embedded block to measure incoming analog signals
- Interface to external functions or devices via Arduino\* UNO R3 connectors or through-hole vias
- Reuse the kit's PCB board and schematic as a model for your design

**Table 1. Ordering Information**

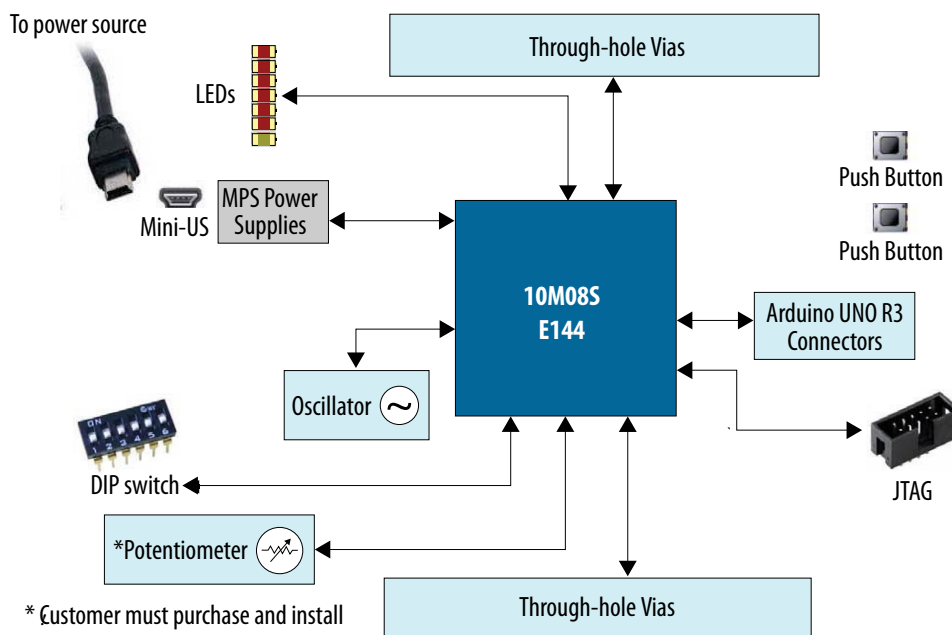
| Development Kit Version  | Ordering Code      | Device Part Number  |
|--|--------------------|---------------------|
| Intel MAX 10 10M08S Evaluation Kit Production 2 (Power Solution 2) | DK-DEV-10M08E144-B | 10M08SA2884 EQFP144 |
| Intel MAX 10 10M08S Evaluation Kit Production 1 (Power Solution 1) | EK-10M08E144       | 10M08SA2884 EQFP144 |

## 1.1. Board Component Blocks

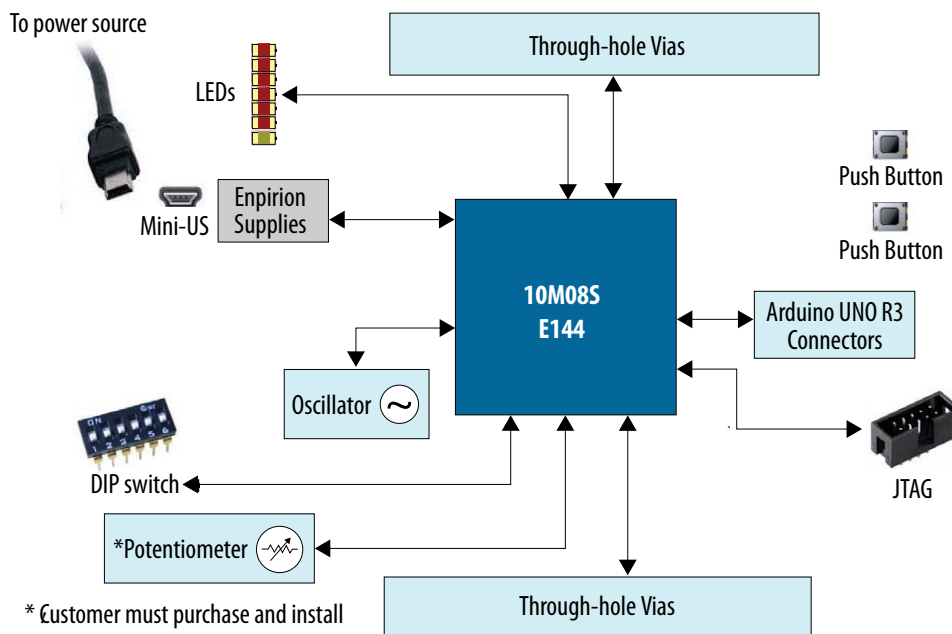
This evaluation kit features the following major component blocks. For a detailed description of the board components, see *Board Components*.

- Intel MAX 10 FPGA, 10M08SAE144C8G, (or ES variant)
  - 8,000 logic elements (LE)
  - 378 kilobits (Kb) M9K memory
  - 32–172 Kb user flash memory
  - One ADC, 1 million samples per second (MSPS), 12-bit
- FPGA configuration circuitry
  - JTAG header for external Intel FPGA Download Cable, Intel FPGA Download Cable II, or Intel FPGA Ethernet Cable
  - Flash storage for two configuration images (factory and user)
  - Dual-image self-configuration via Programmer Object File (.pof)
  - Temporary engineering debug of FPGA design via SRAM Object File (.sof)
- On-Board clocking circuitry
  - 50 MHz oscillator connected to FPGA global clock input
- General user I/O
  - 8 analog input I/O, 14 Arduino I/O, 40 general purpose I/O
  - 5 red user-defined LEDs
  - One green LED to show power from USB cable
- Push button and DIP switches
  - One reconfiguration push button (SW2)
  - One device-wide reset of all registers, push button (SW1)
  - User DIP switch (SW3)
- Power
  - The board is powered by USB cable (from PC or wall jack)
  - One green power-on LED (D6)
  - Probe points for manual, multi-meter measurement of current to calculate power consumption (TP2 - TP5) or to verify voltages on the selected internal nodes (TP1, TP6 - TP9)

**Figure 1. Example Intel MAX 10 Evaluation Kit Block Diagram - Power Solution 2 (DK-DEV-10M08E144-B)**



**Figure 2. Example Intel MAX 10 Evaluation Kit Block Diagram - Power Solution 1 (EK-10M08E144)**



### Related Information

[Board Components](#) on page 9

## 1.2. Supported Items Not Included with the Kit

The following items are not included in the kit but were designed to be used in conjunction with this kit.

**Table 2. Additional Components not Included with the Kit**

| Board Reference | Description   | Manufacturer               | Manufacturing Part Number |
|-----------------|---|----------------------------|---------------------------|
| R94             | Potentiometer   | Bourns                     | 3362P-1-103TLF            |
| J8,J9           | 2x20 0.1-inch headers                                     | Sullins Connector Solution | PPPC202LFBN-RC            |
| J2,J3, J4, J5   | Optional daughter- cards: Arduino UNO R3 revision shields | Arduino                    | —                         |
| J1              | Intel FPGA Download Cable                                 | Intel                      | PL-USB-BLASTER-RCN        |
| J1              | Intel FPGA Download Cable II                              | Intel                      | PL-USB2-BLASTER           |

### Related Information

- [Bourns webpage](#)
- [Sullins webpage](#)
- [Adafruit webpage](#)
- [SainSmart webpage](#)
- [Arduino webpage](#)
- [Intel webpage](#)



## 2. Getting Started

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### 2.1. Powering the Kit

You can apply power to the Intel MAX 10 FPGA Evaluation Kit by plugging in the USB cable (J1) to your PC or wall jack. When powered correctly, a pre-programmed design blinks LEDs D1 through D5 ON half a second then OFF half a second.

### 2.2. Installing the Intel FPGA Download Cable Driver

You can configure the evaluation kit by programming on-chip flash memory using a Intel FPGA Download Cable, Intel FPGA Download Cable II, or Intel FPGA Ethernet Cable. However, for the host computer and board to communicate, you must install the appropriate Intel FPGA Download Cable, Intel FPGA Download Cable II, or Intel FPGA Ethernet Cable driver on the host computer.

Installation instructions for the Blaster driver for your operating system are available on the Intel website. On the *Cable and Adapter Drivers Information* page of the Intel website, locate the table entry for your configuration and click the link to access the instructions.

You can download the Blaster drivers from the *Usb-blaster Driver for Windows 7 and Windows Vista* page.

#### Related Information

- [Cable and Adapter Drivers Information](#)
- [Usb-blaster Driver for Windows 7 and Windows Vista](#)

### 2.3. Handling the Kit

When handling the board, it is important to observe the following static discharge precaution:

- Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.
- The Intel MAX 10 Evaluation Kit must be stored between  $-40^{\circ}\text{C}$  and  $100^{\circ}\text{C}$ . The recommended operating temperature is between  $0^{\circ}\text{C}$  and  $85^{\circ}\text{C}$ .

## 2.4. Factory Default Switch and Jumper Settings

Figure 3. Switch Locations and Default Settings (Board Top)

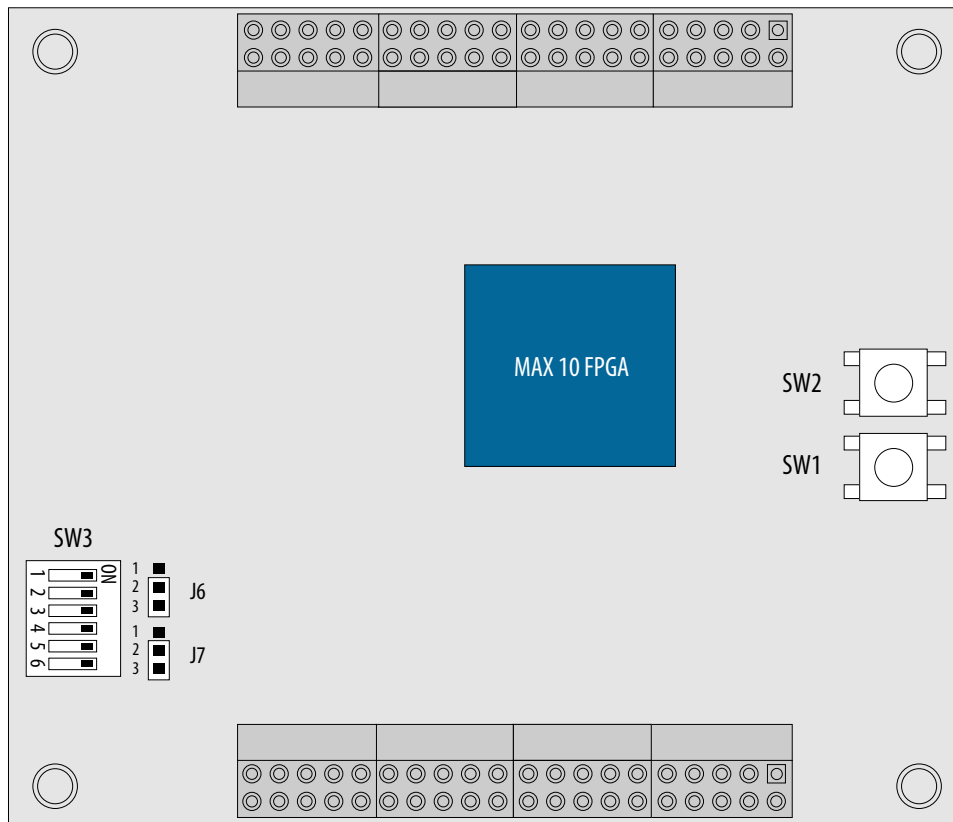


Table 3. Default SW3 DIP Switch Settings

| Switch | Function   | Default Position |
|--------|--|------------------|
| 1      | User-defined   | On               |
| 2      | User-defined   | On               |
| 3      | User-defined   | On               |
| 4      | User-defined   | On               |
| 5      | User-defined   | On               |
| 6      | BOOT_SEL: Use this switch to choose CFM0, CFM1, or CFM2 image as the first image in a dual-image configuration.<br>If BOOT_SEL is set to low, the first boot image is CFM0 image, If set to high, the first boot image is the CFM1 or CFM2 image. By default, the FPGA setting for this pin is tri-stated. | On               |

Table 4. Default Jumper Settings

| Jumper | Function  | Setting      |
|--------|---|--------------|
| J6     | Jumper for analog input channel #8. Default connection is to GND.           | Pins 2 and 3 |
| J7     | Jumper for analog input channel #7. Default connection is to potentiometer. | Pins 2 and 3 |



## 3. Board Components

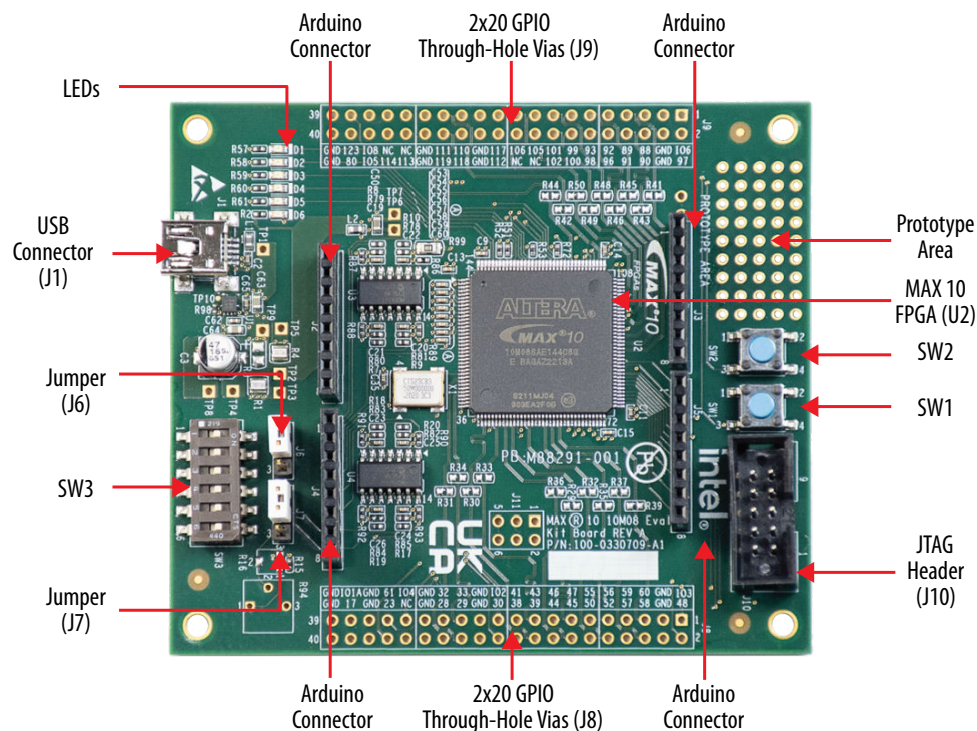
This chapter introduces all the important components on the evaluation kit.

The *Overview of the Intel MAX 10 FPGA Evaluation Kit Features* figure illustrates major component locations and the *Intel MAX 10 FPGA (10M08S, 144-EQFP) Evaluation Kit Components* table provides a brief description of all features of the board.

### 3.1. Board Overview

This section provides an overview of the evaluation kit, including an annotated board image and component descriptions.

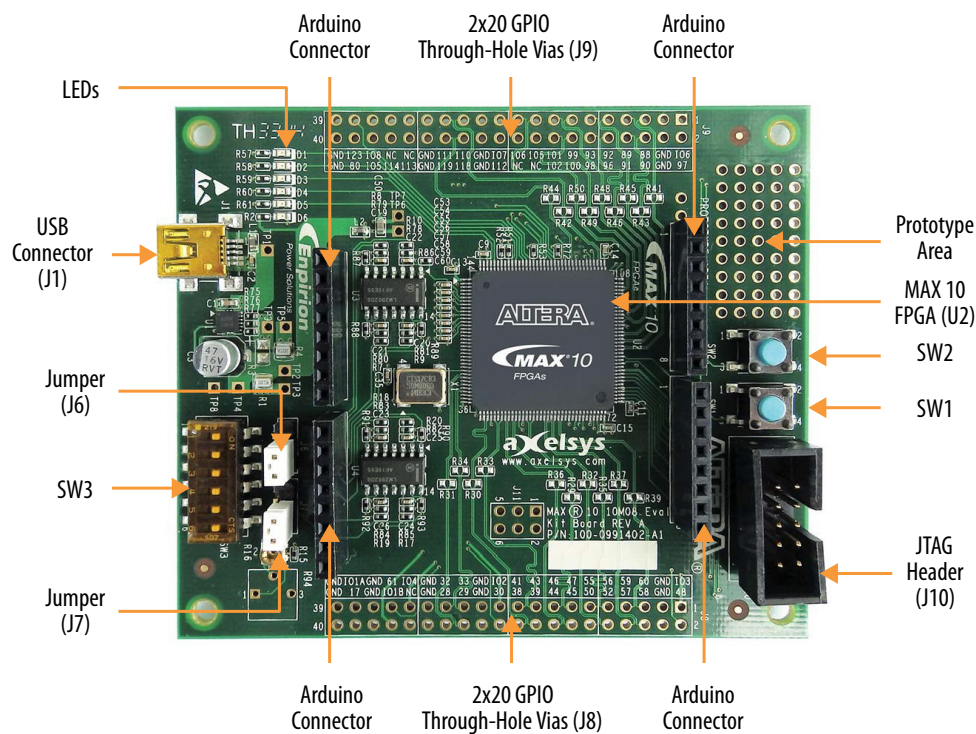
**Figure 4. Overview of the Intel MAX 10 FPGA Evaluation Kit Features - Power Solution 2 (DK-DEV-10M08E144-B)**



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\*Other names and brands may be claimed as the property of others.

**Figure 5. Overview of the Intel MAX 10 FPGA Evaluation Kit Features - Power Solution 1 (EK-10M08E144)**



**Table 5. Intel MAX 10 FPGA (10M08S, 144-EQFP) Evaluation Kit Components**

| Board Reference                                  | Type                               | Description   |
|--|------------------------------------|---|
| <b>Featured Device</b>                           |                                    |   |
| U2   | FPGA                               | 10M08SAE144C8G, (or ES variant) Plastic Enhanced Quad Flat Pack (EQFP), 144 pins, 22 mm x 22 mm.<br>For package details, refer to the <i>Packaging Device Information</i> . |
| <b>Configuration, Status, and Setup Elements</b> |                                    |   |
| J6   | Jumper for analog input channel #8 | Default connection is to GND. Change jumper to pins 1 and 2 to switch analog source to Arduino header.  |
| J7   | Jumper for analog input channel #7 | Default connection is to potentiometer (customer option to purchase and install). Change jumper to pins 1 and 2 to switch analog source to Arduino header.                  |
| SW3  | User-defined DIP switch            | 6-position switch. SW3.1 through SW3.5 are user-defined. SW3.6 is predefined for dual-image configuration.  |
| D1, D2, D3, D4, D5                               | LED, red                           | These LEDs cycle off and on when the kit is powered on.   |
| D6   | Power LED, green                   | Illuminates when USB power is present.  |
| SW2  | FPGA reconfiguration push-button   | Toggling this button causes the FPGA to reconfigure from on-die Configuration Flash Memory (CFM).   |
| <b>Clock Circuitry</b>                           |                                    |   |
| X1   | 50 MHz oscillator                  | 50 MHz crystal oscillator for general purpose logic.  |
| <i>continued...</i>                              |                                    |   |

| Board Reference                      | Type                      | Description  |
|--------------------------------------|---------------------------|--|
| <b>General User Input and Output</b> |                           |  |
| D1, D2, D3, D4, D5                   | User-defined LEDs, red    | User-defined LEDs.   |
| SW1                                  | FPGA register push-button | Toggling this button resets all registers in the FPGA.   |
| R94                                  | Potentiometer             | You must purchase and install this device to provide analog inputs signals to the Intel MAX 10 ADC IP block (analog input channel 8).      |
| <b>Connectors</b>                    |                           |  |
| J2, J3, J4, J5                       | Arduino UNO R3 connectors | You can purchase Arduino UNO R3 compatible Shields (i.e. daughter cards) to connect to the Arduino headers installed on the board.         |
| J10                                  | JTAG header               | Connects an Altera Intel FPGA Download Cable, Intel FPGA Download Cable II, or Intel FPGA Download Cable to program or configure the FPGA. |
| —                                    | Prototype Area            | This through-hole area is not connected to the FPGA. You can use this area to connect or solder additional components.                     |
| <b>Power Supply</b>                  |                           |  |
| J1                                   | USB connector             | Connects a USB cable to a power source.  |

#### Related Information

[Packaging Device Information](#)

### 3.2. Featured Device: Intel MAX 10 FPGA

The evaluation kit features the Intel MAX 10 FPGA 10M08SAE144C8G device (U2) in a 144-pin Plastic Enhanced Quad Flat Pack (EQFP) package.

For more detailed information about the Intel MAX 10 FPGA device family, refer to the *Intel MAX 10 FPGA Device Overview*.

#### Related Information

[Intel® MAX® 10 FPGA Device Overview](#)

### 3.3. Configuration

The evaluation kit supports two configuration methods:

- JTAG header (J10) for configuration by downloading a `.sof` file to the FPGA. Any power cycling of the FPGA or reconfiguration will power up the FPGA to a blank state.
- JTAG header (J10) for programming of the on-die FPGA Configuration Flash Memory (CFM) via a `.pof` file. Any power cycling of the FPGA or reconfiguration will power up the FPGA in self-configuration mode, using the files stored in the CFM.

The Intel Quartus® Prime Convert Programming File (CPF) GUI can be used to generate a `.pof` file that can use for internal configuration. You can directly program the Intel MAX 10 device's flash which included Configuration Flash Memory (CFM) and User Flash Memory (UFM) by using a download cable with the Intel Quartus Prime software programmer.

### 3.3.1. FPGA Programming over External Intel FPGA Download Cable

The JTAG header provides a method for configuring the FPGA (U2) using an external Intel FPGA Download Cable, Intel FPGA Download Cable II or Intel FPGA Ethernet Cable with the Intel Quartus Prime Programmer running on a PC. The external download cable connects to the board through the JTAG header (J10).

### 3.3.2. Configuring the FPGA Using the Intel Quartus Prime Programmer

You can use the Intel Quartus Prime Programmer to configure the FPGA with a `.sof`. Before configuring the FPGA, ensure that the Intel Quartus Prime Programmer and the Intel FPGA Download Cable driver are installed on the host computer, the USB cable is connected to the evaluation kit, power to the board is on, and no other applications that use the JTAG chain are running.

To successfully use the Intel FPGA Download Cable cable, you must disconnect it before power cycling the board. After you power cycled the board, then reconnect the Intel FPGA Download Cable cable.

To configure the Intel MAX 10 FPGA, perform the following steps:

1. Start the Intel Quartus Prime Programmer.
2. Click **Auto Detect** to display the devices in the JTAG chain.
3. Click **Add File** and select the path to the desired `.sof`.
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

### 3.3.3. Selecting Internal Configuration Scheme

For all Intel MAX 10 devices except 10M02 device, there are total of 5 different modes can be selected when using Internal Configuration. The internal configuration scheme needs to be selected before design compilation.

To select the configuration mode, follow these steps:

1. Open the Intel Quartus Prime software and load a project using Intel MAX 10 device family.
2. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
3. In the Category list, select **Device**. The **Device** page appears.
4. Click **Device and Pin Options**.
5. In the **Device and Pin Options** dialog box, click the **Configuration** tab.
6. In the **Configuration Scheme** list, select **Internal Configuration**.
7. In the **Configuration Mode** list, select 1 out of 5 configuration modes except 10M02 device, which has only 2 modes available.
8. Turn on **Generate compressed bitstreams** if needed.
9. Click **OK**.

### 3.3.4. Generating a .pof File with ICB Settings

To generate a .pof file from a .sof file for internal configuration, follow these steps:

1. On the File menu, click **Convert Programming Files**.
2. Under **Output programming file**, select Programmer Object File ( .pof ) in the Programming file type list.
3. In the **Mode** list, select **Internal Configuration**.
4. To set the ICB settings, click **Option/Boot Info** button. An ICB setting dialog box will appear.

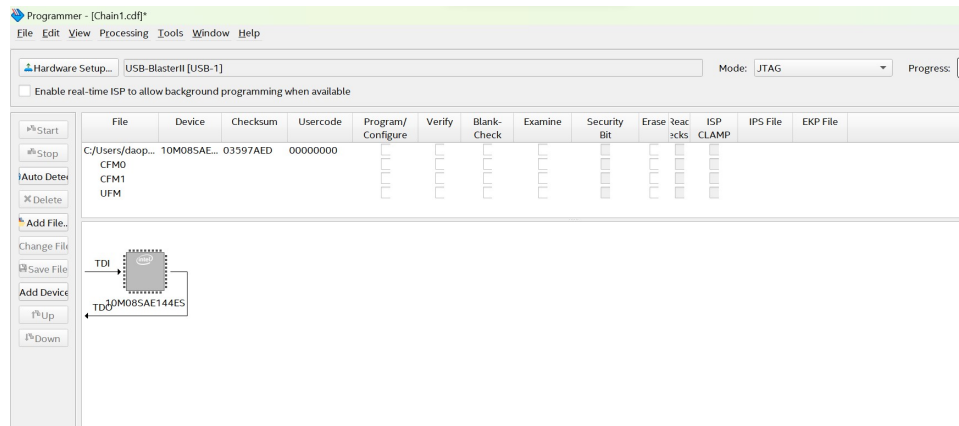
Several ICB settings can be set through the ICB setting dialog box, including:

- Power on Reset Scheme: Instant On, Fast POR Delay or Slow POR Delay.
  - Enable user I/Os weak pull up during configuration check box.
  - Enable the JTAG Security check box.
  - Verify Protect check box.
  - Enable watchdog for dual boot and watching value (initially grayed out, after adding 2 sof pages with 2 design that compiled with Dual Compressed Internal Images, the watchdog setting will then be enable).
  - User Flash Memory settings.
5. In the **Filename** box, specify the file name for the programming file you want to create.
  6. To generate a Memory Map File ( .map ), turn on **Create Memory Map File (Auto generate output\_file.map)**. In the ( .map ) file, not only will show the address of the CFM and UFM, but also will contain the information of the ICB setting that user set through the **Option/Boot Info** dialog box.
  7. You can add an SRAM Object File ( .sof ) through **Input files to convert** list. The maximum sof page is two.
  8. After set all the desirable settings, click **Generate** to generate related programming file.

### 3.3.5. Programming Internal Flash Memory

After generating the .pof file, Intel Quartus Prime Programmer can be used to program the internal flash memory through JTAG connection. The following figure shows an example of the Intel Quartus Prime Programmer.

**Figure 6. Intel Quartus Prime Programmer**



Following are the steps to program a .pof file into Intel MAX 10 devices:

1. Click **Auto Detect** to display the devices in the JTAG chain.
2. Click **Add File** and select the path to the desired .pof.
3. Turn on the **Program/Configure** option for the added file.
4. Click **Start** to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%

## 3.4. Clock Circuitry

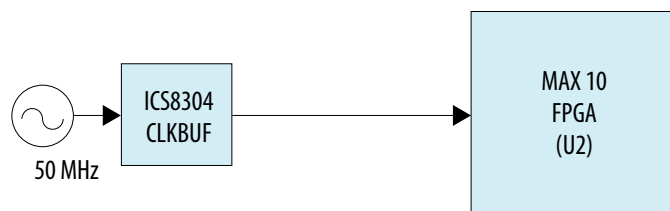
### 3.4.1. General-Purpose Clock

One general-purpose clock is provided to the FPGA global clock inputs for general FPGA design. The clock source is from the following component:

- A 50 MHz oscillator to the clock input `CLK0P` of bank 2.

The following figure shows the general purpose clock going into the evaluation kit.

**Figure 7. Intel MAX 10 FPGA (10M08S, 144-EQFP) Evaluation Kit General Purpose Clock**



## 3.5. Arduino Connectors

Arduino connectors J3, J4, and J5 connect to the Intel MAX 10 FPGA. Any analog inputs signals sourced through the Arduino header J4 are first filtered by the evaluation boards op-amp based circuit. This circuit scales the maximum allowable voltage per the Arduino specification (5.0 V) to the maximum allowable voltage per the Intel MAX 10 FPGA ADC IP block (2.5 V).



You can download an example design with pin locations and assignments completed according to the following table from the *FPGA Design Store*. In the Intel MAX 10 FPGA Evaluation Kit, under **Design Examples**, click **Intel MAX 10 Evaluation Kit Baseline Pinout**.

**Table 6. Arduino Connector Pin Assignments, Signal Names and Functions**

| Board Reference | Schematic Signal Name | Intel MAX 10 FPGA Device Pin Number | Description   |
|-----------------|-----------------------|-------------------------------------|---|
| J3.1            | ANALOG_VREF           | 5                                   | Arduino analog Vref input   |
| J3.2            | GND                   | —                                   | Arduino GND input   |
| J3.3            | ARDUINO_IO13          | 70                                  | Arduino digital I/O input to FPGA   |
| J3.4            | ARDUINO_IO12          | 69                                  | Arduino digital I/O input to FPGA   |
| J3.5            | ARDUINO_IO11          | 66                                  | Arduino digital I/O input to FPGA   |
| J3.6            | ARDUINO_IO10          | 65                                  | Arduino digital I/O input to FPGA   |
| J3.7            | ARDUINO_IO9           | 64                                  | Arduino digital I/O input to FPGA   |
| J3.8            | ARDUINO_IO8           | 62                                  | Arduino digital I/O input to FPGA   |
| J4.1            | ARDUINO_A0            | 6                                   | Arduino analog channel input through the op-amp filter circuit to the FPGA ADC IP input channel ADC1IN1 |
| J4.2            | ARDUINO_A1            | 7                                   | Arduino analog channel input through the op-amp filter circuit to the FPGA ADC IP input channel ADC1IN2 |
| J4.3            | ARDUINO_A2            | 8                                   | Arduino analog channel input through the op-amp filter circuit to the FPGA ADC IP input channel ADC1IN3 |
| J4.4            | ARDUINO_A3            | 10                                  | Arduino analog channel input through the op-amp filter circuit to the FPGA ADC IP input channel ADC1IN4 |
| J4.5            | ARDUINO_A4            | 11                                  | Arduino analog channel input through the op-amp filter circuit to the FPGA ADC IP input channel ADC1IN5 |
| J4.6            | ARDUINO_A5            | 12                                  | Arduino analog channel input through the op-amp filter circuit to the FPGA ADC IP input channel ADC1IN6 |
| J4.7            | ARDUINO_A6            | 13                                  | Arduino analog channel input through the op-amp filter circuit to the FPGA ADC IP input channel ADC1IN7 |
| J4.8            | ARDUINO_A7            | 14                                  | Arduino analog channel input through the op-amp filter circuit to the FPGA ADC IP input channel ADC1IN8 |
| J5.1            | ARDUINO_IO7           | 86                                  | Arduino digital I/O input to FPGA   |
| J5.2            | ARDUINO_IO6           | 84                                  | Arduino digital I/O input to FPGA   |
| J5.3            | ARDUINO_IO5           | 81                                  | Arduino digital I/O input to FPGA   |
| J5.4            | ARDUINO_IO4           | 79                                  | Arduino digital I/O input to FPGA   |
| J5.5            | ARDUINO_IO3           | 77                                  | Arduino digital I/O input to FPGA   |
| J5.6            | ARDUINO_IO2           | 76                                  | Arduino digital I/O input to FPGA   |
| J5.7            | ARDUINO_IO1           | 75                                  | Arduino digital I/O input to FPGA   |
| J5.8            | ARDUINO_IO0           | 74                                  | Arduino digital I/O input to FPGA   |

### Related Information

[FPGA Design Store](#)

## 3.6. General User Input/Output

This section describes the user I/O interface to the FPGA:

- User-defined DIP switch
- User-defined LEDs

### 3.6.1. User-Defined DIP Switch

Board reference SW3 is a 6-pin DIP switch. Switches 1 through 5 are user-defined, and provide additional FPGA input control. When the switch is in the OPEN or OFF position, a logic 1 is selected. When the switch is in the CLOSED or ON position, a logic 0 is selected. There is no board-specific function for these switches.

The following table lists the user-defined DIP switch schematic signal names and their corresponding Intel MAX 10 FPGA pin numbers.

**Table 7. User-Defined DIP Switch Schematic Signal Names and Functions**

| Board Reference SW3 | Schematic Signal Name | I/O Standard (V) | Intel MAX 10 FPGA Device Pin Number |
|---------------------|-----------------------|------------------|-------------------------------------|
| 1                   | Switch1               | 3.3              | 120                                 |
| 2                   | Switch2               | 3.3              | 124                                 |
| 3                   | Switch3               | 3.3              | 127                                 |
| 4                   | Switch4               | 3.3              | 130                                 |
| 5                   | Switch5               | 3.3              | 131                                 |

### 3.6.2. User-Defined LEDs

The development board includes five user-defined LEDs. Board references D1 through D5 are user LEDs that allow status and debugging signals to be driven to the LEDs from the designs loaded into the Intel MAX 10 FPGA device. The LEDs illuminate when a logic 0 is driven, and turn off when a logic 1 is driven. There is no board-specific function for these LEDs.

The following table lists the user-defined LED schematic signal names and their corresponding Intel MAX 10 FPGA pin numbers.

**Table 8. User-Defined LED Schematic Signal Names and Functions**

| Board Reference | Schematic Signal Name | I/O Standard (V) | Intel MAX 10 FPGA Device Pin Number |
|-----------------|-----------------------|------------------|-------------------------------------|
| D1              | LED1                  | 2.0              | 132                                 |
| D2              | LED2                  | 2.0              | 134                                 |
| D3              | LED3                  | 2.0              | 135                                 |
| D4              | LED4                  | 2.0              | 140                                 |
| D5              | LED5                  | 2.0              | 141                                 |

## 3.7. Power Supply

The USB cable powers up the development board. The green LED illuminates when the board is powered up.



### 3.7.1. Power Measurement

To measure the actual power of the FPGA, there are test pads on the board to be used as probe points for multi-meter probes. You can measure the current and using the equation  $P = R \times I^2$ . (Power = Resistance x Current Squared), calculate the power dissipation.

Test pads TP2 and TP3 measure the current consumed by the FPGA core. Test pads TP4 and TP5 measure the current consumed by all of the FPGA's I/O banks. All the other test pads are used to verify the voltage levels of various nodes on the board.

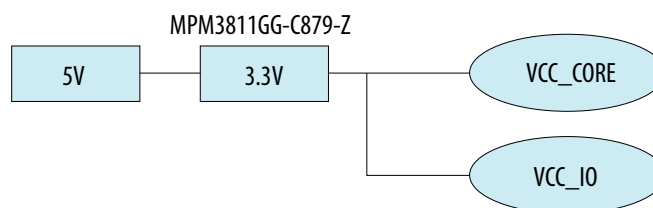
**Table 9. Power Measurement Details**

| Test Pad #'s | Measuring           | Description  | Expected Value |
|--------------|---------------------|--|----------------|
| TP1          | Board input voltage | Verify the USB input voltage   | 5.0 V          |
| TP2 - TP3    | FPGA core current   | Power calculation for FPGA $V_{CC-CORE}$ power consumption. Resistor $R1 = 0.1 \Omega$ . Current measured by user's multi-meter. | -mW            |
| TP4 - TP5    | FPGA I/O current    | Power calculation for FPGA $V_{CC-I/O}$ power consumption. Resistor $R4 = 0.1 \Omega$ . Current measured by user's multi-meter.  | -mW            |
| TP6          | Analog voltage      | Verify the proper voltage required by the FPGA $V_{CCA}$ inputs  | 3.3 V          |
| TP7          | Analog GND          | Verify the proper voltage required by the FPGA ADC IP block GND inputs   | 0 V            |
| TP8          | Digital GND         | Verify the proper voltage required by the FPGA digital GND inputs  | 0 V            |
| TP9          | Digital GND         | Verify the proper voltage required by the FPGA digital GND inputs  | 0 V            |

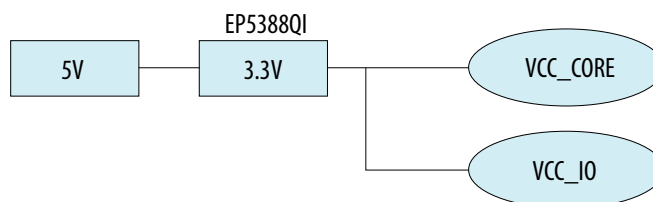
### 3.7.2. Power Distribution System

The following figure shows the power distribution system on the development board.

**Figure 8. Power Distribution System - Power Solution 2 (DK-DEV-10M08E144-B)**



**Figure 9. Power Distribution System - Power Solution 1 (EK-10M08E144)**



### 3.7.3. Temperature Sense

The ADCs provide the devices with built-in capability for on-die temperature monitoring and external analog signal conversion.

Temperature sensing mode—monitors external temperature data input with a sampling rate of up to 50 kilosamples per second. In dual ADC devices, only the first ADC block contains the temperature sensing diode.

For more information on the ADC, refer to the *Intel MAX 10 FPGA Device Overview*.

#### Related Information

[Intel® MAX® 10 FPGA Device Overview](#)

## 4. Document Revision History for Intel MAX 10 FPGA (10M08S, 144-EQFP) Evaluation Kit User Guide

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| Document Version | Changes   |
|------------------|---|
| 2024.01.08       | <ul style="list-style-type: none"> <li>Updated all references of <i>Altera</i> to Intel.</li> <li>Added <i>Ordering Information</i> table in <i>Overview</i> section.</li> <li>Added additional information in <i>Programming Internal Flash Memory</i> section.</li> <li>Added additional figures for <i>Power Solution 2 (DKDEV-10M08E144-B)</i> and <i>Power Solution 1 (EK-10M08E144)</i> in the following sections: <ul style="list-style-type: none"> <li>— <i>Board Component Blocks</i></li> <li>— <i>Board Overview</i></li> <li>— <i>Power Distribution System</i></li> </ul> </li> </ul> |
| 2015.09.30       | <ul style="list-style-type: none"> <li>Corrected sense of switches in <i>User-Defined DIP Switch</i> section.</li> <li>Added link to <i>Altera Design Store</i> in <i>Arduino Connectors</i>.</li> </ul>  |
| 2014.10.30       | Corrected FPGA pin number for SW3.2 from 121 to 124.  |
| 2014.09.30       | Initial release.  |



## A. Additional Information

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This chapter provides additional information about the document and Intel.

### A.1. Safety and Regulatory Information



#### **ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE**

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE & UKCA mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

### A.1.1. Safety Warnings





#### Power Supply Hazardous Voltage

AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.


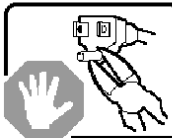
#### Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

|   |                |  |
|---|----------------|--|
|   | <b>WARNING</b> |  |
| <b>RISK OF ELECTRIC SHOCK</b>   |                |  |
| Connect only to a properly earth grounded outlet.<br>Apparaten skall anslutas till jordat uttag när den ansluts till ett nätverk. |                |  |

#### System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached to is also connected to properly wired and grounded receptacles.

|   |                |   |
|---|----------------|---|
|                          | <b>WARNING</b> |  |
| <b>RISK OF ELECTRIC SHOCK</b>   |                |   |
| Do not attempt to modify or use the supplied AC power cord if it is not the exact type and rating required. |                |   |

### Power Cord Requirements

The plug on the power cord must be a grounding-type male plug designed for use in your region. It must have certification marks showing certification by an agency in your region. The connector that plugs into the appliance inlet of the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord, and do not use it with adapters. Use only certified power supply cord with appropriate gauge, designed for use in your region.




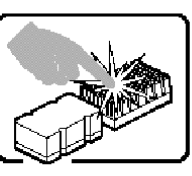
### Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

### Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

## A.1.2. Safety Cautions

|  |  |   |
|--|--|---|
|   | <p><b>CAUTION</b></p>                      |  |
|  | <p><b>Hot Surfaces and Sharp Edges</b></p> |   |
| <p><b>Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp pins and edges on some boards. Contact should be avoided.</b></p> |  |   |

### Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.



### Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

### Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, you are required to take measures to eliminate this interference.

### Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.



### Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

**Attention:** Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

### Lithium Ion Battery Warnings



**Lithium Battery:** Risk of explosion if the lithium battery is replaced by an incorrect type. Risk of fire, explosion, or chemical burn if the battery is mistreated (punctured or crushed). Do not attempt to disassemble. Do not incinerate. Observe proper polarity when replacing battery. Do not dispose—the battery is intended to be serviced and disposed by qualified Intel service personnel only.

**Perchlorate Material:** Special handling may apply. For more details, refer to [www.dtsc.ca.gov/hazardouswaste/perchlorate](http://www.dtsc.ca.gov/hazardouswaste/perchlorate). This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product includes a battery which contains perchlorate material.

### Taiwan battery recycling:



廢電池請回收

(Translation - please recycle batteries)



**Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of product in unsorted municipal waste.**

## A.2. Compliance Information

### CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

