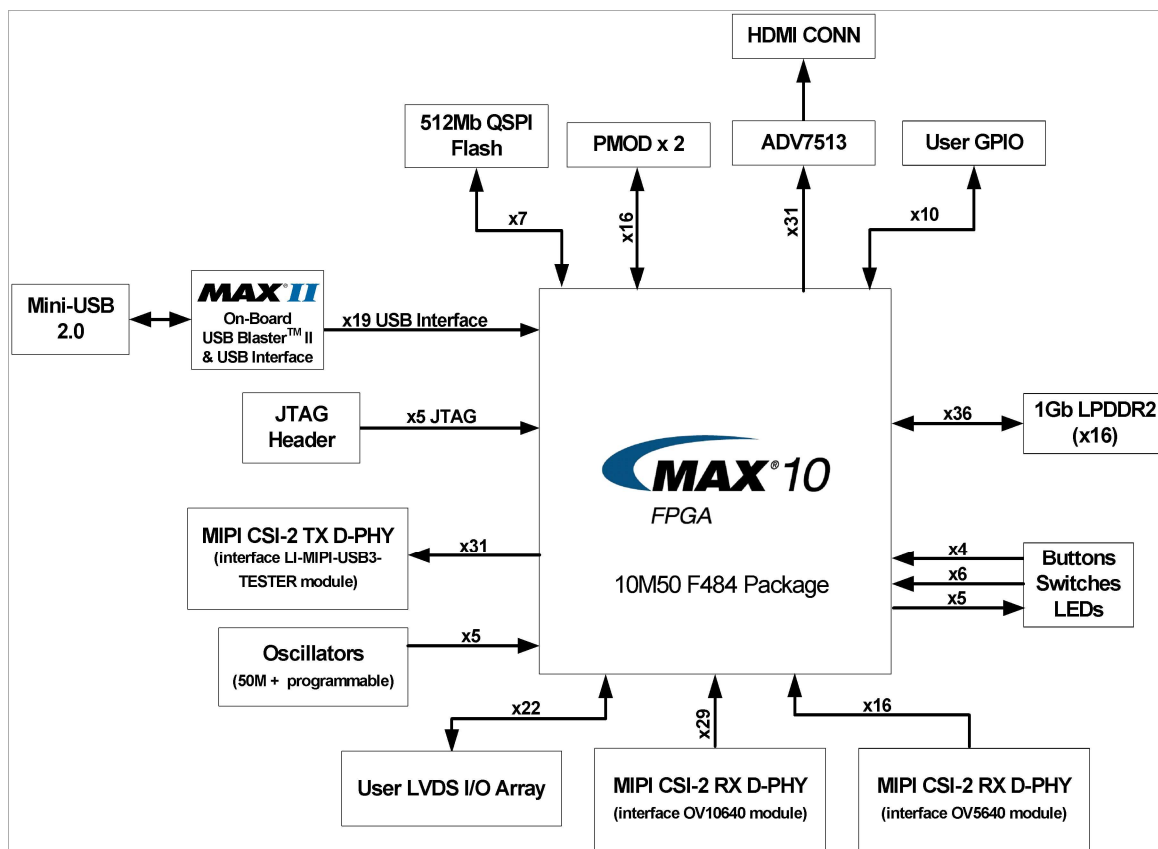


1. Project Drawing Numbers:

PB	M90021-001
PBA	M88454-001
MPN	100-0330711-A1
TA	M88455-001
MMID	99C5LA

# MAX 10 FPGA 10M50 Evaluation Kit Board



NOTE: THIS DESIGN LEVERAGED FROM OLD MMID 980014

[illegible]

PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Rev. History
2	Power Tree
3	Clock Tree
4	MAX10 Banks 1 & 2
5	MAX10 Banks 3 & 4
6	MAX10 Banks 5 & 6
7	MAX10 Banks 7 & 8
8	MAX10 Clocks
9	MAX10 Configuration
10	LPDDR2 SDRAM
11	MIPI CSI-2 Tx D-PHY LI-USB3
12	MIPI CSI-2 Rx D-PHY OV10640
13	MIPI CSI-2 Rx D-PHY OV5640
14	HDMI (VIDEO ONLY)
15	On-Board USB Blaster II -1
16	On-Board USB Blaster II -2
17	PMOD, GPIO, LVDS UserIO
18	Pushbutton, Switch, LED
19	Clocking
20	QSPI Flash
21	Hot Swap and Power 3.3 V
22	Power 2.5 V & 1.8V
23	Power 1.2V
24	MAX 10 Power & Ground
25	Decoupling



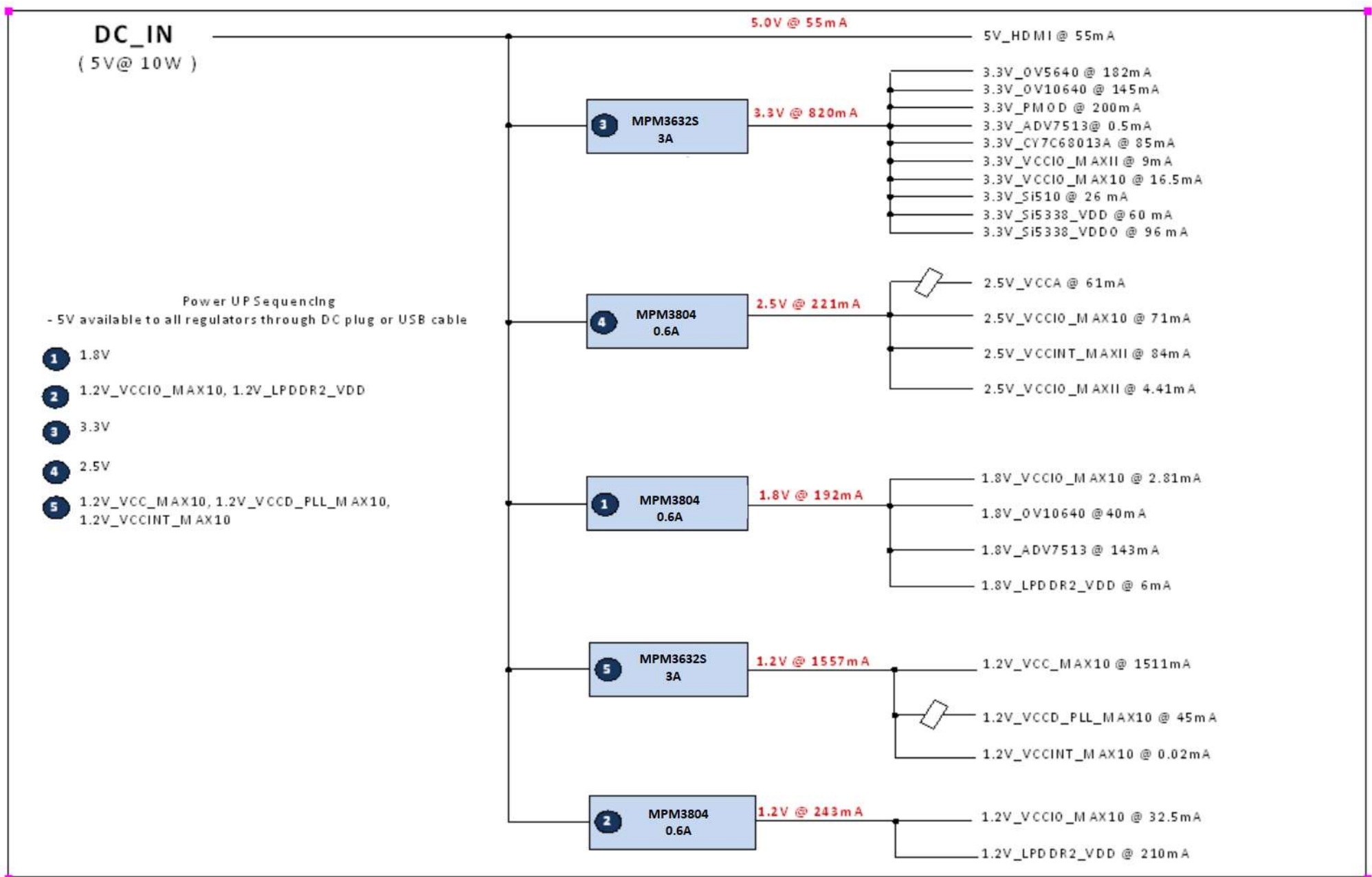
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Title  
**MAX 10 FPGA 10M50 EVAL KIT (NON-ENP)**

Size B	Document Number M88454-001 (100-0330711-A1)
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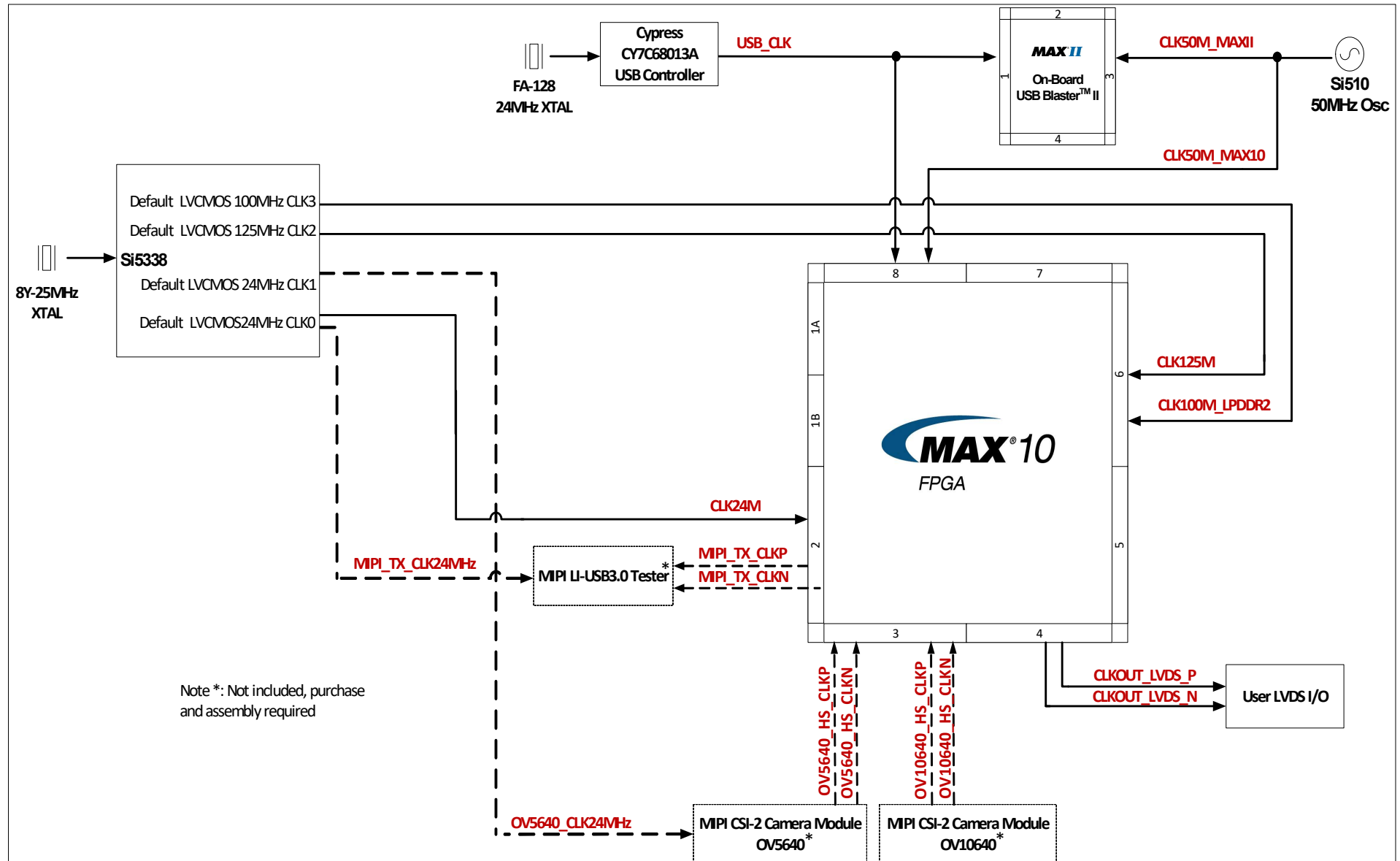
Date: Wednesday, September 28, 2022 Sheet 1 of 25

POWER TREE



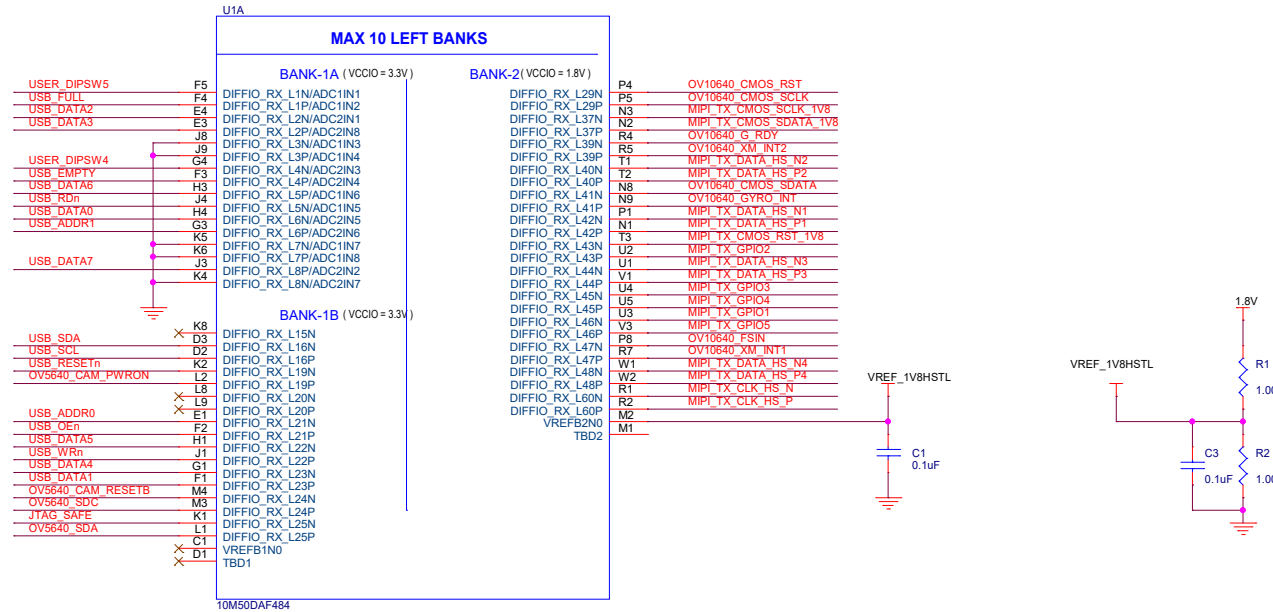
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Title <b>MAX 10 FPGA 10M50 EVAL KIT (NON-ENP)</b>		
Size A3	Document Number M88454-001 (100-0330711-A1)	Rev A
Date: Wednesday, September 28, 2022 Sheet 2 of 25		

# CLOCK TREE

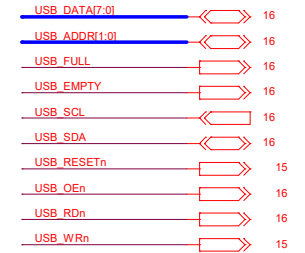


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Title <b>MAX 10 FPGA 10M50 EVAL KIT (NON-ENP)</b>			
Size A3	Document Number <b>M88454-001 (100-0330711-A1)</b>	Rev A	
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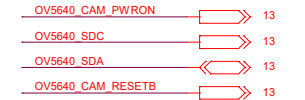
# MAX10 BANKS 1 & 2



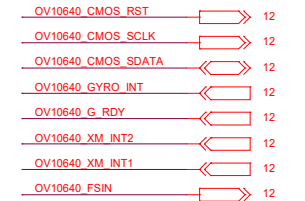
## MAX10 USB Interface



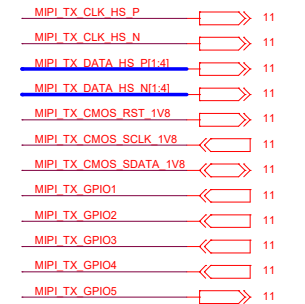
## OV5640 CSI-2 RX Interface



## OV10640 CSI-2 RX Interface



## LI-USB3 CSI-2 TX Interface



## Misc

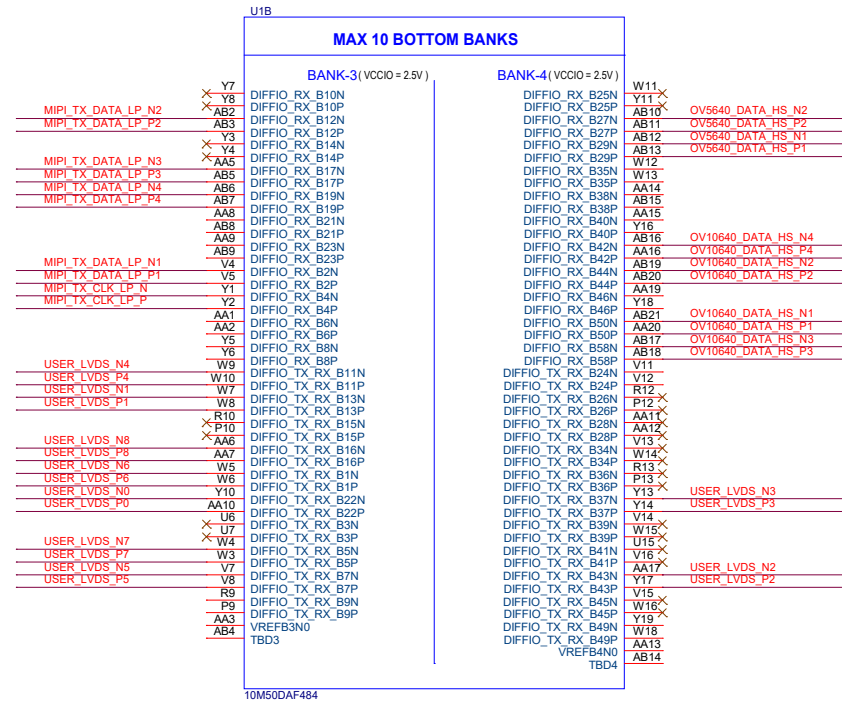


## User DIP Switch

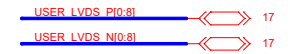


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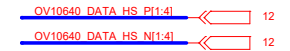
# MAX10 BANKS 3 & 4



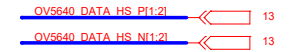
## User LVDS IO



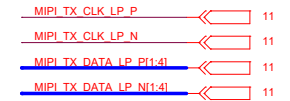
## OV10640 Interface



## OV5640 Interface

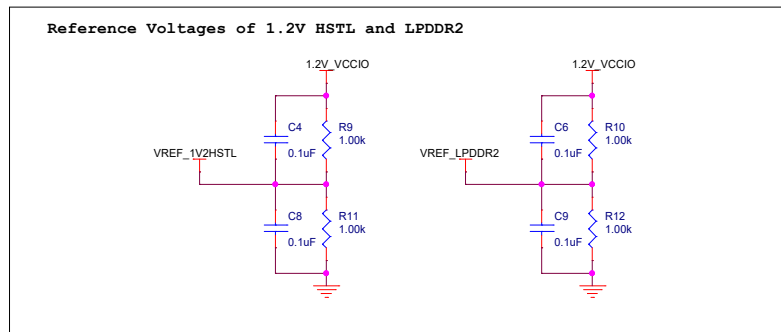
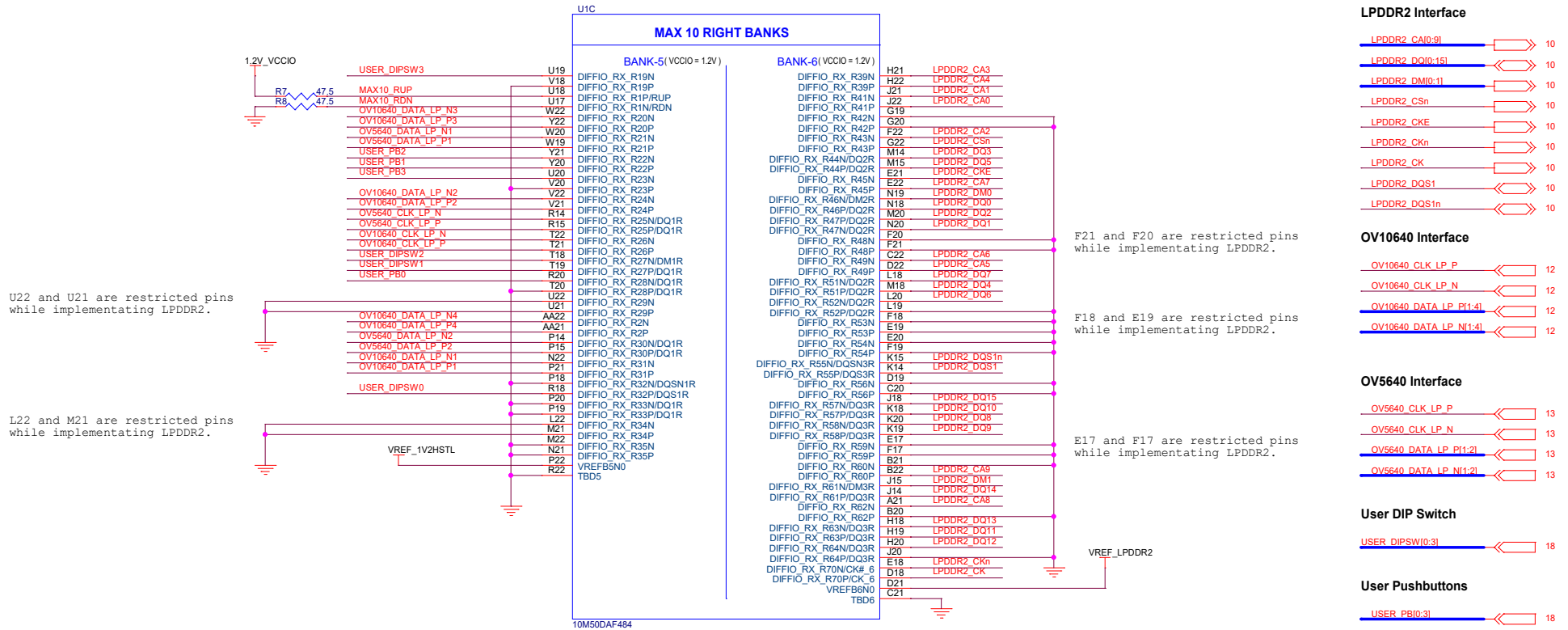


## LI-USB3 CSI-2 TX Interface

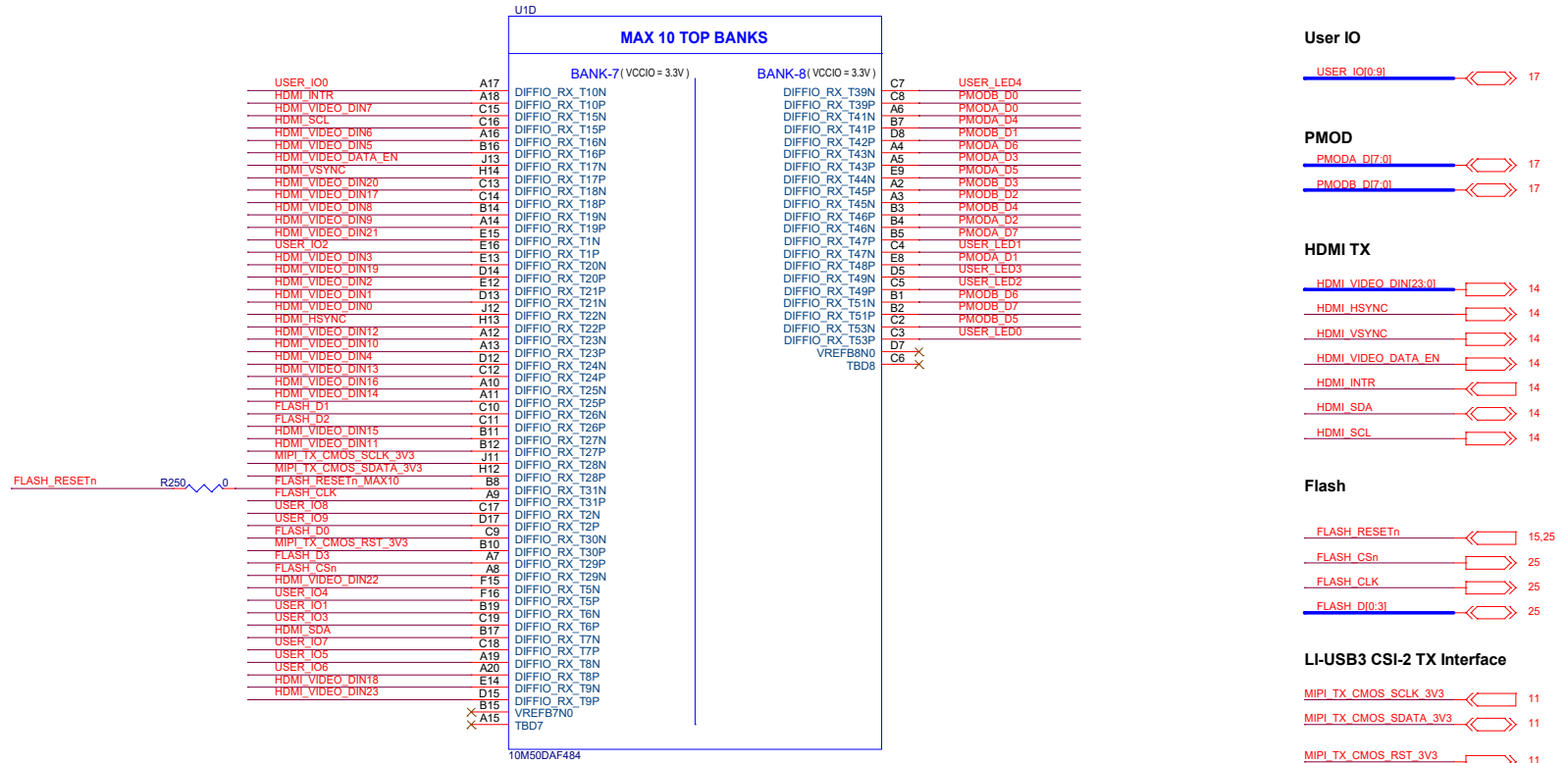


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## MAX10 BANKS 5 & 6

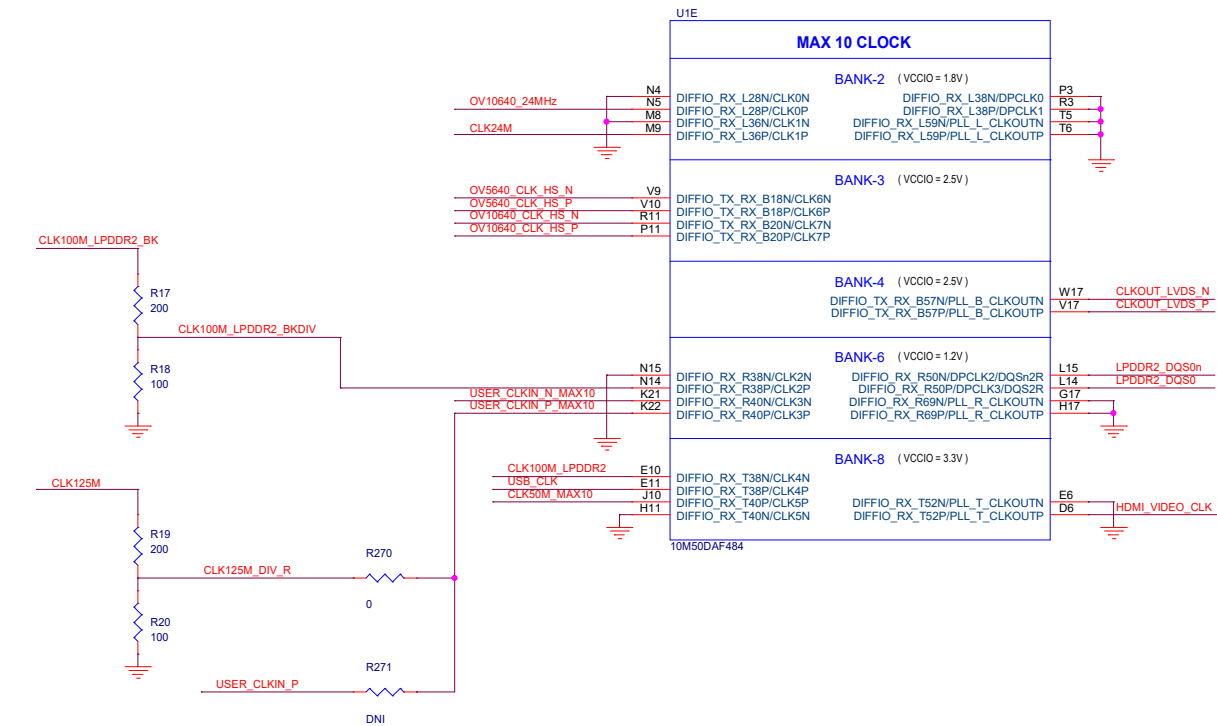


# MAX10 BANKS 7 & 8



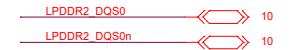
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# MAX10 CLOCKS

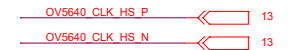


Note: CLK125M\_LVDS is the clock source provided to external LVDS user interface. USER\_CLKIN\_P is used for external single-ended clock input. USER\_CLKIN\_P/N is used for external differential clock input.

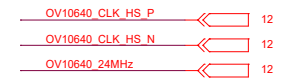
## LPDDR2 Interface



## OV5640 Interface



## OV10640 Interface



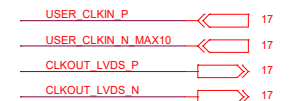
## Si5338



## USB Blaster II



## User LVDS



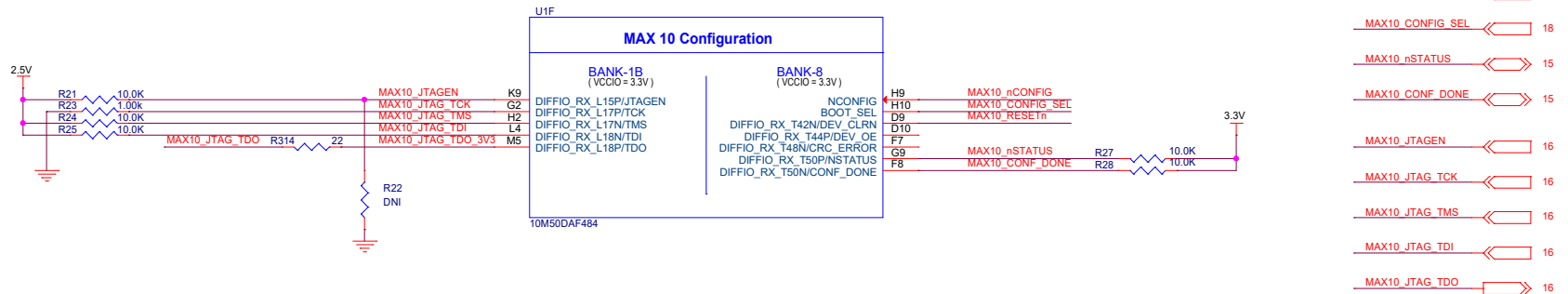
## HDMI



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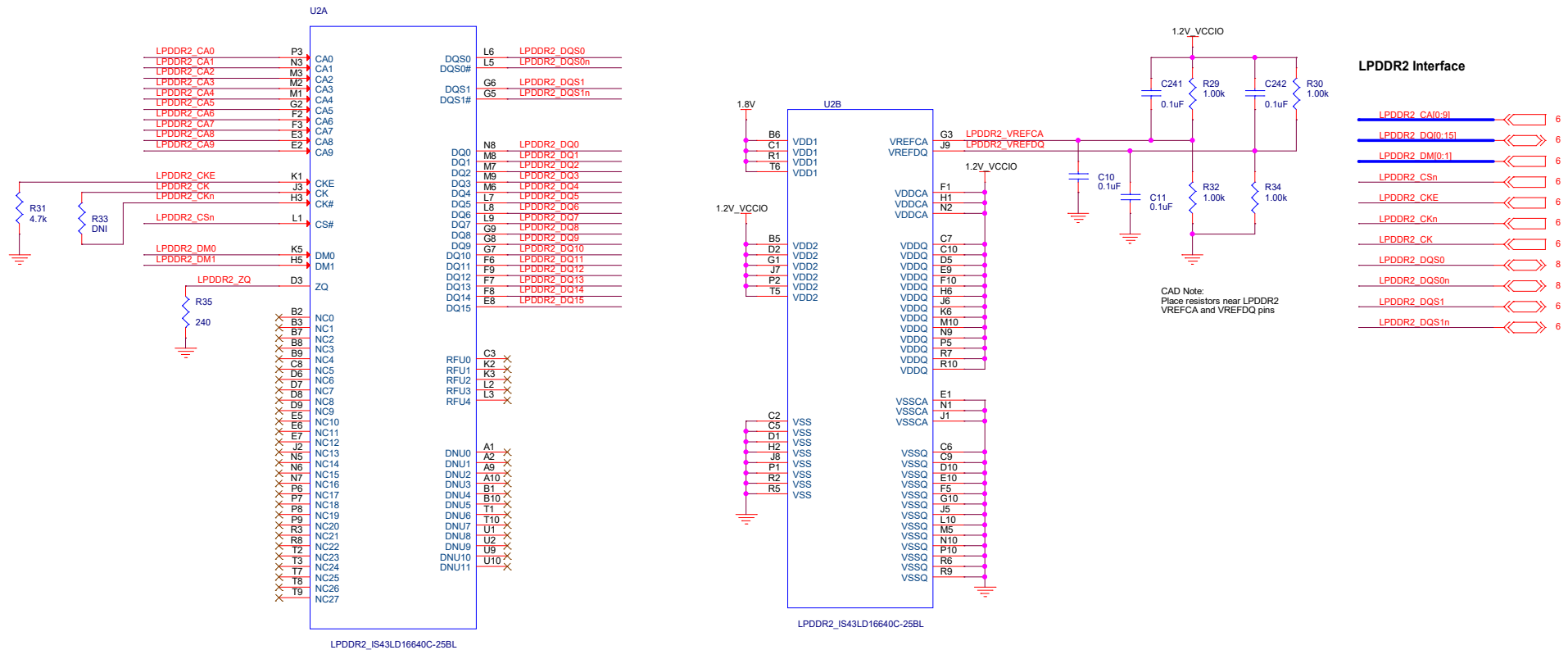


# MAX10 CONFIGURATION

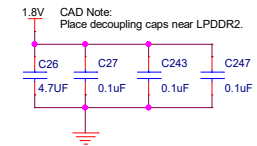
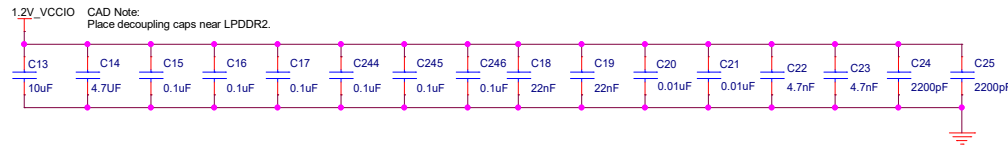


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# LPDDR2 SDRAM x 16

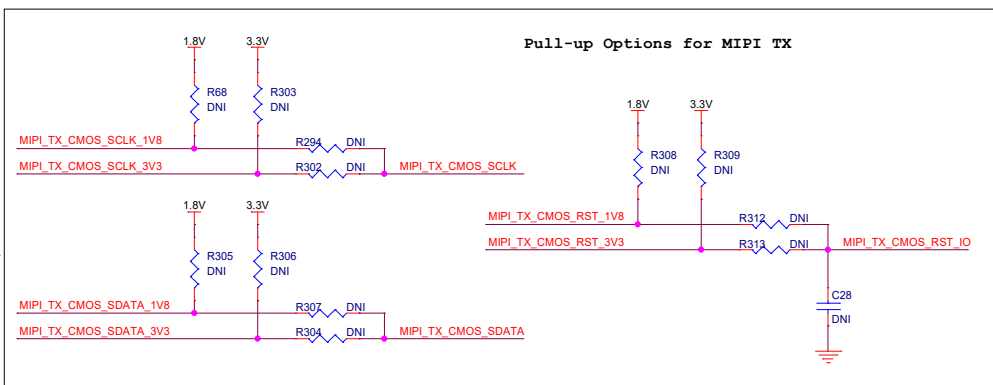
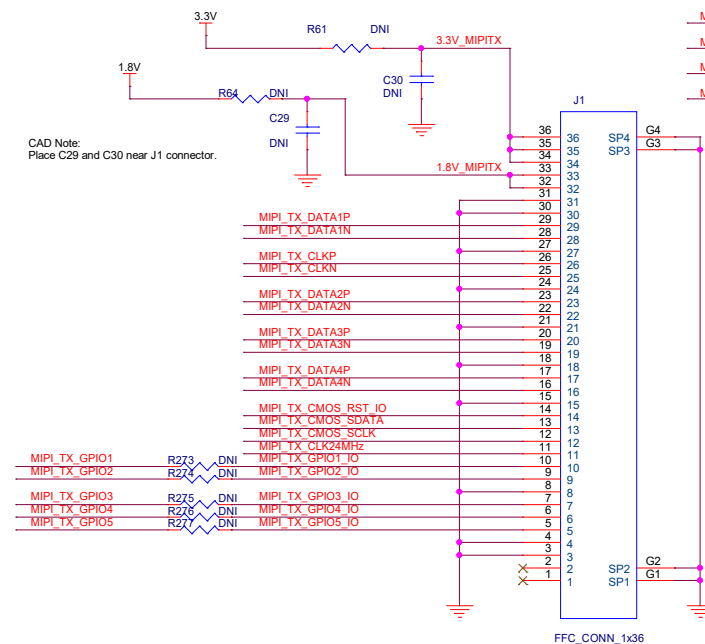
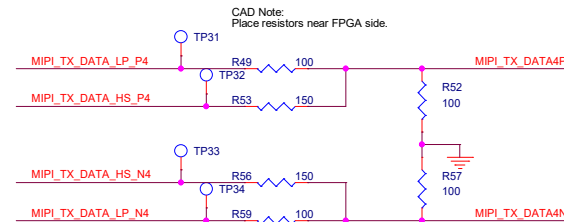
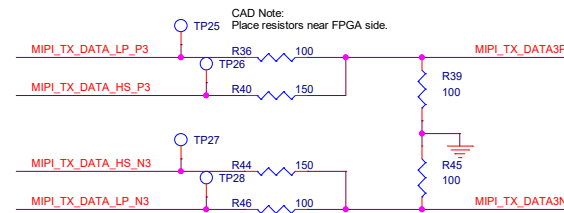
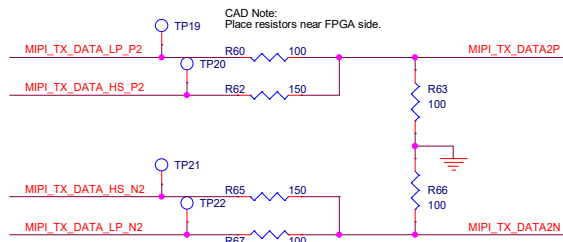
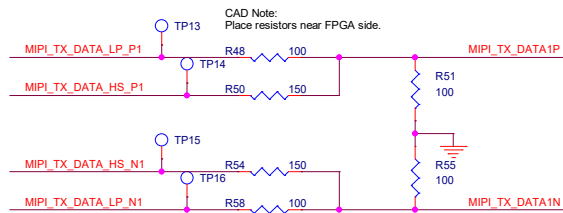
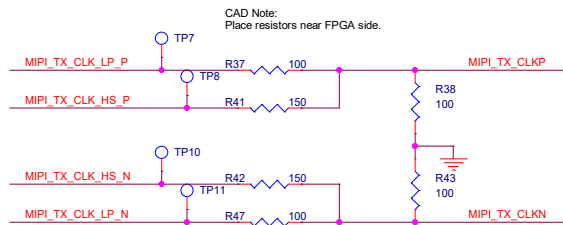


## LPDDR2 Power Decoupling



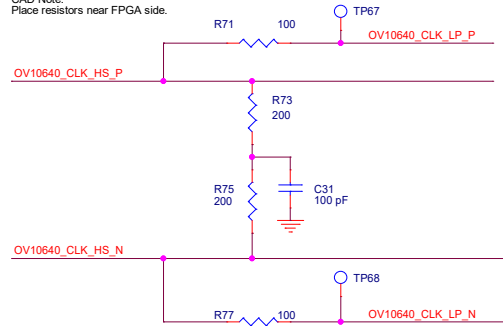
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## MIPI CSI-2 TX D-PHY

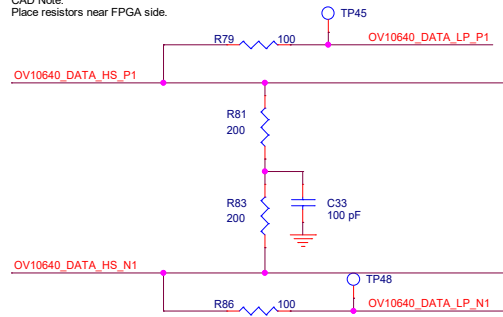


# MIPI CSI-2 RX D-PHY OV10640

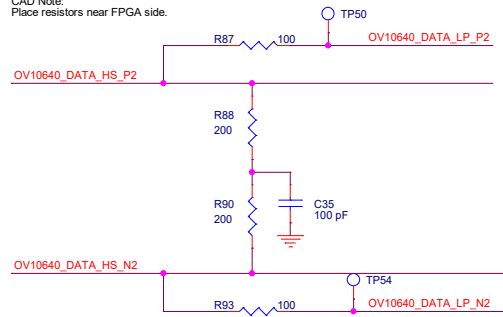
CAD Note:  
Place resistors near FPGA side.



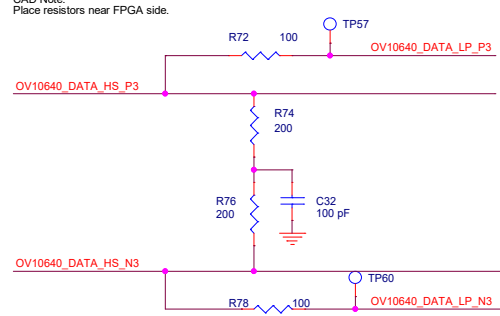
CAD Note:  
Place resistors near FPGA side.



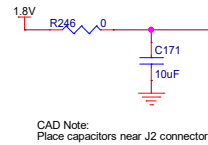
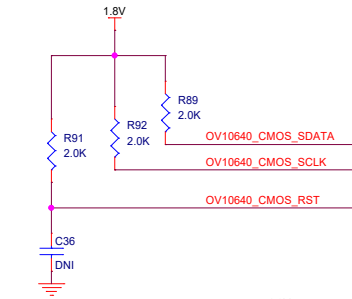
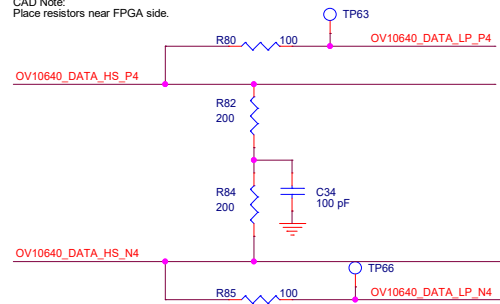
CAD Note:  
Place resistors near FPGA side.



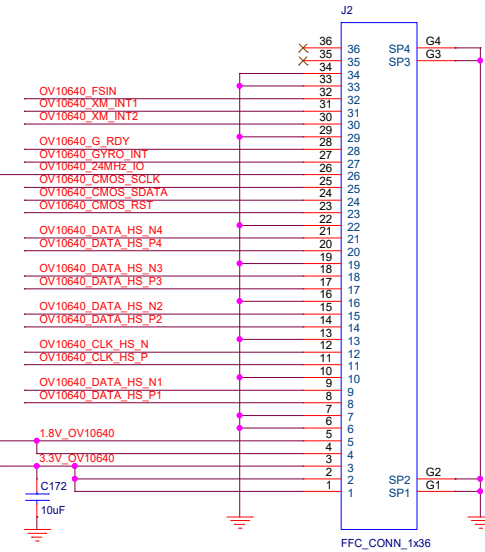
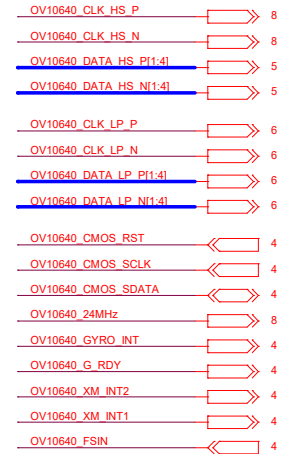
CAD Note:  
Place resistors near FPGA side.



CAD Note:  
Place resistors near FPGA side.



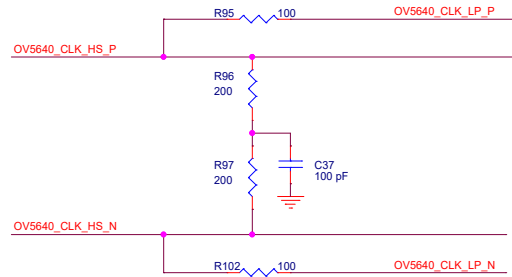
## OV10640 CSI-2 RX Interface



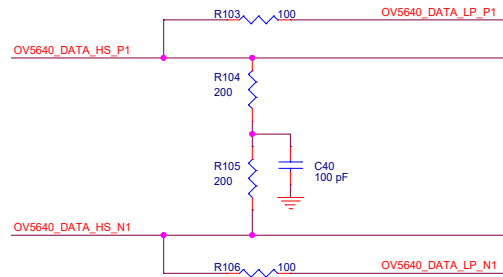
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# MIPI CSI-2 RX D-PHY OV5640

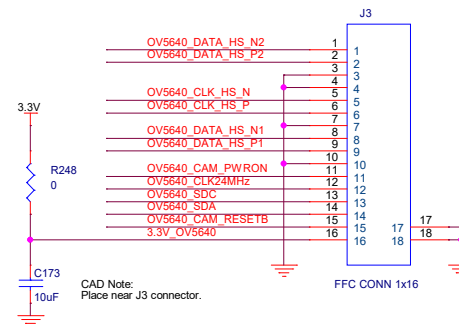
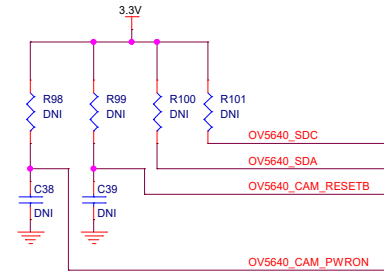
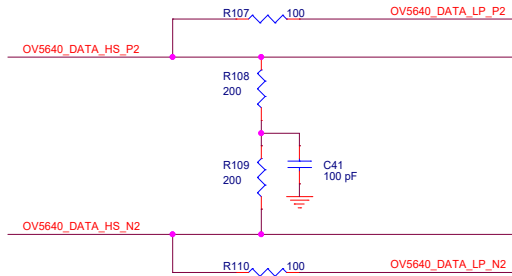
CAD Note:  
Place resistors near FPGA side.



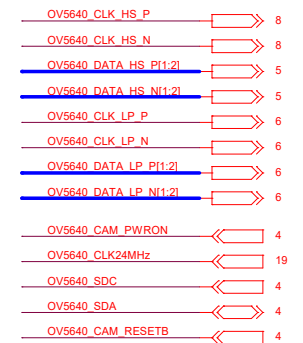
CAD Note:  
Place resistors near FPGA side.



CAD Note:  
Place resistors near FPGA side.

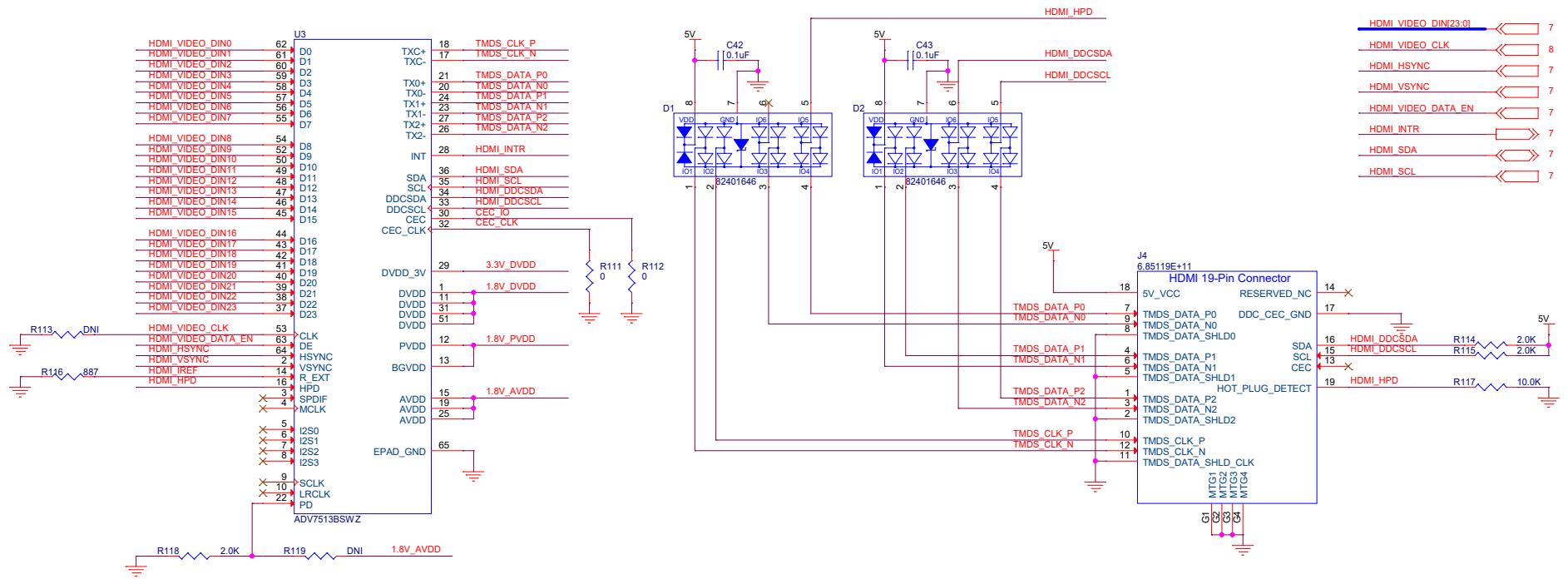


## OV5640 CSI-2 RX Interface

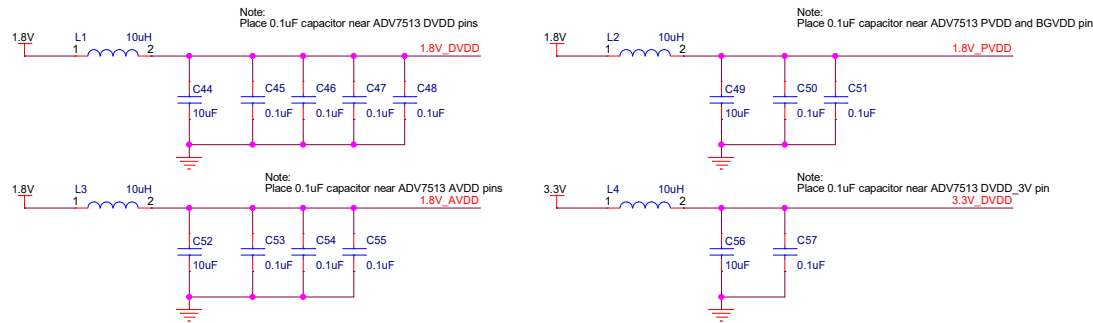


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# HDMI (VIDEO ONLY)



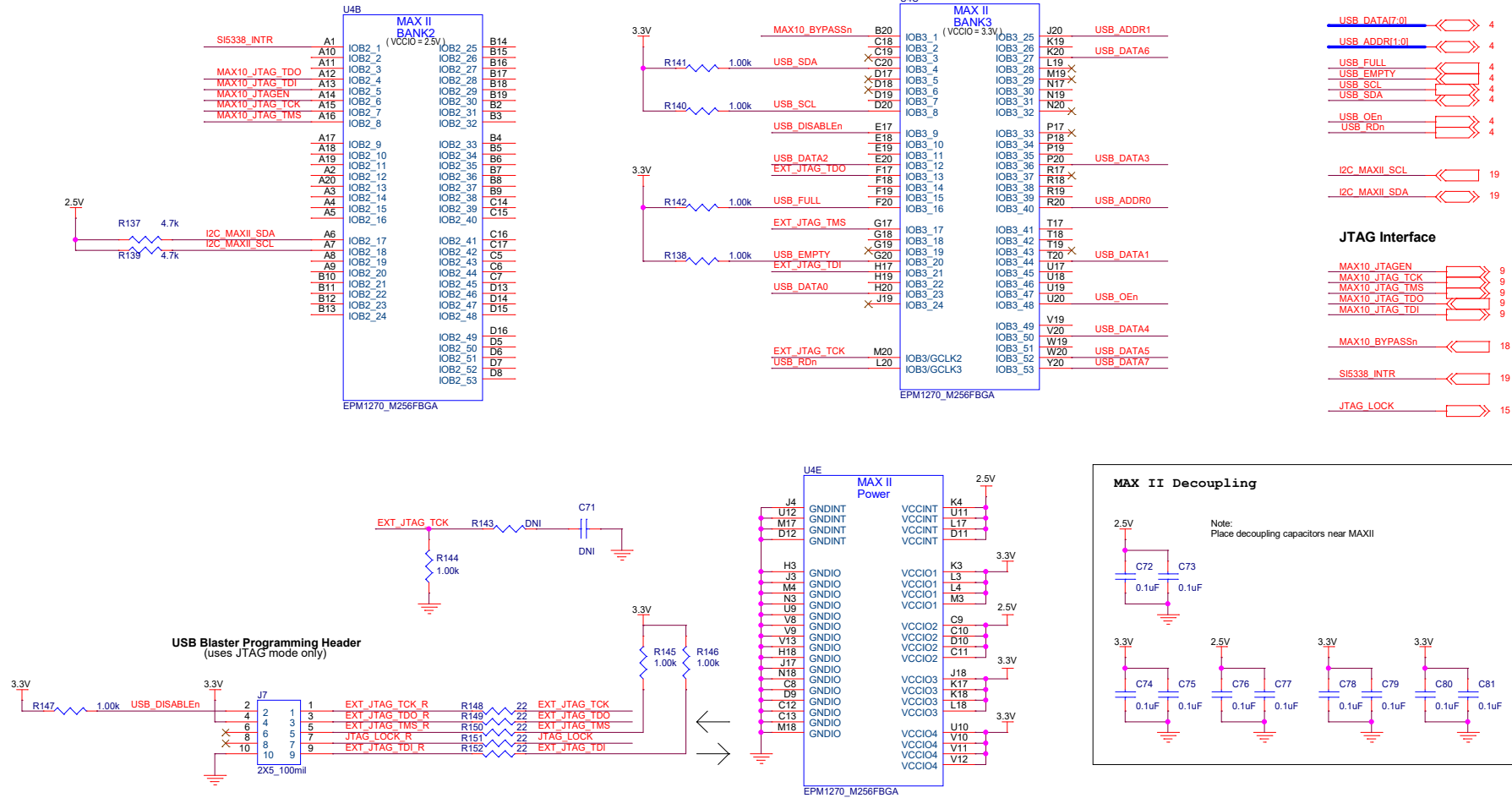
## HDMI Power Decoupling



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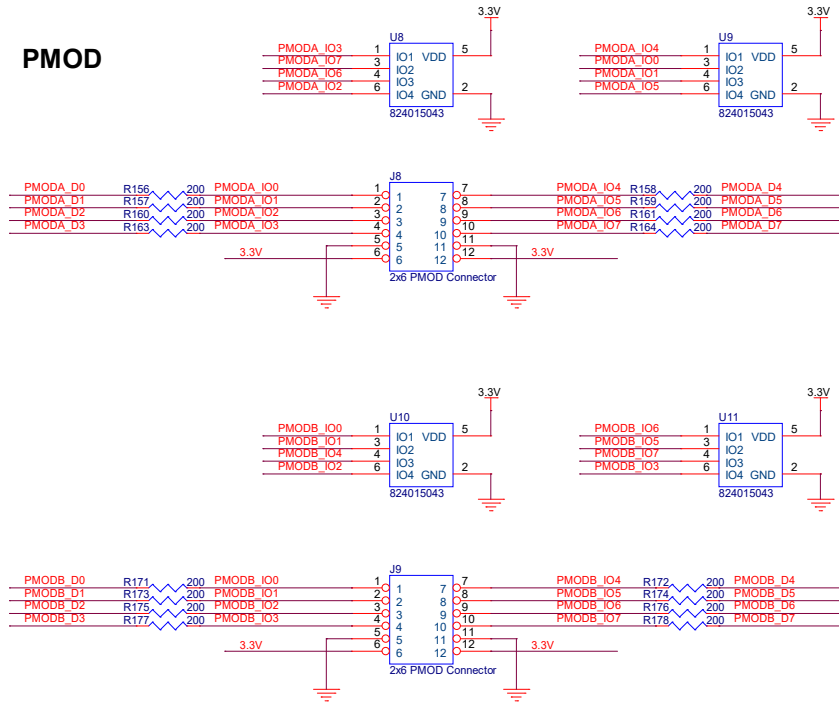
# ON-BOARD USB BLASTER II-2



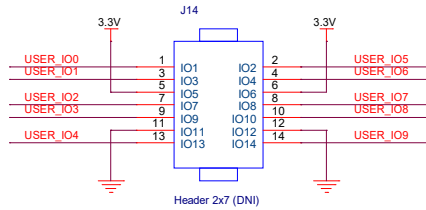


# PMOD, GPIO, LVDS USER IO

## PMOD

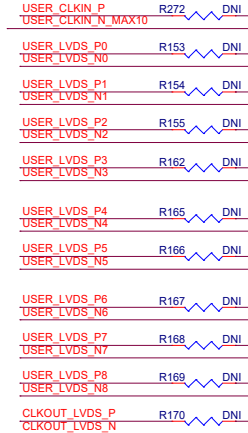


## User GPIO



## LVDS Termination

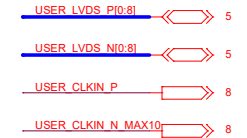
Note: Place near MAX 10 side.



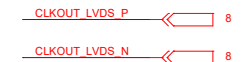
## PMOD



## User LVDS IO



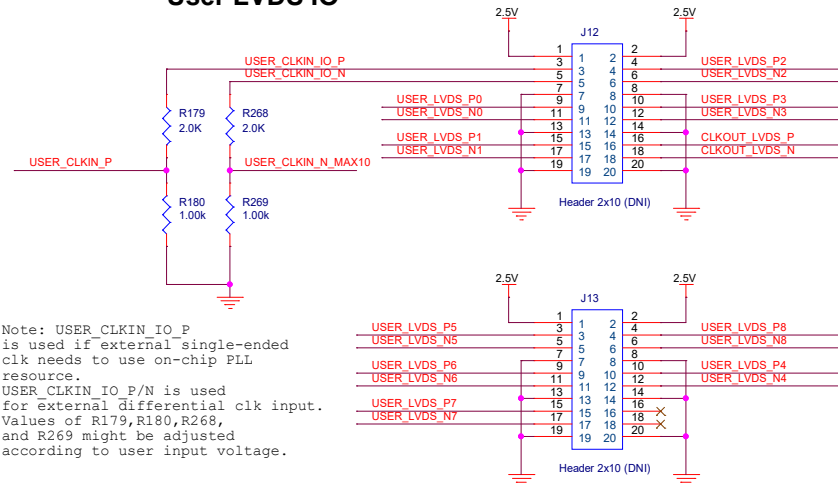
## LVDS



## User IO



## User LVDS IO



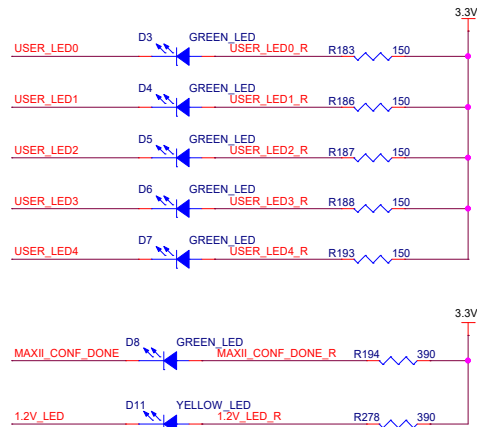
Note: USER\_CLKIN\_IO\_P is used if external single-ended clk needs to use on-chip PLL resource.  
USER\_CLKIN\_IO\_P/N is used for external differential clk input. Values of R179, R180, R268, and R269 might be adjusted according to user input voltage.



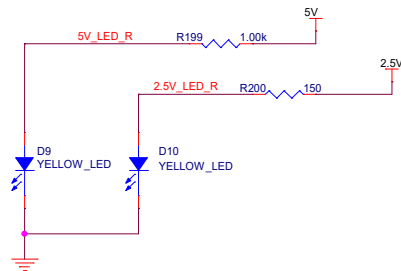
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# PUSHBUTTON, SWITCH, LED

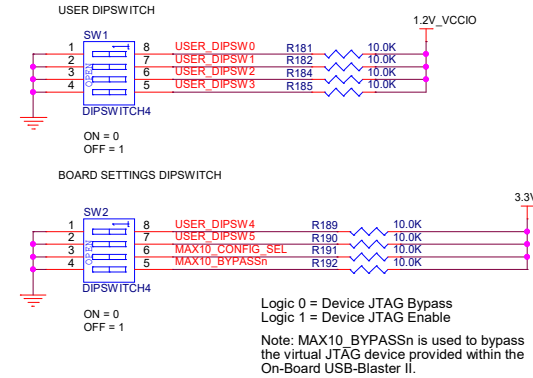
## User LED



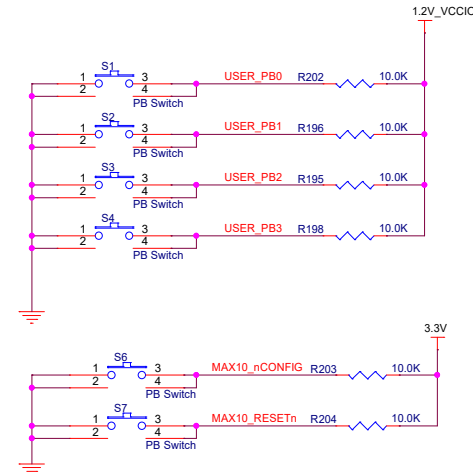
## Power LED



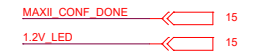
## User DIP Switch



## User Pushbutton



## MAXII



## User LED



## User Pushbutton

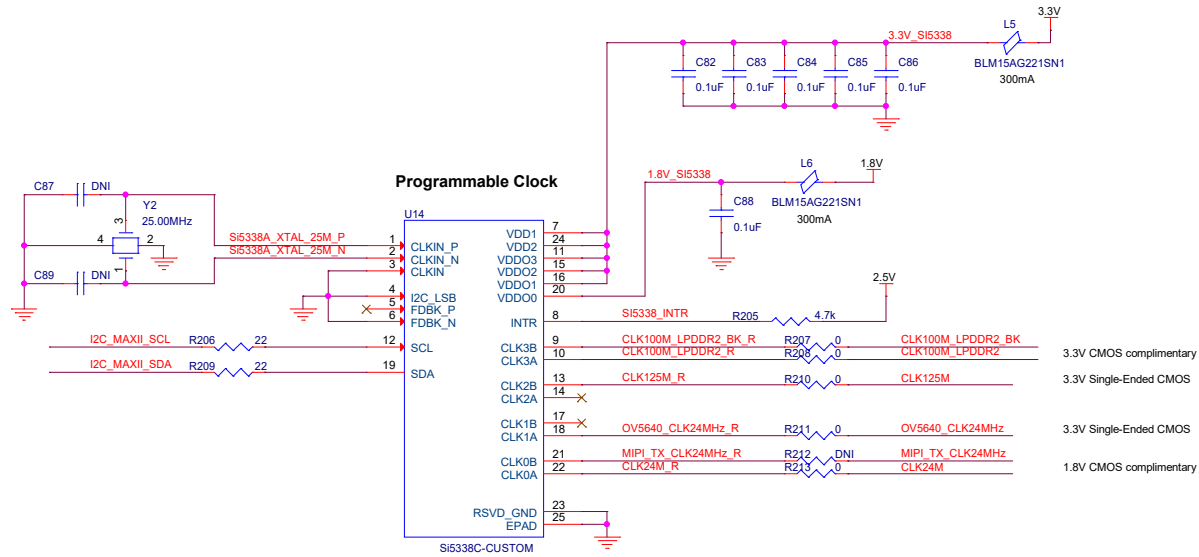


## User DIP Switch

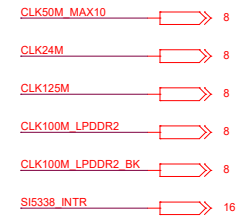


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# CLOCKING



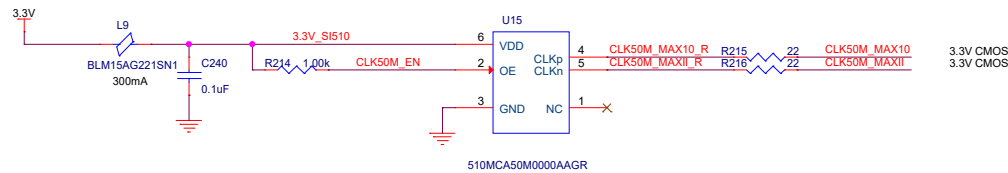
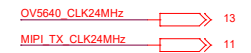
## MAX 10



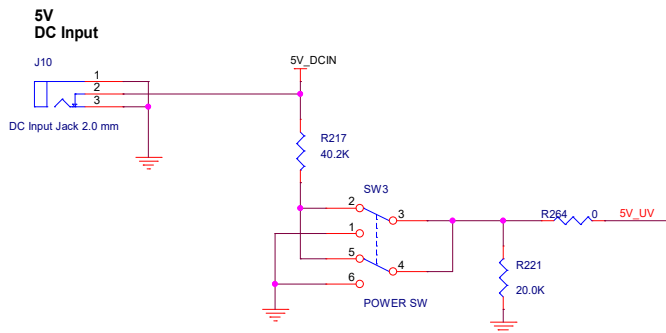
## MAXII



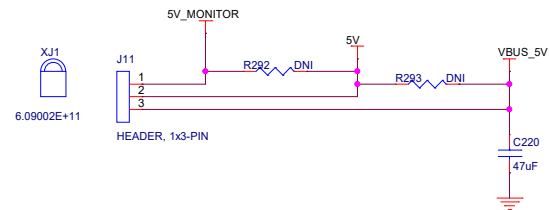
## DM385 CSI-2 TX Interface



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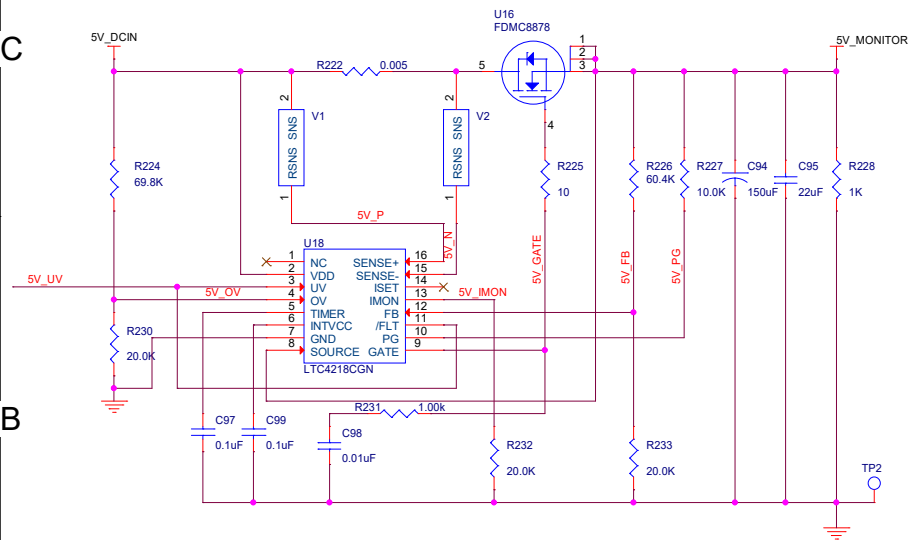


## HOT SWAP and POWER 3.3V



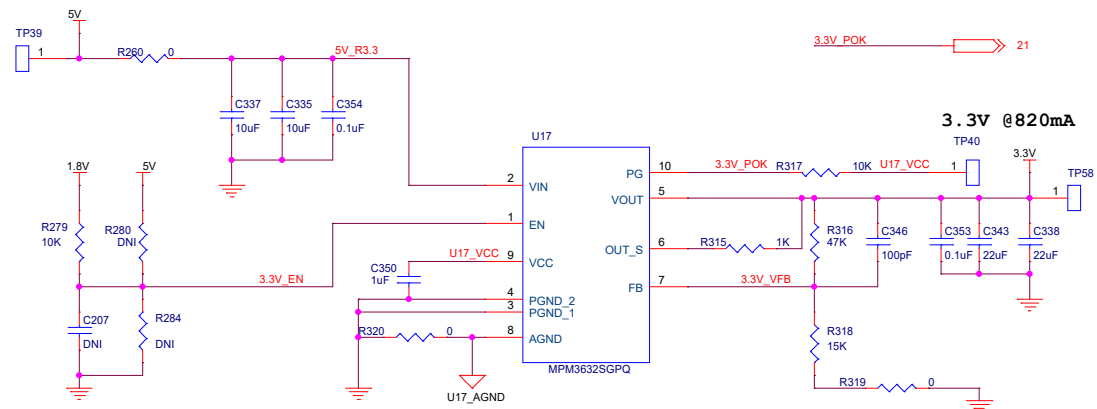
CAUTION:  
When NOT using jumpers,  
solder R292 for power input from DC Jack,  
or solder R293 for USB power.  
SOLDER ONLY ONE POWER OPTION,  
AND SUGGEST NOT TO USE WITH JUMPER.

## Hot Swap for DC Plug



Hot Swap Controller Circuit

## POWER 3.3V



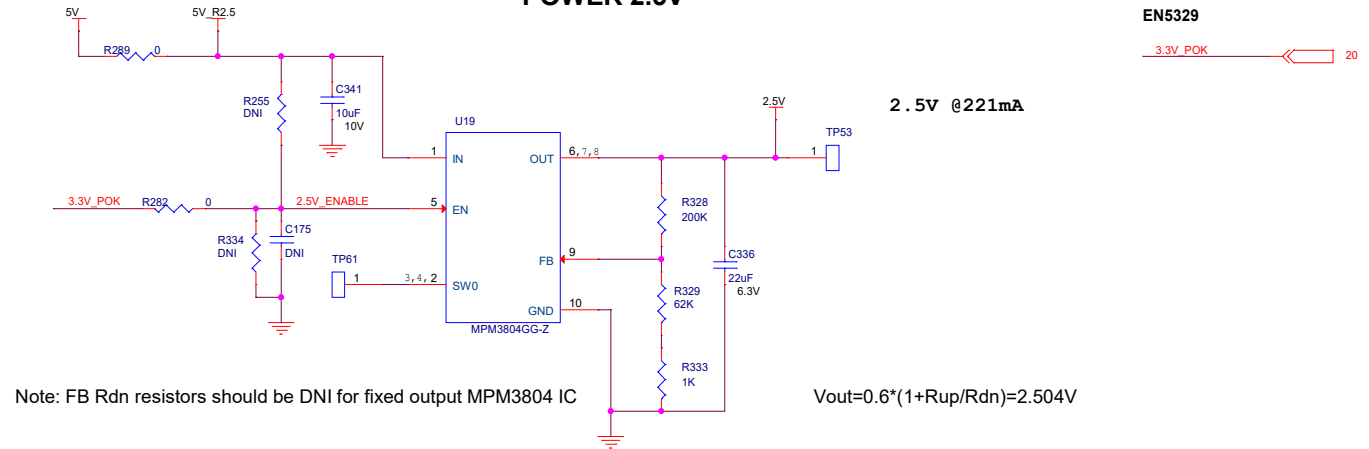
$$V_{out} = 0.8 \cdot (1 + R_{up}/R_{dn}) = 3.306V$$



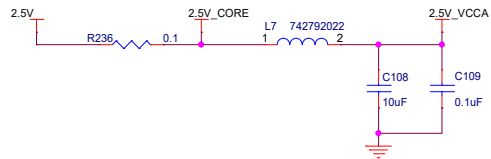
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## POWER 2.5V & 1.8V

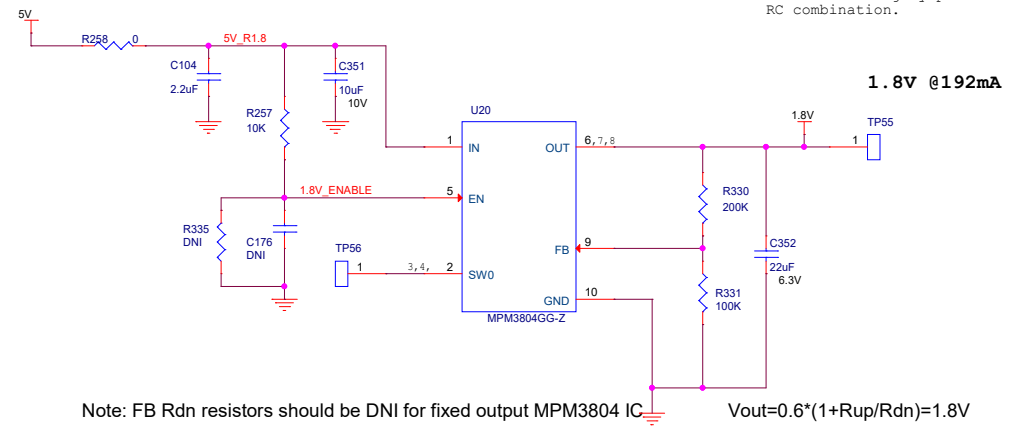
### POWER 2.5V



### POWER 2.5V\_VCCA



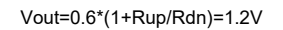
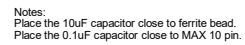
### POWER 1.8V



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**POWER 1.2V\_CORE**

**POWER 1.2V\_VCCIO**



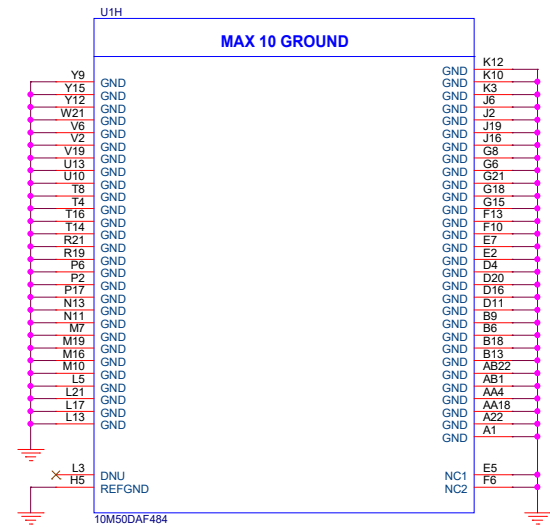
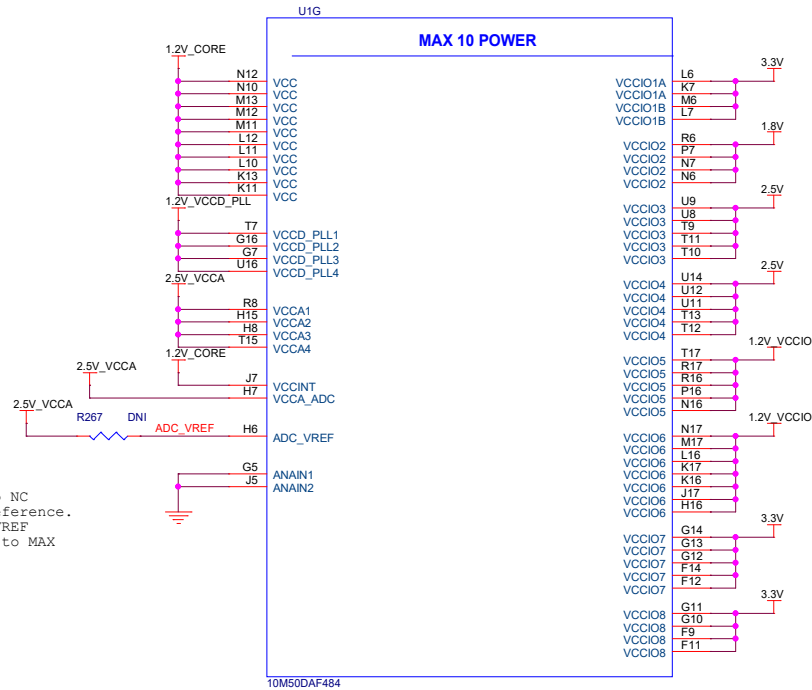
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C

Note:  
According to MAX 10 pin  
connection guideline  
PCG-01018-1.2,  
"Tie the VCCINT pin to any  
1.2V power domain if you  
are not using ADC."  
Therefore, connect VCCINT  
to 1.2V CORE for DC or DF  
production device migration.

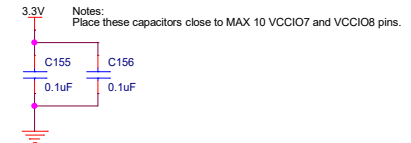
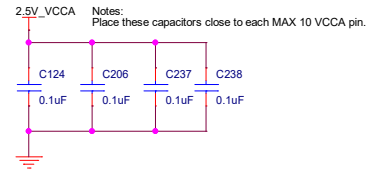
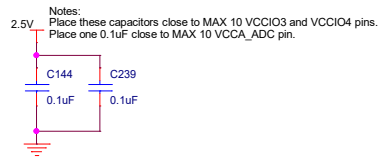
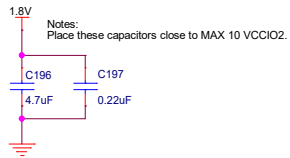
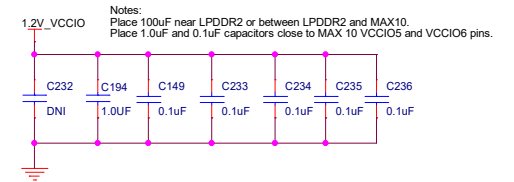
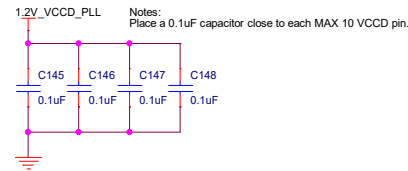
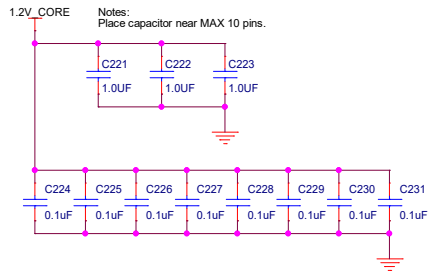
Note:  
According to MAX 10 pin  
connection guideline  
PCG-01018-1.2,  
"Tie the VCCA\_ADC pin  
to any 2.5V power domain  
if you are not using ADC,  
and do not tie the VCCA\_ADC  
pin to GND."  
Therefore, connect VCCA\_ADC  
to 2.5V CORE for DC or DF  
productIon device migration.

Note:  
For ES device, connect ADC\_VREF to NC  
when not using external voltage reference.  
For DC/DF production device, ADC\_VREF  
pin is migrated to VCCA according to MAX  
10 Errata.



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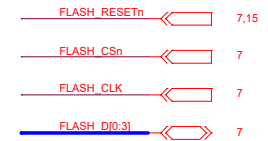
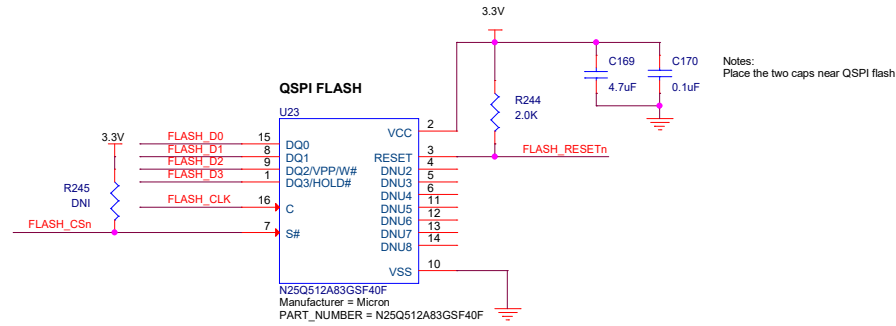
# DECOUPLING



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# QSPI FLASH



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