Product Brief

FPGA

altera™
An Intel Company

MAX® 10 FPGAs

Small, highly integrated, instant-on, single-chip solution

MAX® 10 FPGAs offer a compact, single-supply solution with unmatched ease of use and versatility, making them ideal for adaptable, all-in-one designs.

A simple & efficient Logic fabric architecture

High I/O Density packages, with up to 485 I/O in 19 x 19 mm² variable pitch BGA

Secure on-die flash memory for configuration in less than 10 ms

User Flash Memory up to 32-bit storage, 10K program/erase cycles, & 20-year retention via Avalon-MM I/F

Powering Edge AI with DSP & tinyML capabilities

ADC up to 1 Million Samples per Second sampling rate

MAX® 10 FPGAs are innovative, single-chip solutions that combine advanced processing capabilities with non-volatile flash memory, RAM, digital signal processing (DSP) blocks, and analog-to-digital converters (ADCs). Designed to deliver higher performance in a cost-effective, low-power, and compact form factor, MAX 10 FPGAs are ideal for a variety of markets, including industrial automation, automotive systems, and retail electronics. Their versatility and rich feature set allow designers to reduce board space, simplify system architecture, and lower overall costs without sacrificing functionality or performance.

One of the standout features of MAX 10 FPGAs is their power efficiency, achieved through a flash-enabled fab process technology that supports low static power consumption. Furthermore, it features on-chip flash memory with dual configuration image support, enabling versatile use cases such as factory fallback for recovery from corrupted updates, two-stage configuration for enhanced flexibility, and additional user flash storage—all integrated into a single chip. Additionally, the on-die flash ensures rapid configuration with initialization times of under 10 milliseconds and supports reconfiguration for dynamic system updates. The FPGA also features a sleep mode, enabling significant standby power reduction and resumption in less than 1 ms, further enhancing its efficiency in low-power applications.

MAX 10 FPGAs provide versatile general-purpose I/O support, including multiple I/O standard options, On-Chip Termination (OCT) for improved signal integrity, and support for high-speed LVDS up to 720 Mbps, ensuring reliable performance in a variety of applications. These I/O options make MAX 10 FPGAs a compelling choice for applications requiring reliable performance in space-constrained and noisy environments.

Available in densities ranging from 2,000 to 50,000 logic elements and package sizes as small as 3 x 3 mm². The MAX 10 device family was recently expanded to include high I/O density packages with a smaller form factor – up to 485 I/Os in a 19 x 19 mm² Variable Pitch BGA (VPBGA) package. This high I/O density package enables easy PCB layout by using the equivalent design rules as 0.8 mm ball pitch and standard PTH vias to help keep the board cost low.

MAX 10 FPGAs feature robust DSP capabilities, including up to 144 embedded multiplier blocks, enabling high-performance AI and edge computing solutions. Each block supports 18 × 18-bit or dual 9 × 9-bit multipliers, delivering the computational power needed for demanding AI tasks like real-time signal processing, video analytics, and sensor fusion. With support for DSP IP cores—such as finite impulse response (FIR) filters, fast fourier transform (FFTs), and numerically controlled oscillators (NCOs)—MAX 10 devices provide the flexibility to implement complex DSP and AI algorithms efficiently. Additionally, integration with tools like DSP Builder (from Altera) and MATLAB/Simulink (from MathWorks) simplifies development, ensuring faster time-to-market for DSP or AI-driven edge applications. MAX 10 FPGA also support the Nios® V soft processors based on the RISC-V architecture.

Combining the FPGAs DSP, logic, and memory blocks enables AI capability within compact, power-efficient designs to implement real-time inferencing, edge AI acceleration, and tiny machine learning (tinyML) workloads. By integrating AI tasks into MAX 10 FPGAs, developers can benefit from custom hardware acceleration, deterministic performance, and low-latency execution to process AI models efficiently at the edge without needing a separate AI component. MAX 10 FPGAs provide the intelligence, flexibility, and scalability needed to bring AI to emerging embedded systems.

With all the above features, MAX 10 FPGAs are versatile enough to address a wide range of application needs. The integration of an on-die ADC with the DSP/AI-capable blocks enables real-time signal processing, data conversion, and edge AI solutions such as AI-based sensor control. This facilitates the development of advanced solutions such as motor control, image processing, and industrial IoT. By combining flexibility, low power consumption, and robust features, MAX 10 FPGAs provide a comprehensive platform for designers looking to create efficient and cost-effective solutions for modern applications.

MAX 10 FPGAs Markets

MAX 10 FPGA Feature Options

Option	Feature
Compact	Devices with core architecture featuring single configuration image with self-configuration capability
Flash	Devices with core architecture featuring: ▪ Dual configuration image with self-configuration capability ▪ Remote system upgrade capability ▪ Memory initialization ▪ Hitless Updates with internal & external JTAG mode
Analog	Devices with core architecture featuring: ▪ Dual configuration image with self-configuration capability ▪ Remote system upgrade capability ▪ Memory initialization ▪ Integrated ADC

ADC Features

Feature	Description
12-bit resolution	▪ Translates analog signal to digital data for information processing, computing, data transmission, and control systems ▪ Provides a 12-bit digital representation of the observed analog signal
Up to 1 MSPS sampling rate	Monitors single-ended external inputs with a cumulative sampling rate of 25 kilo samples per second to 1 MSPS in normal mode
Up to 17 single-ended external inputs for single ADC devices	One dedicated analog and 16 dual-function input pins
Up to 18 single-ended external inputs for dual ADC devices	▪ One dedicated analog and eight dual-function input pins in each ADC block ▪ Simultaneous measurement capability for dual ADC devices
On-chip temperature sensor	Monitors external temperature data input with a sampling rate of up to 50 kilo samples per second

UFM Features

Feature	Capacity
Endurance	Counts to at least 10,000 program/erase cycles
Data retention	▪ 20 years at 85° C ▪ 10 years at 100° C
Operating frequency	Maximum 116 MHz for parallel interface and 7.25 MHz for serial interface
Data length	Stores data up to 32 bits length in parallel

MAX 10 FPGA Maximum Resources

Resource			Device						
			10M02	10M04	10M08	10M16	10M25	10M40	10M50
Logic Elements (LE) (K)			2	4	5	16	25	40	50
M9K Memory (Kb)			108	189	378	549	675	1,260	1,638
User Flash Memory (Kb)			96	1,248	1,376	2,368	3,200	5,888	5,888
DSP/AI (18 × 18 Multipliers)			16	20	24	45	55	125	144
PLL			2	2	2	4	4	4	4
Internal Configuration Image			1	2	2	2	2	2	2
ADC			–	1	1	1	2	2	2
Package	**Size (mm²)**	**Pitch (mm)**	**Single Supply Packages**						
V81	4x4	0.4	–	–	58	–	–	–	–
Y180	6x5	0.35	–	–	–	–	–	–	–
M153	8x8	0.5	112	112	112	–	–	–	–
U169	11x11	0.8	130	130	130	–	–	–	–
U324	15x15	0.8	246	246	246	–	–	–	–
B610	19x19	Variable[1]	–	–	–	–	–	485	485
E144	22x22	0.5	101	101	101	101	101	101	101
Package	**Size (mm²)**	**Pitch (mm)**	**Dual Supply Packages**						
V36	3x3	0.4	27	–	–	–	–	–	–
V81	4x4	0.4	–	–	56	–	–	–	–
U324	15x15	0.8	160	246	246	246	–	–	–
F256	17x17	1.0	–	178	178	178	178	178	178
B610	19x19	Variable[1]	–	–	–	–	–	485	485
F484	23x23x	1.0	–	–	250	320	360	360	360
F672	27x27	1.0	–	–	–	–	–	500	500

(1) The ball pitch of Variable Pitch BGA (VPBGA) package is variable. For more details, please refer to MAX® 10 FPGA Signal Integrity Design Guidelines.

For More Information

MAX® 10 FPGA product page

MAX® 10 FPGA Device Overview

MAX® 10 FPGA Device Datasheet

MAX® 10 Development Kits

Contact an Altera sales representative for inquiries

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