



5th Generation Intel[®] Core[™] Processor Family Mobile Thermal Mechanical Design Guide for Embedded Applications

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Internet of Things Group

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Revision History

Revision	Date	Comments
001	January 2015	<ul style="list-style-type: none">Initial Release
002	August 2015	<ul style="list-style-type: none">Updated naming conventions/ brandingUpdated PCH power level consumption per system configurationVarious changes throughout

5th Generation Intel® Core™ Processor Family for Mobile Thermal Mechanical Design Guide for Embedded Applications

This document is intended to provide material and guidance to aid in design of 5th Generation Intel® Core™ processor based on Mobile products into embedded form factors. This document is meant to be a supplement to the *Broadwell Platform Mobile Thermal Mechanical Design Guide* (Document Number: 519826).

For any specification discrepancies between this document and the processor External Design Specification [EDS], the EDS supersedes.

Contents:

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Product Overview

Thermal, Power and SKU Summary

Definition	Units	H-Processor Line	H-Processor Line	U-Processor Line	U-Processor Line
Product		4C+GT3+eDRAM	4C+GT2	2C+GT3+PCH	2C+GT2+PCH
Interconnect to Motherboard				BGA	
TDP Pkg [†]	W	47	47	15	15
cTDP Pkg	W	37	37	9.5	7.5
TDP CPU [†]	W	47	47	15	15
TDP eDRAM	W	4	--	--	--
TDP PCH**	W	--	--	0.6	0.6
TJ _{max} – CPU POR	°C	105	105	105	105
TJ _{max} – eDRAM POR	°C	100	--	--	--
TJ _{max} – PCH POR	°C	--	--	105	105
Notes		CPU + eDRAM	CPU + eDRAM w/ eDRAM disabled	CPU + PCH	CPU + PCH

[†] Includes all power delivery losses on package

Note: Package Powers (“TDP Pkg”) of MCP products are NOT the summation of individual die powers.

**PCH power listed in the table assumes two High Speed I/O (HSIO) ports active during CPU TDP workload; PCH power is listed for the following system configurations and workloads. (HSIO ports are USB3.0, eSATA, PCIe*, Thunderbolt). See *Intel Broadwell-U PCH Power Stress Procedure – Thermal Design Consideration, Doc #557026* for test procedure to generate these power levels.

2 HSIO ports active: 0.6 W

3 HSIO ports active: 0.8 W

4 HSIO ports active: 1.4 W

Package Information

IOTG Packaging

Attribute	U-Processor Line	H-Processor Line
Package Type	Flip Chip Ball Grid Array	
Package Dimension	40x24 mm ²	37.5x32 mm ²
Ball/Pin Count	1168	1364
Ball/Pin Pitch	0.65 mm	0.7 mm
Raw Ball Diameter	0.406 mm (16 mil)	0.431 mm (17 mil)
Land Side Capacitors	Yes	
Separate PCH	No	Yes
Die Configuration	Multi-Chip Package	
Die Side Capacitors	No	Yes
Die Size	2+3: 19.6x6.8 mm 6.1x8.4 mm 2+2: 13.4x6.0 mm 6.1x8.4 mm	13.7x12.3 mm 6.8x11.7 mm
Die Thickness	0.212 mm	0.412 mm
Substrate Thickness	0.757 mm	1.022 mm
Max Z-Height (Post SMT, m+4s)	1.28 mm	1.828 mm
NCTF Corner Balls	9/Corner	13/Corner; 16@A1
Max Static Compressive Load	15 Lbs.. without backing plate	25 Lbs. with backing plate 15 Lbs. without backing plate

Note: Informational only - Refer to 5th Generation Intel® Core™ Processor Family and Intel® Core™ M Processor Family External Design Specification (EDS) – Volume 1 of 2 (Document Number: 514405).

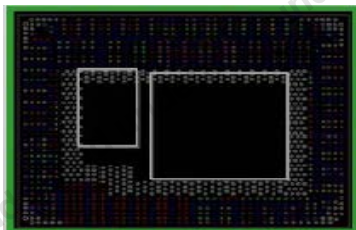
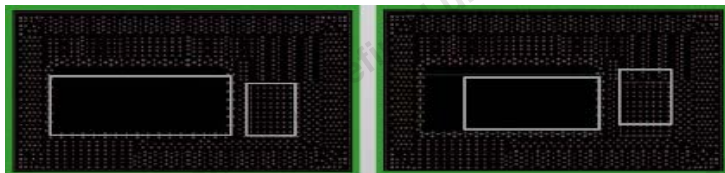
The package mechanical drawings are included in the accompanying TMDG *.zip file

Thermal Considerations

Thermal Considerations Overview

5th Generation Intel® Core™ Processor-ULT

- Slight improvement in cooling solution from previous generations may be needed[†]
- 2+3 and 2+2 are pin compatible
- CPU die center loading is critical to avoid die cracks. In rare instances the load on the PCH die may become concentrated at corners during system assembly and cause damage to the die. In these rare scenarios it is recommended that contact between the thermal solution and the PCH die is minimized or eliminated. See document #556532 for measurement techniques.



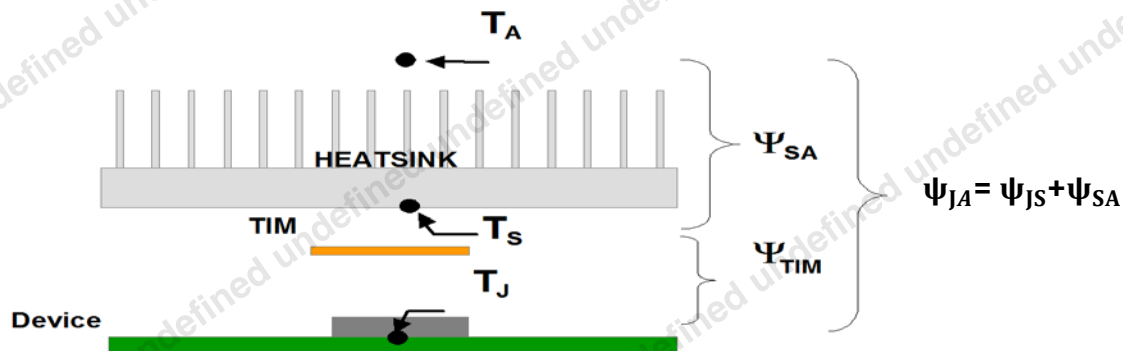
5th Generation Intel® Core™ Processor 4+3e

- Slight improvement in cooling solution from previous generation may be needed[†]
- eDRAM needs to make contact with thermal solution but focus should be on thermal solution attach to CPU

[†] Refer to the the Broadwell Platform Mobile Thermal Mechanical Design Guide 'Thermal Considerations' section for estimates on increased cooling solution needs for each SKU.

Mobile Bare Die Resistance Calculations

The thermal characterization parameter ψ is used to characterize thermal solution performance, as well as compare thermal solutions in identical situations (e.g., heating source, local ambient conditions, etc.)



$$\psi_{JA} = \frac{T_J - T_{LA}}{TDP} = \text{Junction - to - Ambient thermal characterization}$$

$$\psi_{JS} = \frac{T_J - T_S}{TDP} = \text{Junction - to - Sink thermal characterization (TIM Performance)}$$

$$\psi_{SA} = \frac{T_S - T_{LA}}{TDP} = \text{Sink - to - Ambient thermal characterization (Heat Sink Performance)}$$

Mobile Bare Die Resistance Calculations: Example

The below example calculates the heat sink performance required for specified boundary conditions.

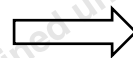
Assumptions:

- TDP=47 W
- $T_{J-Max}=105^{\circ}C$
- $T_A=40^{\circ}C$
- TIM Performance = $0.3^{\circ}C/W = \psi_{JS}$

Resistance Calculation:

$$\psi_{JA} = \frac{T_J - T_A}{TDP} = \frac{105^{\circ}C - 40^{\circ}C}{47 W} = 1.38^{\circ}C/W$$

$$\psi_{JA} = \psi_{JS} + \psi_{SA}$$



$$\psi_{SA} = \psi_{JA} - \psi_{JS}$$

$$\psi_{SA} = 1.38 \frac{^{\circ}C}{W} - 0.3 \frac{^{\circ}C}{W} = 1.08 \frac{^{\circ}C}{W}$$

- The required heat sink performance is $1.08^{\circ}C/W$ under the specified Boundary Conditions
- The thermal characterization parameter assumes all of the power is dissipated through the heat sink which is an idealization
- The resistance model assumptions should be used as a first order approximation only. Modeling and testing must be employed to ensure a proper thermal solution has been selected

Reference Thermal Solutions

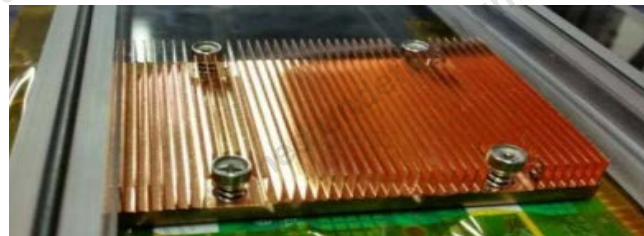
Reference Thermal Solutions

Intel has developed reference thermal solutions designed to meet cooling needs for embedded form factor applications. This document details solutions that are compatible with Mini-ITX* and CompactPCI* form factors.

The data provided herein is based on test data for the reference thermal solutions. The Mini-ITX* and CompactPCI* heat sinks were tested as an assembly with a Thermal Test Vehicle (TTV), thermal interface material, socket, backing plate, and test board. For the CompactPCI* thermal solutions, the test assemblies were placed in a rectangular duct connected to a wind tunnel with no upstream obstructions. Air flow is measured by a calibrated nozzle downstream from the unit under test.



Mini-ITX* (Active)



CompactPCI* (Passive)

Mini-ITX* Reference Heat Sink

This active reference design is compatible with Mini-ITX* and larger form factors. The thermal performances reported within this document are on TTVs running at full fan speed (rated at 12.72 CFM at zero static pressure) with 5Vs supplied to the fan at uniform power. The reference solutions under test were subjected to static compressive loads between 20 to 25 lbs. using a backing plate.

The thermal performance of the heat sink shown below can meet the thermal performance needed to cool the processor in the Mini-iTX* form factor. However, it is up to the system designer to validate the entire thermal solution (heat sink, attach method, and thermal interface material) in its final intended system.

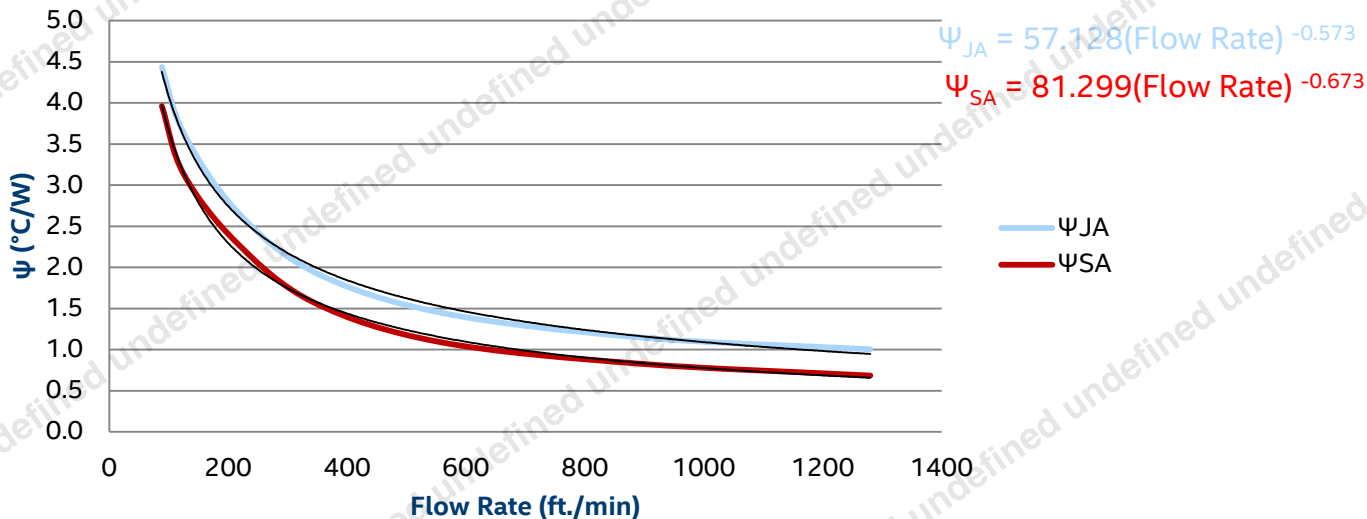
Device Under Test	TDP (W)	$\Psi_{SA} (^{\circ}\text{C}/\text{W})$	$\Psi_{JA} (^{\circ}\text{C}/\text{W})$
4 th Generation Intel [®] Core [™] Processor TTV with 4W eDRAM [†]	47	0.67	0.75
4 th Generation Intel [®] Core [™] Processor TTV	47	0.68	0.76
4 th Generation Intel [®] Core [™] Processor TTV	37	0.67	0.76

[†]4th Generation Intel[®] Core[™] Processor with 4 W eDRAM test was run at 43 W CPU + 4 W eDRAM = 47 W TDP

Note: Laird* TPCM583 phase change material was used for reference design tests.

CompactPCI* Reference Heat Sink

This passive reference heat sink is compatible with CompactPCI* form factors. The thermal performances reported within this document are based on TTVs with uniform power. The reference solutions under test were subjected to static compressive loads between 10 to 15 lbs. using a backing plate. The figure below outlines the heat sink thermal performance parameter at various airflow rates.



Note: Laird* TPCM583 phase change material was used for reference design tests.

Thermal Interface Material (TIM)

The thermal interface material provides improved conductivity between the die and heatsink. It is important to understand and consider the impact of the interface between the die and heatsink base to the overall thermal solution. Specifically, the bond line thickness, interface material area, and interface material thermal conductivity must be selected to optimize the thermal solution.

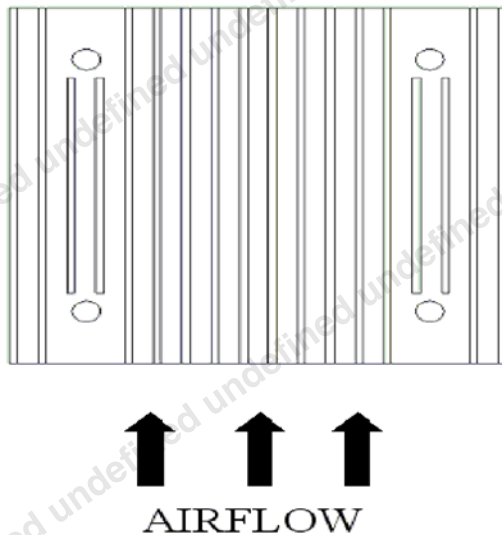
It is important to minimize the thickness of the thermal interface material (TIM), commonly referred to as the bond line thickness. A large gap between the heatsink base and the die yields a greater thermal resistance. The thickness of the gap is determined by the flatness of both the heatsink base and the die, plus the thickness of the thermal interface material, and the clamping force applied by the heatsink attachment method. To ensure proper and consistent thermal performance, the TIM and application process must be properly designed.

Thermal interface materials have thermal impedance (resistance) that will increase over time as the material degrades. It is important for thermal solution designers to take this increase in impedance into consideration when designing a thermal solution. It is recommended that system integrators work with TIM suppliers to determine the performance of the desired thermal interface material. If system integrators wish to maintain maximum thermal solution performance, the TIM could be replaced during standard maintenance cycles.

Some of the Thermal Interface materials that Intel recommends are Shin-Etsu* PCS-LT-30, Honeywell* PCM45F, and Chromerics* T777 phase change materials. Alternative materials can be used at the user's discretion. Regardless, the entire heatsink assembly, including the heatsink, and TIM (including attach method), must be validated together for specific applications.

Heat Sink Orientation

These reference designs must be oriented in a specific direction relative to the processor keep-out zone and airflow. In order to use these designs, the processor must be placed on the PCB in an orientation so the heat sink fins will be parallel to the airflow as illustrated in the figure below.



Reference Thermal Solution Suppliers

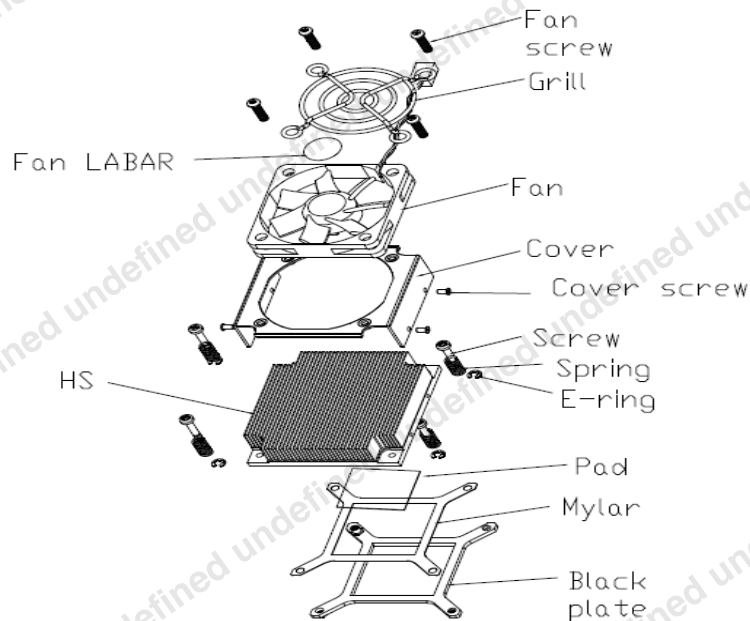
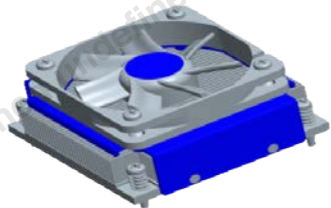
Part	Intel Part Number	Supplier Part Number	Supplier Contact Information
Mini-ITX* Heat Sink Assembly	H33887-001	DEL-00025-N2GP	Cooler Master USA, Inc.* coolermaster.com (510) 770-8566
CompactPCI* Assembly	G32222-001	1A01PS100	Foxconn/FTC Technology, Inc.* foxconn.com (512) 670-2638
Thermal Interface Material	N/A	PCS-LT-30	Shin-Etsu MicroSi* MicroSi.com (480) 584-3887
Thermal Interface Material	N/A	PCM45F	Honeywell* honeywell.com (509) 252-8605
Fan	N/A	MG(T)5005XB-(W)10	Protechnic* protecpnic-us.com (510) 360-9630

- Please contact your local FAE for more information
- The Mini-ITX* and CompactPCI* drawings are included in the accompanying *.zip file

Mechanical Considerations

Mini-ITX* Reference Heat Sink Mechanical Stack-up

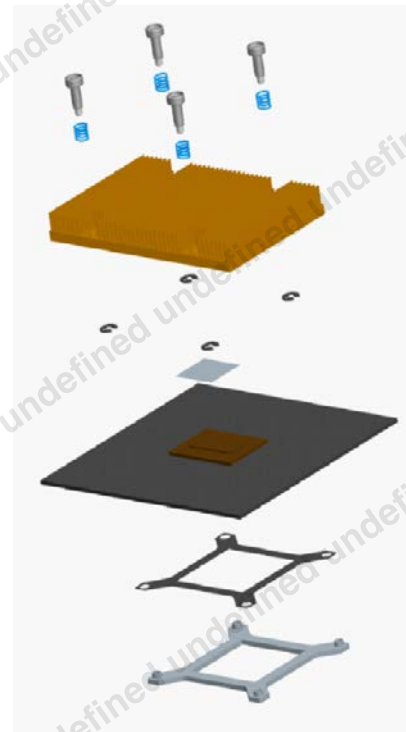
- The Mini-ITX* reference solution uses screws, springs, and a back plate assembly to attach the fan/heat sink to the PCB.
- It is an active fan solution comprised of an aluminum skived heat sink assembly with overall dimensions of 60mm x 60mm x 32mm.
- The maximum heat sink height was constrained so that it will not exceed maximum component height for Mini-ITX* form factors.



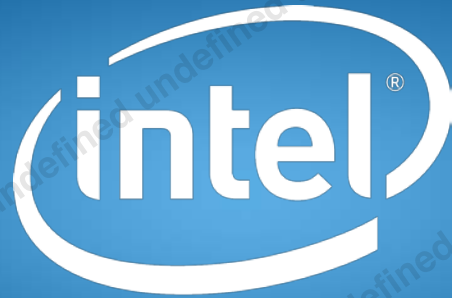
See accompanying TMDG *.zip file for the Mini-ITX* reference thermal solution drawings

CompactPCI* Reference Heat Sink Mechanical Stack-Up

- The CompactPCI* reference solutions use screws, springs, and a back plate assembly to attach the heat sink to the PCB as shown in the adjacent figure.
- It is a passive solution comprised of a copper skived heat sink assembly with overall dimensions of 60 mm x 90 mm x 11.6 mm.
- The maximum heat sink height was constrained so that it will not exceed maximum component height for CompactPCI* form factors.



See accompanying TMDG *.zip file for the Mini-ITX* reference thermal solution drawings



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Backup

Related Documents

Specification and Implementation Guides

Doc.	Document
519826	Broadwell Platform Mobile Thermal Mechanical Design Guide
514405	5th Generation Intel® Core™ Processor Family and Intel® Core™ M Processor Family External Design Specification (EDS) - Volume 1 of 2
519448	Broadwell Package Mechanical Models and Drawings
513915	Broadwell Turbo Implementation Guide
524987	Broadwell Client Platform Thermal Management Design Guide

Thermal Evaluation

Doc.	Document
500815	Haswell-M Processor – Haswell Thermal Test Vehicle - Quick User Guide – (Covers 4c+2 and 4c+3)†
526133	Broadwell Component Thermal Models

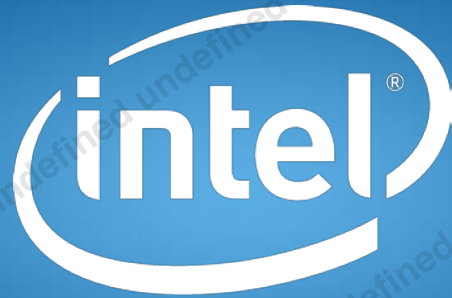
Tools

Doc.	Document
539446	Intel® Thermal Analysis Tool (Windows, Linux and Chrome)
558587	Intel® PECL Stress Tool – Utility Software
351424	Intel® Frequency Display Utility – Utility Software
371149	Intel® GVCycle Utility – Utility Software

†Note: There will be no unique TTV's created for Embedded Broadwell SKU's. Haswell TTV's can be used.

Definitions and Terms

Term	Definition
T_A	The ambient temperature outside of a system; a fixed reference temperature.
T_{LA}	The air temperature "near" a component within a system.
T_J	The silicon junction temperature as reported by an internal silicon sensor (DTS, thermal diode).
T_S	The heat sink base temperature.
Ψ_{JA}	Junction-to-ambient thermal characterization parameter. A measure of heat sink thermal performance using the total package power. Defined as $(T_J - T_{LA}) / \text{Total Package Power}$.
Ψ_{JS}	Junction-to-sink thermal characterization parameter. A measure of thermal interface material performance using total package power. Defined as $(T_J - T_S) / \text{Total Package Power}$. Also referred to as Ψ_{JS} .
Ψ_{SA}	Sink-to-ambient thermal characterization parameter. A measure of heat sink thermal performance using total package power. Defined as $(T_S - T_{LA}) / \text{Total Package Power}$.
TIM	Thermally conductive compound between the heat sink and die.
LFM	Airflow velocity in linear feet per minute.
TDP	Thermal Design Power – recommended power level for thermal solution design.
PMD	Package Mechanical Drawing.
PCB	Printed Circuit Board.
MCP	Multi-Chip Package.
FCBGA	Flip Chip Ball Grid Array – a ball grid array packaging technology where the die is exposed on the package substrate.



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