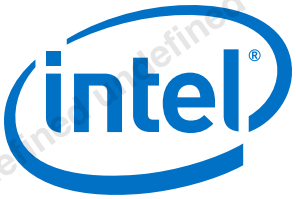

Intel® Xeon® Processor E5 v4 Product Family Datasheet, Volume One: Electrical

Volume 1 of 2

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Revision History

Document Number	Revision Number	Description	Date
333809	-001	Initial release	March 2016
333809	-002	Added Statement of Volatility	April 2016
333809	-003	Added Intel® Xeon® Processor E5-1600 and E5-4600 v4 Product Family	June 2016

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1.0 Introduction

The Datasheet provides descriptions of the Intel® Xeon® processor E5 v4 product family registers and Electrical specifications (including DC electrical specifications, signal integrity, and land and signal definitions).

This document is distributed as a part of the complete Datasheet consisting of two volumes.

Note: Unless specified otherwise, the term "Intel® Xeon® processor E5 v4 product family", "server processor", or "processor" will represent the following processors throughout the rest of the document. Features within this document may not be supported on all processor types and SKUs.

This document covers the following processors:

- Intel® Xeon® Processor E5 v4 Product Family; for Efficient Performance Server, Workstation, HPC, Storage and Embedded.
- Intel® Core™ i7 X-Series Processor; for High-End Desktop (HEDT).

The Intel® Xeon® processor E5 v4 product family is the next generation of 64-bit, multi-core enterprise processor built on 14-nm process technology. Based on the low power / high performance processor microarchitecture, the processor is designed for a platform consisting of a processor and the Platform Controller Hub (PCH).

Note: Some processor features are not available on all platform segments, processor types, and processor SKUs.

The processor supports up to 46 bits of physical address space and 48-bit of virtual address space.

- The Intel® Xeon® Processor E5 v4 Product Family features (per socket) two Intel® QuickPath Interconnect point-to-point links capable of up to 9.6 GT/s, up to 40 lanes of PCI Express* 3.0 links capable of 8.0 GT/s, and 4 lanes of DMI2/PCI Express* 2.0. It features 2 IMCs (Integrated Memory Controller), which support DDR4 DIMMs.

Included in this family of processors is an integrated memory controller (IMC) and an integrated I/O (IIO) on a single silicon die. This single die solution is known as a monolithic processor.

For supported processor configurations, refer to:

- *Intel® 64 and IA-32 Architectures Software Developer's Manuals*

1.1 Electrical Datasheet Introduction

This is volume one (Vol 1) of the processor Datasheet, which provides DC electrical specifications, signal integrity, differential signaling specifications, and land and signal definitions of the processor.

Additionally, this document may be used by system test engineers, board designers, and BIOS developers.

1.1.1 Structure and Scope

The following table summarizes the structure and scope of each volume of the processor Datasheet.

Table 1. Structure of the Processor Datasheet

Volume One: Electrical Datasheet
• Introduction
• Electrical Specifications
• Processor Land Listing
• Processor Signal Descriptions
Volume Two: Register Information
• Configuration Process and Registers Overview
• Configuration Space Registers (CSR)
• Model Specific Registers (MSR)

1.1.2 Related Publications

Refer to the following documents for additional information.

Table 2. Public Publications

Document	Document Number/Location
Advanced Configuration and Power Interface Specification 4.0	http://www.acpi.info/
PCI Local Bus Specification 3.0	http://www.pcisig.com/
PCI Express Base Specification, Revision 3.0	http://www.pcisig.com/
PCI Express Base Specification, Revision 2.1	
PCI Express Base Specification, Revision 1.1	
PCIe Gen 3 Connector High Speed Electrical Test Procedure*	325028-001 / http://www.intel.com/content/www/us/en/io/pci-express/pci-express-architecture-devnet-resources.html
Connector Model Quality Assessment Methodology	326123-002 / http://www.intel.com/content/www/us/en/architecture-and-technology/intel-connector-model-paper.html
DDR4 SDRAM Specification and Register Specification	http://www.jedec.org/
Intel® 64 and IA-32 Architectures Software Developer's Manuals • *Volume 1: Basic Architecture* • *Volume 2A: Instruction Set Reference, A-M* • *Volume 2B: Instruction Set Reference, N-Z* • *Volume 3A: System Programming Guide*	325462 / http://www.intel.com/products/processor/manuals/index.htm

continued...

Document	Document Number/Location
• *Volume 3B: System Programming Guide* *Intel® 64 and IA-32 Architectures Optimization Reference Manual*	
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	http://www.intel.com/content/www/us/en/intelligent-systems/intel-technology/vt-directed-io-spec.html
Intel® Trusted Execution Technology Software Development Guide	http://www.intel.com/technology/security/

1.1.3 Terminology

Term	Description
ASPM	Active State Power Management
BMC	Baseboard Management Controller
Cbo	Caching Agent (also referred to as CA). It is a term used for the internal logic providing ring interface to LLC and Core. The Cbo is a functional unit in the processor. A Caching Agent is defined per the *RS - Intel® QuickPath Interconnect External Link Specification*.
DDR4	Fourth generation Double Data Rate SDRAM memory technology.
DMA	Direct Memory Access
DMI2	Direct Media Interface Gen2 operating at PCI Express 2.0 speed.
DSB	Data Stream Buffer. Part of the processor core architecture.
DTLB	Data Translation Look-aside Buffer. Part of the processor core architecture.
DTS	Digital Thermal Sensor
ECC	Error Correction Code
Enhanced Intel SpeedStep® Technology	Allows the operating system to reduce power consumption when performance is not needed.
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
FLIT	Flow Control Unit. The Intel QPI Link layer's unit of transfer; 1 Flit = 80-bits.
Functional Operation	Refers to the normal operating conditions in which all processor specifications, including DC, system bus, signal quality, mechanical, and thermal, are satisfied.
GSSE	Extension of the SSE/SSE2 (Streaming SIMD Extensions) floating point instruction set to 256b operands.
HA	A Home Agent (HA) orders read and write requests to a piece of coherent memory.
ICU	Instruction Cache Unit. Part of the processor core architecture.
IFU	Instruction Fetch Unit. Part of the processor core.

continued...

Term	Description
IIO	The Integrated I/O Controller. An I/O controller that is integrated in the processor die.
IMC	The Integrated Memory Controller. A Memory Controller that is integrated in the processor die.
IQ	Instruction Queue. Part of the core architecture.
Intel® ME	Intel® Management Engine
Intel® QuickData Technology	Intel® QuickData Technology is a platform solution designed to maximize the throughput of server data traffic across a broader range of configurations and server environments to achieve faster, scalable, and more reliable I/O.
Intel® QuickPath Interconnect (Intel® QPI)	A cache-coherent, link-based Interconnect specification for Intel processors, chipsets, and I/O bridge components.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture. Further details on Intel 64 architecture and programming model can be found at http://developer.intel.com/technology/intel64/.
Intel® Turbo Boost Technology	A feature that opportunistically enables the processor to run a faster frequency. This results in increased performance of both single and multi-threaded applications.
Intel® TXT	Intel® Trusted Execution Technology
Intel® Virtualization Technology (Intel® VT)	Processor Virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
Intel® VT-d	Intel® Virtualization Technology (Intel® VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or OS) control, for enabling I/O device Virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.
Integrated Heat Spreader (IHS)	A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
IOV	I/O Virtualization
IVR	Integrated Voltage Regulation (IVR): The processor supports several integrated voltage regulators.
Jitter	Any timing variation of a transition edge or edges from the defined Unit Interval (UI).
LGA 2011-3 Socket	The 2011-3 land FC-LGA package mates with the system board through this surface mount, 2011-3 contact socket.
LLC	Last Level Cache
LRDIMM	Load Reduced Dual In-line Memory Module
LRU	Least Recently Used. A term used in conjunction with cache allocation policy.
MESIF	Modified/Exclusive/Shared/Invalid/Forwarded. States used in conjunction with cache coherency
MLC	Mid Level Cache
NCTF	Non-Critical to Function: NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.

continued...

Term	Description
NID	Node ID (NID) or NodeID (NID). The processor implements up to 4-bits of NodeID (NID).
NodeID	Node ID (NID) or NodeID (NID).
pcode	Pcode is microcode which is run on the dedicated microcontroller within the PCU.
PCH	Platform Controller Hub. A chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security and storage features.
PCU	Power Control Unit.
PCI Express 3.0	The third generation PCI Express specification that operates at twice the speed of PCI Express 2.0 (8 Gb/s); PCI Express 3.0 is completely backward compatible with PCI Express 1.0 and 2.0.
PCI Express 2.0	PCI Express Generation 2.0
PECI	Platform Environment Control Interface
Phit	An Intel® QPI terminology defining bits at physical layer.
Processor	Includes the 64-bit cores, uncore, I/Os and package
Processor Core	The term "processor core" refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache.
R3QPI	Intel QPI Agent. An internal logic block providing interface between internal Ring and external Intel QPI.
Rank	A unit of DRAM corresponding four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DDR4 DIMM.
RDIMM	Registered Dual In-line Memory Module
RTID	Request Transaction IDs are credits issued by the Cbo to track outstanding transaction, and the RTIDs allocated to a Cbo are topology dependent.
SCI	System Control Interrupt. Used in ACPI protocol.
SKU	Stock Keeping Unit (SKU) is a subset of a processor type with specific features, electrical, power and thermal specifications. Not all features are supported on all SKUs. A SKU is based on specific use condition assumption.
SSE	Intel® Streaming SIMD Extensions (Intel® SSE)
SMBus	System Management Bus. A two-wire interface through which simple system and power management related devices can communicate with the rest of the system.
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
TAC	Thermal Averaging Constant
TDP	Thermal Design Power

continued...

Term	Description
TSOD	Temperature Sensor On DIMM
UDIMM	Unbuffered Dual In-line Memory Module
Uncore	The portion of the processor comprising the shared LLC cache, Cbo, IMC, HA, PCU, Ubox, IIO and Intel QPI link interface.
Unit Interval	Signaling convention that is binary and unidirectional. In this binary signaling, one bit is sent for every edge of the forwarded clock, whether it be a rising edge or a falling edge. If a number of edges are collected at instances t_1, t_2, t_n,...., t_k then the UI at instance "n" is defined as: $UI_n = t_n - t_{n-1}$
V_{CCIN}	Primary voltage input to the voltage regulators integrated into the processor.
VSS	Processor ground
V_{CCIO_IN}	IO voltage supply input
V_{CCD}	DDR power rail
x1	Refers to a Link or Port with one Physical Lane
x4	Refers to a Link or Port with four Physical Lanes
x8	Refers to a Link or Port with eight Physical Lanes
x16	Refers to a Link or Port with sixteen Physical Lanes

1.1.4 Statement of Volatility (SOV)

The Intel® Xeon® Processor E5 v4 Product Family does not retain any end-user data when powered down and / or the processor is physically removed from the socket.

1.1.5 State of Data

The data contained within this document is final. It is the most accurate information available by the publication date of this document. Electrical DC specifications are based on estimated I/O buffer behavior.

2.0 Electrical Specifications

This chapter describes processor signaling, DC specifications, and signal quality. References to various interfaces (memory, PCIe*, Intel QPI, PECI, etc.) are also described.

2.1 Integrated Voltage Regulation

A new feature to the processor is the integration of platform voltage regulators into the processor. Due to this integration, the Intel® Xeon® Processor E5 v4 Product Family processor has one main voltage rail (V_{CCIN}) and a voltage rail for the memory interface (V_{CCD01}, V_{CCD23} - one for each memory channel pair), compared to five voltage rails (V_{CC}, V_{TTA}, V_{TTD}, V_{SA}, and V_{CCPLL}) on previous processors. The V_{CCIN} voltage rail will supply the integrated voltage regulators which in turn will regulate to the appropriate voltages for the cores, cache, and system agents. This integration allows the processor to better control on-die voltages to optimize for both performance and power savings. The processor V_{CCIN} rail will remain a sVID -based voltage with a loadline similar to the core voltage rail (called V_{CC}) in previous processors.

2.2 Processor Signaling

TheIntel® Xeon® Processor E5 v4 Product Family includes 2011 lands, which utilize various signaling technologies. Signals are grouped by electrical characteristics and buffer type into various signal groups. These include DDR4 (Reference Clock, Command, Control, and Data), PCI Express*, DMI2, Intel® QuickPath Interconnect, Platform Environmental Control Interface (PECI), System Reference Clock, SMBus, JTAG and Test Access Port (TAP), SVID Interface, Processor Asynchronous Sideband, Miscellaneous, and Power/Other signals. Refer to Table 7 on page 23 for details.

2.2.1 System Memory Interface Signal Groups

The system memory interface utilizes DDR4 technology, which consists of numerous signal groups. These include: Reference Clocks, Command Signals, Control Signals, and Data Signals. Each group consists of numerous signals, which may utilize various signaling technologies. Please refer to Table 7 on page 23 for further details. Throughout this chapter the system memory interface may be referred to as DDR4.

2.2.2 PCI Express Signals

The PCI Express Signal Group consists of PCI Express* ports 1, 2, and 3, and PCI Express miscellaneous signals. Please refer to Table 7 on page 23 for further details.

2.2.3 DMI2/PCI Express Signals

The Direct Media Interface Gen 2 (DMI2) sends and receives packets and/or commands to the PCH. The DMI2 is an extension of the standard PCI Express Specification. The DMI2/PCI Express Signals consist of DMI2 receive and transmit input/output signals and a control signal to select DMI2 or PCIe* 2.0 operation for port 0. Please refer to Table 7 on page 23 for further details.

2.2.4 Intel® QuickPath Interconnect (Intel® QPI)

The processor provides two Intel QPI ports for high speed serial transfer between other processors. Each port consists of two uni-directional links (for transmit and receive). A differential signaling scheme is utilized, which consists of opposite-polarity (DP, DN) signal pairs.

2.2.5 Platform Environmental Control Interface (PECI)

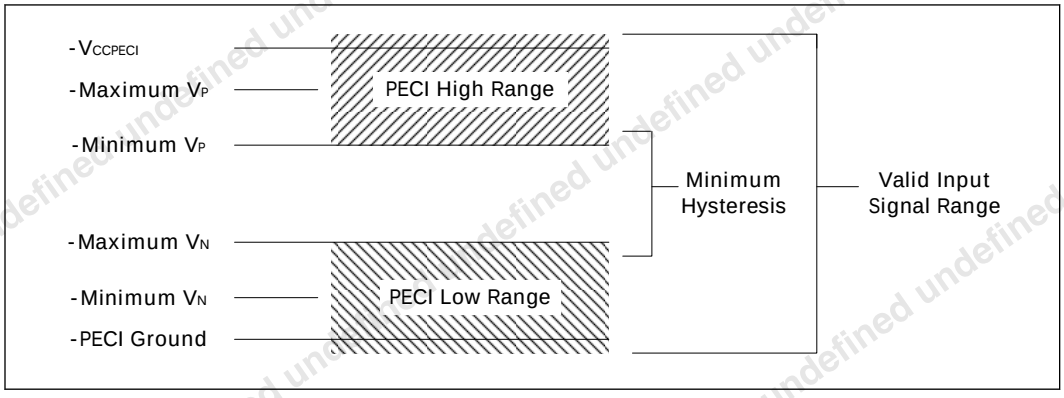
PECI is an Intel proprietary interface that provides a communication channel between Intel processors and chipset components to external system management logic and thermal monitoring devices. The processor contains a Digital Thermal Sensor (DTS) that reports a relative die temperature as an offset from Thermal Control Circuit (TCC) activation temperature. Temperature sensors located throughout the die are implemented as analog-to-digital converters calibrated at the factory. PECI provides an interface for external devices to read processor temperature, perform processor manageability functions, and manage processor interface tuning and diagnostics.

The PECI interface operates at a nominal voltage set by V_{CCPECI}. The set of DC electrical specifications shown in PECI DC Specifications on page 38 is used with devices normally operating from a V_{CCPECI} interface supply.

Input Device Hysteresis

The PECI client and host input buffers must use a Schmitt-triggered input design for improved noise immunity. Please refer to the following image and PECI DC Specifications on page 38.

Figure 1. Input Device Hysteresis



2.2.6 System Reference Clocks (BCLK{0/1}_DP, BCLK{0/1}_DN)

The processor Core, processor Uncore, Intel® QuickPath Interconnect link, PCI Express* and DDR4 memory interface frequencies) are generated from BCLK{0/1}_DP and BCLK{0/1}_DN signals. There is no direct link between core frequency and Intel QuickPath Interconnect link frequency (e.g., no core frequency to Intel QuickPath Interconnect multiplier). The processor maximum core frequency, Intel QuickPath Interconnect link frequency and DDR memory frequency are set during manufacturing. It is possible to override the processor core frequency setting using software (see the *Intel® 64 and IA-32 Architectures Software Developer's Manuals*). This permits operation at lower core frequencies than the factory set maximum core frequency.

The processor core frequency is configured during reset by using values stored within the device during manufacturing. The stored value sets the lowest core multiplier at which the particular processor can operate. If higher speeds are desired, the appropriate ratio can be configured via the IA32_PERF_CTL MSR (MSR 199h); Bits [15:0]. For details of operation at core frequencies lower than the maximum rated processor speed, refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* .

Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK{0/1}_DP, BCLK{0/1}_DN input, with exceptions for spread spectrum clocking. DC specifications for the BCLK{0/1}_DP, BCLK{0/1}_DN inputs are provided in Processor Asynchronous Sideband DC Specifications on page 42. These specifications must be met while also meeting the associated signal quality specifications outlined in Signal Quality on page 45.

2.2.7 JTAG and Test Access Port (TAP) Signals

Due to the voltage levels supported by other components in the JTAG and Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. Please refer to the *Intel® Xeon® Processor E5 v4 Product Family Boundary Scan Description Lanuguage (BSDL)* file more details. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.

2.2.8 Processor Sideband Signals

The Intel® Xeon® Processor E5 v4 Product Family includes asynchronous sideband signals that provide asynchronous input, output or I/O signals between the processor and the platform or Platform Controller Hub. Details can be found in Table 7 on page 23.

All Processor Asynchronous Sideband input signals are required to be asserted/de-asserted for a defined number of BCLKs in order for the processor to recognize the proper signal state, these are outlined in Processor Asynchronous Sideband DC Specifications on page 42 (DC specifications). Refer to Signal Quality on page 45 for applicable signal integrity specifications.

2.2.9 Power, Ground and Sense Signals

Processors also include various other signals, including power / ground and sense points. Details can be found in Table 7 on page 23.

Power and Ground Lands

All V_{CCD}, V_{CCIN}, and V_{CCIO_IN}, and V_{CCPECI} lands must be connected to their respective processor power planes, while all V_{SS} lands must be connected to the system ground plane.

For clean on-chip power distribution, processors include lands for all required voltage supplies. These are listed in the following table.

Table 3. Power and Ground Lands

Power and Ground Lands	Number of Lands	Comments
V_{CCIN}	173	Each V_{CCIN} land must be supplied with the voltage determined by the SVID Bus signals. Table 5 on page 21 defines the voltage level associated with each core SVID pattern. Table 15 on page 34 and Figure 4 on page 35 represent V_{CCIN} static and transient limits.
V_{CCD_01} V_{CCD_23}	56	Each V_{CCD} land is connected to a switchable 1.20 V supply, provide power to the processor DDR4 interface. V_{CCD} is also controlled by the SVID Bus. V_{CCD} is the generic term for V_{CCD_01} and V_{CCD_23}.
V_{CCIO_IN}	1	IO voltage supply input
V_{CCPECI}	1	Power supply for PECI.
V_{SS}	631	Ground

Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the Intel® Xeon® Processor E5 v4 Product Family is capable of generating large current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Large electrolytic bulk capacitors (CBULK), help maintain the output voltage during current transients, for example coming out of an idle condition. Care must be taken in the baseboard design to ensure that the voltages provided to the processor remain within the specifications listed in Table 13 on page 31. Failure to do so can result in timing violations or reduced lifetime of the processor.

Voltage Identification (VID)

The reference voltage or the VID setting is set via the SVID communication bus between the processor and the voltage regulator controller chip. The VID settings are the nominal voltages to be delivered to the processor's V_{CCIN} lands. Table 5 on page 21 specifies the reference voltage level corresponding to the VID value transmitted over serial VID. The VID codes will change due to temperature and/or current load changes in order to minimize the power and to maximize the performance of the part. The specifications are set so that a voltage regulator can operate with all supported frequencies.

Individual processor VID values may be calibrated during manufacturing such that two processor units with the same core frequency may have different default VID settings.

The processor uses voltage identification signals to support automatic selection of V_{CCIN} power supply voltage. If the processor socket is empty (SKTOCC_N high), or a "not supported" response is received from the SVID bus, then the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable

itself or not power on. Vout MAX register (30h) is programmed by the processor to set the maximum supported VID code and if the programmed VID code is higher than the VID supported by the VR, then VR will respond with a "not supported" acknowledgment.

SVID Commands

The processor provides the ability to operate while transitioning to a new VID setting and its associated processor voltage rail (V_{CCIN}). This is represented by a DC shift. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target voltage. Transitions above the maximum specified VID are not supported. The processor supports the following VR commands:

- SetVID_Fast (20 mV/µs)
- SetVID_Slow (5 mV/µs)
- Slew Rate Decay (downward voltage only and it's a function of the output capacitance's time constant) commands. Table 5 on page 21 includes SVID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in Table 13 on page 31.

The VRM or EVRD utilized must be capable of regulating its output to the value defined by the new VID.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

SetVID Fast Command

The SetVID_Fast command contains the target VID in the payload byte. The range of voltage is defined in the VID table. The VR should ramp to the new VID setting with a fast slew rate as defined in the slew rate data register. It is minimum of 20 mV/µs, depending on the amount of decoupling capacitance.

The SetVID_Fast command is preemptive. The VR interrupts its current processes and moves to the new VID. The SetVID_Fast command operates on 1 VR address at a time. This command is used in the processor for package C6 fast exit.

SetVID Slow

The SetVID_Slow command contains the target VID in the payload byte. The range of voltage is defined in the VID table. The VR should ramp to the new VID setting with a "slow" slew rate as defined in the slow slew rate data register. The SetVID_Slow is nominally 4x slower than the SetVID_Fast slew rate.

The SetVID_Slow command is preemptive, the VR interrupts its current processes and moves to the new VID. This is the instruction used for normal P-state voltage change. This command is used in the processor for the Intel Enhanced SpeedStep Technology transitions.

SetVID Decay

The SetVID_Decay command is the slowest of the DVID transitions. It is normally used for VID down transitions. The VR does not control the slew rate, the output voltage declines with the output load current only.

The SetVID_Decay command is preemptive, the VR interrupts its current processes and moves to the new VID. This command is used in the processor for package C6 entry, allowing capacitor discharge by the leakage, thus saving energy.This command is normally used in VID down direction in the processor package C6 entry.

SVID Power State Functions: SetPS

The processor has three power state functions and these will be set seamlessly via the SVID bus using the SetPS command. Based on the power state command, the SetPS commands sends information to VR controller to configure the VR to improve efficiency, especially at light loads. For example, typical power states are:

- PS0(00h): Represents full power or active mode
- PS1(01h): Represents a light load 5A to 20A
- PS2(02h): Represents a very light load <5A

Note: In PS2 some CPUs can have idle or leakage currents up to 20A. the MBVR must handle high idle currents if they are present even in PS2 condition.

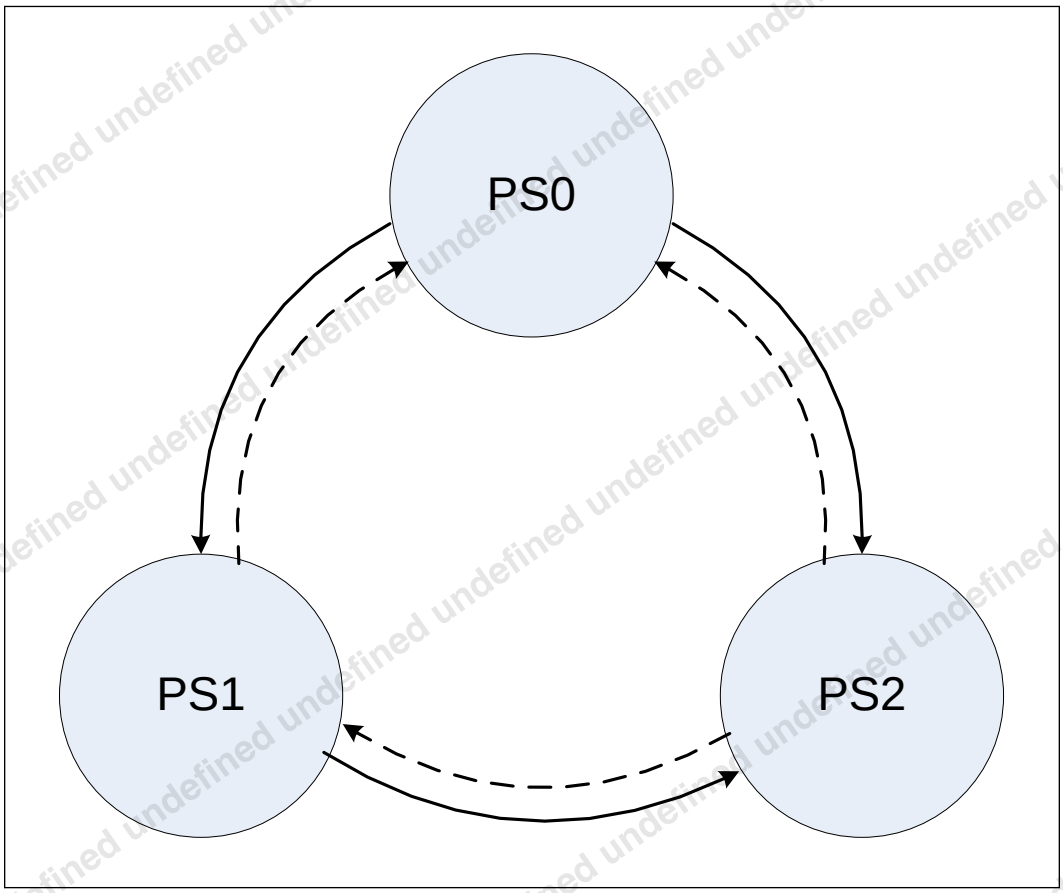
The VR may change its configuration to meet the processor's power needs with greater efficiency. For example, it may reduce the number of active phases, transition from CCM (Continuous Conduction Mode) to DCM (Discontinuous Conduction Mode) mode, reduce the switching frequency or pulse skip, or change to asynchronous regulation. For example, typical power states are 00h = run in normal mode; a command of 01h = shed phases mode, and an 02h = pulse skip.

The VR may reduce the number of active phases from PS(00h) to PS(01h) or PS(00h) to PS(02h) for example. There are multiple VR design schemes that can be used to maintain a greater efficiency in these different power states, please work with your VR controller suppliers for optimizations.

If a power state is not supported by the controller, the slave should acknowledge the SetPS command and enter the lowest power state that is supported.

If the VR is in a low power state and receives a SetVID command moving the VID up then the VR exits the low power state to normal mode (PS0) to move the voltage up as fast as possible. The processor must re-issue low power state (PS1 or PS2) command if it is in a low current condition at the new higher voltage. See the figure below for VR power state transitions.

Figure 2. VR Power State Transitions



SVID Voltage Rail Addressing

The processor addresses 3 different voltage rail control segments within VR12.5 (V_{CCIN}, V_{CCD_01}, and V_{CCD_23}). The SVID data packet contains a 4-bit addressing code:

Table 4. SVID Address Usage

PWM Address (HEX)	Intel® Xeon® Processor E5 v4 Product Family
00	V_{CCIN}
01	NA
02	V_{CCD_01}
03	+1 not used
04	V_{CCD_23}
05	+1 not used

Note:
1. Check with VR vendors for determining the physical address assignment method for their controllers.
2. VR addressing is assigned on a per voltage rail basis.
3. Dual VR controllers will have two addresses with the lowest order address, always being the higher phase count.

continued...

PWM Address (HEX)	Intel® Xeon® Processor E5 v4 Product Family
4. For future platform flexibility, the VR controller should include an address offset, as shown with +1 not used.	

Table 5. VR12.5 Reference Code Voltage Identification (VID) Table

HEX	VCCIN	HEX	VCCIN	HEX	VCCIN	HEX	VCCIN	HEX	VCCIN	HEX	VCCIN
00	0.00	55	1.34	78	1.69	9B	2.04	BE	2.39	E1	2.74
33	1.00	56	1.35	79	1.70	9C	2.05	BF	2.40	E2	2.75
34	1.01	57	1.36	7A	1.71	9D	2.06	C0	2.41	E3	2.76
35	1.02	58	1.37	7B	1.72	9E	2.07	C1	2.42	E4	2.77
36	1.03	59	1.38	7C	1.73	9F	2.08	C2	2.43	E5	2.78
37	1.04	5A	1.39	7D	1.74	A0	2.09	C3	2.44	E6	2.79
38	1.05	5B	1.40	7E	1.75	A1	2.10	C4	2.45	E7	2.80
39	1.06	5C	1.41	7F	1.76	A2	2.11	C5	2.46	E8	2.81
3A	1.07	5D	1.42	80	1.77	A3	2.12	C6	2.47	E9	2.82
3B	1.08	5E	1.43	81	1.78	A4	2.13	C7	2.48	EA	2.83
3C	1.09	5F	1.44	82	1.79	A5	2.14	C8	2.49	EB	2.84
3D	1.10	60	1.45	83	1.80	A6	2.15	C9	2.50	EC	2.85
3E	1.11	61	1.46	84	1.81	A7	2.16	CA	2.51	ED	2.86
3F	1.12	62	1.47	85	1.82	A8	2.17	CB	2.52	EE	2.87
40	1.13	63	1.48	86	1.83	A9	2.18	CC	2.53	EF	2.88
41	1.14	64	1.49	87	1.84	AA	2.19	CD	2.54	F0	2.89
42	1.15	65	1.50	88	1.85	AB	2.20	CE	2.55	F1	2.90
43	1.16	66	1.51	89	1.86	AC	2.21	CF	2.56	F2	2.91
44	1.17	67	1.52	8A	1.87	AD	2.22	D0	2.57	F3	2.92
45	1.18	68	1.53	8B	1.88	AE	2.23	D1	2.58	F4	2.93
46	1.19	69	1.54	8C	1.89	AF	2.24	D2	2.59	F5	2.94
47	1.20	6A	1.55	8D	1.90	B0	2.25	D3	2.60	F6	2.95
48	1.21	6B	1.56	8E	1.91	B1	2.26	D4	2.61	F7	2.96
49	1.22	6C	1.57	8F	1.92	B2	2.27	D5	2.62	F8	2.97
4A	1.23	6D	1.58	90	1.93	B3	2.28	D6	2.63	F9	2.98
4B	1.24	6E	1.59	91	1.94	B4	2.29	D7	2.64	FA	2.99
4C	1.25	6F	1.60	92	1.95	B5	2.30	D8	2.65	FB	3.00
4D	1.26	70	1.61	93	1.96	B6	2.31	D9	2.66	FC	3.01
4E	1.27	71	1.62	94	1.97	B7	2.32	DA	2.67	FD	3.02
4F	1.28	72	1.63	95	1.98	B8	2.33	DB	2.68	FE	3.03
50	1.29	73	1.64	96	1.99	B9	2.34	DC	2.69	FF	3.04
51	1.30	74	1.65	97	2.00	BA	2.35	DD	2.70		

continued...

HEX	VCCIN	HEX	VCCIN	HEX	VCCIN	HEX	VCCIN	HEX	VCCIN	HEX	VCCIN
52	1.31	75	1.66	98	2.01	BB	2.36	DE	2.71		
53	1.320	76	1.67	99	2.02	BC	2.37	DF	2.72		
54	1.33	77	1.68	9A	2.03	BD	2.38	E0	2.73		

Note:
1. 00h = Off State
2. VID Range HEX 01-32 are not used by the Intel® Xeon® Processor E5 v4 Product Family
3. For VID Ranges supported see Table 13 on page 31
4. V_{CCD} is a fixed voltage of 1.20V

Reserved or Unused Signals

All Reserved (RSVD) signals must not be connected. Connection of these signals to V_{CCIN}, V_{CCD}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within ± 20% of the impedance of the baseboard trace.

2.2.10 Reserved or Unused Signals

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2.3 Signal Group Summary

Signals are grouped by buffer type and similar characteristics as listed in the following table. The buffer type indicates which signaling technology and specifications apply to the signals.

Table 6. Signal Description Buffer Types

Signal	Description
Analog	Analog reference or output. May be used as a threshold voltage or for buffer compensation
Asynchronous[1]	Signal has no timing relationship with any system reference clock.
CMOS	CMOS buffers: 1.05V
DDR4	buffers: 1.2V
DMI2	Direct Media Interface Gen 2 signals. These signals are compatible with PCI Express* 2.0 and 1.0 Signaling Environment AC Specifications.
Intel® QPI	Current-mode 9.6 GT/s, 8.0 GT/s, and 6.4 GT/s, forwarded-clock Intel QuickPath Interconnect signaling
Open Drain CMOS	Open Drain CMOS (ODCMOS) buffers: 1.05V tolerant
PCI Express*	PCI Express* interface signals. These signals are compatible with PCI Express 3.0 Signalling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Refer to the PCIe specification.
Reference	Voltage reference signal.
SSTL	Source Series Terminated Logic (JEDEC SSTL_15)

Note:
1. Qualifier for a buffer type.

Table 7. Signal Groups

Differential/Single Ended	Buffer Type	Signal
DDR4 Reference Clocks		
Differential	SSTL Output	DDR{0/1/2/3}_CLK_D[N/P][3:0]
DDR4 Command Signals		
Single-ended	SSTL Output	DDR{0/1/2/3}_ACT_N DDR{0/1/2/3}_BA[1:0] DDR{0/1/2/3}_BG[1:0] DDR{0/1/2/3}_MA[17] DDR{0/1/2/3}_MA[16]/_RAS_N DDR{0/1/2/3}_MA[15]/_CAS_N DDR{0/1/2/3}_MA[14]/_WE_N DDR{0/1/2/3}_MA[13:0] DDR{0/1/2/3}_PAR
DDR4 Control Signals		
Single-ended	SSTL Output	DDR{0/1/2/3}_CS_N[9:8] DDR{0/1/2/3}CS_N[7]/CID[4] DDR{0/1/2/3}CS_N[6]/CID[3] DDR{0/1/2/3}_CS_N[5:4] DDR{0/1/2/3}CS_N[3]/CID[1] DDR{0/1/2/3}CS_N[2]/CID[0] DDR{0/1/2/3}_CS_N[1:0] DDR{0/1/2/3}_CID[2] DDR{0/1/2/3}_ODT[5:0] DDR{0/1/2/3}_CKE[5:0]

continued...

Differential/Single Ended	Buffer Type	Signal
DDR4 Data Signals		
Differential	SSTL Input/Output	DDR{0/1/2/3}_DQS_D[N/P][17:0]
Single ended	SSTL Input/Output	DDR{0/1/2/3}_DQ[63:0] DDR{0/1/2/3}_ECC[7:0]
DDR4 Miscellaneous Signals		
Single ended	SSTL Input	DDR{0/1/2/3}_ALERT_N
	CMOS Input *Note:* Input voltage from platform cannot exceed 1.08V max. Refer to PDG for implementation details.	DRAM_PWR_OK_C01 DRAM_PWR_OK_C23
	CMOS 1.2V Output	DDR_RESET_C{01/23}_N
	Open Drain CMOS Input/Output	DDR_SCL_C01 DDR_SCL_C23 DDR_SDA_C01 DDR_SDA_C23
	DC Output	DDR01_VREF DDR23_VREF
PCI Express* Port 1, 2, & 3 Signals		
Differential	PCI Express* Input	PE1A_RX_D[N/P][3:0] PE1B_RX_D[N/P][7:4] PE2A_RX_D[N/P][3:0] PE2B_RX_D[N/P][7:4] PE2C_RX_D[N/P][11:8] PE2D_RX_D[N/P][15:12] PE3A_RX_D[N/P][3:0] PE3B_RX_D[N/P][7:4] PE3C_RX_D[N/P][11:8] PE3D_RX_D[N/P][15:12]
Differential	PCI Express* Output	PE1A_TX_D[N/P][3:0] PE1B_TX_D[N/P][7:4] PE2A_TX_D[N/P][3:0] PE2B_TX_D[N/P][7:4] PE2C_TX_D[N/P][11:8] PE2D_TX_D[N/P][15:12] PE3A_TX_D[N/P][3:0] PE3B_TX_D[N/P][7:4] PE3C_TX_D[N/P][11:8] PE3D_TX_D[N/P][15:12]
PCI Express* Miscellaneous Signals		
Single ended	Open Drain CMOS Input/Output	PE_HP_SCL
		PE_HP_SDA
DMI2/PCI Express* Signals		
Differential	DMI2 Input	DMI_RX_D[N/P][3:0]
	DMI2 Output	DMI_TX_D[N/P][3:0]

continued...

Differential/Single Ended	Buffer Type	Signal
Intel® QuickPath Interconnect (Intel® QPI) Signals		
Differential	Intel® QPI Input	QPI{0/1}_DRX_D[N/P][19:0] QPI{0/1}_CLKRX_D[N/P]
	Intel® QPI Output	QPI{0/1}_DTX_D[N/P][19:0] QPI{0/1}_CLKTX_D[N/P]
Platform Environmental Control Interface (PECI)		
Single ended	PECI Input/Output	PECI
System Reference Clock (BCLK{0/1})		
Differential	CMOS 1.05V Input	BCLK{0/1}_D[N/P]
JTAG & TAP Signals		
Single ended	CMOS 1.05V Input	TCK TDI TMS TRST_N
	CMOS 1.05V Input/Output	PREQ_N
	CMOS1.05V Output	PRDY_N
	Open Drain CMOS Input/Output	BPM_N[7:0]
	Open Drain CMOS Output	TDO
Serial VID Interface (SVID) Signals		
Single ended	CMOS 1.05V Input	SVIDALERT_N
	Open Drain CMOS Input/Output	SVIDDATA
	Open Drain CMOS Output	SVIDCLK
Processor Asynchronous Sideband Signals		
Single ended	CMOS 1.05V Input	BIST_ENABLE BMCINIT DEBUG_EN_N FRMAGENT PWRGOOD PMSYNC RESET_N SAFE_MODE_BOOT SOCKET_ID[1:0] TXT_AGENT TXT_PLTEN
	CMOS 1.05V Output	FIVR_FAULT
	Open Drain CMOS Input/Output	CATERR_N MEM_HOT_C01_N MEM_HOT_C23_N MSMI_N PM_FAST_WAKE_N PROCHOT_N
	Open Drain CMOS Output	ERROR_N[2:0] THERMTRIP_N

continued...

Differential/Single Ended	Buffer Type	Signal
Miscellaneous Signals		
	CMOS 1.05V Input	EAR_N
	Output	SKTOCC_N
Power/Other Signals		
	Power / Ground	V_{CCIN}, V_{CCD_01}, V_{CCD_23}, V_{CCIO_IN}, V_{CCPECI}, V_{SS}
	Sense Points	VCCIN_SENSE VSS_VCCIN_SENSE

Note:
1. Refer to "Signal Descriptions" for signal description details.
2. DDR{0/1/2/3} refers to DDR4 Channel 0, DDR4 Channel 1, DDR4 Channel 2 and DDR4 Channel 3.

Table 8. Signals with On-Die Weak PU/PD

Signal Name	Pull Up/Pull Down	Rail	Value	Units
BIST_ENABLE	Pull Up	VCCIO_IN	5K-15K	Ω
BMCINIT	Pull Down	VSS	5K-15K	Ω
DEBUG_EN_N	Pull Up	VCCIO_IN	5K-15K	Ω
EAR_N	Pull Up	VCCIO_IN	5K-15K	Ω
FRMAGENT	Pull Down	VSS	5K-15K	Ω
PM_FAST_WAKE_N	Pull Up	VCCIO_IN	5K-15K	Ω
PREQ_N	Pull Up	VCCIO_IN	5K-15K	Ω
SAFE_MODE_BOOT	Pull Down	VSS	5K-15K	Ω
SOCKET_ID[1:0]	Pull Down	VSS	5K-15K	Ω
TCK	Pull Down	VSS	5K-15K	Ω
TDI	Pull Up	VCCIO_IN	5K-15K	Ω
TMS	Pull Up	VCCIO_IN	5K-15K	Ω
TRST_N	Pull Up	VCCIO_IN	5K-15K	Ω
TXT_AGENT	Pull Down	VSS	5K-15K	Ω
TXT_PLTEN	Pull Up	VCCIO_IN	5K-15K	Ω

2.4 Power-On Configuration (POC) Options

Several configuration options can be configured by hardware. The processor samples its hardware configuration at reset, on the active-to-inactive transition of RESET_N, or upon assertion of PWRGOOD (inactive-to-active transition). For specifics on these options, please refer to the table below.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset transition of the latching signal (RESET_N or PWRGOOD).

Table 9. Power-On Configuration Option Lands

Configuration Option	Land Name	Notes
Output tri state	PROCHOT_N	1
Execute BIST (Built-In Self Test)	BIST_ENABLE	2
Enable Service Processor Boot Mode	BMCINIT	3
Power-up Sequence Halt	EAR_N	3
Enable Intel® Trusted Execution Technology (Intel® TXT) Platform	TXT_PLTEN	3
Enable Bootable Firmware Agent	FRMAGENT	3
Enable Intel Trusted Execution Technology (Intel TXT) Agent	TXT_AGENT	3
Enable Safe Mode Boot	SAFE_MODE_BOOT	3
Configure Socket ID	SOCKET_ID[1:0]	3
Enables debug from cold boot	DEBUG_EN_N	3

Note:

1. Output tri-state option enables Fault Resilient Booting (FRB), for FRB details see the Fault Resilient Booting (FRB) Section. The signal used to latch PROCHOT_N for enabling FRB mode is RESET_N.
2. BIST_ENABLE is sampled at RESET_N de-assertion
3. This signal is sampled after PWRGOOD assertion.

2.5 Fault Resilient Booting (FRB)

The Intel® Xeon® processor E5 v4 product family supports both socket and core level Fault Resilient Booting (FRB), which provides the ability to boot the system as long as there is one processor functional in the system. One limitation to socket level FRB is that the system cannot boot if the legacy socket that connects to an active PCH becomes unavailable since this is the path to the system BIOS. See the table below for a list of output tri-state FRB signals.

Socket level FRB will tri-state processor outputs via the PROCHOT_N signal. Assertion of the PROCHOT_N signal through RESET_N de-assertion will tri-state processor outputs. Note, that individual core disabling is also supported for those cases where disabling the entire package is not desired.

The Intel® Xeon® processor E5 v4 product family extends the FRB capability to the core granularity by maintaining a register in the Uncore so that BIOS or another entity can disable one or more specific processor cores.

Table 10. Fault Resilient Booting (Output Tri-State) Signals

Output Tri-State Signal Groups	Signals
Intel QPI	QPI0_CLKTX_DN[1:0] QPI0_CLKTX_DP[1:0] QPI0_DTX_DN[19:00] QPI0_DTX_DP[19:00] QPI1_CLKTX_DN[1:0] QPI1_CLKTX_DP[1:0] QPI1_DTX_DN[19:00]

continued...

Output Tri-State Signal Groups	Signals
	QPI1_DTX_DP[19:00]
PCI Express*	PE1A_TX_DN[3:0] PE1A_TX_DP[3:0] PE1B_TX_DN[7:4] PE1B_TX_DP[7:4] PE2A_TX_DN[3:0] PE2A_TX_DP[3:0] PE2B_TX_DN[7:4] PE2B_TX_DP[7:4] PE2C_TX_DN[11:8] PE2C_TX_DP[11:8] PE2D_TX_DN[15:12] PE2D_TX_DP[15:12] PE3A_TX_DN[3:0] PE3A_TX_DP[3:0] PE3B_TX_DN[7:4] PE3B_TX_DP[7:4] PE3C_TX_DN[11:8] PE3C_TX_DP[11:8] PE3D_TX_DN[15:12] PE3D_TX_DP[15:12] PE_HP_SCL PE_HP_SDA
DMI2	DMI_TX_DN[3:0] DMI_TX_DP[3:0]
SMBus	DDR_SCL_C01 DDR_SDA_C01 DDR_SCL_C23 DDR_SDA_C23
Processor Sideband	CATERR_N ERROR_N[2:0] BPM_N[7:0] PRDY_N THERMTRIP_N PROCHOT_N PECI MEM_HOT_C01_N MEM_HOT_C23_N PM_FAST_WAKE_N FIVR_FAULT
SVID	SVIDCLK SVIDDATA

2.6 Mixing Processors

Intel supports and validates two configurations only in which all processors operate with the same Intel® QuickPath Interconnect frequency, core frequency, power segment, and have the same internal cache sizes. Mixing components operating at different internal clock frequencies is not supported and will not be validated by Intel. Combining processors from different power segments is also not supported.

Note: All processors within a system must run at a common maximum non-Turbo ratio. The system BIOS may be required to program the FLEX_RATIO register if mixed frequency processors are populated.

Not all operating systems can support dual processors with mixed frequencies. Mixing processors of different steppings but the same model (as per CPUID instruction) is supported, provided there is no more than one stepping delta between the processors, for example, S and S+1.

S and S+1 is defined as mixing of two CPU steppings in the same platform where one CPU is S (stepping) = CPUID.(EAX=01h):EAX[3:0], and the other is S+1 = CPUID.(EAX=01h):EAX[3:0]+1. The stepping ID is found in EAX[3:0] after executing the CPUID instruction with Function 01h. Details regarding the CPUID instruction are provided in the *Intel® 64 and IA-32 Architectures Software Developer's Manuals*, *Volume 2A: Instruction Set Reference, A-M*.

2.7 Flexible Motherboard Guidelines (FMB)

The Flexible Motherboard (FMB) guidelines are estimates of the maximum values the Intel® Xeon® processor E5 v4 product family will have over certain time periods. The values are only estimates and actual specifications for future processors may differ. Processors may or may not have specifications equal to the FMB value in the foreseeable future. System designers should meet the FMB values to ensure their systems will be compatible with future processors.

2.8 Absolute Maximum and Minimum Ratings

The table below specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

Although the processor contains protective circuitry to resist damage from Electro-Static Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

Table 11. Processor Absolute Minimum and Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CCIN}	Processor input voltage with respect to Vss	-0.3	1.98	V
V_{CCD}	Processor IO supply voltage for DDR4 (standard voltage) with respect to V_{SS}	-0.3	1.35	V
V_{CCIO_IN}	IO voltage supply input with respect to V_{SS}	-0.3	1.35	V
V_{CCPECI}	Power supply for PECI with respect to V_{SS}	-0.3	1.35	V
Note: 1. For functional operation, all processor electrical, signal quality, mechanical, and thermal specifications must be satisfied.				

continued...

Symbol	Parameter	Min	Max	Unit
2. Overshoot and undershoot voltage guidelines for input, output, and I/O signals are outlined in Overshoot/ Undershoot Tolerance on page 46. Excessive Overshoot or undershoot on any signal will likely result in permanent damage to the processor.				

Storage Conditions Specifications

Environmental storage condition limits define the temperature and relative humidity limits to which the device is exposed to while being stored in a Moisture Barrier Bag. The specified storage conditions are for component level prior to board attach (see notes in the table below for post board attach limits).

The table below specifies absolute maximum and minimum storage temperature limits which represent the maximum or minimum device condition beyond which damage, latent or otherwise, may occur. The table also specifies sustained storage temperature, relative humidity, and time-duration limits. These limits specify the maximum or minimum device storage conditions for a sustained period of time. At conditions outside sustained limits, but within absolute maximum and minimum ratings, quality and reliability may be affected.

Table 12. Storage Condition Ratings

Symbol	Parameter	Min	Max	Unit
$T_{absolute\ storage}$	The minimum/maximum device storage temperature beyond which damage (latent or otherwise) may occur when subjected to for any length of time.	-25	125	°C
$T_{sustained\ storage}$	The minimum/maximum device storage temperature for a sustained period of time.	-5	40	°C
$T_{short\ term\ storage}$	The ambient storage temperature (in shipping media) for a short period of time.	-20	85	°C
$RH_{sustained\ storage}$	The maximum device storage relative humidity for a sustained period of time.	60% @ 24		°C
$Time_{sustained\ storage}$	A prolonged or extended period of time; typically associated with sustained storage conditions Unopened bag, includes 6 months storage time by customer.	0	30	months
$Time_{short\ term\ storage}$	A short period of time (in shipping media).	0	72	hours

Note:

1. Storage conditions are applicable to storage environments only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
2. These ratings apply to the Intel component and do not include the tray or packaging.
3. Failure to adhere to this specification can affect the long-term reliability of the processor.
4. Non-operating storage limits post board attach: Storage condition limits for the component once attached to the application board are not specified. Intel does not conduct component level certification assessments post board attach given the multitude of attach methods, socket types and board types used by customers. Provided as general guidance only, Intel board products are specified and certified to meet the following temperature and humidity limits (Non-Operating Temperature Limit: -40C to 70C & Humidity: 50% to 90%, non condensing with a maximum wet bulb of 28°C).
5. Device storage temperature qualification methods follow JEDEC High and Low Temperature Storage Life Standards: *JESD22-A119* (low temperature) and *JESD22-A103* (high temperature).

2.9 DC Specifications

DC specifications are defined at the processor pads, unless otherwise noted. DC specifications are only valid while meeting specifications for case temperature (TCASE specified in the *Intel® Xeon® Processor E5 v4 Product Family Thermal Mechanical Specification and Design Guide*, clock frequency, and input voltages. Care should be taken to read all notes associated with each specification.

2.9.1 Voltage and Current Specifications

Table 13. Voltage Specification

Symbols	Parameter	Voltage Plane	Min	Nom	Max	Unit	Notes[1]
V_{CCIN}	Input to Integrated Voltage Regulator (Launch - FMB)	V_{CCIN}	1.47	1.82	1.85	V	2, 3, 4, 5, 8, 10, 13
V_{VID_STEP} (V_{CCIN}, V_{CCD})	VID step size during a transition			10.0		mV	6
V_{CCD} (V_{CCD_01}, V_{CCD_23})	I/O Voltage for DDR4 (Standard Voltage)	V_{CCD}	0.97*V_{CCD_NOM}	1.2	1.044*V_{CCD_NOM}	V	7, 9, 10, 11, 12

Note:

1. Unless otherwise noted, all specifications in this table apply to all processors. These specifications are based on final characterization.
2. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required.
3. The V_{CCIN} voltage specification requirements are measured across the remote sense pin pairs (V_{CCIN_SENSE} and $V_{SS\_VCCIN\_SENSE}$) on the processor package. Voltage measurement should be taken with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20MHz for older model oscilloscopes), using a 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
4. Refer to Table 15 on page 34 and corresponding Figure 4 on page 35. The processor should not be subjected to any static V_{CCIN} level that exceeds the V_{CCIN_MAX} associated with any particular current. Failure to adhere to this specification can shorten processor lifetime.
5. Minimum V_{CCIN} and maximum I_{CCIN} are specified at the maximum processor case temperature (T_{CASE}) shown in the *Intel® Xeon® Processor E5 v4 Product Family Thermal Mechanical Specification and Design Guide*. I_{CCIN_MAX} is specified at the relative V_{CC_MAX} point on the V_{CCIN} load line. The processor is capable of drawing I_{CCIN_MAX} for up to 4 ms.
6. This specification represents the V_{CCIN} reduction or V_{CCIN} increase due to each VID transition. For Voltage Identification (VID) see Voltage Identification (VID) on page 17. AC timing requirements for VID transitions are included in Figure 3 on page 32.
7. Baseboard bandwidth is limited to 20 MHz.
8. FMB is the flexible motherboard guidelines. See Flexible Motherboard Guidelines (FMB) on page 29 for details.
9. DC + AC + Ripple = Total Tolerance
10. For SVID Power State Functions (SetPS) see SVID Power State Functions: SetPS on page 19.
11. V_{CCD} tolerance at processor pins. Required in order to meet +/-5% tolerance at processor die.
12. The V_{CCD01}, V_{CCD23} voltage specification requirements are measured across vias on the platform. Choose V_{CCD01} or V_{CCD23} vias close to the socket and measure with a DC to 100MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using 1.5 pF maximum probe capacitance, and 1M ohm minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
13. V_{CCIN} has a V_{boot} setting of 1.7V and is not included in the PWRGOOD indication.

Figure 3. Serial VID Interface (SVID) Signals Clock Timings

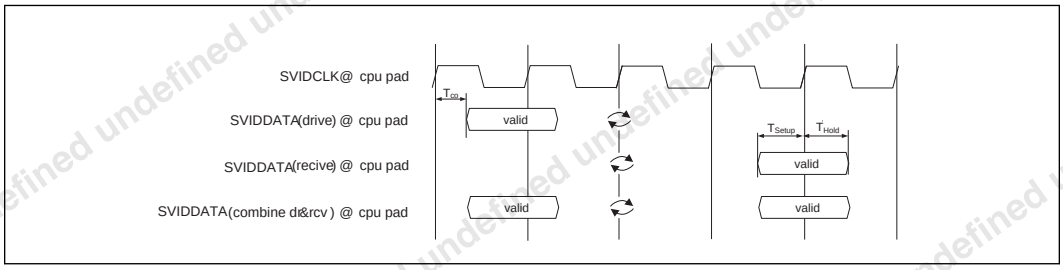


Table 14. CPU Power Rails Load Specification

Segment	TDP	ICCIN_MAX @ VCCIN(A)	ICC_MAX @ VCCIO_IN (A)	ICC_MAX @ VCCPECI (A)	ICCD01_MAX (A)[5]	ICCD23_MAX (A)[5]	ICCIN_TDC[3] @ VCCIN(A)	ICC_TDC[3] @ VCCIO_IN(A)	ICC_TDC[3] @ VCCPECI(A)	ICCD01_TDC (A)[5]	ICCD23_TDC[3] (A)[5]	Pmax[4] @ VCCIN(W)	Pmax_Package[4] (W)	Note
Segment Optimized	145W 22-Core	176	0.1	0.001	1.4 (2.45)	1.4 (2.45)	83	0.02	0.001	0.8 (2.2)	0.8 (2.2)	288	290	2, 4
	145W 18-Core	176	0.1	0.001	1.4 (2.45)	1.4 (2.45)	83	0.02	0.001	0.8 (2.2)	0.8 (2.2)	288	290	2, 4
	145W 16-Core	176	0.1	0.001	1.4 (2.45)	1.4 (2.45)	83	0.02	0.001	0.8 (2.2)	0.8 (2.2)	288	290	2, 4
	135W 20-Core	162	0.1	0.001	1.4 (2.45)	1.4 (2.45)	76	0.02	0.001	0.8 (2.2)	0.8 (2.2)	267	270	2, 4
	120W 18-Core	142	0.1	0.001	1.4 (2.45)	1.4 (2.45)	68	0.02	0.001	0.8 (2.2)	0.8 (2.2)	237	240	2, 4
	120W 16-Core	142	0.1	0.001	1.4 (2.45)	1.4 (2.45)	68	0.02	0.001	0.8 (2.2)	0.8 (2.2)	237	240	2, 4
Workstation	160W 12-Core	189	0.1	0.001	1.4 (2.45)	1.4 (2.45)	92	0.02	0.001	0.8 (2.2)	0.8 (2.2)	307	309	2, 4
	140W 8-Core	170	0.1	0.001	1.4 (2.45)	1.4 (2.45)	80	0.02	0.001	0.8 (2.2)	0.8 (2.2)	279	280	2,4
	140W 6-Core	170	0.1	0.001	1.4 (2.45)	1.4 (2.45)	80	0.02	0.001	0.8 (2.2)	0.8 (2.2)	279	280	2,4
	140W 4-Core	170	0.1	0.001	1.4 (2.45)	1.4 (2.45)	80	0.02	0.001	0.8 (2.2)	0.8 (2.2)	279	280	2,4
Frequency Optimized	135W 8-Core	162	0.1	0.001	1.4 (2.45)	1.4 (2.45)	76	0.02	0.001	0.8 (2.2)	0.8 (2.2)	267	270	2, 4
	135W 6-Core	162	0.1	0.001	1.4 (2.45)	1.4 (2.45)	76	0.02	0.001	0.8 (2.2)	0.8 (2.2)	267	270	2, 4
	135W 4-Core	162	0.1	0.001	1.4 (2.45)	1.4 (2.45)	76	0.02	0.001	0.8 (2.2)	0.8 (2.2)	267	270	2, 4
	85W 4-Core	98	0.1	0.001	1.4 (2.45)	1.4 (2.45)	47	0.02	0.001	0.8 (2.2)	0.8 (2.2)	168	170	2, 4

continued...

Segment	TDP	I_{CCIN_MAX} @ V_{CCIN}(A)	I_{CC_MAX} @ V_{CCIO_IN} (A)	I_{CC_MAX} @ V_{CCPECI} (A)	I_{CCD01_MAX} (A)[5]	I_{CCD23_MAX} (A)[5]	I_{CCIN_TDC}[3] @ V_{CCIN}(A)	I_{CC_TDC}[3] @ V_{CCIO_IN}(A)	I_{CC_TDC}[3] @ V_{CCPECI}(A)	I_{CCD01_TDC} (A)[5]	I_{CCD23_TDC}[3] (A)[5]	P_{max}[4] @ V_{CCIN}(W)	$P_{max\_Package}$[4] (W)	Note
Advanced Server	135W 14-Core	162	0.1	0.001	1.4 (2.45)	1.4 (2.45)	76	0.02	0.001	0.8 (2.2)	0.8 (2.2)	267	270	2, 4
	120W 14-Core	142	0.1	0.001	1.4 (2.45)	1.4 (2.45)	68	0.02	0.001	0.8 (2.2)	0.8 (2.2)	237	240	2, 4
	105W 12-Core	123	0.1	0.001	1.4 (2.45)	1.4 (2.45)	59	0.02	0.001	0.8 (2.2)	0.8 (2.2)	208	210	2, 4
Standard Server	90W 10-Core	104	0.1	0.001	1.4 (2.45)	1.4 (2.45)	50	0.02	0.001	0.8 (2.2)	0.8 (2.2)	178	180	2, 4
	85W 10-Core	98	0.1	0.001	1.4 (2.45)	1.4 (2.45)	47	0.02	0.001	0.8 (2.2)	0.8 (2.2)	168	170	2, 4
	85W 8-Core	98	0.1	0.001	1.4 (2.45)	1.4 (2.45)	47	0.02	0.001	0.8 (2.2)	0.8 (2.2)	168	170	2,4
Basic	85W 8-Core	98	0.1	0.001	1.4 (2.45)	1.4 (2.45)	47	0.02	0.001	0.8 (2.2)	0.8 (2.2)	168	170	2, 4
	85W 6-Core	98	0.1	0.001	1.4 (2.45)	1.4 (2.45)	47	0.02	0.001	0.8 (2.2)	0.8 (2.2)	168	170	2, 4
Low Power	65W 14-Core	73	0.1	0.001	1.4 (2.45)	1.4 (2.45)	35	0.02	0.001	0.8 (2.2)	0.8 (2.2)	127	130	2, 4
	55W 10-Core	61	0.1	0.001	1.4 (2.45)	1.4 (2.45)	30	0.02	0.001	0.8 (2.2)	0.8 (2.2)	107	210	2, 4
Embedded	120W 18-Core	142	0.1	0.001	1.4 (2.45)	1.4 (2.45)	68	0.02	0.001	0.8 (2.2)	0.8 (2.2)	237	240	2, 4
	120W 16-Core	142	0.1	0.001	1.4 (2.45)	1.4 (2.45)	68	0.02	0.001	0.8 (2.2)	0.8 (2.2)	237	240	2, 4
	120W 14-Core	142	0.1	0.001	1.4 (2.45)	1.4 (2.45)	68	0.02	0.001	0.8 (2.2)	0.8 (2.2)	237	240	2, 4
	105W 14-Core	123	0.1	0.001	1.4 (2.45)	1.4 (2.45)	59	0.02	0.001	0.8 (2.2)	0.8 (2.2)	208	210	2, 4
	105W 12-Core	123	0.1	0.001	1.4 (2.45)	1.4 (2.45)	59	0.02	0.001	0.8 (2.2)	0.8 (2.2)	208	210	2, 4
	85W 8-Core	98	0.1	0.001	1.4 (2.45)	1.4 (2.45)	47	0.02	0.001	0.8 (2.2)	0.8 (2.2)	168	170	2, 4
	75W 14-Core	86	0.1	0.001	1.4 (2.45)	1.4 (2.45)	41	0.02	0.001	0.8 (2.2)	0.8 (2.2)	149	150	2, 4
	75W 12-Core	86	0.1	0.001	1.4 (2.45)	1.4 (2.45)	41	0.02	0.001	0.8 (2.2)	0.8 (2.2)	149	150	2, 4

continued...

Segment	TDP	ICCIN_MAX @ VCCIN(A)	ICC_ MAX @ VCCIO_ IN (A)	ICC_ MAX @ VCCPECI (A)	ICCD01_ MAX (A)[5]	ICCD23_ MAX (A)[5]	ICCIN_ TDC[3] @ VCCIN(A)	ICC_ TDC[3] @ VCCIO_ IN(A)	ICC_ TDC[3] @ VCCPECI(A)	ICCD01_ TDC (A)[5]	ICCD23_ TDC[3] (A)[5]	Pmax[4] @ VCCIN(W)	Pmax_ Package[4] (W)	Note
	75W 10-Core	86	0.1	0.001	1.4 (2.45)	1.4 (2.45)	41	0.02	0.001	0.8 (2.2)	0.8 (2.2)	149	150	2, 4
	50W 8-Core	56	0.1	0.001	1.4 (2.45)	1.4 (2.45)	27	0.02	0.001	0.8 (2.2)	0.8 (2.2)	99	100	2, 4

Note:

1. Unless otherwise noted, all specifications in this table apply to all processors. These specifications are based on final characterization.
2. FMB is the flexible motherboard guidelines. See Flexible Motherboard Guidelines (FMB) on page 29 for further details.
3. I_{CCIN_TDC} (Thermal Design Current) is the sustained (DC equivalent) current that the processor is capable of drawing indefinitely and should be used for the voltage regulator thermal assessment. The voltage regulator is responsible for monitoring its temperature and asserting the necessary signal to inform the processor of a thermal excursion.
4. Minimum V_{CCIN} and maximum I_{CCIN} are specified at the maximum processor case temperature (T_{CASE}). I_{CCIN_MAX} is specified at the relative V_{CCIN_MAX} point on the V_{CCIN} load line. The processor is capable of drawing I_{CCIN_MAX} for up to 4 ms.
5. The numbers in parentheses are due to a DDR4 memory initialization load pulse occurring at system boot that may last up to 5s.

Table 15. V_{CCIN} Static and Transient Tolerance

I_{CCIN} (A)	V_{CCIN_Max} (V)	V_{CCIN_Nom} (V)	V_{CCIN_Min} (V)	Notes
0	VID + 0.022	VID - 0.000	VID - 0.022	
10	VID + 0.012	VID - 0.011	VID - 0.033	
20	VID + 0.001	VID - 0.021	VID - 0.043	
30	VID - 0.010	VID - 0.032	VID - 0.054	
40	VID - 0.020	VID - 0.042	VID - 0.064	
50	VID - 0.031	VID - 0.053	VID - 0.075	
60	VID - 0.041	VID - 0.063	VID - 0.085	
70	VID - 0.052	VID - 0.074	VID - 0.096	
80	VID - 0.062	VID - 0.084	VID - 0.106	
90	VID - 0.073	VID - 0.095	VID - 0.117	
100	VID - 0.083	VID - 0.105	VID - 0.127	
110	VID - 0.094	VID - 0.116	VID - 0.138	
120	VID - 0.104	VID - 0.126	VID - 0.148	
130	VID - 0.115	VID - 0.137	VID - 0.159	
140	VID - 0.125	VID - 0.147	VID - 0.169	
150	VID - 0.136	VID - 0.158	VID - 0.180	
160	VID - 0.146	VID - 0.168	VID - 0.190	
170	VID - 0.157	VID - 0.179	VID - 0.201	
180	VID - 0.167	VID - 0.189	VID - 0.211	
190	VID - 0.178	VID - 0.200	VID - 0.222	

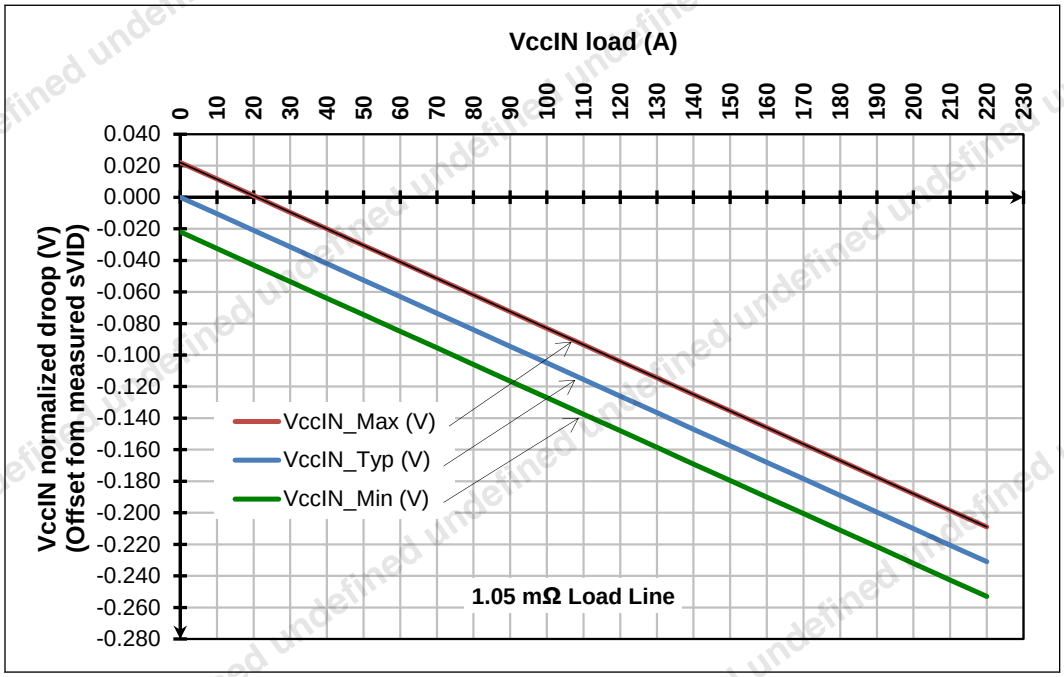
continued...

I_{CCIN} (A)	V_{CCIN_Max} (V)	V_{CCIN_Nom} (V)	V_{CCIN_Min} (V)	Notes
200	VID - 0.188	VID - 0.210	VID - 0.232	
210	VID - 0.199	VID - 0.221	VID - 0.243	
220	VID - 0.209	VID - 0.231	VID - 0.253	

Note:

1. The V_{CCIN_MIN} and V_{CCIN_MAX} loadlines represent static and transient limits. Please see Die Voltage Validation on page 35 for V_{CCIN} Overshoot specifications.
2. This table is intended to aid in reading discrete points on graph in Figure 4 on page 35.
3. The loadlines specify voltage limits at the die measured at the V_{CCIN_SENSE} and $V_{SS\_VCCIN\_SENSE}$ lands. Voltage regulation feedback for voltage regulator circuits must also be taken from processor V_{CCIN_SENSE} and $V_{SS\_VCCIN\_SENSE}$ lands.
4. The Adaptive Loadline Positioning slope is 1.05 mΩ (mohm) with +/- 22mV TOB (Tolerance of Band).
5. Processor current (I_{CCIN}) ranges are valid up to I_{CCIN_MAX} of the processor SKU as defined in the previous table above.

Figure 4. V_{CCIN} Static and Transient Tolerance Loadlines



2.9.2 Die Voltage Validation

Overshoot events at the processor must meet the specifications in Table 16 on page 36 when measured across the V_{CCIN_SENSE} and $V_{SS\_VCCIN\_SENSE}$ lands. Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

V_{CCIN} Overshoot Specifications

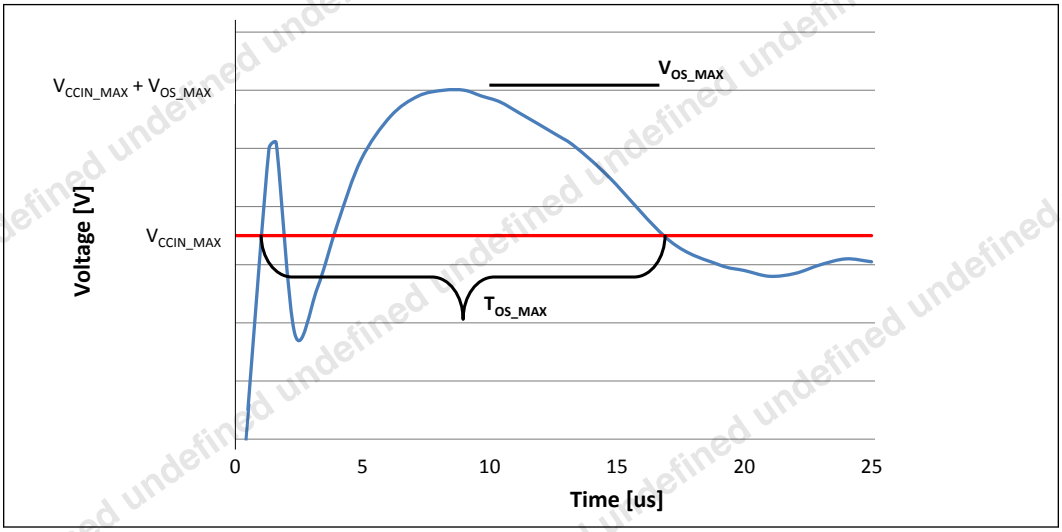
The Intel® Xeon® Processor E5 v4 Product Family can tolerate short transient overshoot events where V_{CCIN} exceeds the VID voltage when transitioning from a high-to-low current load condition. This overshoot cannot exceed VID + V_{OS_MAX}

(V_{OS_MAX} is the maximum allowable overshoot above VID). These specifications apply to the processor die voltage as measured across the V_{CCIN_SENSE} and $V_{SS\_VCCIN\_SENSE}$ lands.

Table 16. V_{CCIN} Overshoot Specifications

Symbol	Parameter	Min	Max	Units	Figure	Notes
V_{OS_MAX}	Magnitude of V_{CCIN} overshoot above VID		50	mV	Figure 5 on page 36	
T_{OS_MAX}	Time duration of V_{CCIN} overshoot above V_{CCIN_Max} value at the new lighter load		25	µs	Figure 5 on page 36	

Figure 5. V_{CCIN} Overshoot Example Waveform



Note:

1. V_{OS_MAX} is the measured overshoot voltage above V_{CCIN_MAX}.
2. T_{OS_MAX} is the measured time duration above V_{CCIN_MAX}.
3. V_{CCIN_MAX} = VID + TOB

2.9.3 Signal DC Specifications

For additional specifications, refer to Related Publications on page 9.

2.9.3.1 DDR4 Signal DC Specifications

Symbol	Parameter	Min	Nom	Max	Units	Notes[1]
I_{IL}	Input Leakage Current	-1.4		+1.4	mA	9
Data Signals						
R_{ON}	DDR4 Data Buffer On Resistance	27		33	ohm	6
Data ODT	On-Die Termination for Data Signals	45		55	ohm	8

continued...

Symbol	Parameter	Min	Nom	Max	Units	Notes[1]
Reference Clock and Command Signals						
V_{OL}	Output Low Voltage		$(V_{CCD} / 2)* (R_{ON} / (R_{ON} + R_{VTT\_TERM}))$		V	2, 7
V_{OH}	Output High Voltage		$V_{CCD} - ((V_{CCD} / 2)* (R_{ON} / (R_{ON} + R_{VTT\_TERM}))$		V	2, 5, 7
Data Signals						
V_{OL}	Output Low Voltage		Varies			10
V_{OH}	Output High Voltage		V_{CCD}			
Reference Clock Signal						
R_{ON}	DDR4 Clock Buffer On Resistance	27		33	ohm	6
Command Signals						
R_{ON}	DDR4 Command Buffer On Resistance	16		20	ohm	6
R_{ON}	DDR4 Reset Buffer On Resistance		78		ohm	6
$V_{OL\_CMOS1.2V}$	Output Low Voltage, Signals DDR_RESET_ C{01/23}_N			$0.2*V_{CCD}$	V	1, 2
$V_{OH\_CMOS1.2V}$	Output High Voltage, Signals DDR_RESET_ C{01/23}_N	$0.9*V_{CCD}$			V	1, 2
Control Signals						
R_{ON}	DDR4 Control Buffer On Resistance	27		33	ohm	6
DDR4 Miscellaneous Signals						
ALERT_N	On-Die Termination for Parity Error Signals	81	90	99	ohm	

continued...

Symbol	Parameter	Min	Nom	Max	Units	Notes[1]
V_{IL}	Input Low Voltage DRAM_PWR_OK_C{01/23}			304	mV	2, 3
V_{IH}	Input High Voltage DRAM_PWR_OK_C{01/23}	800			mV	2, 4, 5

Note:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The voltage rail V_{CCD} which will be set to 1.2V nominal depending on the voltage of all DIMMs connected to the processor.
3. V_{IL} is the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
4. V_{IH} is the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
5. V_{IH} and V_{OH} may experience excursions above V_{CCD}. However, input signal drivers must comply with the signal quality specifications. Refer to Signal Quality on page 45.
6. This is the pull down driver resistance. Reset drive does not have a termination.
7. R_{VTT_TERM} is the termination on the DIMM and not controlled by the processor. Refer to the applicable DIMM datasheet.
8. The minimum and maximum values for these signals are programmable by BIOS to one of the pairs.
9. Input leakage current is specified for all DDR4 signals.
10. Vol = Ron * [VCCD/(Ron + Rtt_Eff)], where Rtt_Eff is the effective pull-up resistance of all DIMMs in the system, including ODTs and series resistors on the DIMMs.

2.9.3.2 PECI DC Specifications

Symbol	Definition and Conditions	Min	Max	Units	Figure	Notes[1]
V_{In}	Input Voltage Range	-0.150	V_{CCPECI} + 0.150	V		
$V_{Hysteresis}$	Hysteresis	0.100 * V_{CCPECI}		V		
V_N	Negative-edge threshold voltage	0.275 * V_{CCPECI}	0.500 * V_{CCPECI}	V	Figure 1 on page 15	2
V_P	Positive-edge threshold voltage	0.550 * V_{CCPECI}	0.725 * V_{CCPECI}	V	Figure 1 on page 15	2
I_{Source}	Pullup Resistance (V_{OH} = 0.75 * V_{CCPECI})	-6.00		mA		
I_{Leak+}	High impedance state leakage to V_{CCIO_IN} (V_{leak} = V_{OL})	50	200	µA		
R_{ON}	High impedance leakage to GND (V_{leak} = V_{OH})	20	36	Ω		
C_{Bus}	Bus capacitance per node	N/A	10	pF		4, 5
V_{Noise}	Signal noise immunity above 300 MHz	0.100 * V_{CCPECI}	N/A	V_{p-p}		
	Output Edge Rate (50 ohm to V_{SS}, between V_{IL} and V_{IH})	1.5	4	V/ns		

Note:

1. V_{CCPECI} supplies the PECI interface. PECI behavior does not affect V_{CCPECI} min/max specification.

continued...

Symbol	Definition and Conditions	Min	Max	Units	Figure	Notes[1]

2. It is expected that the PECI driver will take into account, the variance in the receiver input thresholds and consequently, be able to drive its output within safe limits (-0.150 V to 0.275*V_{CCPECI} for the low level and 0.725*V_{CCPEC} to V_{CCPECI}+0.150 V for the high level).
3. The leakage specification applies to powered devices on the PECI bus.
4. One node is counted for each client and one node for the system host. Extended trace lengths might appear as additional nodes.
5. Excessive capacitive loading on the PECI line may slow down the signal rise/fall times and consequently limit the maximum bit rate at which the interface can operate.

2.9.3.3 System Reference Clock (BCLK{0/1}) DC Specifications

Symbol	Parameter	Signal	Min	Max	Unit	Figure	Notes[1]
$V_{BCLK\_diff\_ih}$	Differential Input High Voltage	Differential	0.150	N/A	V	Figure 6 on page 40	9
$V_{BCLK\_diff\_il}$	Differential Input Low Voltage	Differential		-0.150	V	Figure 6 on page 40	9
V_{cross} (abs)	Absolute Crossing Point	Single Ended	0.250	0.550	V	Figure 7 on page 40 Figure 8 on page 40	2, 4, 7, 9
V_{cross} (rel)	Relative Crossing Point	Single Ended	0.250 + 0.5*(VH$_{avg}$ - 0.700)	0.550 + 0.5*(VH$_{avg}$ - 0.700)	V	Figure 7 on page 40	3, 4, 5, 9
ΔV_{cross}	Range of Crossing Points	Single Ended	N/A	0.140	V	Figure 9 on page 41	6, 9
V_{TH}	Threshold Voltage	Single Ended	Vcross - 0.1	Vcross + 0.1	V		9
I_{IL}	Input Leakage Current	N/A		1.50	mA		8, 9
C_{pad}	Pad Capacitance	N/A	1.12	1.7	pF		9

Note:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as the instantaneous voltage value when the rising edge of BCLK{0/1}_DN is equal to the falling edge of BCLK{0/1}_DP.
3. V_{Havg} is the statistical average of the VH measured by the oscilloscope.
4. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
5. V_{Havg} can be measured directly using "Vtop" on Agilent* and "High" on Tektronix oscilloscopes.
6. V_{CROSS} is defined as the total variation of all crossing voltages as defined in Note 3.
7. The rising edge of BCLK{0/1}_DN is equal to the falling edge of BCLK{0/1}_DP.
8. For Vin between 0 and Vih.
9. Specifications can be validated at the pin.

Figure 6. BCLK{0/1} Differential Clock Measurement Point for Ringback

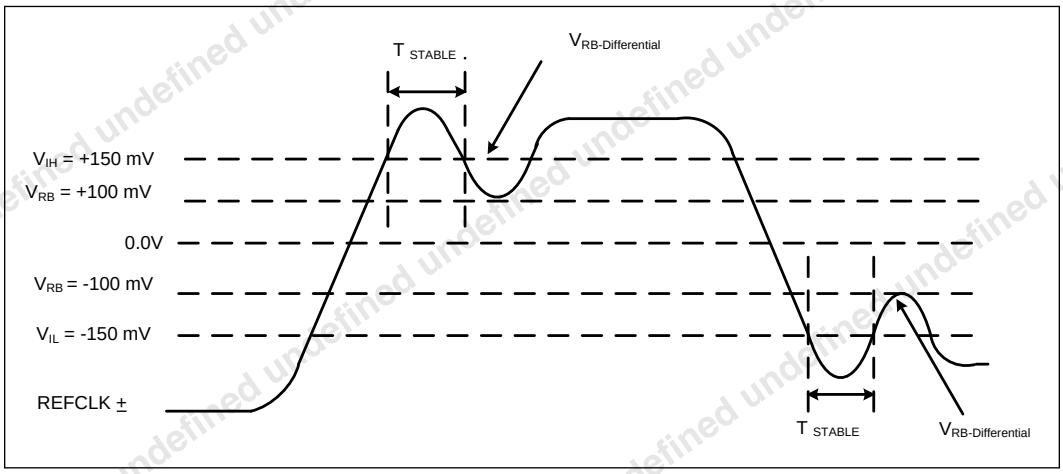


Figure 7. BCLK{0/1} Differential Clock Crosspoint Specification

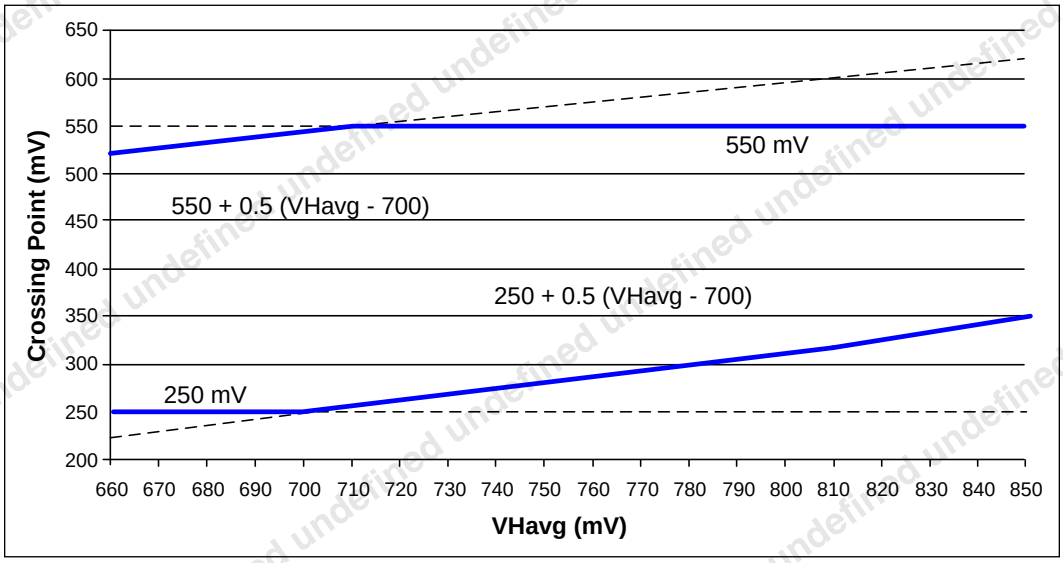


Figure 8. BCLK{0/1} Single Ended Clock Measurement Points for Absolute Cross Point and Swing

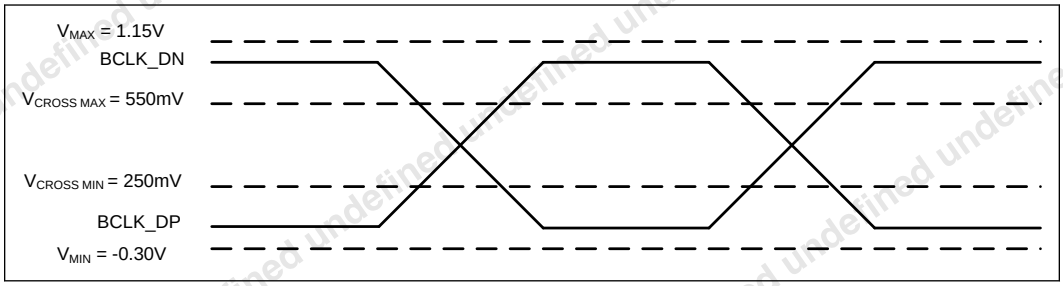
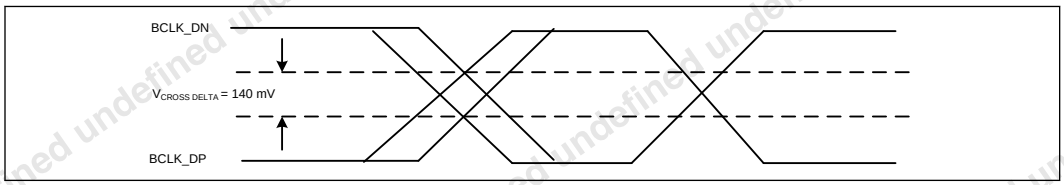


Figure 9. BCLK{0/1} Single Ended Clock Measure Points for Delta Cross Point



2.9.3.4 SMBus DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.3*V_{CCIO_IN}	V	
V_{IH}	Input High Voltage	0.7*V_{CCIO_IN}		V	
$V_{Hysteresis}$	Hysteresis	0.1*V_{CCIO_IN}		V	
V_{OL}	Output Low Voltage		0.2*V_{CCIO_IN}	V	
R_{ON}	Buffer On Resistance	4	14	Ω	
I_L	Leakage Current Signals	50	200	µA	
	Output Edge Rate (50 ohm to V_{CCIO_IN}, between V_{IL} and V_{IH})	0.05	0.6	V/ns	1

Note:
1. Value obtained through test bench with 50Ω pull up to V_{CCIO_IN}.

2.9.3.5 JTAG and TAP Signals DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.4*V_{CCIO_IN}	V	
V_{IH}	Input High Voltage	0.8*V_{CCIO_IN}		V	
V_{IL}	Input Low Voltage: TCK		0.4*V_{CCIO_IN}	V	
V_{IH}	Input High Voltage: TCK	0.6*V_{CCIO_IN}		V	
V_{OL}	Output Low Voltage		0.2*V_{CCIO_IN}	V	
$V_{Hysteresis}$	Hysteresis	0.1*V_{CCIO_IN}			
R_{ON}	Buffer On Resistance Signals BPM_N[7:0], TDO	4	14	Ω	
I_{IL}	Input Leakage Current Signals	50	200	µA	
	Output Edge Rate (50 ohm to V_{CCIO_IN}) Signal: BPM_N[7:0], PRDY_N, TDO	0.2	1.5	V/ns	1

Note:
1. These are measured between V_{IL} and V_{IH}.
2. The signal edge rate must be met or the signal must transition monotonically to the asserted state.

2.9.3.6 Serial VID Interface (SVID) DC Specifications

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{CCIO_IN}	CPU I/O Voltage	V_{CCIO_IN} - 5%	0.95	V_{CCIO_IN} + 5%	V	1
V_{IL}	Input Low Voltage Signals SVIDDATA, SVIDALERT_N			$0.4*V_{CCIO\_IN}$	V	1
V_{IH}	Input High Voltage Signals SVIDDATA, SVIDALERT_N	$0.7*V_{CCIO\_IN}$			V	1
V_{OL}	Output Low Voltage Signals: SVIDCLK, SVIDDATA			$0.2*V_{CCIO\_IN}$	V	1, 5
$V_{Hysteresis}$	Hysteresis	$0.05*V_{CCIO\_IN}$			V	1
R_{ON}	Buffer On Resistance Signals SVIDCLK, SVIDDATA	4		14	Ω	2
I_{IL}	Input Leakage Current	50		200	µA	3
	Input Edge Rate Signal: SVIDALERT_N	0.05			V/ns	4
	Output Edge Rate	0.20		1.5	V/ns	4, 5

Note:
1. V_{CCIO_IN} refers to instantaneous V_{CCIO_IN}.
2. Measured at $0.31*V_{CCIO\_IN}$.
3. Vin between 0V and V_{CCIO_IN} (applies to SVIDDATA and SVIDALERT_N only).
4. These are measured between V_{IL} and V_{IH}.
5. Value obtained through test bench with 50Ω pull up to V_{CCIO_IN}.

2.9.3.7 Processor Asynchronous Sideband DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
CMOS1.05v Signals					
$V_{IL\_CMOS1.05V}$	Input Low Voltage		$0.4*V_{CCIO\_IN}$	V	1, 2
$V_{IH\_CMOS1.05V}$	Input High Voltage	$0.6*V_{CCIO\_IN}$		V	1, 2
$I_{IL\_CMOS1.05V}$	Input Leakage Current	50	200	µA	1,2
Open Drain CMOS (ODCMOS) Signals					
V_{IL_ODCMOS}	Input Low Voltage Signals: CATERR_N, MSMI_N, PM_FAST_WAKE_N		$0.4*V_{CCIO\_IN}$	V	1, 2
V_{IL_ODCMOS}	Input Low Voltage Signals: MEM_HOT_C01/23_N, PROCHOT_N		$0.3*V_{CCIO\_IN}$	V	1, 2
V_{IH_ODCMOS}	Input High Voltage	$0.7*V_{CCIO\_IN}$		V	1, 2
V_{OL_ODCMOS}	Output Low Voltage		$0.2*V_{CCIO\_IN}$	V	1, 2
$V_{Hysteresis}$	Hysteresis Signals: MEM_HOT_C01/23_N, PROCHOT_N	$0.1*V_{CCIO\_IN}$			
$V_{Hysteresis}$	Hysteresis Signal: CATERR_N, MSMI_N, PM_FAST_WAKE_N	$0.05*V_{CCIO\_IN}$			
I_L	Input Leakage Current	50	200	µA	
R_{ON}	Buffer On Resistance	4	14	Ω	1, 2

continued...

Symbol	Parameter	Min	Max	Units	Notes
	Output Edge Rate Signal: MEM_HOT_C{01/23}_ N, ERROR_N[2:0], THERMTRIP, PROCHOT_N	0.05	0.60	V/ns	3
	Output Edge Rate Signal: CATERR_N, MSMI_N, PM_FAST_WAKE_N	0.2	1.5	V/ns	3

Note:
1. This table applies to the processor sideband and miscellaneous signals specified in Table 7 on page 23.
2. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
3. These are measured between V_{IL} and V_{IH}.

2.9.3.8 Miscellaneous Signals DC Specifications

Symbol	Parameter	Min	Nominal	Max	Units
SKTOCC_N Signal					
$V_{O\_ABS\_MAX}$	Output Absolute Max Voltage		3.30	3.50	V
I_{OMAX}	Output Max Current			1	mA

2.10 Package C-State Power Specifications

The following table lists the processor package C-state power specifications for the various processor SKUs.

Segment	Model Number	TDP	C1E (W) [2]	C3 (W) [2]	C6 (W)
Segment Optimized	E5-2699 v4	145W 22-Core	55	35	14
	E5-2698 v4	135W 20-Core	47	34	14
	E5-2697 v4	145W 18-Core	46	33	14
	E5-2695 v4	120W 18-Core	46	33	14
	E5-2697A v4	145W 16-Core	45	32	14
	E5-2683 v4	120W 16-Core	45	32	14
	E5-2699 v3	145W 18-Core	56	36	14
	E5-2698 v3	135W 16-Core	47	33	14
	E5-2697 v3	145W 14-Core	45	34	14
	E5-2695 v3	120W 14-Core	46	34	14
	E5-2683 v3	120W 14-Core	55	38	20
Workstation	E5-2687W v4	160W 12-Core	41	31	13
	E5-2687 v3	160W 10-Core	41	31	13
	E5-1680 v3	140W 8-Core	34	25	12
	E5-1660 v3	140W 8-Core	34	25	12
	E5-1650 v3	140W 6-Core	30	22	12
	E5-1630 v3	140W 4-Core	26	20	12
	E5-1620 v3	140W 4-Core	26	20	12

continued...

Segment	Model Number	TDP	C1E (W) [2]	C3 (W) [2]	C6 (W)
Frequency Optimized	E5-2667 v4	135W 8-Core	35	25	12
	E5-2643 v4	135W 6-Core	35	25	12
	E5-2637 v4	135W 4-Core	35	25	12
	E5-2623 v4	85W 4-Core	35	25	12
	E5-2667 v3	135W 8-Core	32	26	12
	E5-2643 v3	135W 6-Core	32	26	12
	E5-2637 v3	135W 4-Core	30	25	12
	E5-2623 v3	105W 4-Core	33	26	12
Advanced Server	E5-2690 v4	135W 14-Core	42	32	13
	E5-2680 v4	120W 14-Core	42	32	13
	E5-2660 v4	105W 14-Core	42	32	13
	E5-2650 v4	105W 12Core	41	31	13
	E5-2690 v3	135W 12-Core	38	30	13
	E5-2680 v3	120W 12-Core	44	33	13
	E5-2670 v3	120W 12-Core	44	33	13
	E5-2660 v3	105W 10-Core	38	30	13
	E5-2650 v3	105W 10-Core	43	33	13
Standard Server	E5-2640 v4	90W 10-Core	35	25	12
	E5-2630 v4	85W 10-Core	35	25	12
	E5-2620 v4	85W 8-Core	35	25	12
	E5-2640 v3	90W 8-Core	33	25	12
	E5-2630 v3	85W 8-Core	34	26	12
	E5-2620 v3	85W 6-Core	36	28	12
Basic	E5-2609 v4	85W 8-Core	35	25	12
	E5-2603 v4	85W 6-Core	35	25	12
	E5-2609 v3	85W 6-Core	28	24	20
	E5-2603 v3	85W 6-Core	28	24	20
Low Power	E5-2650L v4	65W 14-Core	37	27	13
	E5-2630L v4	55W 10-Core	35	25	12
	E5-2650L v3	65W 12-Core	38	38	13
	E5-2630L v3	55W 8-Core	27	23	13
Embedded	E5-2663 v3	120W 10-Core	34	28	13
	E5-2658 v3	105W 12-Core	39	30	13
	E5-2628 v3	85W 8-Core	33	25	12
	E5-2648L v3	75W 12-Core	36	28	13
	E5-2628L v3	75W 10-Core	33	27	13

continued...

Segment	Model Number	TDP	C1E (W) [2]	C3 (W) [2]	C6 (W)
	E5-2618L v3	75W 8-Core	29	24	12
	E5-2608L v3	52W 6-Core	26	22	12

Notes: 1. Package C6 power specified at Tcase = 50°C.
2. Characterized but not tested.

2.11 Signal Quality

Data transfer requires the clean reception of data signals and clock signals. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swings will adversely affect system timings. Ringback and signal non-monotonicity cannot be tolerated since these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and can cause device failure if absolute voltage limits are exceeded. Overshoot and undershoot can also cause timing degradation due to the build up of inter-symbol interference (ISI) effects.

For these reasons, it is crucial that the designer work towards a solution that provides acceptable signal quality across all systematic variations encountered in volume manufacturing.

This section documents signal quality metrics used to derive topology and routing guidelines through simulation. All specifications are specified at the processor die (pad measurements).

Specifications for signal quality are for measurements at the processor core only and are only observable through simulation. Therefore, proper simulation is the only way to verify proper timing and signal quality.

2.11.1 DDR Signal Quality Specifications

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below VSS. The overshoot/undershoot specifications limit transitions beyond specified maximum voltages or VSS due to the fast signal edge rates. The processor can be damaged by single and/or repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (i.e., if the over/undershoot is great enough). Baseboard designs which meet signal integrity and timing requirements and which do not exceed the maximum overshoot or undershoot limits listed in Table 17 on page 46 will ensure reliable IO performance for the lifetime of the processor.

2.11.2 I/O Signal Quality Specifications

Signal Quality specifications for PCIe* Signals are included as part of the PCIe DC specifications.

2.11.3 Input Reference Clock Signal Quality Specifications

Overshoot/Undershoot and Ringback specifications for BCLK{0/1}_D[N/P] are found in Table 17 on page 46. Overshoot/Undershoot and Ringback specifications for the DDR4 Reference Clocks are specified by the DIMM.

2.11.4 Overshoot/Undershoot Tolerance

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below VSS, see Figure 10 on page 47. The overshoot/undershoot specifications limit transitions beyond VCCD or VSS due to the fast signal edge rates. The processor can be damaged by single and/or repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (i.e., if the over/undershoot is great enough). Baseboard designs which meet signal integrity and timing requirements and which do not exceed the maximum overshoot or undershoot limits listed in the following table will insure reliable IO performance for the lifetime of the processor.

Table 17. Processor I/O Overshoot/Undershoot Specifications

Signal Group	Maximum Undershoot	Maximum Overshoot	Overshoot Duration	Undershoot Duration	Notes
Intel QuickPath Interconnect	-0.2 * V_{CCIO_IN}	1.2 * V_{CCIO_IN}	39 ps	15 ps	1, 2
DDR4	-0.22*V_{CCD}	1.22*V_{CCD}	0.25*T_{CH}	0.1*T_{CH}	1, 2, 3
Processor Asynchronous Sideband Signals	-0.35 * V_{CCIO_IN}	1.35 * V_{CCIO_IN}	1.25 ns	0.5 ns	1, 2
System Reference Clock (BCLK{0/1})	-0.3V	1.15V	N/A	N/A	1, 2
PWRGOOD Signal	-0.420V	V_{CCIO_IN} + 0.28	1.25 ns	0.5 ns	3

Notes:
1. These specifications are measured at the processor pad.
2. Refer to Figure 10 on page 47 for description of allowable Overshoot/Undershoot magnitude and duration.
3. T_{CH} is the minimum high pulse width duration.
4. For PWRGOOD DC specifications see Processor Asynchronous Sideband DC Specifications on page 42.

Overshoot/Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level. For the processor, both are referenced to VSS. It is important to note that the overshoot and undershoot conditions are separate and their impact must be determined independently.

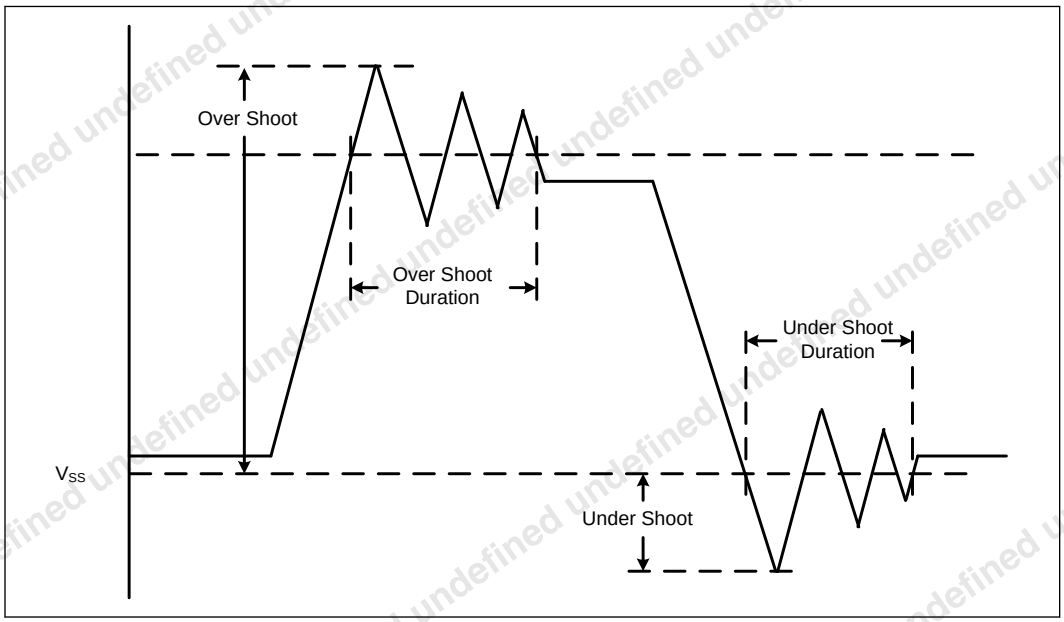
The pulse magnitude and duration must be used to determine if the overshoot/ undershoot pulse is within specifications.

Overshoot/Undershoot Pulse Duration

Pulse duration describes the total amount of time that an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage. The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

Note: Oscillations below the reference voltage cannot be subtracted from the total overshoot/undershoot pulse duration.

Figure 10. Maximum Acceptable Overshoot/Undershoot Waveform



Activity Factor

Activity factor (AF) describes the frequency of overshoot (or undershoot) occurrence relative to a clock. Since the highest frequency of assertion of any common clock signal is every other clock, an AF = 0.1 indicates that the specific overshoot (or undershoot) waveform occurs every other clock cycle.

The specification provided in the table shows the maximum pulse duration allowed for a given overshoot/undershoot magnitude at a specific activity factor. Each table entry is independent of all others, meaning that the pulse duration reflects the existence of overshoot/undershoot events of that magnitude ONLY. A platform with an overshoot/undershoot that just meets the pulse duration for a specific magnitude where the AF < 0.1, means that there can be no other overshoot/undershoot events, even of lesser magnitude (note that if AF = 0.1, then the event occurs at all times and no other events can occur).

Reading Overshoot/Undershoot Specification Tables

The overshoot/undershoot specification for the processor is not a simple single value. Instead, many factors are needed to determine the over/undershoot specification. In addition to the magnitude of the overshoot, the following parameters must also be known: the width of the overshoot and the activity factor (AF). To determine the allowed overshoot for a particular overshoot event, the following must be done:

1. Determine the signal group a particular signal falls into.
2. Determine the magnitude of the overshoot or the undershoot (relative to VSS).
3. Determine the activity factor (How often does this overshoot occur?).
4. Next, from the appropriate specification table, determine the maximum pulse duration (in nanoseconds) allowed.

5. Compare the specified maximum pulse duration to the signal being measured. If the pulse duration measured is less than the pulse duration shown in the table, then the signal meets the specifications.

Undershoot events must be analyzed separately from overshoot events as they are mutually exclusive.

Determining if a System Meets the Overshoot/Undershoot Specifications

The overshoot/undershoot specifications listed in the table specify the allowable overshoot/undershoot for a single overshoot/undershoot event. However most systems will have multiple overshoot and/or undershoot events that each have their own set of parameters (duration, AF and magnitude). While each overshoot on its own may meet the overshoot specification, when you add the total impact of all overshoot events, the system may fail. A guideline to ensure a system passes the overshoot and undershoot specifications is shown below.

1. If only one overshoot/undershoot event magnitude occurs, ensure it meets the over/undershoot specifications in the following tables, OR
2. If multiple overshoots and/or multiple undershoots occur, measure the worst case pulse duration for each magnitude and compare the results against the AF = 0.1 specifications. If all of these worst case overshoot or undershoot events meet the specifications (measured time < specifications) in the table (where AF= 0.1), then the system passes.

Table 18. Processor Sideband Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF=0.1	Pulse Duration (ns) AF=0.01
1.3335 V	0.2835 V	3 ns	5 ns
1.2600 V	0.210 V	5 ns	5 ns

3.0 Processor Land Listing

Refer to Appendix A in this document.

4.0 Signal Descriptions

This chapter describes theIntel® Xeon® Processor E5 v4 Product Family signals. They are arranged in functional groups according to their associated interface or category.

4.1 System Memory Interface

Table 19. Memory Channel DDR0, DDR1, DDR2, DDR3

Signal Name	Description
DDR{0/1/2/3}_ACT_N	Activate. When asserted, indicates MA[16:14] are command signals (RAS_N, CAS_N, WE_N).
DDR{0/1/2/3}_ALERT_N	Parity Error detected by the DIMM (one for each channel).
DDR{0/1/2/3}_BA[1:0]	Bank Address. Defines which bank is the destination for the current Activate, Read, Write, or Precharge command.
DDR{0/1/2/3}_BG[1:0]	Bank Group: Defines which bank group is the destination for the current Active, Read, Write or Precharge command. BG0 also determines which mode register is to be accessed during a MRS cycle.
DDR{0/1/2/3}_CAS_N	Column Address Strobe. MUXed with DDR{0/1/2/3}_MA[15].
DDR{0/1/2/3}_CID[4:0]	Chip ID. Used to select a single die out of the stack of a 3DS device. CID[4:3] are MUXed with CS_N[7:6], respectively. CID[1:0] are MUXed with CS_N[3:2], respectively.
DDR{0/1/2/3}_CKE[5:0]	Clock Enable.
DDR{0/1/2/3}_CLK_DN[3:0] DDR{0/1/2/3}_CLK_DP[3:0]	Differential clocks to the DIMM. All command and control signals are valid on the rising edge of clock.
DDR{0/1/2/3}_CS_N[9:0]	Chip Select. Each signal selects one rank as the target of the command and address. CS_N[7:6] are MUXed with CID[4:3], respectively. CS_N[3:2] are MUXed with CID[1:0], respectively.
DDR{0/1/2/3}_DQ[63:0]	Data Bus. DDR4 Data bits.
DDR{0/1/2/3}_DQS_DP[17:0] DDR{0/1/2/3}_DQS_DN[17:0]	Data strobes. Differential pair, Data/ECC Strobe. Differential strobes latch data/ECC for each DRAM. Different numbers of strobes are used depending on whether the connected DRAMs are x4,x8. Driven with edges in center of data, receive edges are aligned with data edges.
DDR{0/1/2/3}_ECC[7:0]	Check bits. An error correction code is driven along with data on these lines for DIMMs that support that capability
DDR{0/1/2/3}_MA[17:0]	Memory Address. Selects the Row address for Reads and writes, and the column address for activates. Also used to set values for DRAM configuration registers. MA[16], MA[15], and MA[14] are MUXed with RAS_N, CAS_N, and WE_N, respectively.
DDR{0/1/2/3}_PAR	Even parity across Address and Command.

continued...

Signal Name	Description
DDR{0/1/2/3}_ODT[5:0]	On Die Termination. Enables DRAM on die termination during Data Write or Data Read transactions.
DDR{0/1/2/3}_RAS_N	Row Address Strobe. MUXed with DDR{0/1/2/3}_MA[16].
DDR{0/1/2/3}_WE_N	Write Enable. MUXed with DDR{0/1/2/3}_MA[14].

Table 20. Memory Channel Miscellaneous

Signal Name	Description
DDR_RESET_C01_N DDR_RESET_C23_N	System memory reset: Reset signal from processor to DRAM devices on the DIMMs. DDR_RESET_C01_N is used for memory channels 0 and 1 while DDR_RESET_C23_N is used for memory channels 2 and 3.
DDR_SCL_C01 DDR_SCL_C23	SMBus clock for the dedicated interface to the serial presence detect (SPD) and thermal sensors (TSoD) on the DIMMs. DDR_SCL_C01 is used for memory channels 0 and 1 while DDR_SCL_C23 is used for memory channels 2 and 3.
DDR_SDA_C01 DDR_SDA_C23	SMBus data for the dedicated interface to the serial presence detect (SPD) and thermal sensors (TSoD) on the DIMMs. DDR_SDA_C01 is used for memory channels 0 and 1 while DDR_SDA_C23 is used for memory channels 2 and 3.
DDR01_VREF DDR23_VREF	Voltage reference for CMD/ADD to the DIMMs. DDR01_VREF is used for memory channels 0 and 1 while DDR23_VREF is used for memory channels 2 and 3.
DRAM_PWR_OK_C01 DRAM_PWR_OK_C23	Power good for V_{CCD} rail used by the DRAM. This is an input signal used to indicate the V_{CCD} power supply is stable for memory channels 0 & 1 and channels 2 & 3.

4.2 PCI Express* Based Interface Signals

Note: PCI Express* Ports 1, 2 and 3 Signals are receive and transmit differential pairs.

Table 21. PCI Express Port 1 Signals

Signal Name	Description
PE1A_RX_DN[3:0] PE1A_RX_DP[3:0]	PCIe Receive Data Input
PE1B_RX_DN[7:4] PE1B_RX_DP[7:4]	PCIe Receive Data Input
PE1A_TX_DN[3:0] PE1A_TX_DP[3:0]	PCIe Transmit Data Output
PE1B_TX_DN[7:4] PE1B_TX_DP[7:4]	PCIe Transmit Data Output

Table 22. PCI Express Port 2 Signals

Signal Name	Description
PE2A_RX_DN[3:0] PE2A_RX_DP[3:0]	PCIe Receive Data Input
PE2B_RX_DN[7:4] PE2B_RX_DP[7:4]	PCIe Receive Data Input

continued...

Signal Name	Description
PE2C_RX_DN[11:8] PE2C_RX_DP[11:8]	PCIe Receive Data Input
PE2D_RX_DN[15:12] PE2D_RX_DP[15:12]	PCIe Receive Data Input
PE2A_TX_DN[3:0] PE2A_TX_DP[3:0]	PCIe Transmit Data Output
PE2B_TX_DN[7:4] PE2B_TX_DP[7:4]	PCIe Transmit Data Output
PE2C_TX_DN[11:8] PE2C_TX_DP[11:8]	PCIe Transmit Data Output
PE2D_TX_DN[15:12] PE2D_TX_DP[15:12]	PCIe Transmit Data Output

Table 23. PCI Express Port 3 Signals

Signal Name	Description
PE3A_RX_DN[3:0] PE3A_RX_DP[3:0]	PCIe Receive Data Input
PE3B_RX_DN[7:4] PE3B_RX_DP[7:4]	PCIe Receive Data Input
PE3C_RX_DN[11:8] PE3C_RX_DP[11:8]	PCIe Receive Data Input
PE3D_RX_DN[15:12] PE3D_RX_DP[15:12]	PCIe Receive Data Input
PE3A_TX_DN[3:0] PE3A_TX_DP[3:0]	PCIe Transmit Data Output
PE3B_TX_DN[7:4] PE3B_TX_DP[7:4]	PCIe Transmit Data Output
PE3C_TX_DN[11:8] PE3C_TX_DP[11:8]	PCIe Transmit Data Output
PE3D_TX_DN[15:12] PE3D_TX_DP[15:12]	PCIe Transmit Data Output

Table 24. PCI Express Miscellaneous Signals

Signal Name	Description
PE_HP_SCL	PCI Express* Hot-Plug SMBus Clock: Provides PCI Express* hot-plug support via a dedicated SMBus interface. Requires an external general purpose input/output (GPIO) expansion device on the platform.
PE_HP_SDA	PCI Express* Hot-Plug SMBus Data: Provides PCI Express* hot-plug support via a dedicated SMBus interface. Requires an external general purpose input/output (GPIO) expansion device on the platform.

4.3 DMI2/PCI Express Port 0 Signals

Table 25. DMI2 and PCI Express Port 0 Signals

Signal Name	Description
DMI_RX_DN[3:0] DMI_RX_DP[3:0]	DMI2 Receive Data Input
DMI_TX_DP[3:0] DMI_TX_DN[3:0]	DMI2 Transmit Data Output

4.4 Intel® QuickPath Interconnect Signals

Table 26. Intel QPI Port 0 and 1 Signals

Signal Name	Description
QPI{0/1}_CLKRX_DN/DP	Reference Clock Differential Input. These pins provide the PLL reference clock differential input. 100 MHz typical.
QPI{0/1}_CLKTX_DN/DP	Reference Clock Differential Output. These pins provide the PLL reference clock differential input. 100 MHz typical.
QPI{0/1}_DRX_DN/DP[19:0]	QPI Receive data input.
QPI{0/1}_DTX_DN/DP[19:0]	QPI Transmit data output.

4.5 PECI Signal

Table 27. PECI Signal

Signal Name	Description
PECI	PECI (Platform Environment Control Interface) is the serial sideband interface to the processor and is used primarily for thermal, power and error management.

4.6 System Reference Clock Signals

Table 28. System Reference Clock (BCLK{0/1}) Signals

Signal Name	Description
BCLK{0/1}_D[N/P]	Reference Clock Differential input. These pins provide the required reference inputs to various PLLs inside the processor, such as Intel QPI and PCIe. BCLK0 and BCLK1 run at 100MHz from the same clock source.

4.7 JTAG and TAP Signals

Table 29. JTAG and TAP Signals

Signal Name	Description
BPM_N[7:0]	Breakpoint and Performance Monitor Signals: I/O signals from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. These are 100 MHz signals.
PRDY_N	Probe Mode Ready is a processor output used by debug tools to determine processor debug readiness.
PREQ_N	Probe Mode Request is used by debug tools to request debug operation of the processor.
TCK	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TMS	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRST_N	TRST_N (Test Reset) resets the Test Access Port (TAP) logic. TRST_N must be driven low during power on Reset.

4.8 Serial VID Interface (SVID) Signals

Table 30. SVID Signals

Signal Name	Description
SVIDALERT_N	Serial VID alert.
SVIDCLK	Serial VID clock.
SVIDDATA	Serial VID data out.

4.9 Processor Asynchronous Sideband and Miscellaneous Signals

Table 31. Processor Asynchronous Sideband Signals

Signal Name	Description
CATERR_N	Indicates that the system has experienced a fatal or catastrophic error and cannot continue to operate. The processor will assert CATERR_N for unrecoverable machine check errors and other internal unrecoverable errors. It is expected that every processor in the system will wire-OR CATERR_N for all processors. Since this is an I/O land, external agents are allowed to assert this land which will cause the processor to take a machine check exception. This signal is sampled after PWRGOOD assertion. On the Intel® Xeon® processor E5 v4 product family, CATERR_N is used for signaling the following types of errors: • Legacy MCERR's, CATERR_N is asserted for 16 BCLKs. • Legacy IERR's, CATERR_N remains asserted until warm or cold reset.
ERROR_N[2:0]	Error status signals for integrated I/O (IIO) unit:

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Signal Name	Description
	• 0 = Hardware correctable error (no operating system or firmware action necessary) • 1 = Non-fatal error (operating system or firmware action required to contain and recover) • 2 = Fatal error (system reset likely required to recover)
MEM_HOT_C01_N MEM_HOT_C23_N	Memory throttle control. Signals external BMC-less controller that DIMM is exceeding temperature limit and needs to increase to max fan speed. MEM_HOT_C01_N and MEM_HOT_C23_N signals have two modes of operation - input and output mode. Input mode is externally asserted and is used to detect external events such as VR_HOT# from the memory voltage regulator and causes the processor to throttle the appropriate memory channels. Output mode is asserted by the processor known as level mode. In level mode, the output indicates that a particular branch of memory subsystem is hot. MEM_HOT_C01_N is used for memory channels 0 & 1 while MEM_HOT_C23_N is used for memory channels 2 & 3.
MSMI_N	Machine Check Exception (MCE) is signaled via this pin when eMCA2 is enabled.
PMSYNC	Power Management Sync. A sideband signal to communicate power management status from the Platform Controller Hub (PCH) to the processor.
PROCHOT_N	PROCHOT_N will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal can also be driven to the processor to activate the Thermal Control Circuit. This signal is sampled after PWRGOOD assertion on a cold boot. If PROCHOT_N is asserted at the assertion of RESET_N on a warm boot, the processor will tristate its outputs.

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Signal Name	Description
PWRGOOD	PWRGOOD is a processor input. The processor requires this signal to be a clean indication that all processor clocks and power supplies are stable and within their specifications. "Clean" implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. PWRGOOD transitions from inactive to active when all supplies except VCCIN are stable. The signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
RESET_N	Global reset signal. Asserting the RESET_N signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. Note some PLL, Intel QuickPath Interconnect and error states are not affected by reset and only PWRGOOD forces them to a known state.
THERMTRIP_N	Assertion of THERMTRIP_N (Thermal Trip) indicates one of two possible critical over-temperature conditions: One, the processor junction temperature has reached a level beyond which permanent silicon damage may occur and Two, the system memory interface has exceeded a critical temperature limit set by BIOS. Measurement of the processor junction temperature is accomplished through multiple internal thermal sensors that are monitored by the Digital Thermal Sensor (DTS). Simultaneously, the Power Control Unit (PCU) monitors external memory temperatures via the dedicated SMBus interface to the DIMMs. If any of the DIMMs exceed the BIOS defined limits, the PCU will signal THERMTRIP_N to prevent damage to the DIMMs. Once activated, the processor will stop all execution and shut down all PLLs. To further protect the processor, its core voltage (V_{CCIN}), V_{CCD}, V_{CCIO_IN}, V_{CCPECI} supplies must be removed following the assertion of THERMTRIP_N. Once activated, THERMTRIP_N remains latched until RESET_N is asserted. While the assertion of the RESET_N signal may de-assert THERMTRIP_N, if the processor's junction temperature remains at or above the trip level, THERMTRIP_N will again be asserted after RESET_N is de-asserted. This signal can also be asserted if the system memory interface has exceeded a critical temperature limit set by BIOS.

Table 32. Miscellaneous Signals

Signal Name	Description
BIST_ENABLE	BIST Enable Strap. Input which allows the platform to enable or disable built-in self test (BIST) on the processor. This signal is pulled up on the die. Rrefer to Table 8 on page 26 for details.
BMCINIT	BMC Initialization Strap. Indicates whether Service Processor Boot Mode should be used. Used in combination with FRMAGENT and SOCKET_ID inputs. • 0: Service Processor Boot Mode Disabled. Example boot modes: Local PCH (this processor hosts a legacy PCH with firmware behind it), Intel QPI Link Boot (for processors one hop away from the FW agent), or Intel QPI Link Init (for processors more than one hop away from the firmware agent). • 1: Service Processor Boot Mode Enabled. In this mode of operation, the processor performs the absolute minimum internal configuration and then waits for the Service Processor to complete its initialization. The socket boots after receiving a "GO" handshake signal via a firmware scratchpad register.

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Signal Name	Description
	This signal is pulled down on the die, refer to Table 8 on page 26 for details.
EAR_N	External Alignment of Reset, used to bring the processor up into a deterministic state. This signal is pulled up on the die, refer to Table 8 on page 26 for details.
FIVR_FAULT	Indicates an internal error has occurred with the integrated voltage regulator. The FIVR_FAULT signal can be sampled any time after 1.5 ms after the assertion of PWRGOOD. FIVR_FAULT must be qualified by THERMTRIP_N assertion.
FRMAGENT	Bootable Firmware Agent Strap. This input configuration strap used in combination with SOCKET_ID to determine whether the socket is a legacy socket, bootable firmware agent is present, and DMI links are used in PCIe* mode (instead of DMI2 mode). The firmware flash ROM is located behind the local PCH attached to the processor via the DMI2 interface.This signal is pulled down on the die, refer to Table 8 on page 26 for details.
PM_FAST_WAKE_N	Power Management Fast Wake. Enables quick package C3 - C6 exits of all sockets. Asserted if any socket detects a break from package C3 - C6 state requiring all sockets to exit the low power state to service a snoop, memory access, or interrupt. Expected to be wired-OR among all processor sockets within the platform.
PROC_ID	This output can be used by the platform to determine if the installed processor is an Intel® Xeon® Processor E5 v4 Product Family. There is no connection to the processor silicon for this signal. The processor package grounds or floats the pin to set '0' or '1', respectively. 1: Intel® Xeon® processor E5-1600 and E5-2600 v3 product families 0: Intel® Xeon® Processor E5-2600 v4 Product Family
RSVD	RESERVED. All signals that are RSVD must be left unconnected on the board. Refer to Reserved or Unused Signals on page 22 for details.
SAFE_MODE_BOOT	Safe Mode Boot Strap. SAFE_MODE_BOOT allows the processor to wake up safely by disabling all clock gating. This allows BIOS to load registers or patches if required. This signal is sampled after PWRGOOD assertion. The signal is pulled down on the die. Refer to Table 8 on page 26 for details.
SKTOCC_N	SKTOCC_N (Socket Occupied) is used to indicate that a processor is present. This is pulled to ground on the processor package; there is no connection to the processor silicon for this signal.
SOCKET_ID[1:0]	Socket ID Strap. Socket identification configuration straps for establishing the PECI address, Intel® QPI Node ID, and other settings. This signal is used in combination with FRMAGENT to determine whether the socket is a legacy socket, bootable firmware agent is present, and DMI links are used in PCIe* mode (instead of DMI2 mode). Each processor socket consumes one Node ID, and there are 128 Home Agent tracker entries. This signal is pulled down on the die. Refer to Table 8 on page 26 for details.
TEST[3:0]	Test[3:0] must be individually connected to an appropriate power source or ground through a resistor for proper processor operation.
TXT_AGENT	Intel® Trusted Execution Technology (Intel® TXT) Agent Strap. 0 = Default. The socket is not the Intel TXT Agent. 1 = The socket is the Intel TXT Agent. The legacy socket (identified by SOCKET_ID[1:0] = 00b) with Intel TXT Agent should always set the TXT_AGENT to 1b. This signal is pulled down on the die, refer to Table 8 on page 26 for details.
TXT_PLTEN	Intel Trusted Execution Technology (Intel TXT) Platform Enable Strap. 0 = The platform is not Intel TXT enabled. All sockets should be set to zero. Scalable DP (sDP) platforms should choose this setting if the Node Controller does not support Intel TXT.

Signal Name	Description
	1 = Default. The platform is Intel TXT enabled. All sockets should be set to one. In a non-Scalable DP platform this is the default. When this is set, Intel TXT functionality requires user to explicitly enable Intel TXT via BIOS setup. This signal is pulled up on the die, refer to Table 8 on page 26 for details.

4.10 Processor Power and Ground Supplies

Table 33. Power and Ground Signals

Signal Name	Description
V_{CCIN}	Input to the Integrated Voltage Regulator (IVR) for the processor cores, lowest level caches (LLC), ring interface, PLL, IO, and home agent. It is provided by a VR 12.5 compliant motherboard voltage regulator (MBVR) for each CPU socket. The output voltage of this MBVR is controlled by the processor, using the serial voltage ID (SVID) bus.
V_{CCIN_SENSE} $V_{SS\_VCCIN\_SENSE}$	V_{CCIN_SENSE} and $V_{SS\_VCCIN\_SENSE}$ are remote sense signals for V_{CCIN} MBVR12.5 and are used by the voltage regulator to ensure accurate voltage regulation. These signals must be connected to the voltage regulator feedback circuit, which ensures the output voltage remains within specification.
V_{CCD_01} V_{CCD_23}	Fixed 1.2V power supply for the processor system memory interface. Provided by two MBVR 12.0 or 12.5 compliant regulators per CPU socket. V_{CCD_01} and V_{CCD_23} are used for memory channels 0 &1 and 2 & 3, respectively. The valid voltage of this supply (1.20V) is configured by BIOS after determining the operating voltages of the installed memory. V_{CCD_01} and V_{CCD_23} will also be referred to as V_{CCD}. *Note:* The processor must be provided V_{CCD_01} and V_{CCD_23} for proper operation, even in configurations where no memory is populated. A MBVR 12.0 or 12.5 controller is required.
V_{SS}	Processor ground return.
V_{CCIO_IN}	IO voltage supply input.
V_{CCPECI}	Power supply for PECI.