

Intel® Quark™ SE Microcontroller C1000 Development Platform

Schematics

November 2016



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Revision History

Date	Revision	Description
November 2016	001	Initial release.

INTEL QUARK SE MICROCONTROLLER C1000 DEVELOPMENT PLATFORM

DEV KIT

J12658-105 PB
J29379-500 PBA
J29378-500 TA

EVAL KIT

J12658-105 PB
J35534-500 PBA
J35533-500 TA

LB5
LABEL

SERIAL NUMBER

A88430-001

LABEL_JEDEC_E1

e1

LABEL_JEDEC_B4

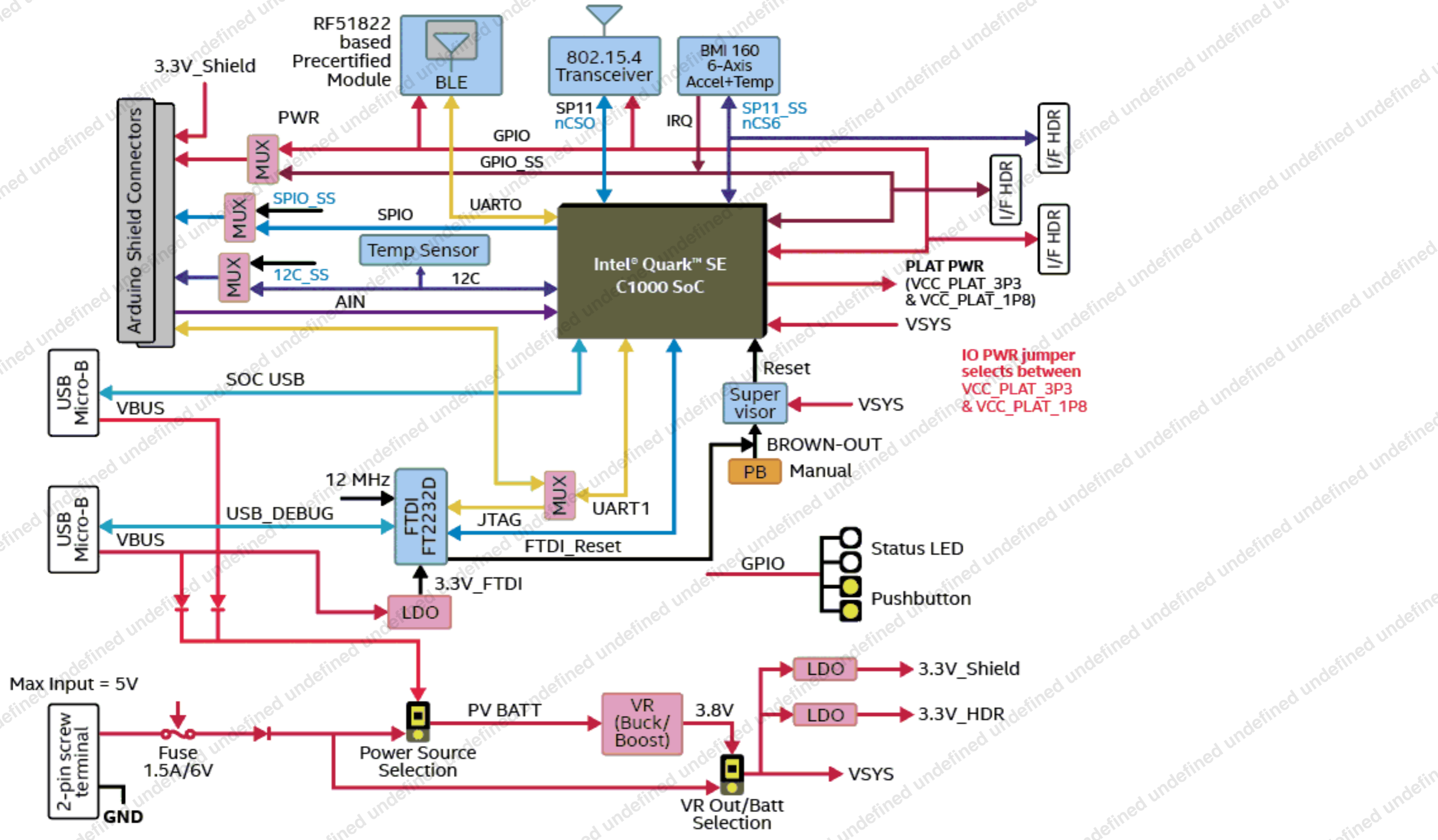
b4

LABEL_CHINA_ROHS_10

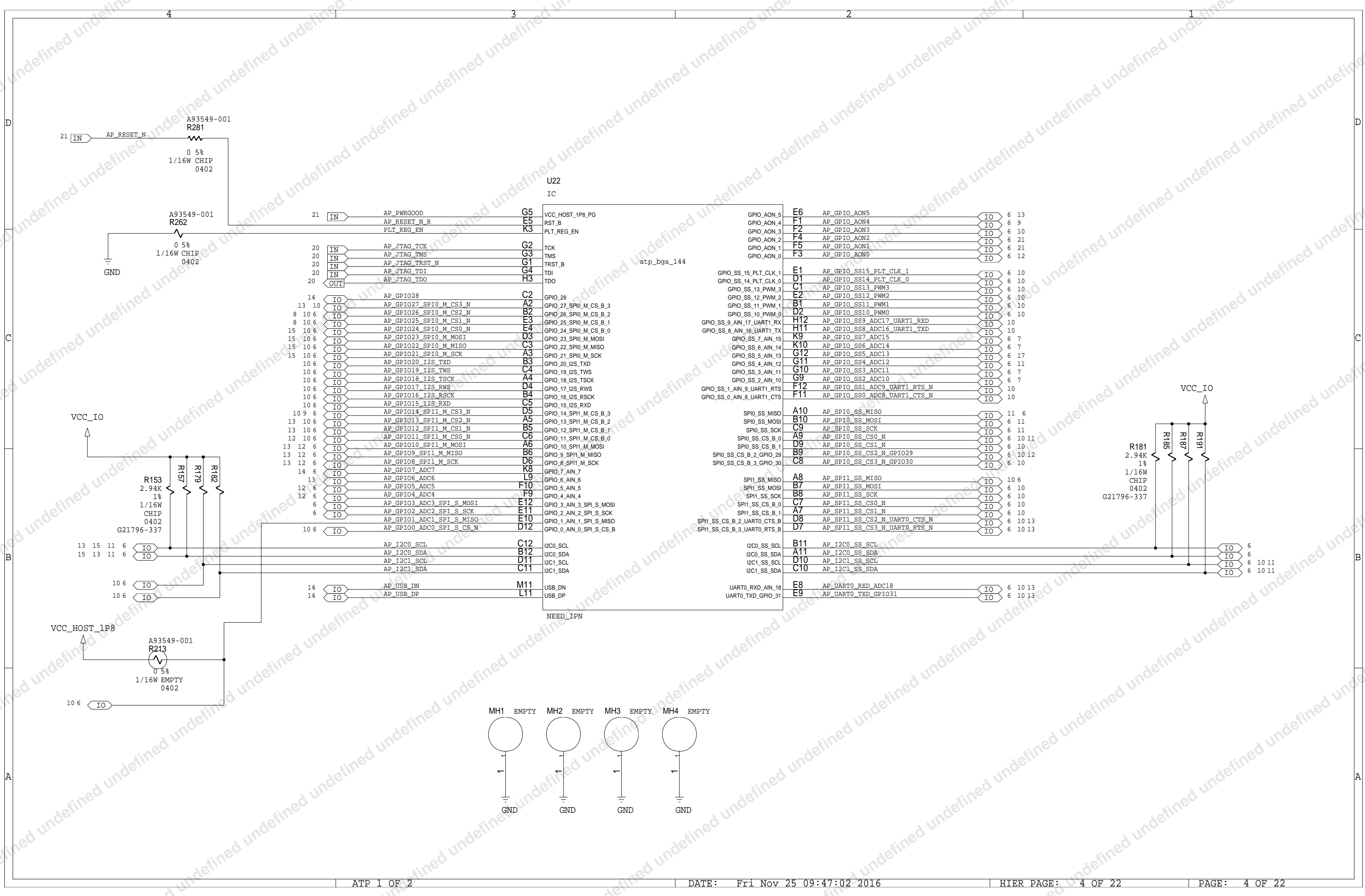
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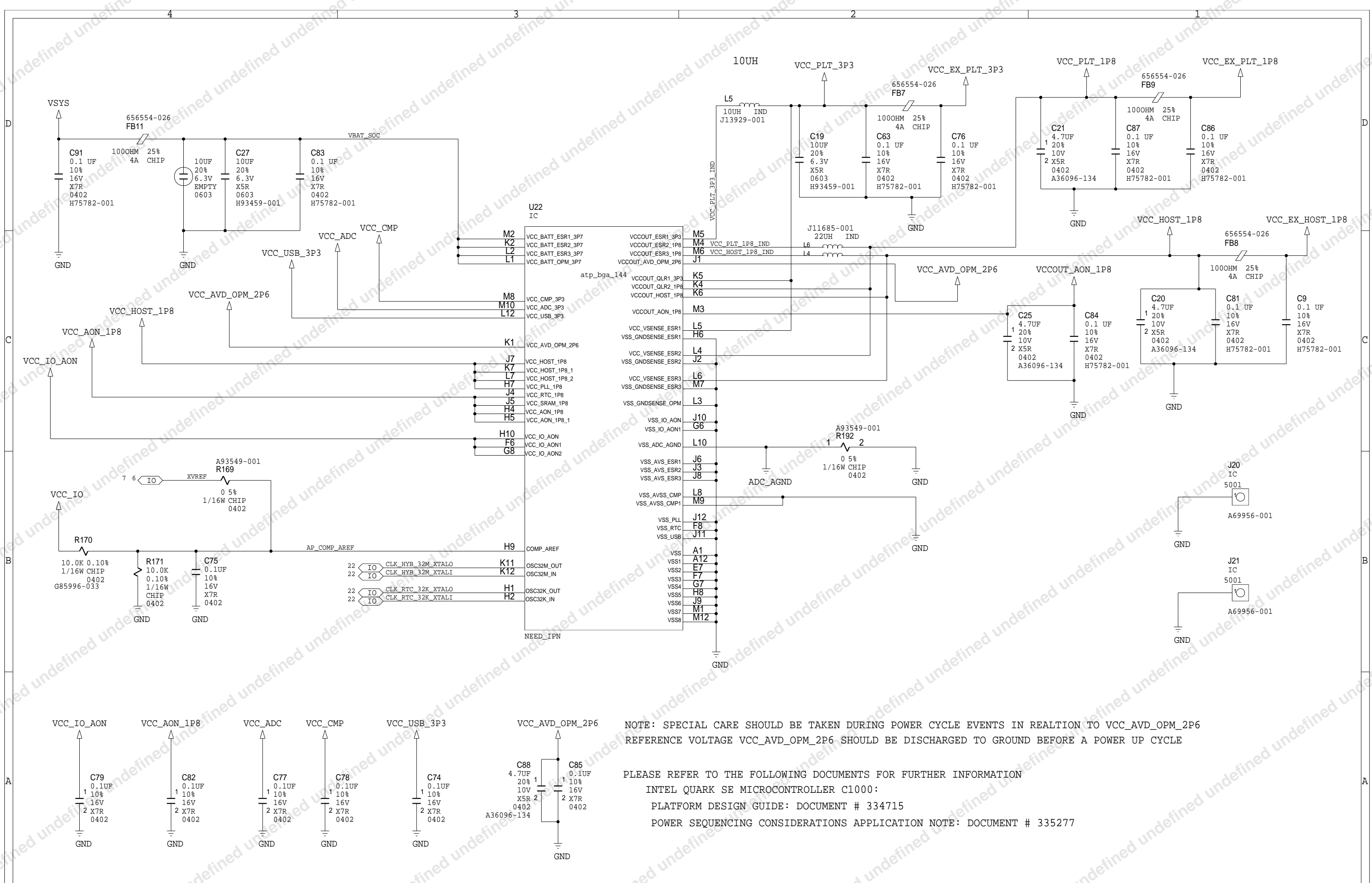
TABLE OF CONTENTS

PAGE	SHEET NAME	PAGE	SHEET NAME
1	INTRO		
2	TABLE OF CONTENTS		
3	BLOCK DIAGRAM		
4	ATP 1 OF 2		
5	ATP 2 OF 2		
6	IO HEADERS		
7	ARDUINO HEADERS		
8	LEDS		
9	SWITCHES		
10	MUXES		
11	SENSORS		
12	RADIO 15.4		
13	RADIO BLUETOOTH		
14	ATP USB		
15	FLASH		
16	VOLTAGE REGULATOR		
17	POWER SELECT		
18	POWER DISTRIBUTION		
19	FTDI 2232D		
20	FTDI ISOLATION		
21	RESET LOGIC		
22	CRYSTALS		



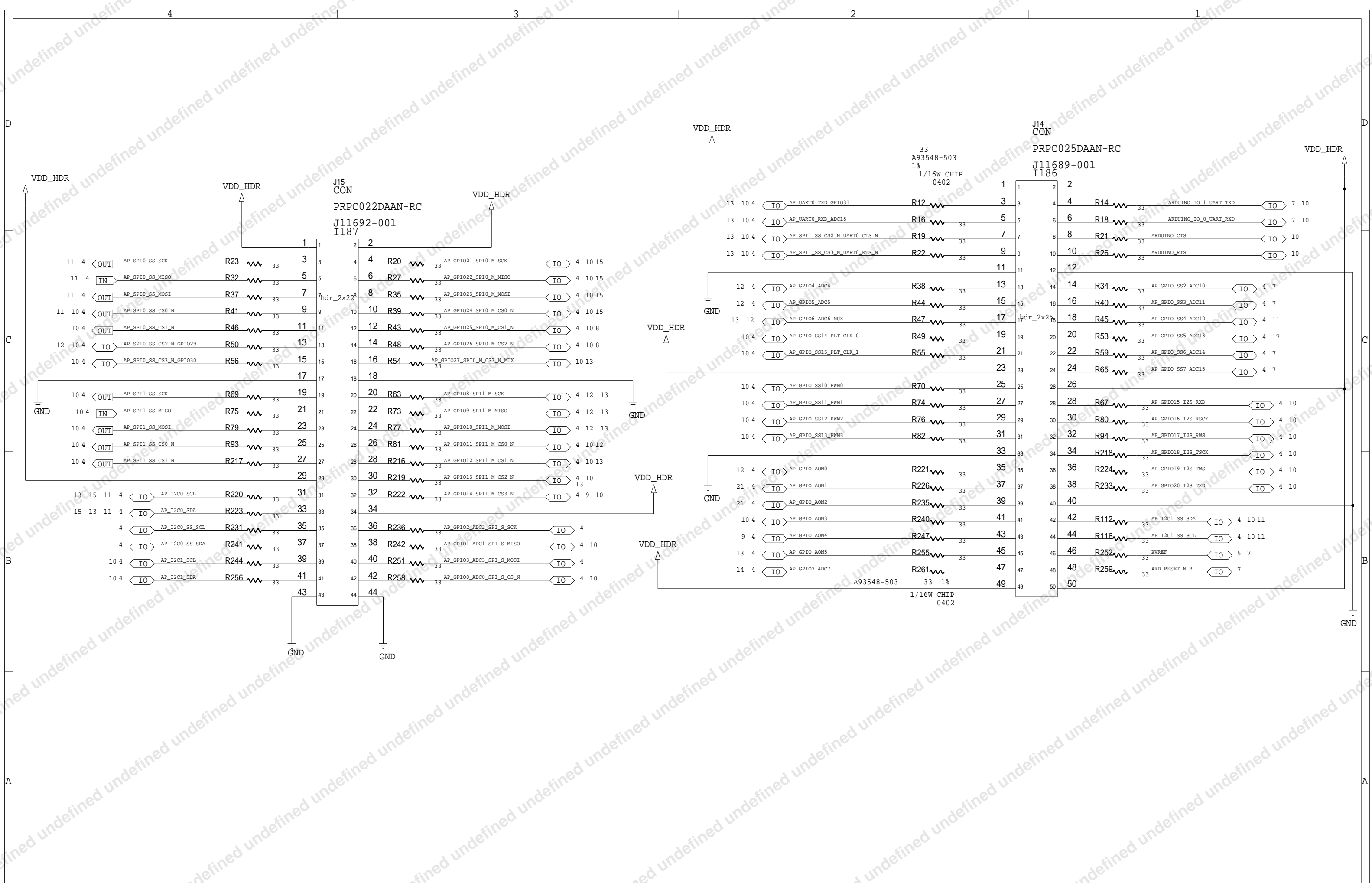
BLOCK DIAGRAM

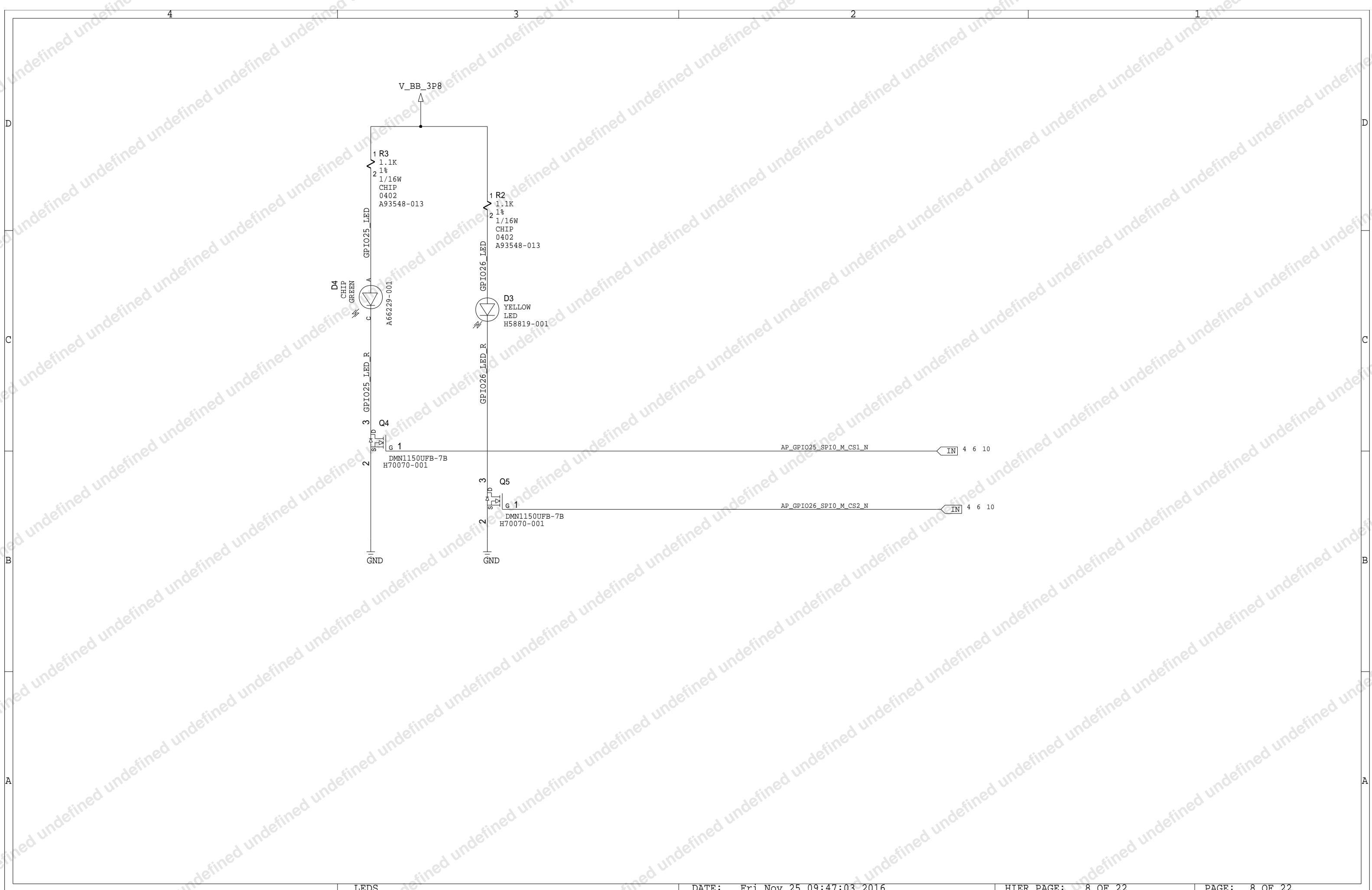


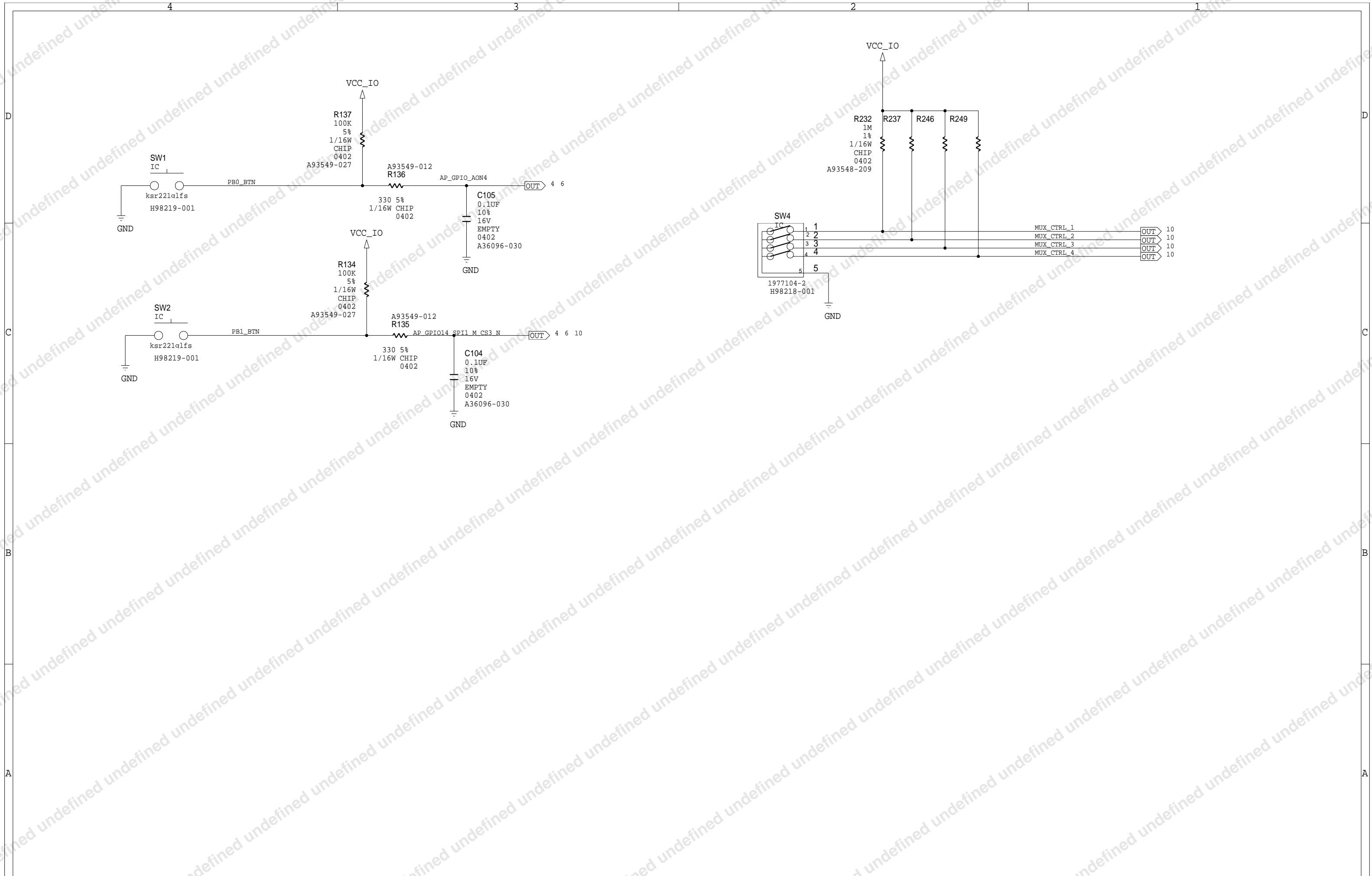


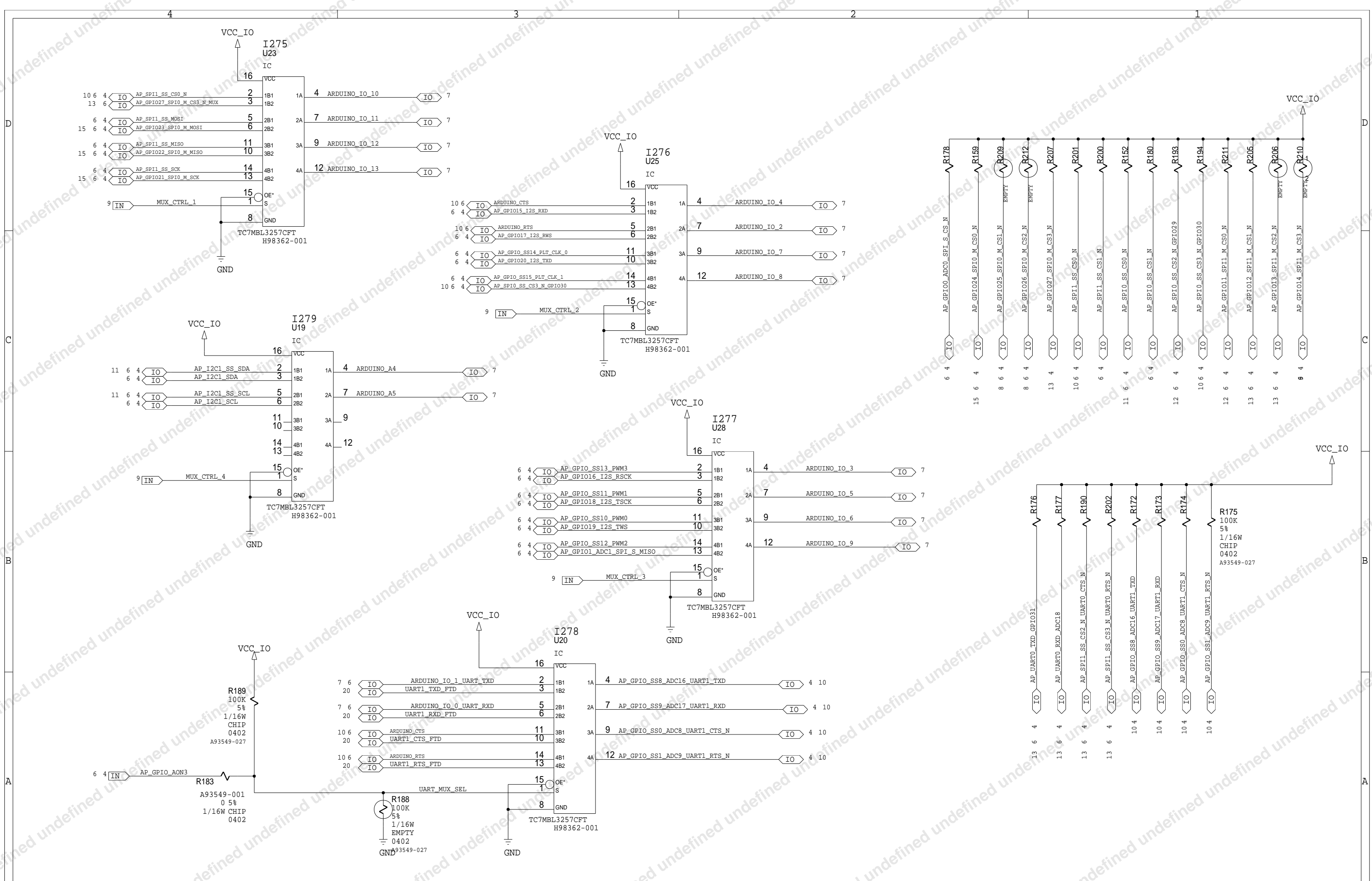
NOTE: SPECIAL CARE SHOULD BE TAKEN DURING POWER CYCLE EVENTS IN REACTION TO VCC_AVN_OPM_2P6 REFERENCE VOLTAGE VCC_AVN_OPM_2P6 SHOULD BE DISCHARGED TO GROUND BEFORE A POWER UP CYCLE

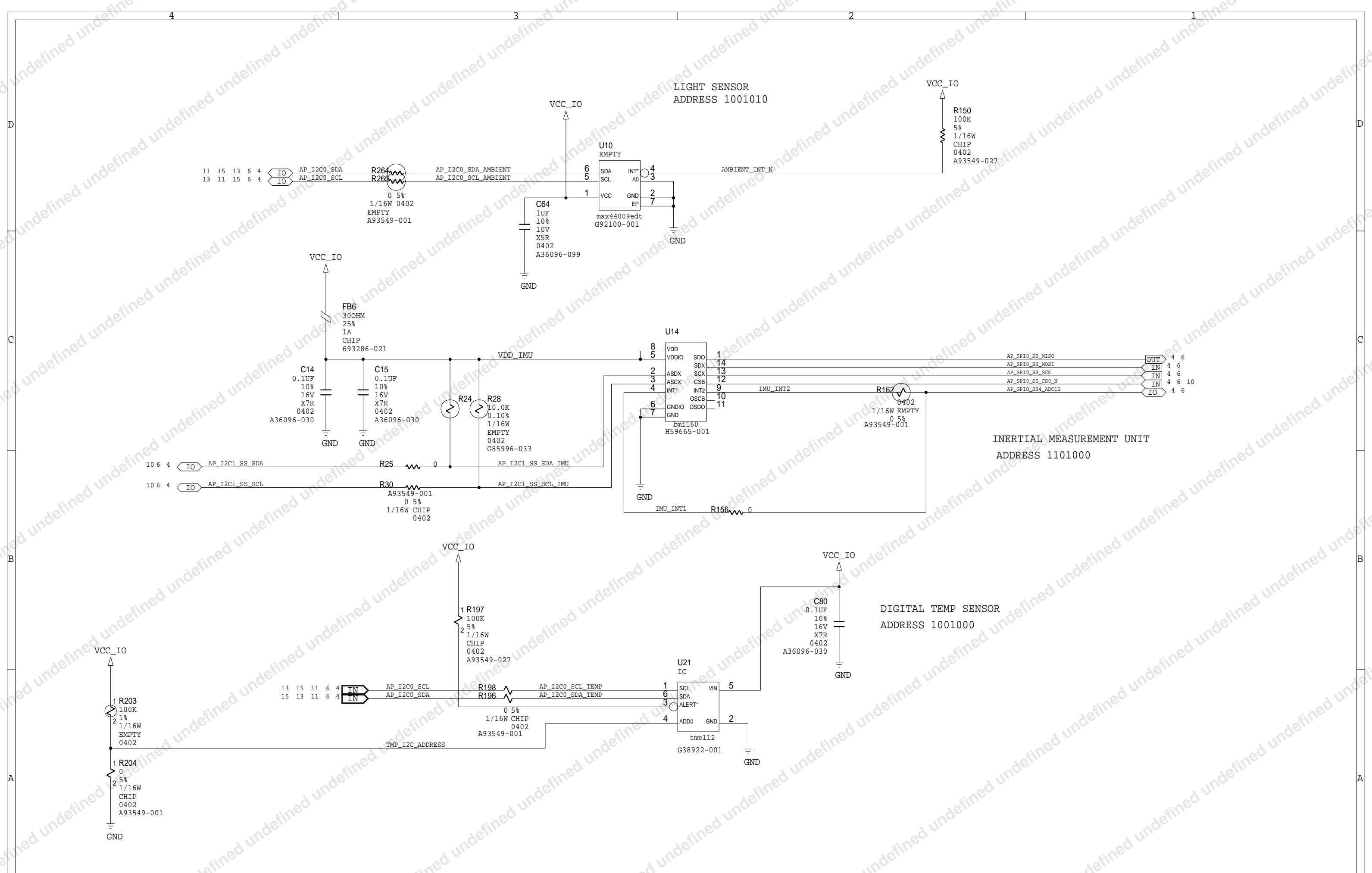
PLEASE REFER TO THE FOLLOWING DOCUMENTS FOR FURTHER INFORMATION
 INTEL QUARK SE MICROCONTROLLER C1000:
 PLATFORM DESIGN GUIDE: DOCUMENT # 334715
 POWER SEQUENCING CONSIDERATIONS APPLICATION NOTE: DOCUMENT # 335277

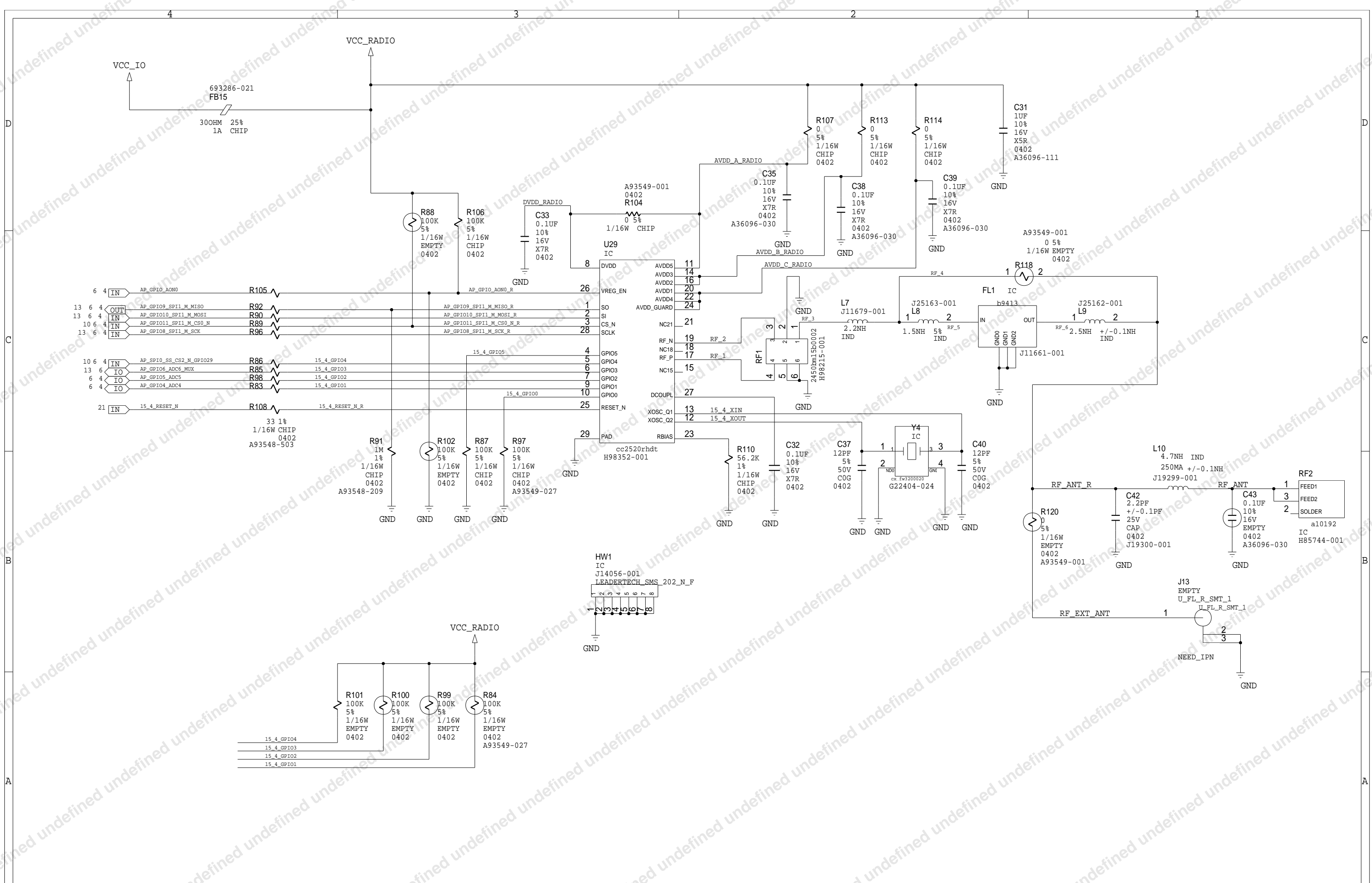


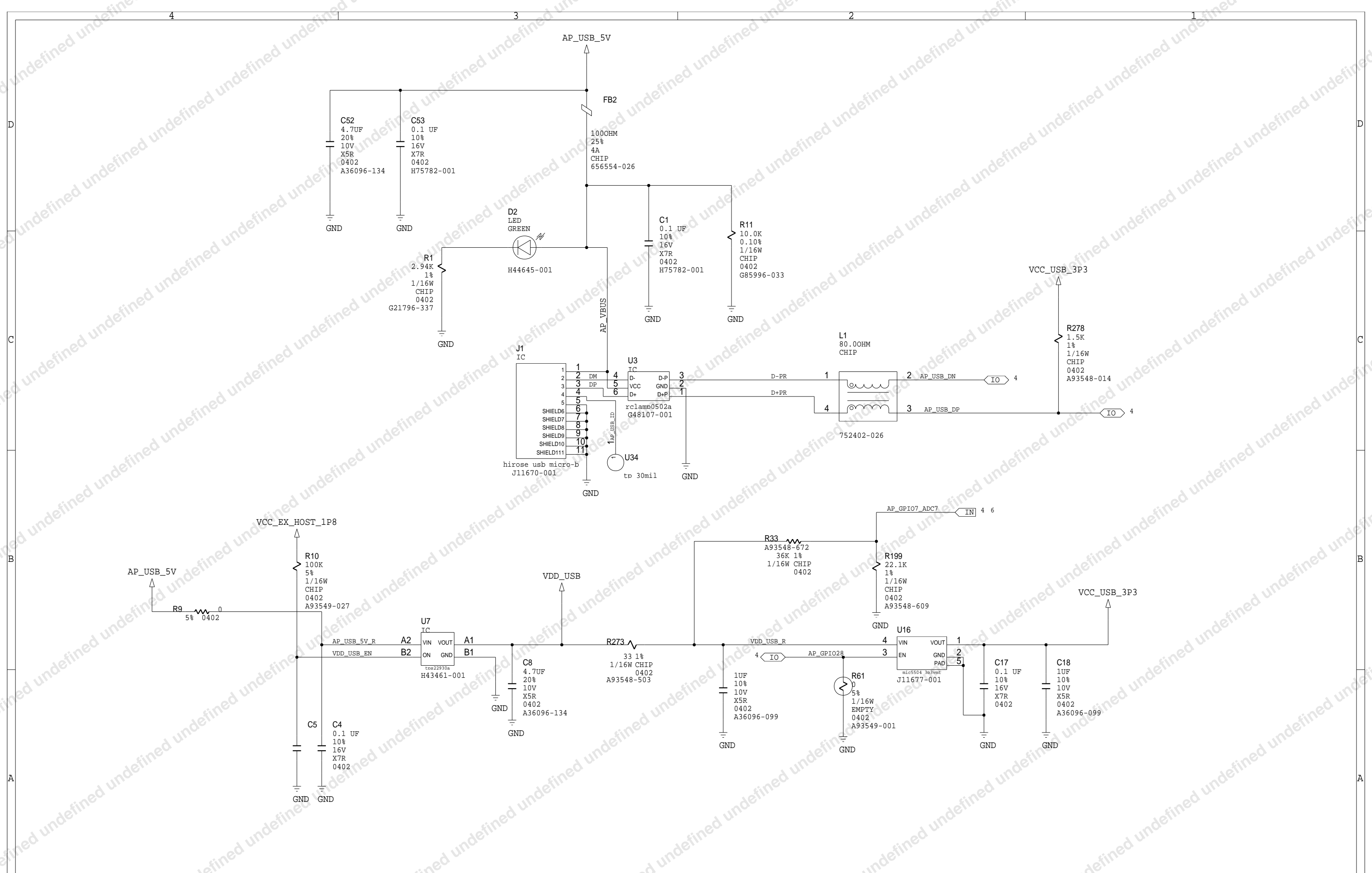


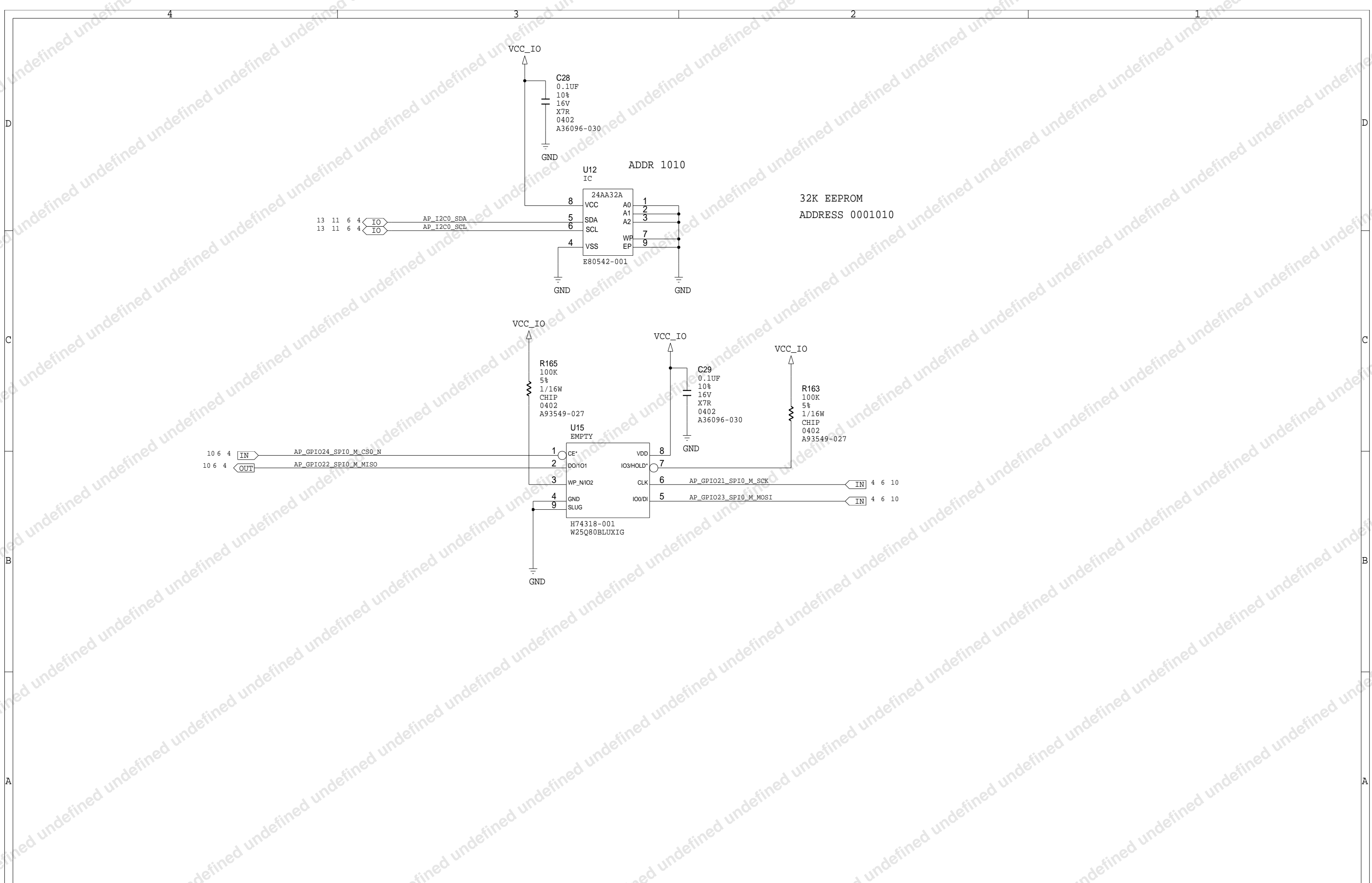


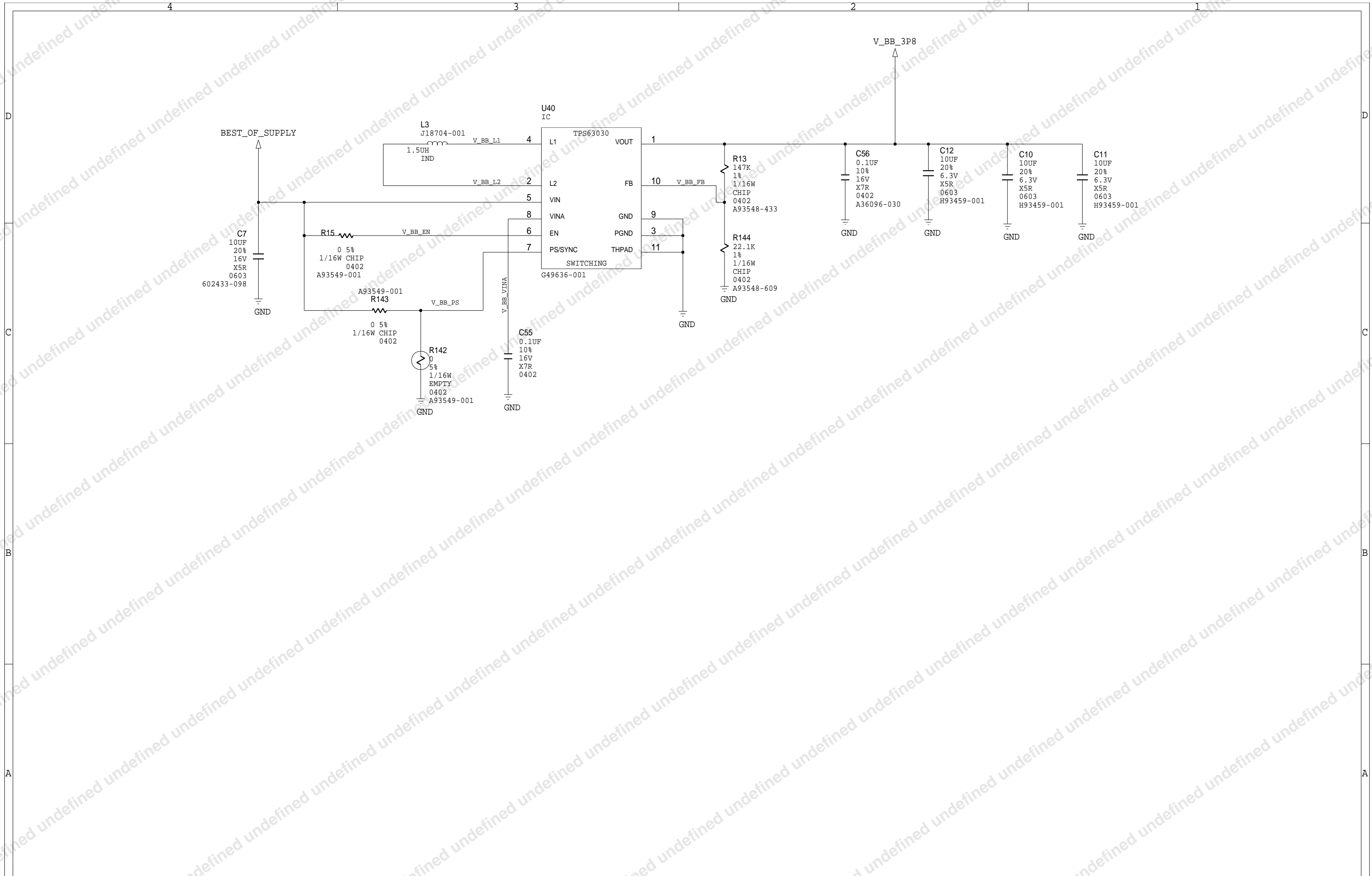


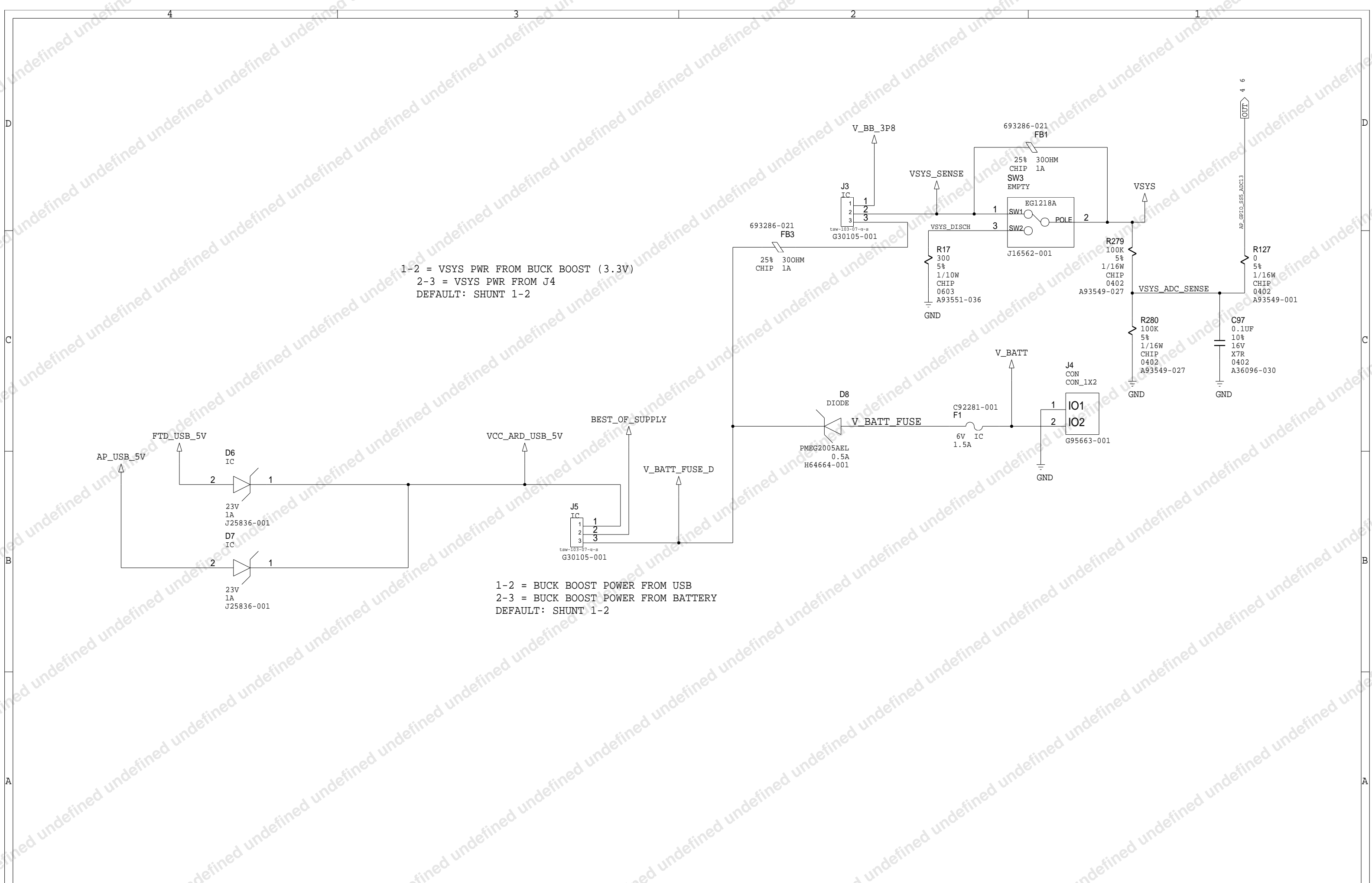












1-2 = VSYS PWR FROM BUCK BOOST (3.3V)
 2-3 = VSYS PWR FROM J4
 DEFAULT: SHUNT 1-2

1-2 = BUCK BOOST POWER FROM USB
 2-3 = BUCK BOOST POWER FROM BATTERY
 DEFAULT: SHUNT 1-2

