

# Intel<sup>®</sup> Quark<sup>™</sup> SE Microcontroller C1000 Power Sequencing Considerations

Application Note

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*February 2017*



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## Revision History

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Date	Revision	Description
February 2017	002	Silego part number updated (new specific part number for ATP1).
November 2016	001	Initial release.

## 1.0 Introduction

### 1.1 Power Sequencing Failure

If the voltage transition on the power supply pin (VSYS) of the Intel® Quark™ SE Microcontroller C1000 causes a power down followed by a power up sequence before its internal reference voltage OPM2P6\_VOUT drops below 100mV, an incorrect power sequence may occur. If an incorrect power sequence happens the device may enter an indeterminate state in which the correct operation of the device is not guaranteed.

The reference voltage OPM2P6\_VOUT must remain below 100mV at the start of a power up sequence. If not, certain internal signals within the Intel® Quark™ SE Microcontroller C1000 might not initialize correctly. [Figure 1](#) illustrates the sequence of events during a power up cycle for both a normal and incorrect power sequence:

- VSYS – main input power rail (Pin: K2, L1, L2, M2)
- OPM2P6\_VOUT – 2.6V reference voltage output (Pin: J1)
- VCC\_AON\_1P8 – 1.8V AON Domain Supply input (Pin: H4, H5)
- VCC\_HOST\_1P8 – 1.8V power to HOST generated by regulator ESR3 (ESR3 Inductor out / Host QLR Pin K6 to J7, K7, L7 Inputs)

**Figure 1. Intel® Quark™ SE Microcontroller C1000 Power Sequencing**



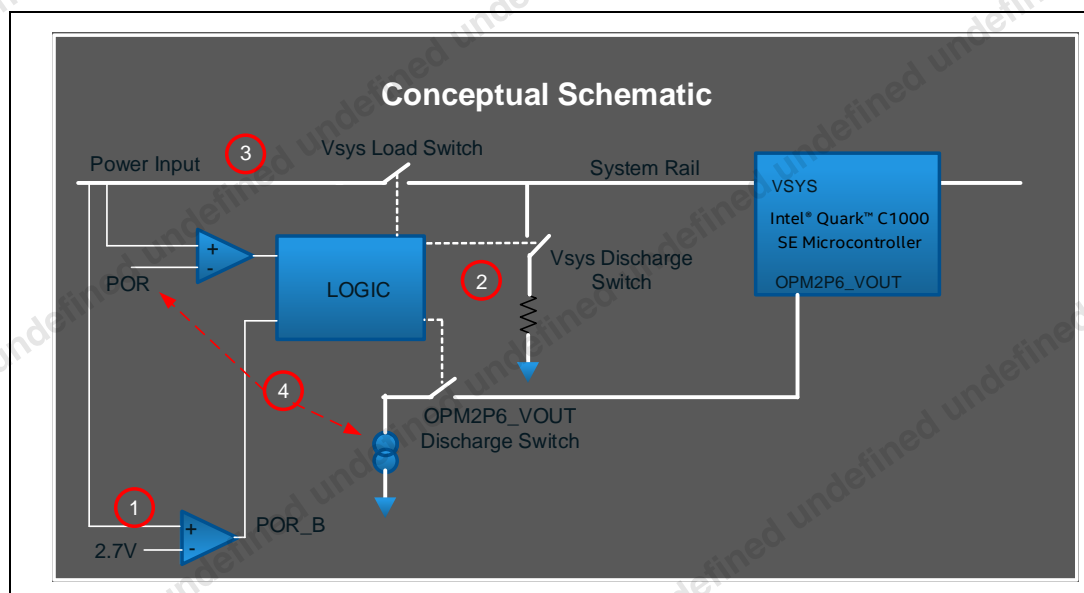
Intel's recommendation is to ensure that OPM2P6\_VOUT node is discharged to ground (zero volts) before a power up cycle. The subsequent sections in this document describe the generic implementation needed to ensure a correct power sequence, followed by a detailed example.



## 2.0 Ensuring Correct OPM2P6 Discharge

### 2.1 OPM2P6\_VOUT Rail Discharge Concept

Figure 2. Intel® Quark™ SE Microcontroller C1000 with OPM2P6\_VOUT Discharge



The block diagram shown in [Figure 2](#) shows the conceptual solution to ensure the correct OPM2P6\_VOUT discharge is achieved by using a voltage monitor, a load switch and active discharge circuitry. Operation of the circuit is achieved by using two voltage thresholds:

- POR\_B – Generates a falling edge (high to low transition) that indicates input power supply to the Intel® Quark™ SE Microcontroller C1000 has dropped below 2.7V.
- POR – Power up threshold for the system. Its voltage value needs to be selected based on desired hysteresis from 2.7V to meet system requirements.

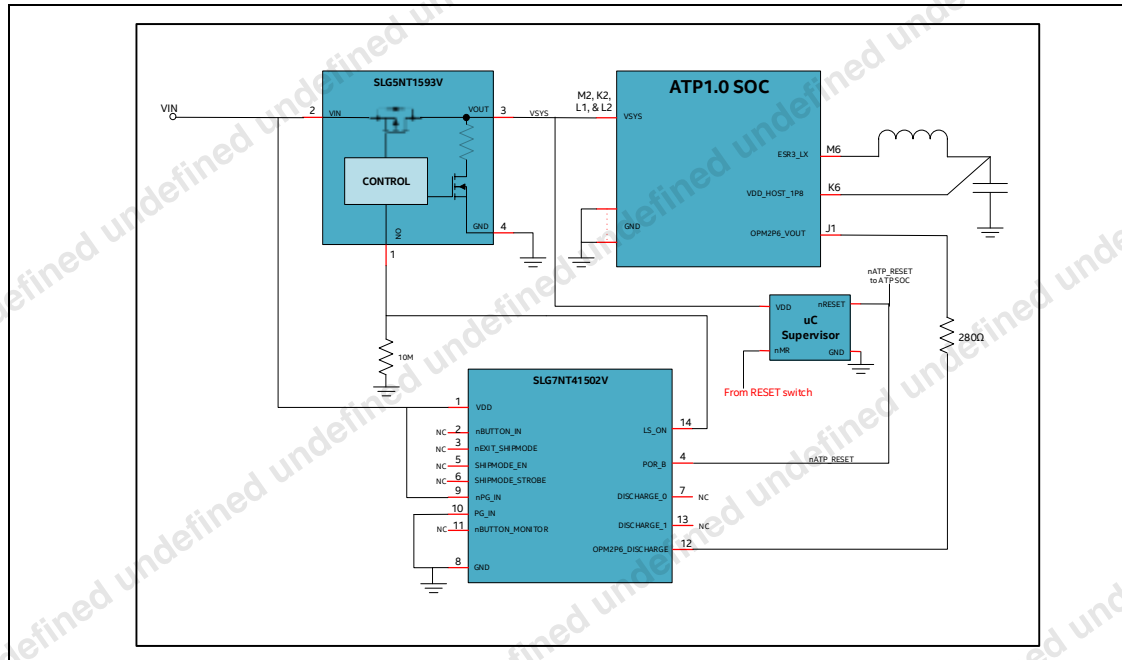
The sequence of events during the power-down/power-up cycle is as follows:

1. During power down, when the system rail falls below 2.7V the POR\_B signal generates a high to low transition.
2. This falling edge transition enables discharge of Intel® Quark™ SE Microcontroller C1000 pins OPM2P6\_VOUT and VSYS to GND. The load switch is also disabled.
3. Power is re-applied to the system.
4. First, discharge OPM2P6\_VOUT to GND. Disable active discharge circuitry on the system rail and OPM2P6\_VOUT when the voltage rises above POR threshold, after ensuring that OPM2P6\_VOUT is fully discharged to GND. Enable the load switch that provides power to the Intel® Quark™ SE Microcontroller C1000.

## 2.2 Application Schematic of a Proposed Implementation

The schematic block diagram shown in [Figure 3](#) shows one possible implementation of circuitry that is used to guarantee proper power sequencing of the Intel® Quark™ SE Microcontroller C1000, as modelled on the Intel® Quark™ SE Microcontroller C1000 Evaluation Board.

**Figure 3. Schematic Connectivity of Implementation**



The proposed implementation consists of using two devices from Silego and a Voltage Monitor from Microchip:

1. A programmable mixed signal device (SLG7NT41502V) controls power sequencing and discharge of OPM2P6\_VOUT rail.  
**Note:** SLG7NT41502V “Ship Mode” is not required and in general pins 2,3,5,6,7,11 and 13 are normally NC.
2. A second device (SLG5NT1593V) gates the power supply input to the VSYS pin of the Intel® Quark™ SE Microcontroller C1000, and also discharges the system rail. If inrush current control is desired, use SLG5NT1729V instead of SLG5NT1593V.
3. A voltage supervisor monitors the power input rail and triggers the SLG7NT41502V by setting POR\_B low when the input voltage drops below 2.7V.

The OPM2P6\_VOUT voltage is generated by an embedded linear regulator that is supplied by the VSYS pin. Since the power drain on this pin is very small, and due to external capacitance on the OPM2P6\_VOUT rail, there could be situations where the input supply (VSYS) is fully discharged during a power cycle but the voltage on OPM2P6\_VOUT has not been discharged below 100mV to guarantee proper power





sequencing. To facilitate this, a load switch with active discharge controls the power delivery to the microcontroller. The active discharge circuitry inside the load switch ensures that the voltage on VSYS is discharged to GND. Disconnecting and discharging VSYS protects the internal OPM2P6\_VOUT regulator. This prevents the regulator from having a valid supply voltage on its input while its output discharges to GND.

The operation of the schematics above can be explained more clearly with the captured waveforms shown in [Figure 4](#), which utilizes SLG7NT41502V and SLG5NT1593V to control the microcontroller.

**Figure 4. Operation of Circuitry Controlling OPM2P6\_VOUT Discharge during a Power Cycle**



The waveform shows the behavior of the OPM2P6\_VOUT rail when the power Input is powered down and subsequently powered up after 100ms.

1. When the voltage on the input power rail decays to ~2.7V, the POR\_B signal from the voltage monitor is asserted.
2. Assertion of this signal causes the signal PFET ON (pin 14 - output from SLG7NT41502V device) to be de-asserted, disabling load switch and initially discharging Vsys. Simultaneously, the OPM2P6 Discharge (pin 12 – open drain output on SLG7NT41502V device) is driven low, causing the OPM2P6\_VOUT to be discharged to GND through the 330Ω resistor.
3. Once the input power drops below the operational voltage of the Silego parts, active discharge no longer occurs and supplies discharge more slowly.
4. When input power is reapplied, active discharge of the Vsys and OPM2P6\_VOUT rail is applied. Once the internal POR Threshold of the SLG7NT41502V device is exceeded (3.582V), the device ensures the load switch is enabled only after a



minimum of ~380mS of forced discharging of Vsys and OPM2P6\_VOUT (to guarantee proper power sequencing).

5. Once power is applied, the Intel® Quark™ SE Microcontroller C1000 proceeds with its normal power sequencing of OPM2P6\_VOUT rising to 2.6V, followed by the powering up of AON\_IO\_VCC (not shown) and the VCC\_HOST\_1P8 domain.

### 2.3 Alternate Implementation using POWER GOOD (PG) Signal to Control VSYS and OPM2P6\_VOUT Discharge

If your platform implementation uses an onboard system regulator that provides a self-contained power good indicator, the Silego part (SLG7NT41502V) can use this to enable the load switch after a minimum off time of ~180ms of forced discharge of VSYS and OPM2P6\_VOUT (to guarantee proper power sequencing). Load switch disable and VSYS and OPM2P6\_VOUT discharge is still enabled by the system input voltage decaying to ~2.7V, which causes the POR\_B to assert.

For power up enabling, an active high PG (Power Good) indicator from an onboard regulator should be connected to pin 10 (PG) of the Silego SLG7NT42414V, instead of hard wiring this to GND, as shown in [Figure 3](#).