Intel® UHD Graphics Open Source

Programmer's Reference Manual

For the 2021 11th Generation Intel Core™ Processors, Intel Xeon® Processors, and Intel 500 Series Chipsets based on the "Rocket Lake" Platform

Volume 3: Configurations

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Configurations

This chapter contains configurations details as described in the following sections:

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Product Mapping Table

NOTE: This information is preliminary, and subject to change.

Product Configuration Attribute Table

SKU Name	GT1
Status	POR
	Global Attributes
Render Engine	1x2x16
Media Engine	XeM
Display Engine	XeD
LLC Size	12MB
In-Package Memory	N/A
Main Memory	LP4x-3733 128bit (60GBps)

Top Level Diagrams

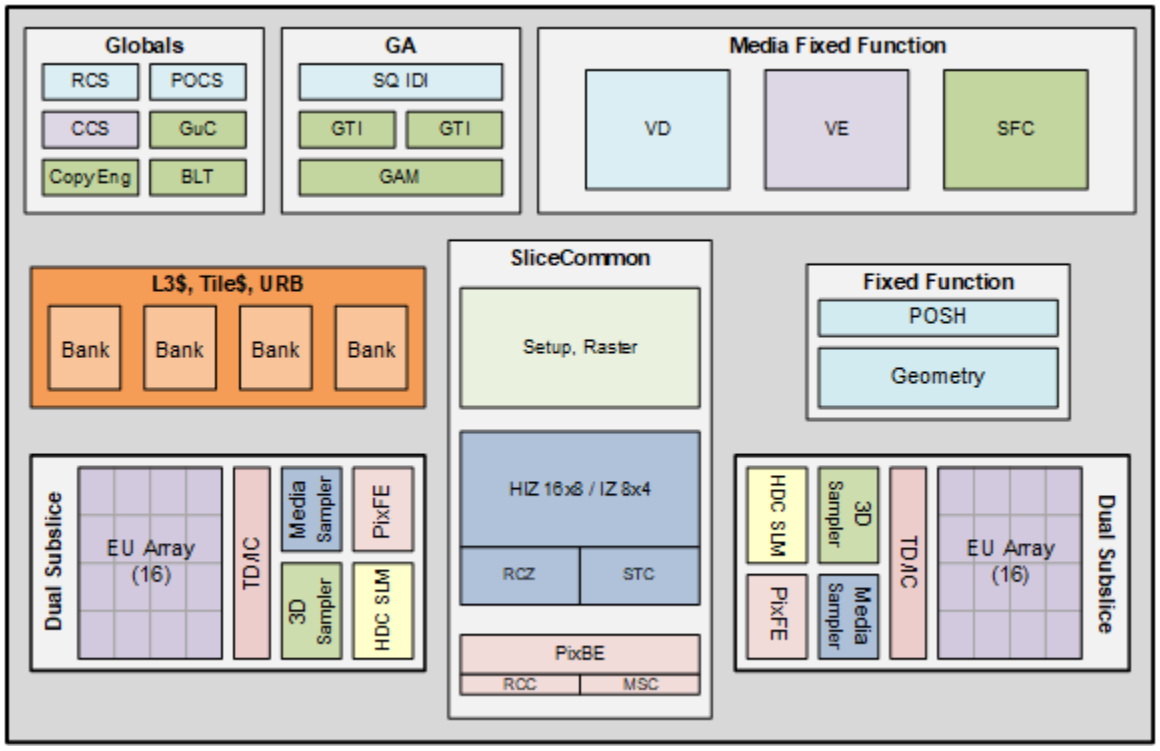
GT1 Top Level Diagram

Overview

The RKL-GT1 native slice is constructed of 2 dual subslices, each containing 16eus and a double sampler each capable of 8 tex/clk. Slice common will be constructed of a single Z pipe, capable of 16x8 HIZ and 8x4 IZ. 1 Color pipe capable of 8f8b. Total L3 cache size is defined to be ~2MB, built from 4 banks of 480kB each, single node. The machine will consist of a single geometry fixed function pipeline and maintain the position only shading (POSH) pipeline.

Media fixed function blocks are as follows: 1 VDBox, 1 VEBox, and 1 SFC. These assets are deemed sufficient to meet usage and throughput requirements for a majority of SKUs. Within the slice, there will be a total of 2 VME and 2 AVS; built 1 per dual subslice.

1x2x16



Device Attributes RKL

NOTE: This information is preliminary, and subject to change.

Product Configuration Attribute Table

Product Family	RKL
Architectural Name	1x2x16
SKU Name	GT1
	Global Attributes
Slice count	1
Dual-Subslice (DSS) Count	2
EU/DSS	16
EU count (total)	32
Threads / EU	7
Thread Count (Total)	224
FLOPs/Clk - Half Precision, MAD (peak)	1024
FLOPs/Clk - Single Precision, MAD (peak)	512
FLOPs/Clk - Double Precision, MAD (peak)	N/A
Unslice clocking (coupled/decoupled from Cr slice)	Coupled
GTI / Ring Interfaces	1
GTI bandwidth (bytes/unslice-clk)	r: 64
	w: 64
eDRAM Support	N/A
Graphics Virtual Address Range	48 bit
Graphics Physical Address Range	39 bit
	Caches & Dedicated Memories
L3 Cache, total size (bytes)	1920k
L3 Cache, bank count	4
L3 Cache, bandwidth (bytes/clk)(1)	4x 64 R|W
L3 Cache, URB bandwidth (bytes/clk)(1)	4x 64 R|W
L3 Cache, D$ Size (Kbytes)(2)	704K
L3 Cache, Tile cache size (Kbytes)(2)	1024K
L3 Cache, Command buffer cache size (Kbytes)(2)	64K
URB Size (kbytes)(2)	256K
SLM Size (kbytes)	256k
Instruction Cache (instances, bytes ea.)	2x 48k
Color Cache (RCC, bytes)	1x 32k
MSC Cache (MSC, bytes)	1x 16k
HiZ Cache (HZC, bytes)	1x 12k

Z Cache (RCZ, bytes)	1x 32k
	1x 8k
	Instruction Issue Rates
FMAD, SP (ops/EU/clk)	8
FMUL, SP (ops/EU/clk)	8
FADD, SP (ops/EU/clk)	8
MIN,MAX, SP (ops/EU/clk)	8
CMP, SP (ops/EU/clk)	8
INV, SP (ops/EU/clk)	2
SQRT, SP (ops/EU/clk)	2
RSQRT, SP (ops/EU/clk)	2
LOG, SP (ops/EU/clk)	2
EXP, SP (ops/EU/clk)	2
IDIV, SP (ops/EU/clk)	1-6
TRIG, SP (ops/EU/clk)	2
	Load/Store
Data Ports (HDC)	2
L3 Load/Store - same addresses within msg (Bytes/clk)	128
L3 Load/Store - unique addresses within msg (Bytes/clk)	128
SLM Load//Store - same addresses within msg (Bytes/clk)	256
SLM Load//Store - unique addresses within msg (Bytes/clk)	256
Atomic, Local 32b - same addresses within msg (dwords/clk)	2
Atomic, Global 32b - unique addresses within msg (dwords/clk)	32
	3D Attributes
Geometry pipes	1
Samplers (3D)	2
2D Texel Rate, point, 32b (tex/clk)	16
2D Texel Rate, point, 64b (tex/clk)	16
2D Texel Rate, point, 128b (tex/clk)	16
2D Texel Rate, bilinear, 32b (tex/clk)	16
2D Texel Rate, bilinear, 64b (tex/clk)	16
2D Texel Rate, bilinear, 128b (tex/clk)	4
2D Texel Rate, trilinear, 32b (tex/clk)	8
2D Texel Rate, trilinear, 64b (tex/clk)	8
2D Texel Rate, trilinear, 128b (tex/clk)	2
2D Texel Sample Rate, aniso 2x (MIP nearest), 32b (tex/clk)	16
2D Texel Sample Rate, aniso 4x (MIP nearest), 32b (tex/clk)	8
2D Texel Sample Rate, ansio 8x (MIP nearest), 32b (tex/clk)	4

2D Texel Sample Rate, ansio 16x (MIP nearest), 32b (tex/clk)	2
3D Texel Sample Rate, point, 32b (tex/clk)	16
3D Texel Sample Rate, point, 64b (tex/clk)	16
3D Texel Sample Rate, point, 128b (tex/clk)	8
3D Texel Sample Rate, bilinear, 32b (tex/clk)	8
3D Texel Sample Rate, bilinear, 64b (tex/clk)	8
3D Texel Sample Rate, bilinear, 128b (tex/clk)	2
HiZ Rate, (ppc)	1x128
IZ Rate, (ppc)	1x32
Stencil Rate (ppc)	1x128
(500 MHz, DDR-4267; Range depends on dynamic compression ratio)	
Pixel Rate, fill, 32bpp (pix/clk, RCC hit)	8
Pixel Rate, fill, 32bpp (pix/clk, LLC hit @ 1.0x unslice clk)	8
Pixel Rate, fill, 32bpp (pix/clk, LLC hit, @ 1.5x unslice clk)	N/A
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.0x unslice clk)	8
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.5x unslice clk)	N/A
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)	
Pixel Rate, blend, 32bpp (p/clk, RCC hit)	8
Pixel Rate, blend, 32bpp (p/clk, RCC miss, @ 1.0x unslice clk)	8
Pixel Rate, blend, 32bpp (p/clk, RCC miss, @ 1.5x unslice clk)	N/A
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.0x unslice clk)	8
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.5x unslice clk)	N/A

Notes:

* Architectural Name = Slice Count x Subslice Count x EUs per Subslice

(1) L3 cache and URB share the write bandwidth. Read bandwidths of 64B/clk can be achieved independently

(2) URB/Data cache/Tile cache/Command buffer cache sizes are programmable. Indicative values presented in this table.

Device Attributes Media

NOTE: This information is preliminary, and subject to change.

Product Configuration Attribute Table

Product Family	RKL
Architectural Name	1x2x16
SKU Name	GT1
	Media Attributes
Samplers (VME)	2
Samplers (AVS)	2
VDBox Instances (See VDBOX configuration)	1
VEBox Instances	1
SFC Instances	1

Device Attributes Display

Refer to XeD Overview

Stepping and Device IDs

Steppings Info

The following table details all currently planned steppings. Graphics stepping goes by IP TI timeline. This information is subject to change at any time based on roadmap plans.

SOC Type	SOC Stepping	Graphics/Media Stepping	Display Stepping	Dev2 RevID
U61	A0	A0	A0	0
S81	A0	B0	B0	1
S81	B0	C0	C0	4

SKUs and Device IDs

Segment	SKU	GT	EU Config	Total EUs	VDBoxes	TDP (W)	CPU Brand	Graphics Brand Number	Dev2 ID
									0x4C81 - 0x4C89
Desktop	S81/Downbin	GT1	1x2x16	32	1	35/65/125	i9/i7/i5	Intel® UHD Graphics 750	0x4C8A
Desktop	S81/Downbin	GT1	1x2x12	24	1	35/65	i5	Intel® UHD Graphics 730	0x4C8B
									0x4C8D - 0x4C8F
Workstation	S81/Downbin	GT1	1x2x16	32	1	35/80/125	Xeon W	Intel® UHD Graphics P750	0x4C90
									0x4C91 - 0x4C99
Server	S81/Downbin	GT1	1x2x16	32	1	65/80/95	N/A	Intel® UHD Graphics P750	0x4C9A
									0x4C9B - 0x4C9E