Intel® Arc™ A-Series Graphics and Intel Data Center GPU Flex Series

Open-Source Programmer's Reference Manual

For the discrete GPUs code named "Alchemist" and "Arctic Sound-M"

Volume 14: Workarounds

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Display Workarounds

Impact	
Title	LACE histograms don't properly get cleared due to timing issue related to vblank vs pipe enable signals
Bspec_wa_details	To mitigate this issue, essentially, we need to keep the LACE gated clock toggling during vblank_rise edge. In order to do this, we could use one of the three options 1. we could move the LACE function disable to after the poll on TRANS_CONF_A to wait till the pipe transcoder is OFF. this way we will still have clocks toggling during vblank_rise and clear the frame_histograms_done flag. 2. During the modeset disable sequence, we could not disable LACE function and keep it asserted so that the LACE gated clocks continue to toggle. However, this works only if LACE is expected to be enabled back during the re-enable sequence. 3. Set clock DCPR gating disable during the modeset disable sequence and re-enable them after-wards.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	driver_permanent_wa

Impact	
Title	FBC to force 512B segment alignment
Bspec_wa_details	512B alignment is required. The following calculation will provide for 512B alignment. Enable FBC_STRIDE override and program with the following value. Compressed buffer stride in cachelines = roundup to 8((ceiling [(at least plane width in pixels) / (32 * compression limit factor)] * 8) + 1) Data stolen memory allocation in bytes = min(640, ceiling (plane height / 4))* Compressed buffer stride in cachelines * 64
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	
Title	BW Buddy CTL Register has incorrect default value for TLB Request timeout
Bspec_wa_details	Program BW_BUDDY_CTL0 and BW_BUDDY_CTL1 "TLB Request Timer" field to 8h.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	
Title	dupunit not generating line_pop indication for plane with minimum size
Bspec_wa_details	plane horizontal minimum size in PLANE_SIZE register need to be increased according to the following: 8bpp: 18 16bpp: 10 32bpp,yuv212,yuv216: 6 64bpp: 4 NV12: 20 P010,P012,P016: 12
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Data corruption
Title	PLANE_CC_VAL not getting updated immediately on async flip
Bspec_wa_details	Display async flips will not update the clear color value at the right point. Limit use of display clear color to sync flips.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	
Title	Display Error Fatal Mask - default register value should be all 1's
Bspec_wa_details	The default register value should be all 1's for Display Error Fatal Mask register. With the current default value of 0, any fatal error condition will escape to dgsa unless programmed by software.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Data corruption
Title	Scaler detecting false ECC errors
Bspec_wa_details	Software will need to mask the "PS ECC Double Error" within the DISPLAY_ERR_FATAL_MASK register before enabling the Scaler After enabling Scaler, if Software wishes to unmask "PS ECC Double Error" or "PS ECC Single Error" (in DISPLAY_ERR_COR) then it will need to: 1) Wait for at least 1 frame 2) Clear "Double Error Detected" and "Single Error Detected" in PS_ECC_STAT 3) Unmask "PS ECC * Error" interrupts within DISPLAY_ERR_FATAL_MASK or DISPLAY_ERR_COR
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	
Title	Remove PM Req with unblock/memup + fill support -- SAGV enhancement not working as expected
Bspec_wa_details	Set register bits (0x46434) bits 24,25,26,27) to 1 at display initialization.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Data corruption
Title	[ACTIVE VIP]: Panel replay + Audio (sdp splitting enabled): VSC SDP is not being sent
Bspec_wa_details	DP2.x panel replay failures with secondary data packet splitting. Do not enable audio secondary data splitting in AUD_DP_2DOT0_CTRL together with enabling the Panel Replay feature on DP2.x. If a panel requires audio splitting to support a resolution, then do not enable Panel Replay.
Sku	All
Stepping_impacted	B0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Data corruption
Title	Display underrun can occur on cursor plane if WM0 is used without WM1
Bspec_wa_details	Cursor watermark 1 (WM1) value is being used when WM1 is disabled, causing underrun in some cases. WA: When cursor WM1 is disabled, copy contents of CUR_WM_0[30:0] (exclude the enable bit) into CUR_WM_1[30:0].
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Data corruption
Title	Jitter in DP output with MST + DSC + FEC enabled
Bspec_wa_details	Issue: Higher than expected line to line jitter of the horizontal blank start when using DP multi-stream with FEC (mainly used for DSC). WA: Adjust the transcoder data M and N values to fully utilize the VC payload by setting data M = VC payload size and data N = 64. This over allocates data within the payload, causing line pixel data to finish consistently early.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Data corruption
Title	TG DDA LinkM/LINKN >4 required for DP2.0 8K60
Bspec_wa_details	DisplayPort 2 128b/132b encoding limited to pixel rates less than or equal to 1,250 Megapixels/second. Use 8b/10b encoding for higher pixel rates.
Sku	All
Stepping_impacted	B0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Other
Title	dpst vblank delay counter does not reset
Bspec_wa_details	DPST guard band interrupt delay counter can go into a bad state and not trigger histogram interrupts correctly. Workaround: When servicing DPST histogram event status interrupt, follow below sequence to reset the delay counter. 1. Program DPST_CTL.Restore DPST (bit 28) = 0. 2. Read/Write DPST registers as needed to service the interrupt. 3. Program DPST_CTL.Restore DPST (bit 28) = 1 and Guardband Interrupt Delay Counter (bits 23:16) = 0 in a single register write. • Keep DPST_CTL.Restore DPST (bit 28) set afterwards When enabling DPST or doing a DPST configuration adjustment 1. Program any DPST related register other than DPST_CTL as needed. 2. Finally, when done with all other DPST programming then: 1. Read DPST_CTL register 2. Program DPST_CTL.Restore DPST (bit28) = 1 and Guard band Interrupt Delay Counter (bits 23:16) = value read from DPST_CTL Keep DPST_CTL.Restore DPST (bit 28) set afterwards
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Other
Title	Panel Replay VSC SDP not getting sent when VRR is enabled and W1 and W2 are 0
Bspec_wa_details	Program Set Context Latency in TRANS_SET_CONTEXT_LATENCY register to at least a value of 1 when Panel Replay is enabled with VRR.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

General Workarounds

Impact	
Title	EM/DPAS collision is causing EM W2W data hazard
Bspec_wa_details	SW needs to track WAW dependency for EM.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	
Title	For call/callA register source JIP offset incorrectly decoded by GA
Bspec_wa_details	Issue: When call/callA have register operand and the source and destination have different offsets, the source data is not sent to GA correctly. WA: Only .0 destination/source subregister is allowed for CALL and CALLA opcode
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	
Title	NoMask within goto-join with call return subroutine Issue with Fusion
Bspec_wa_details	Only full returns are supported. Partial returns need to be emulated using goto/join.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Hang
Title	VFURB dropping data in some scenarios involving 256 bit element format
Bspec_wa_details	Component packing of vertex elements associated with 256-bit surface formats is not supported due to a HW bug. WA: All components of vertex elements associated with 256-bit surface formats MUST be enabled.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Data corruption
Title	NoMask within goto-join with call return subroutine Issue with Fusion
Bspec_wa_details	Only full returns are supported. Partial returns need to be emulated using goto/join.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Other
Title	PSDunit is dropping MSB of the blend state pointer from SD FIFO
Bspec_wa_details	WA: Limit the Blend State pointer
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Hang
Title	Issue with Guc load after FLR
Bspec_wa_details	FSP will reprogram the 2 Guc registers. • SG sends FLR exit req to Punit • Punit sends message to GSC to program GT (The sub-cmd id being sent is Sgunit (no sub-cmd id for GT is present) • GSC program registers in GT (0xC050/0xC340) • GSC sends Ack back to Punit • Punit send FLR exit ack back to SG
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Data corruption
Title	Unexpected ResInfo results with LOD out of bounds.
Bspec_wa_details	When doing a resinfo message SW needs to check if any of the LOD values in an aligned 4 channel group is different: channel 0-3, 5-7, 8-11, etc. If any of them are different It must sequence the resinfo message so that there is at most one unique LOD per valid channel in each 4 pixel group.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	
Title	Need read/write access to 0xDB1C register
Bspec_wa_details	It is implemented as part of per context DFD as conditional whitelisted. if required to be unconditional whitelist, force to non priv can be used.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Other
Title	PSD is indicating the first payload phase as null for PSD_REG_P_BARY_PLANE phase
Bspec_wa_details	Corruption can exist in Fused SIMD16 threads if R68-R71 is the first phase after R1. This scenario might happen if experimenting with "remove BC" kernel. Enable any phase from R3-R67 to prevent the issue.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Data corruption
Title	Corruption on 3D engine writes to media compressible render target due to incorrect memory cycle type used for read operations when RHWO optimization is enabled
Bspec_wa_details	WA: Set 3DSTATE_3D_MODE.dw3.[15] (RHWO disable) to 1, for all media compressed Render Targets.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Hang
Title	EU instructions: Indirect address access with Acc destination doesn't work correctly on fused EU pair
Bspec_wa_details	WA: Shader compiler should not generate EU instruction that has both indirect addressing and Acc destination. Indirect addressing can be used with non-Acc destinations; Acc destination can be used in cases other than indirect addressing.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Other
Title	Clock ratio signal not connected to OAM
Bspec_wa_details	OAM reports will need to depend on OAG reports to get the time of occurrence of clock ratio changes. User will need to depend on the OAM counter values from the OAM report most close to the timestamp shown in OAG report with clock ratio change.
Sku	All
Stepping_impacted	B0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	
Title	MESH SVRANDOM:SOL input and output bypass out of syn, causing distrib cycle to get dropped
Bspec_wa_details	SW must insert a PIPE_CONTROL cmd before and after the 3dstate_so_buffer_index_0/1/2/3 states to ensure so_buffer_index_* state is not combined with other state changes.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	
Title	CCS is not sending flush to cfeg for chromakey command
Bspec_wa_details	WA1: SW must program stalling pipecontrol with HDC pipeline flush enabled before programming 3DSTATE_CHROMA_KEY for CCS W/L Or W/A2: SW must program STATE_SIP command with same filed values (last sent values or default values in case previously not sent) before programming 3DSTATE_CHROMA_KEY for CCS W/L
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	
Title	Texture sampler incorrectly handles cube face determination with float 16 cube maps for certain texture coordinate values
Bspec_wa_details	The WA must be applied only for cubes+half-float types When in float16 cube: 1. Convert the coordinate to float 2. Do the math operation in float, (inv and multiplication) à the part of the cube coords normalization code 3. Convert back to half-float This resolves issues with cube FaceID determination in SSLA unit in regards to a "tolerance" check of the coordinate mantissa bits to detect cases of 1.0f.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Data corruption
Title	DAPRSS Dropping Subspan Due to Alpha2Coverage
Bspec_wa_details	In the Color Calc State, the Alpha Reference Value should not be programmed to NaN while using a Foat32 Alpha Test Format.
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	
Title	GTPM : Full soft reset: GUC HW is unable to support Full soft reset flow
Bspec_wa_details	WA1 : FLR is required to recover from an active WL hang condition. (Whenever Full soft reset is required, KMD software will do a driver FLR.) OR WA2: Whenever Full soft reset is required, reset all individual engines (*cs/media) first, and then do a full soft reset. (preferred)
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

System Workarounds

Impact	
Title	Sideclk pointers stalled from resetting due to clock gating issue
Bspec_wa_details	This is a clock gating issue near warm reset entry. Suggested workaround is for SW to disable sideclk clock gating in SGSIunit: Disable sideclk clock gating in SGSIunit: MMIO offset 101014h bit 17 = 1
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Media Workarounds

Impact	Hang
Title	Hang on VECS reset due to clk gating issue in IECP
Bspec_wa_details	WA: Disable IECP clkgating by writing to 0x1C3F10[22]=1, 0x1D3F10[22]=1, 0x1E3F10[22]=1, 0x1F3F10[22]=1
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	Hang
Title	HWM unit doesn't check for ack response from downstream unit (backpressure) on tile boundaries, results in hang
Bspec_wa_details	WA: Real Tile Scal Decoder insert below commands after every HCP_BSD_OBJECT: (Tile boundary) • MFX_WAIT (with MFX_Sync_Control_Flag=1) VD_PIPELINE_FLUSH (with HEVC flush + VDcmd flush + HEVC done=1)
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa

Impact	
Title	HCP + SFC reset doesn't work correctly
Bspec_wa_details	This bug would affect the VDBOX-SFC reset sequence. We need to VE-SFC forced lock to get around this issue. Here are the steps: 1. Check MFX-SFC usage 2. If (MFX-SFC usage is 1) { a. Issue a MFX-SFC forced lock b. Wait for MFX-SFC forced lock ack c. Check the MFX-SFC usage bit d. If (MFX-SFC usage bit is 1) Reset VDBOX and SFC else Reset VDBOX f. Release the force lock MFX-SFC } 3. else (check HCP-SFC usage). 4. if(HCP+SFC usage is 1) 1. Issue a VE-SFC forced lock 2. Wait for SFC forced lock ack 3. Check the VE-SFC usage bit 4. If (VE-SFC usage bit is 1) Reset VDBOX else Reset VDBOX and SFC 5. Release the force lock VE-SFC. else Reset VDBOX
Sku	All
Stepping_impacted	A0
Stepping_fixed	
WA_status	Driver_permanent_wa